SXS046 / AD9361

Power-Up Configuration and Calibration

Application Manual

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This RevC customer reference revision clarifies confirmed SXS046 requirements, corrects arithmetic and ADC equation ordering, and identifies unresolved engineering details. TBC means confirmation is required; it is not an approved timing limit. Use completion-bit polling with a validated timeout policy. SXS055 is outside the scope of this manual.

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1. Overview

The SXS046 / AD9361 is a high-performance, highly integrated wideband RF transceiver. After each power-up or hardware reset, the device enters the SLEEP state (ENSM State = 0). A sequence of initialization calibrations must be completed before normal operation. All calibration results are stored in the SPI register map and remain valid while power is maintained, including in the SLEEP state.

Calibration execution principles

- Execute calibrations in the order specified by the initialization script generated by the official evaluation software (SXS046 Customer Software).
- Some calibrations depend on earlier calibrations and must not start until those preceding operations have completed.
- For TDD applications, complete all initialization calibrations in FDD mode first, then switch back to the TDD settings.
- Some operations are parameter-configuration tasks: calculate the values using the specified formulas and write them to registers. No start or wait sequence is required.

2. Calibration Overview

No.	Operation	Type	Start method	Completion indicator	Repeat when
0	Power-up and reset	Initialization	Apply power or pull RESETB low	SPI read/write works; verify 0x037 = 0x0A	Every power-up / hardware reset
1	BBPLL VCO calibration	Automatic / manual	Write integer divider word, or set 0x03F[D2] = 1	0x05E[7] = 1	BBPLL frequency changes
2	Enter ALERT	State transition	Set 0x014[D2] = 1 or pulse ENABLE	0x017[3:0] = 5	Every initialization
3	RF synthesizer charge pump calibration	Manual	Set 0x23D[2] = 1 and 0x27D[2] = 1 separately	0x244[7] = 1 / 0x284[7] = 1	Once only
4	RF synthesizer VCO calibration	Automatic	Write integer divider word	0x247[1] = 1 / 0x287[1] = 1	Frequency changes / TDD switching
5	RX baseband analog filter tuning	Manual	Set 0x016[7] = 1	0x016[7] self-clears	Bandwidth changes
6	TX baseband analog filter tuning	Manual	Set 0x016[6] = 1	0x016[6] self-clears	Bandwidth changes
7	RX TIA calibration	Parameter configuration	Calculate and write register values	None; configuration only	Bandwidth changes
8	TX secondary baseband filter tuning	Parameter configuration	Calculate and write register values	None; configuration only	Bandwidth changes
9	RX ADC setup	Parameter configuration	Calculate and write 0x200-0x227	None; configuration only	ADC clock or bandwidth changes
10	Baseband DC calibration	State machine	Set 0x016[0] = 1	0x016[0] self-clears	Once during initialization
11	RF DC calibration	State machine	Set 0x016[1] = 1	0x016[1] self-clears	LO change > 100 MHz
12	TX quadrature calibration	State machine	Set 0x016[4] = 1	0x016[4] self-clears	LO change > 100 MHz / temperature changes
13	RX quadrature calibration	State machine / tracking	Set 0x016[5] = 1 (one-shot), or enable tracking in 0x169	0x016[5] self-clears	LO change > 100 MHz
14	TX monitor DC calibration	State machine	Set 0x016[2] = 1	0x016[2] self-clears	LO change > 100 MHz
15	RX gain-step calibration	State machine	Set 0x016[3] = 1	0x016[3] self-clears	Factory calibration / field update

3. Detailed Calibration Procedures

3.0 Power-Up and Reset

Purpose: Perform basic initialization after power-up or hardware reset and place the device in an operational SLEEP state.

Prerequisites: Device supplies are stable and a reference clock is present at REF_CLK_IN.

Step 1 - Apply power or perform a hardware reset

Power-up: Apply DVDD, AVDD, VDD_GPO and the other supplies as required by the datasheet. Hardware reset: Pull RESETB low for at least 1 µs, then release it. The device enters reset.

Step 2 - Wait for the device to stabilize

Wait at least 20 ms after power-up/reset to allow the internal power-management circuitry to stabilize. The device automatically enters SLEEP (ENSM State = 0).

Step 3 - Verify the SPI interface

Read the device ID register (for example, 0x037) through SPI and confirm that the returned value is 0x0A. Verify normal SPI read/write operation; all subsequent calibrations depend on it.

Step 4 - Initialize SPI registers in the official script order

Configure clock dividers (BBPLL and RF synthesizer reference clocks, etc.), the data interface (LVDS/CMOS, data rate, frame format, etc.), FIR filter coefficients, the gain table and other basic registers.

Step 5 - Confirm the SLEEP state

Read 0x017[3:0] (ENSM State) and verify 0x0 (SLEEP). Confirm that no abnormal alarm flags are present.

Timing estimate

Item	Time	Basis
Supply stabilization	~20 ms	Internal POR requirement; typical datasheet value
SPI verification	~1 ms	Depends on SPI clock; typically 4 read/write operations
Basic register initialization	TBC [S1]	Script length and SPI rate; at the default 20 MHz SPI clock, approximately 200 registers × 2 µs = 0.4 ms; actual time including waits is approximately 5-50 ms
Total	TBC [S1]	Estimated for typical 40 MHz REF_CLK and 20 MHz SPI

3.1 Baseband PLL VCO Calibration (BBPLL VCO Cal)

Purpose: Calibrate the baseband PLL VCO so that the baseband clocks (ADC/DAC clocks, digital clocks, etc.) lock stably.

Prerequisites: Power-up initialization is complete and the BBPLL setup registers have been configured.

Key registers: 0x03F, 0x04B, 0x045, 0x04E, 0x05E.

Step 1 - Configure the basic BBPLL parameters

Write the BBPLL divider, loop-filter and other setup registers according to the official script. Write all other BBPLL setup registers first, then write the integer divider word last.

Step 2 - Enable frequency calibration

Write 0x04B and ensure D7 (Freq Cal Enable) = 1. To disable this calibration, write 0x04B = 0x40 (clear D7).

Step 3 - Start BBPLL VCO calibration manually

Set 0x03F[D2] = 1. This bit is not self-clearing and must be cleared manually after calibration is started.

Step 4 - Wait for calibration to complete

Poll 0x05E[D7] (BBPLL Lock). A value of 1 indicates that the BBPLL is locked and calibration is complete. As an additional check, read 0x04B[2:0] after completion; the VCO band result should be between 0 and 4.

Step 5 - Clear the start bit

Set 0x03F[D2] = 0.

Step 6 - Verify lock

Read 0x05E[7] again and confirm it remains 1. If lock fails, check the reference clock, supplies and register configuration.

Timing estimate

```
BBPLL_maxVCOcalTime =
(1 / ((REF_CLK_IN / DivideSetting) × Scale)) × 3 × (Counter + 128)
```

Parameter	Register	Meaning
Scale	0x045[1:0]	00 = 1; 01 = 1/2; 10 = 1/4; 11 = 2
Counter	0x04B[6:5]	00 = 128; 01 = 256; 10 = 512; 11 = 1024
DivideSetting	0x04E[4]	0 = 1; 1 = 4

Typical calculation: REF_CLK_IN = 40 MHz, Scale = 1, Counter = 128, DivideSetting = 1.

```
BBPLL_maxVCOcalTime = (1 / ((40 MHz / 1) × 1)) × 3 × (128 + 128)
= 25 ns × 3 × 256 = 19.2 µs
```

Configuration	Maximum calibration time
Scale = 1, Counter = 128, DivideSetting = 1	~19.2 µs
Scale = 1, Counter = 256, DivideSetting = 1	~28.8 µs
Scale = 1, Counter = 512, DivideSetting = 1	~48.0 µs
Scale = 1, Counter = 1024, DivideSetting = 1	~86.4 µs
Scale = 2, Counter = 1024, DivideSetting = 1	~43.2 µs

Recommended allowance including SPI read/write and polling overhead: TBC [S1].

3.2 Entering the ALERT State

Purpose: Transition from SLEEP to ALERT, powering the RF synthesizers in preparation for subsequent RF calibrations.

Prerequisites: BBPLL VCO calibration has completed and the BBPLL is locked.

Key registers: 0x013, 0x014, 0x015, 0x017, 0x024, 0x025.

Step 1 - Configure FDD mode (recommended during initialization)

Set 0x013[D0] = 1 to enable FDD mode. Set 0x015[D2] = 1 (Dual Synthesizer) so that both RX and TX synthesizers are powered in ALERT. For TDD operation, complete all initialization calibrations in FDD mode first, then restore the TDD configuration.

Step 2 - Select ENSM control

SPI control: Ensure 0x014[D4] (ENSM Pin Control) = 0. Pin control: Set 0x014[D4] = 1; ENABLE/TXNRX pin levels control the state.

Step 3 - Configure the ALERT transition delay

Write 0x024 and 0x025 to set the fixed delay from SLEEP to ALERT. This delay allows the internal supplies and synthesizers to power up stably.

Step 4 - Trigger ALERT

SPI control: Set 0x014[D2] (Force Alert State) = 1. Pin control: In the 0x014[D3] level mode, trigger the transition with a pulse on ENABLE.

Step 5 - Wait for the ENSM transition

After Force Alert, the device passes through the fixed State 4 delay. Poll 0x017[3:0]. A value of 5 (0x05, ALERT) indicates completion.

Step 6 - Confirm RF synthesizer power-up

The RF synthesizers power up automatically on entering ALERT. Read the relevant status registers to verify normal power status.

Step 7 - Wait for synthesizer stabilization

Allow an additional 2-5 µs after entering ALERT. This interval is related to the delay configured in 0x024/0x025.

Timing estimate

Item	Time	Basis
SPI configuration writes	~10 µs	3-4 registers × SPI transfer time
Fixed SLEEP-to-ALERT delay	2-10 µs	Set by 0x024/0x025; typical values
Synthesizer stabilization	2-5 µs	Internal supply stabilization
State polling	~5 µs	2-3 SPI reads
Total	TBC [S1]	Typical configuration

3.3 RF Synthesizer Charge Pump Calibration

Purpose: Match the RF PLL charge pump up/down currents to ensure PLL locking performance.

Prerequisites: The device is in ALERT; FDD mode and Dual Synthesizer are enabled.

Key registers: 0x23D, 0x244, 0x27D, 0x284, 0x2AB, 0x2AC.

Step 1 - Confirm FDD settings

Read 0x013[D0] and verify FDD is enabled (= 1). Read 0x015[D2] and verify Dual Synthesizer is enabled (= 1).

Step 2 - Confirm ALERT

Verify 0x017[3:0] = 5 (ALERT).

Step 3 - Start RX charge pump calibration

Set 0x23D[D2] = 1 (RX CP Cal Enable).

Step 4 - Wait for RX completion

Poll 0x244[D7] (CP Cal Valid). A value of 1 indicates completion. As an additional check, 0x244[D5] (CP Cal Done) = 1 indicates that the current calibration succeeded.

Step 5 - Clear the RX start bit

Set 0x23D[D2] = 0.

Step 6 - Start TX charge pump calibration

Set 0x27D[D2] = 1 (TX CP Cal Enable).

Step 7 - Wait for TX completion

Poll 0x284[D7] (CP Cal Valid) until it reads 1.

Step 8 - Clear the TX start bit

Set 0x27D[D2] = 0.

Step 9 - Save results (optional)

Read 0x244[3:0] for the RX CP result and 0x284[3:0] for the TX CP result. This calibration only needs to run once; results are retained while device power is maintained.

Timing estimate

Dimensionally consistent time expression from the source worked example [S2]; Scale semantics require confirmation:

```
Max CP Cal Time = 36864 / (REF_CLK_IN × Scale)
REF_CLK_IN is in Hz; the result is in seconds.
```

Scale is selected by {0x2AB[0], 0x2AC[7]} for RX and 0x2AC[3:2] for TX. Both mappings are 00 = 1, 01 = 1/2, 10 = 1/4, 11 = 2.

Calculation at REF_CLK_IN = 40 MHz and Scale = 1:

```
Max CP Cal Time = 36864 / (40 MHz × 1) = 921.6 µs
```

REF_CLK_IN	Scale	Maximum per channel	RX + TX total
40 MHz	1	921.6 µs	~1.84 ms
40 MHz	1/2	TBC [S2]	TBC [S2]
40 MHz	2	TBC [S2]	TBC [S2]
19.2 MHz	1	1.92 ms	~3.84 ms
30.72 MHz	1	1.2 ms	~2.4 ms

Recommended allowance including SPI polling: ~2 ms (40 MHz, default Scale = 1).

3.4 RF Synthesizer VCO Calibration

Purpose: Calibrate the RF synthesizer VCO bands so that the RX/TX LO frequencies lock accurately.

Prerequisites: Charge pump calibration is complete. Synthesizer setup and loop-filter registers have been configured from the LUT for the VCO frequency.

Key registers: 0x231, 0x271, 0x247, 0x287, 0x230, 0x270.

Step 1 - Configure basic synthesizer parameters

Obtain setup values from the official software LUT for the target VCO frequency. Write the loop-filter registers and the fractional divider-word registers.

Step 2 - Trigger RX VCO calibration

Write 0x231 (RX integer divider word); the write automatically triggers RX VCO calibration. For Fast Lock or HFDD mode, first set 0x230[D0] = 1 to inhibit calibration.

Step 3 - Wait for RX completion

Poll 0x247[D1] (Rx PLL Lock). A value of 1 indicates completion and PLL lock. While calibration is running, 0x244[D4] (VCO Cal Busy) = 1.

Step 4 - Trigger TX VCO calibration

Write 0x271 (TX integer divider word); the write automatically triggers TX VCO calibration. For Fast Lock or HFDD mode, first set 0x270[D0] = 1 to inhibit calibration.

Step 5 - Wait for TX completion

Poll 0x287[D1] (Tx PLL Lock). A value of 1 indicates completion and PLL lock. While calibration is running, 0x284[D4] (VCO Cal Busy) = 1.

Step 6 - Verify both synthesizers are locked

Read 0x247[1] and 0x287[1] and confirm both equal 1. If lock fails, check that the frequency setting is within the VCO range.

Step 7 - Fine-tune the frequency if required

Write the frequency correction words at 0x24E/0x24F (RX) and 0x28E (TX). These writes do not trigger another VCO calibration.

Additional TDD information

In TDD mode, a TXNRX transition that powers the synthesizer back up automatically triggers VCO calibration. A high-to-low transition triggers RX VCO calibration; a low-to-high transition triggers TX VCO calibration.

Timing estimate

Maximum calibration time using default FDD settings:

```
RFPLL_maxVCOcalTime = wait_1 + wait_2
+ ((N_ALC + N_count) / (REF_CLK_IN × Scale) + wait_ALC) × 9
wait_1 = RX delay set by Reg0x024 (typically 2 µs)
wait_2 = 8/REF_CLK + 18/(REF_CLK × Scale)
wait_ALC = (1 + {0x249[6:4],Rx} × 40) / (REF_CLK × Scale)
N_ALC = 6 × 2^(1 + {0x23D[7],Rx})
N_count = 2^(7 + {0x249[3:2],Rx})
```

Mode (40 MHz REF_CLK, defaults)	Typical time	Notes
Default FDD	~123.5 µs	9 ALC iterations; highest accuracy
Default TDD	~37.1 µs	Fewer iterations to reduce turnaround time
Relock at the same frequency	<25 µs	PLL relock only; no full VCO calibration

These times exclude the additional PLL lock-settling interval after calibration (approximately 10-50 µs).

Recommended allowance: 200 µs for FDD initialization; 100 µs for TDD initialization.

3.5 RX Baseband Analog Filter Tuning (RX BBF Tune)

Purpose: Tune the cutoff frequency of the RX baseband analog filter (third-order Butterworth anti-aliasing filter) so that the signal bandwidth before the ADC is correct.

Prerequisites: The device is in ALERT and no other calibration is running.

Key registers: 0x1F8, 0x1F9, 0x1FB, 0x1FC, 0x1E2, 0x1E3, 0x016.

Step 1 - Confirm ALERT

Verify 0x017[3:0] = 5.

Step 2 - Confirm no other calibration is running

Read 0x017[7:4] (Calibration Sequence State) and verify 0x1 (done) or 0x0 (wait). Ensure no other calibration start bit in 0x016[7:0] is 1.

Step 3 - Calculate and set the RX tune-clock divider

```
Desired_f_RXTuneCLK = (1.4 × BBBW × 2π) / ln(2)
RXBBF_Divide[8:0] = min(511, ceiling(BBPLL_Freq / Desired_f_RXTuneCLK))
0x1F8[7:0] = Divide[7:0]
0x1F9[D0] = Divide[8]
```

Preserve the existing values of 0x1F9[D7:D1].

SXS046 requirement: 0x1F8[D0] must be 0 before calibration. Apply Divide_even = Divide & 0x1FE to the computed 9-bit divider, then write its low byte and ninth bit while preserving unrelated register bits. Reapply this rule whenever retuning is required. [S6]

Step 4 - Write the target baseband bandwidth (BBBW)

Limit BBBW to 0.2-28 MHz. Write the integer MHz part to 0x1FB (1 MHz/LSB). Write the kHz part to 0x1FC using:

```
BBBW_kHz[6:0] = min(127,
Round((BBBW_MHz - Floor(BBBW_MHz)) × 1000 / 7.8125))
```

Step 5 - Enable the RX baseband filter tuning circuitry

Set 0x1E2[D0] = 0 and 0x1E3[D0] = 0.

Step 6 - Start RX BBF calibration

Set 0x016[D7] = 1.

Step 7 - Wait for completion

Poll 0x016[D7] until it self-clears to 0. Completion can also be monitored through a control output pin.

Step 8 - Disable the tuning circuitry

Set 0x1E2[D0] = 1 and 0x1E3[D0] = 1.

Step 9 - Verify the result

Read 0x1EB, 0x1EC and 0x1E6 for subsequent TIA and ADC configuration. Confirm the filter corner is calibrated to 1.4 × BBBW.

Timing estimate

The calibration uses a binary search with a maximum of 610 RX tune-clock cycles.

```
Max Rx BBF Cal Time = 610 / f_RXTuneCLK
```

Standard	BBBW	BBPLL	RXBBF divider	Actual f_RXTuneCLK	Maximum time
LTE 5 MHz	2.5 MHz	983.04 MHz	30 [S6]	32.768 MHz	18.616 µs
LTE 10 MHz	5 MHz	983.04 MHz	16	61.44 MHz	9.928 µs
LTE 15 MHz	7.5 MHz	737.28 MHz	8	92.16 MHz	6.619 µs
LTE 20 MHz	10 MHz	983.04 MHz	8	122.88 MHz	4.964 µs
WiMax 10 MHz	5 MHz	716.8 MHz	12	59.733 MHz	10.212 µs

Recommended allowance including SPI configuration and polling: ~25 µs (typical LTE 10 MHz).

3.6 TX Baseband Analog Filter Tuning (TX BBF Tune)

Purpose: Tune the cutoff frequency of the TX baseband analog filter (third-order Butterworth anti-imaging filter) so that the signal bandwidth after the DAC is correct.

Prerequisites: The device is in ALERT and no other calibration is running.

Key registers: 0x0CA, 0x0D6, 0x0D7, 0x016.

Step 1 - Confirm ALERT

Verify 0x017[3:0] = 5.

Step 2 - Confirm no other calibration is running

Read 0x017[7:4] and verify the calibration state machine is in the done or wait state. Ensure no other calibration start bit in 0x016[7:0] is 1.

Step 3 - Enable the TX baseband filter tuning circuitry

Set 0x0CA[D2] = 0.

Step 4 - Calculate and set the TX tune-clock divider

```
Desired_f_TXTuneCLK = (1.6 × BBBW × 2π) / ln(2)
TXBBF_Divide[8:0] = min(511, ceiling(BBPLL_Freq / Desired_f_TXTuneCLK))
0x0D6[7:0] = Divide[7:0]
0x0D7[D0] = Divide[8]
```

Preserve the existing values of 0x0D7[D7:D1].

SXS046 requirement: 0x0D6[D0] must be 0 before calibration. Apply Divide_even = Divide & 0x1FE to the computed 9-bit divider, then write its low byte and ninth bit while preserving unrelated register bits. Reapply this rule whenever retuning is required. [S6]

Step 5 - Start TX BBF calibration

Set 0x016[D6] = 1.

Step 6 - Wait for completion

Poll 0x016[D6] until it self-clears to 0.

Step 7 - Disable the tuning circuitry

Set 0x0CA[D2] = 1.

Step 8 - Verify the result

Confirm the filter corner is calibrated to 1.6 × BBBW. Limit BBBW to 0.625-20 MHz.

Timing estimate

The calibration uses a binary search with a maximum of 355 TX tune-clock cycles.

```
Max Tx BBF Cal Time = 355 / f_TXTuneCLK
```

Standard	BBBW	BBPLL	TXBBF divider	Actual f_TXTuneCLK	Maximum time
LTE 5 MHz	2.5 MHz	983.04 MHz	28	35.109 MHz	10.112 µs
LTE 10 MHz	5 MHz	983.04 MHz	14	70.217 MHz	5.056 µs
LTE 15 MHz	7.5 MHz	737.28 MHz	6 [S6]	122.88 MHz	2.889 µs
LTE 20 MHz	10 MHz	983.04 MHz	6 [S6]	163.84 MHz	2.167 µs
WiMax 10 MHz	5 MHz	716.8 MHz	10	71.68 MHz	4.953 µs

Recommended allowance including SPI configuration and polling: ~15 µs (typical LTE 10 MHz).

3.7 RX TIA Calibration (Parameter Configuration)

Purpose: Calculate and configure the RX transimpedance amplifier (TIA) capacitance from BBBW and the RX BBF calibration results, placing the TIA single-pole filter corner at 2.5 × BBBW.

Prerequisites: RX BBF Tune completed successfully and its result registers have been read.

Key registers: 0x1DB, 0x1DC, 0x1DD, 0x1DE, 0x1DF.

Step 1 - Read the RX BBF calibration results

Read 0x1EB (RX BBF C3 MSB), 0x1EC (RX BBF C3 LSB) and 0x1E6 (RX BBF R2346).

Step 2 - Determine TIA Sel CC

Set 0x1DB[D7:D5] (TIA Sel CC[2:0]) according to BBBW:

BBBW	TIA Sel CC	Register field value
<3 MHz	7	0xE0
≥3 MHz and <10 MHz	3	0x60
≥10 MHz	1	0x20

Step 3 - Calculate C_rxbbf

```
C_rxbbf = (reg1EB × 160 fF) + (reg1EC × 10 fF) + 140 fF
```

Step 4 - Calculate R_2346

```
R_2346 = reg1E6[2:0] × 18300 Ω
```

Valid values: reg1E6 = 1 gives 18300 Ω; 2 gives 36600 Ω; 4 gives 73200 Ω.

Step 5 - Calculate CTIA

```
CTIA_fF = (C_rxbbf × R_2346 × 0.56) / 3500
```

Step 6 - Calculate and write the TIA capacitance registers

```
If CTIA > 2920 fF:
reg1DC = reg1DE = 0x40 // TIA1/TIA2 C LSB; RFCNT=01, C_LSB=0
temp = min(127, Round((CTIA_fF - 400) / 320))
reg1DD = reg1DF = temp // TIA1/TIA2 C MSB
If CTIA ≤ 2920 fF:
temp = Round((CTIA_fF - 400) / 40) + 0x40
reg1DC = reg1DE = temp // TIA1/TIA2 C LSB
reg1DD = reg1DF = 0 // TIA1/TIA2 C MSB
```

Step 7 - Configure the override bits

Ensure 0x1DB[D4:D0] (override bits) = 0 so that the device automatically scales the capacitance according to the gain table.

Step 8 - Write the TIA registers

```
SPIWrite(0x1DB, reg1DB); SPIWrite(0x1DC, reg1DC);
SPIWrite(0x1DD, reg1DD); SPIWrite(0x1DE, reg1DE);
SPIWrite(0x1DF, reg1DF);
```

Timing estimate

Item	Time	Basis
Read 3 result registers	~3 µs	3 SPI reads, approximately 1 µs each
Formula calculation	~1 µs	MCU/DSP calculation time
Write 5 registers	~5 µs	5 SPI writes
Total	~10 µs	Software operations only; no hardware wait

3.8 TX Baseband Secondary Filter Tuning (Parameter Configuration)

Purpose: Set the TX secondary baseband filter (single-pole) corner to 5 × BBBW to suppress out-of-band transmit noise.

Prerequisites: The target BBBW has been determined.

Key registers: 0x0D0, 0x0D1, 0x0D2, 0x0D3.

Step 1 - Calculate the target corner frequency

```
corner = 5 × BBBW_MHz × 2π // Mrad/s
```

Limit BBBW to 0.53-20 MHz.

Step 2 - Try resistor values to obtain a valid capacitance

Start with R = 100 Ω, then try 200 Ω, 400 Ω and 800 Ω:

```
cap = Round((1 / (corner × R × 1e6)) × 1e12) - 12
```

The 12 pF term is the parasitic capacitance when the cap register is 0. If cap ≤ 63, the current R/cap combination is valid; exit the loop. If cap > 63, double R and try the next resistor value.

Step 3 - Limit the maximum capacitance value

If cap remains greater than 63 after all resistor values have been tried, set cap = 63.

Step 4 - Determine 0x0D0

BBBW	reg0D0
≤9 MHz	0x55
>9 MHz and ≤24 MHz	0x5A
>24 MHz	0x5F

Step 5 - Determine 0x0D1

Selected R	reg0D1
100 Ω	0x0C
200 Ω	0x04
400 Ω	0x03
800 Ω	0x01

Step 6 - Determine 0x0D2

Set reg0D2 = cap (6-bit capacitance word).

Step 7 - Write the registers

```
SPIWrite(0x0D0, reg0D0)
SPIWrite(0x0D1, reg0D1)
SPIWrite(0x0D2, reg0D2)
SPIWrite(0x0D3, 0x60) // Retain default 0x60 for best performance
```

Timing estimate

Item	Time	Basis
Formula calculation (loop)	~1 µs	MCU/DSP calculation time
Write 4 registers	~4 µs	4 SPI writes
Total	~5 µs	Software operations only; no hardware wait

3.9 RX ADC Setup (Parameter Configuration)

Purpose: Calculate and configure 40 RX ADC register values from the RX BBF calibration results and ADC sample rate to compensate for process variation. The RX ADC is a third-order continuous-time Σ-Δ modulator.

Prerequisites: RX BBF Tune is complete and its results have been read; FsADC has been determined.

Key registers: 0x200-0x227 (40 registers).

Step 1 - Read RX BBF calibration results

Read 0x1EB (rxbbf_c3_msb), 0x1EC (rxbbf_c3_lsb) and 0x1E6 (rxbbf_r2346).

Step 2 - Determine input parameters

FsADC is the ADC clock frequency in MHz. BBBW_MHz is the baseband bandwidth, clamped to 0.2-28 MHz.

```
if (BBBW_MHz > 28) BBBW_MHz = 28
if (BBBW_MHz < 0.2) BBBW_MHz = 0.2
if (FsADC < 80) scale_snr_dB = 0
else scale_snr_dB = 2
```

Step 3 - Calculate the RC time constant

```
If BBBW < 18 MHz:
rc_timeConst = 1 / ((1.4 × 2π) × (18300 × rxbbf_r2346)
× (160e-15 × rxbbf_c3_msb + 10e-15 × rxbbf_c3_lsb + 140e-15)
× (BBBW_MHz × 1e6))

If BBBW ≥ 18 MHz:
rc_timeConst = 1 / ((1.4 × 2π) × (18300 × rxbbf_r2346)
× (160e-15 × rxbbf_c3_msb + 10e-15 × rxbbf_c3_lsb + 140e-15)
× (BBBW_MHz × 1e6) × (1 + 0.01 × (BBBW_MHz - 18)))
```

Step 4 - Calculate scale factors

```
scale_res = sqrt(1 / rc_timeConst)
scale_cap = sqrt(1 / rc_timeConst)
scale_snr = 10^(scale_snr_dB / 10)
maxsnr = 640 / 160 = 4
```

Step 5 - Calculate the 40 ADC configuration values

Calculate data[0]-data[39] using the following formulas, corresponding to registers 0x200-0x227. Compute data[10] before data[9], because data[9] depends on data[10]. The following listing is ordered accordingly; register write order remains 0x200 through 0x227.

```
data[0] = 0x00; // 0x200
data[1] = 0x00; // 0x201
data[2] = 0x00; // 0x202
data[3] = 0x24; // 0x203
data[4] = 0x24; // 0x204
data[5] = 0x00; // 0x205
data[6] = 0x00; // 0x206
data[7] = min(124, floor(-0.5 + 80 × scale_snr × scale_res × min(1, sqrt(maxsnr ×
FsADC / 640)))); // 0x207
data[8] = min(255, floor(0.5 + 20 × (640/FsADC) × (data[7]/80) / (scale_res ×
scale cap))); // 0x208
data[10] = min(127, floor(-0.5 + 77 × scale_res × min(1, sqrt(maxsnr × FsADC /
640)))); // 0x20A
data[9] = min(127, floor(0.8 × data[10])); // 0x209
data[11] = min(255, floor(0.5 + 20 × (640/FsADC) × (data[10]/77) / (scale_res ×
scale cap))); // 0x20B
data[12] = min(127, floor(-0.5 + 80 × scale_res × min(1, sqrt(maxsnr × FsADC /
640)))); // 0x20C
data[13] = min(255, floor(-1.5 + 20 × (640/FsADC) × (data[12]/80) / (scale_res ×
scale cap))); // 0x20D
data[14] = 21 × floor(0.1 × 640 / FsADC); // 0x20E
```

```
data[15] = min(127, int(1.025 × data[7])); // 0x20F
data[16] = min(127, floor(data[15] × (0.98 + 0.02 × max(1, (640/FsADC) / maxsnr)))); // 0x210
data[17] = data[15]; // 0x211
data[18] = min(127, int(0.975 × data[10])); // 0x212
data[19] = min(127, floor(data[18] × (0.98 + 0.02 × max(1, (640/FsADC) / maxsnr)))); // 0x213
data[20] = data[18]; // 0x214
data[21] = min(127, int(0.975 × data[12])); // 0x215
data[22] = min(127, floor(data[21] × (0.98 + 0.02 × max(1, (640/FsADC) / maxsnr)))); // 0x216
data[23] = data[21]; // 0x217
data[24] = 0x2E; // 0x218
data[25] = floor(128 + min(63, 63 × (FsADC / 640))); // 0x219
data[26] = floor(0 + min(63, 63 × (FsADC / 640) × (0.92 + 0.08 × (640/FsADC)))); // 0x21A
data[27] = floor(0 + min(63, 32 × sqrt(FsADC / 640))); // 0x21B
data[28] = floor(128 + min(63, 63 × (FsADC / 640))); // 0x21C
data[29] = floor(0 + min(63, 63 × (FsADC / 640) × (0.92 + 0.08 × (640/FsADC)))); // 0x21D
data[30] = floor(0 + min(63, 32 × sqrt(FsADC / 640))); // 0x21E
data[31] = floor(128 + min(63, 63 × (FsADC / 640))); // 0x21F
data[32] = floor(0 + min(63, 63 × (FsADC / 640) × (0.92 + 0.08 × (640/FsADC)))); // 0x220
data[33] = floor(0 + min(63, 63 × sqrt(FsADC / 640))); // 0x221
data[34] = min(127, floor(64 × sqrt(FsADC / 640))); // 0x222
data[35] = 0x40; // 0x223
data[36] = 0x40; // 0x224
data[37] = 0x2C; // 0x225
data[38] = 0x00; // 0x226
data[39] = 0x00; // 0x227
```

Step 6 - Write the ADC registers

Write the 40 values consecutively from 0x200 through 0x227. Continuous SPI burst writes are recommended for efficiency.

Timing estimate

Item	Time	Basis
Read 3 result registers	~3 µs	3 SPI reads
Calculate 40 values	TBC [S1]	MCU/DSP floating-point operations
Write 40 registers	TBC [S1]	40 SPI writes at 1-2 µs each; burst mode can reduce this to ~20 µs
Total	TBC [S1]	Depends on SPI rate and use of burst writes

3.10 Baseband DC Offset Calibration (BB DC Offset Cal)

Purpose: Calibrate DC offsets in the baseband path. Correction values are stored separately for 25 RX BBF gain settings and applied automatically when gain changes.

Prerequisites: The device is in ALERT and the baseband path is stable.

Key registers: 0x016, 0x185, 0x190, 0x193, 0x18B.

Step 1 - Confirm ALERT

Verify 0x017[3:0] = 5.

Step 2 - Verify default register settings

Confirm 0x185 (WaitTime), 0x190 (CountSize control), 0x193 (DCOffsetcount) and related registers have their default values or have been configured as required. 0x190[7] = 1 selects CountSize = 1024; 0 selects CountSize = 256.

Step 3 - Start baseband DC calibration

Set 0x016[D0] = 1 (SXS046_bb_dc_offset_calib). If both RX channels are enabled, they calibrate in parallel.

Step 4 - Wait for completion

Poll 0x016[D0] until it self-clears to 0.

Step 5 - Verify results (optional)

Results are automatically stored in an internal LUT indexed by the 25 RX BBF gain settings. Manual result readback is unnecessary; the device applies the values automatically when gain changes.

Step 6 - Enable baseband DC tracking if required

Complete a one-shot calibration first, then set 0x18B[D5] = 1 to enable BB DC tracking. Tracking is disabled by default.

Timing estimate

```
BB DC Cal Time = ((DCOffsetcount × CountSize) + 0x185) × 25 ClkRF cycles
```

DCOffsetcount = 0x193[7:0] (the default is normally an appropriate value). CountSize is 1024 or 256, selected by 0x190[7]. 0x185 is WaitTime (default). ClkRF is the RX FIR input clock, normally the ADC clock divided by the half-band decimation factor.

Typical calculation: DCOffsetcount = 16, CountSize = 1024, 0x185 = 10, ClkRF = 61.44 MHz.

```
BB DC Cal Time = ((16 × 1024) + 10) / 61.44 MHz × 25
= 16394 / 61.44 MHz × 25
= 266.8 µs × 25 = ~6.67 ms
```

With two channels enabled, calibration runs in parallel and the total time does not double.

Configuration	Typical time
Defaults, ClkRF = 61.44 MHz	TBC [S1]
Defaults, ClkRF = 30.72 MHz	TBC [S1]
Reduced settings (CountSize = 256)	TBC [S1]

Recommended allowance: ~10 ms.

3.11 RF DC Offset Calibration (RF DC Offset Cal)

Purpose: Calibrate DC offsets introduced by the RF front end (LNA and mixer), proceeding from minimum to maximum gain and storing the results in a LUT.

Prerequisites: The device is in ALERT and the RX synthesizer is enabled.

Key registers: 0x016, 0x185, 0x186, 0x187.

Step 1 - Confirm ALERT and RX synthesizer enable

Verify 0x017[3:0] = 5. Confirm the RX synthesizer is powered (FDD mode, or TXNRX = 0 in TDD).

Step 2 - Configure calibration parameters

Write 0x185 = WaitTime (wait per gain setting), 0x186 = DCcount (count for each average), and 0x187[D3:D0] = DCcalTime (calibration timing control).

Step 3 - Start RF DC calibration

Set 0x016[D1] = 1 (SXS046_rf_dc_offset_calib). If both channels are enabled, calibration runs in parallel.

Step 4 - Wait for completion

Poll 0x016[D1] until it self-clears to 0.

Step 5 - Verify calibration coverage

Calibration advances from minimum gain (index = 0) to maximum gain. It runs only at indexes where front-end gain actually changes, reducing time. With a Split RX Gain Table, calibration runs at each front-end gain LUT index.

Step 6 - Handle multiple input ports if required

The RF RX A port has separate calibration results. For RX B/C, select the required ports and run calibration; B and C share one result set. After changing input ports, recalibrate if the LO change exceeds 100 MHz.

Step 7 - Confirm RF DC tracking is enabled (default)

RF DC tracking is enabled by default and updates on gain changes, no-energy detection or exit from RX. Register settings can enable or disable each trigger event.

Timing estimate

```
LengthOfEachAverage = [(DCcount × 256) + 255] + WaitTime
numberOfAverages = ((DCcalTime + 1) × 4) + 1
CalTimePerGainIndex = LengthOfEachAverage × numberOfAverages
TotalCalTime = CalTimePerGainIndex × (NumberOfEnabledGainIndexes + 1)
```

Arithmetic-corrected illustration [S3]: DCcount = 4, WaitTime = 10, DCcalTime = 3, ClkRF = 61.44 MHz. This example assumes 25 total evaluated gain indexes, including any extra index in the general formula. Confirm the actual index count for the selected gain table.

```
LengthOfEachAverage = [(4 × 256) + 255] + 10
= 1024 + 255 + 10 = 1289 cycles
numberOfAverages = ((3 + 1) × 4) + 1 = 17
CalTimePerGainIndex = 1289 × 17 = 21913 cycles
TotalCalTime = 21913 × 25 = 547825 cycles
= 547825 / 61.44 MHz ≈ 8.916 ms
```

Configuration	Typical time
Defaults, 25 gain settings, ClkRF = 61.44 MHz	TBC [S1]
Reduced settings, ClkRF = 61.44 MHz	TBC [S1]
Defaults, ClkRF = 30.72 MHz	TBC [S1]

Recommended allowance: ~15 ms.

3.12 TX Quadrature Calibration (TX Quad Cal)

Purpose: Use an internal test tone to converge TX DC offset (LO leakage), gain error and phase error, improving transmit-path performance.

Prerequisites: The device is in ALERT.

Key registers: 0x016, 0x0A0-0x0AE.

Step 1 - Confirm ALERT

Verify 0x017[3:0] = 5.

Step 2 - Configure preliminary parameters

Write 0x0A0 for NCO phase (determine the optimum value through measurement sweeps). Set 0x0A1[D5] = 1 to enable the relevant function. Set 0x0A1[D1:D0] = m (0-3; affects iteration count). Write 0x0A4 for Settle (settling time = 0x0A4 + 1), 0x0A5 = 0x01, 0x0A6 = 0x01, and 0x0A9 = 0xFF (cal = 0x0A9 + 1 = 256).

Step 3 - Start TX quadrature calibration

Set 0x016[D4] = 1 (SXS046_tx_quad_calib). With both channels enabled, TX1 calibrates first and TX2 second, sequentially.

Step 4 - Wait for completion

Poll 0x016[D4] until it self-clears to 0.

Step 5 - Check convergence

Read 0x0A7 and 0x0A8. D1 = 1 indicates LO Conv (leakage convergence); D0 = 1 indicates SSB Conv (quadrature convergence). If convergence fails, adjust the NCO phase in 0x0A0 and repeat calibration.

Step 6 - Handle multiple output ports if required

TX_A and TX_B have separate calibration results. If both are used, select each port and calibrate it separately.

Step 7 - Retain results and exit

Results are saved automatically. If the LO later changes by more than 100 MHz or temperature changes significantly, return to ALERT and refresh calibration.

Timing estimate

```
TX_QuadCalTime = #TxChannels × 4 × (m + 2) × (Settle + 2) × cal
```

m = 0x0A1[D1:D0] (0-3), Settle = 0x0A4 + 1, and cal = 0x0A9 + 1. The clock is CLKRF (TX FIR output clock).

Typical calculation: m = 0, Settle = 4, cal = 256, two channels, CLKRF = 61.44 MHz.

```
TX_QuadCalTime = 2 × 4 × (0 + 2) × (4 + 2) × 256 / 61.44 MHz
= 2 × 4 × 2 × 6 × 256 / 61.44 MHz
= 24576 / 61.44 MHz = 400 µs
```

Configuration	One channel	Two channels
m = 0, Settle = 4, cal = 256, CLKRF = 61.44 MHz	~200 µs	~400 µs
m = 3, Settle = 4, cal = 256, CLKRF = 61.44 MHz	~500 µs	~1 ms
m = 0, Settle = 4, cal = 256, CLKRF = 30.72 MHz	~400 µs	~800 µs

Recommended allowance: ~1 ms for two channels.

3.13 RX Quadrature Calibration (RX Quad Cal)

Purpose: Minimize receive-path phase and gain errors.

Prerequisites: The device is in ALERT.

Key registers: 0x016, 0x169-0x16B, 0x057, 0x27A.

Mode 1 - One-shot calibration (recommended in Calibration Guide v2.0)

Step 1 - Confirm ALERT: Verify 0x017[3:0] = 5.

Step 2 - Disable Free Run: Write 0x169 = 0xC0 and confirm D3 (Free Run) = 0.

Step 3 - Power down the TX mixer: Write 0x057 = 0x33. This improves calibration results.

Step 4 - Reset TX VCO calibration logic: Write 0x27A[D6] = 0, then write D6 = 1.

Step 5 - Set the TX LO frequency: Set TX LO = RX LO + BBBW/2 so that it falls inside the RX passband. If the TX LO integer divider word is written, wait for TX VCO calibration to complete.

Step 6 - Start RX quadrature calibration: Write 0x016 = 0x20 (D5 = 1).

Step 7 - Wait for completion: Poll 0x016 until 0x016 = 0x00 (D5 self-clears).

Step 8 - Restore the TX LO frequency: Write 0x27A[D6] = 0, then D6 = 1 to reset TX VCO calibration logic. Restore the original TX LO operating frequency.

Step 9 - Re-enable the TX mixer: Write 0x057 = 0x30.

Step 10 - Handle multiple input ports: RF RX_A has separate results; RX_B and RX_C share a result set. If RX_A and RX_B/C are both used, select each and calibrate separately.

Mode 2 - Tracking calibration

Step 1 - Enable tracking: In 0x169, set D1 = 1 for CH2 tracking and D0 = 1 for CH1 tracking. Optionally set D3 = 1 for Free Run.

Step 2 - Enter RX or FDD: Tracking starts automatically when the ENSM enters RX or FDD. Allow a short settling period for initial convergence.

Step 3 - Monitor continuously: Tracking runs continuously, with no completion wait. The official customer software uses tracking mode only by default.

Timing estimate

Maximum one-shot calibration-time formula [S5]:

```
RX_QuadCalTime = #RxChannels × ([Decimation × (Settle + cal)] + SettleDC)
```

Decimation = 2048 when 0x169[2] = 0, or 2^(4+m) when 0x169[2] = 1 and 0 ≤ m ≤ 5. Settle = 0x16C; cal = 0x16D; SettleDC depends on 0x169[5:4].

Typical calculation: one channel, Decimation = 2048, Settle = 10, cal = 10, SettleDC = 0.

```
RX_QuadCalTime = 1 × (2048 × (10 + 10) + 0) / ClkRF
= 40960 / 61.44 MHz = 667 µs
```

Mode	Typical time
One-shot, one channel, defaults	TBC [S1]
One-shot, two channels, defaults	TBC [S1, S5]
Tracking	Continuous; initial convergence approximately TBC [S1]

One-shot calibration is accurate only for LO < 3 GHz. It is not recommended at ≥3 GHz.

Recommended allowance: 2 ms for one-shot; 500 µs for initial tracking convergence on entering RX.

3.14 TX Monitor DC Offset Calibration

Purpose: Calibrate DC offset in the TX Monitor (TX RSSI / power detection) path.

Prerequisites: The device is in ALERT. Required only when TX Monitor is used.

Key registers: 0x016, 0x187, 0x189, 0x18A.

Step 1 - Determine whether calibration is required

Run this calibration only if the system uses TX Monitor (TX RSSI / power detection). Otherwise, skip it.

Step 2 - Confirm ALERT

Verify 0x017[3:0] = 5.

Step 3 - Configure calibration parameters

Write 0x187[D3:D0] = CalTime. Confirm the controlled TxCount field mapping before programming 0x189/0x18A; the source bit-field and width descriptions conflict [S4].

Step 4 - Start TX Monitor DC calibration

Set 0x016[D2] = 1. The calibration state machine enters 0x8.

Step 5 - Wait for completion

Poll 0x016[D2] until it self-clears to 0.

Step 6 - Verify results

Results are stored automatically. Repeat calibration if the LO changes by more than 100 MHz.

Important limitations

TX Monitor uses part of the RX baseband path. It is intended only for TDD systems. In FDD mode, it overwrites the data of the selected RX input.

Timing estimate

```
TxDCCalTime = TxCount × (((CalTime + 1) × 4) + 1) ClkRF cycles
```

The exact TxCount bit mapping and width require confirmation [S4]. The following timing examples use the source numerical counts and do not establish a field definition. CalTime = 0x187[3:0] (4-bit, range 0-15).

Typical calculation: TxCount = 256, CalTime = 3, ClkRF = 61.44 MHz.

```
TxDCCalTime = 256 × (((3 + 1) × 4) + 1) / 61.44 MHz
= 256 × 17 / 61.44 MHz
= 4352 / 61.44 MHz = 70.8 µs
```

Configuration	Typical calibration time
TxCount = 256, CalTime = 3	~70 µs
TxCount = 512, CalTime = 7	~280 µs
TxCount = 1023, CalTime = 15	~1.1 ms

Recommended allowance: ~100 µs.

3.15 RX Gain-Step Calibration (GM/LNA Gain Step Cal)

Purpose: Calibrate LNA/mixer gain-step errors to improve RX RSSI accuracy and linearity.

Prerequisites: An external RF signal must be present at the RX input and the device must be in ALERT.

Key register: 0x016.

Step 1 - Determine whether calibration is required

Skip this calibration if the system does not use an external calibration signal source. It is primarily intended for factory calibration.

Step 2 - Confirm an external RF input signal

Do not run this calibration without an external RF signal at the RX input. Use a CW signal of known power or a standard test signal.

Step 3 - Confirm ALERT

Verify 0x017[3:0] = 5.

Step 4 - Start RX gain-step calibration

Set 0x016[D3] = 1. The calibration state machine enters 0x9.

Step 5 - Wait for completion

Poll 0x016[D3] until it self-clears to 0.

Step 6 - Record factory calibration data

Record the internal temperature-sensor reading during calibration and the gain-step error at each gain setting. Generate a LUT of temperature, gain slope and corrected expected values.

Step 7 - Apply in the field

The BBIC writes the factory-calibrated temperature, gain slope and corrected expected values to the device to improve RX RSSI absolute-power accuracy and linearity.

Execution order

Perform this calibration before calibrations associated with RX RSSI absolute power. Factory calibration is recommended; only the pre-calibrated data need to be loaded in the field.

Timing estimate

The duration depends on the internal state machine and number of gain settings. The official documentation does not provide an exact formula. The source gives these empirical estimates:

Configuration	Typical time
Standard gain table, one channel	TBC [S1]
Standard gain table, two channels	TBC [S1]
Split gain table	TBC [S1]

Recommended allowance: ~20 ms.

4. Calibration Timing Summary

Typical configuration: REF_CLK_IN = 40 MHz, LTE 10 MHz (BBBW = 5 MHz), two channels, ClkRF = 61.44 MHz and default calibration parameters.

No.	Operation	Type	Estimated time	Basis
0	Power-up and reset	Initialization	TBC [S1]	20 ms supply stabilization + SPI initialization
1	BBPLL VCO calibration	Automatic / manual	~50 µs	3 × (Counter + 128) / (REF_CLK × Scale)
2	Enter ALERT	State transition	TBC [S1]	Fixed 2-10 µs delay + synthesizer stabilization + polling
3	RF synthesizer charge pump calibration	Manual	~2 ms	36864 / (REF_CLK × Scale) × 2 channels [S2]
4	RF synthesizer VCO calibration	Automatic	~200 µs	Default FDD ~123.5 µs + PLL lock settling
5	RX BBF Tune	Manual	~25 µs	610 / f_RXTuneCLK + SPI overhead
6	TX BBF Tune	Manual	~15 µs	355 / f_TXTuneCLK + SPI overhead
7	RX TIA calibration	Parameter configuration	~10 µs	3 reads + calculation + 5 writes
8	TX secondary filter	Parameter configuration	~5 µs	Calculation + 4 writes
9	RX ADC setup	Parameter configuration	TBC [S1]	3 reads + calculation + 40 writes
10	Baseband DC calibration	State machine	~10 ms	((DCOffsetcount × CountSize) + WaitTime) × 25 / ClkRF
11	RF DC calibration	State machine	~15 ms	LengthOfEachAverage × numberOfAverages × GainIndexes / ClkRF
12	TX quadrature calibration	State machine	~1 ms	4 × (m + 2) × (Settle + 2) × cal × channel count / CLKRF
13	RX quadrature calibration	State machine / tracking	~2 ms	One-shot: Decimation × (Settle + cal) × channel count / ClkRF [S5]
14	TX Monitor DC calibration	State machine	~100 µs	TxCount × ((CalTime + 1) × 4 + 1) / ClkRF
15	RX gain-step calibration	State machine	~20 ms	Empirical; depends on gain settings and state machine

Typical total power-up initialization time

Scenario	Estimated total	Notes
Minimum configuration (optional calibrations skipped)	30-50 ms	Excludes items identified in the source as factory calibration (7, 8, 9, 15) and TX Monitor (14)
Standard configuration (full initialization calibration)	50-80 ms	Includes all initialization calibrations, excluding factory calibration
Full configuration (including factory calibration)	80-120 ms	Includes all calibrations

- These estimates include hardware calibration and typical SPI polling overhead.
- Actual total time also depends on SPI clock rate, MCU/DSP processing speed and the software polling strategy.
- Interrupts or control-output monitoring can reduce polling overhead.
- In TDD, if every TXNRX transition triggers VCO calibration, allow an additional TBC [S1] in the turnaround-time budget.

5. Precautions and Frequently Asked Questions

5.1 Do not change the calibration order

Calibrations have dependencies and must follow the official script order. In particular, RX BBF Tune must complete before RX TIA and RX ADC setup; charge pump calibration must precede VCO calibration; and ALERT is a prerequisite for every RF calibration.

5.2 Recommended TDD initialization

- Complete all initialization calibrations in FDD mode first.
- Restore TDD only after all calibrations finish (0x013[0] = 0).
- This substantially simplifies initialization and avoids repeated synthesizer power cycling in TDD.

5.3 Calibration result retention

- All calibration results are stored in SPI registers.
- They are retained while device power is maintained, including in SLEEP.
- After hardware reset or power cycling, all calibrations must be repeated.

5.4 Conditions requiring recalibration

Calibration	Trigger
BBPLL VCO	BBPLL frequency changes
RF Synth VCO	LO frequency changes; TXNRX transitions in TDD
RX/TX BBF Tune	Baseband bandwidth changes
RX TIA / TX secondary filter / RX ADC	Baseband bandwidth or ADC clock changes
RF DC / TX Quad / RX Quad / TX Monitor DC	LO change exceeds 100 MHz
TX Quad	Significant temperature change (can be monitored with AuxADC)

5.5 Two-channel operation

- Baseband DC and RF DC calibrations run in parallel on both channels. RX quadrature channel scheduling and timing require confirmation [S5]; do not assume either parallel operation or doubled duration.
- TX quadrature calibration runs TX1 first, then TX2, approximately doubling the time.
- RX gain-step calibration may run in parallel or sequentially, depending on the implementation.

5.6 Register-specific precautions

- 0x03F[D2]: BBPLL VCO calibration start bit; not self-clearing. Clear it manually.
- 0x1F8[D0]: Must be set to 0 for SXS046.
- 0x0D6[D0]: Must be set to 0 for SXS046.
- 0x016[D7:D6]: RX/TX BBF Tune is outside the calibration sequence state machine. Start it only when no other calibration is running.
- 0x169[D5:D4]: Selects the RX Quad SettleDC mode and affects calibration time.

5.7 Monitoring calibration

- SPI polling: Read the applicable completion bit; suitable for software control.
- Control output pins: Map calibration completion to CTRL_OUT for hardware monitoring.

• Interrupts: If supported by the BBIC, use interrupts to reduce polling overhead.

5.8 Timeout handling

Set a timeout for each calibration: timeout = estimated maximum duration × 2 (margin).

After a timeout, check: (1) reference-clock operation; (2) supply stability; (3) register configuration; and (4) whether all prerequisites are satisfied.

Appendix A. Calibration State-Machine States

Value	State name	Description
0x0	Calibration WAIT State	Waiting for calibration to start
0x1	Calibrations Done	All calibrations complete
0x2	Baseband DC Offset Calibration	Baseband DC calibration in progress
0x3	RF RX DC Offset Calibration	RF DC calibration in progress
0x4	TX1 Quadrature Calibration	TX1 quadrature calibration in progress
0x5	TX2 Quadrature Calibration	TX2 quadrature calibration in progress
0x6	RX1 Quadrature Calibration	RX1 quadrature calibration in progress
0x7	RX2 Quadrature Calibration	RX2 quadrature calibration in progress
0x8	Tx Monitor Calibration	TX Monitor DC calibration in progress
0x9	RX GM/LNA Gain Step Calibration	RX gain-step calibration in progress
0xA-0xF	Flush states	Flush / exit states

Appendix B. Key Register Reference

Register	Name	Key bits	Function
0x016	Calibration Control	D7-D0	Calibration start / status
0x017	State	D7:D4 = Cal State; D3:D0 = ENSM State	State monitoring
0x03F	BBPLL VCO Cal Start	D2	Start BBPLL VCO calibration
0x045	BBPLL Scale	D1:D0	BBPLL calibration Scale
0x04B	BBPLL Freq Cal	D7 = Enable; D6:D5 = Counter	BBPLL calibration configuration
0x05E	BBPLL Lock	D7	BBPLL lock indication
0x23D	RX CP Cal	D2	Start RX charge pump calibration
0x244	RX CP Cal Status	D7 = Valid; D5 = Done; D4 = Busy	RX CP calibration status
0x247	RX PLL Lock	D1	RX PLL lock
0x27D	TX CP Cal	D2	Start TX charge pump calibration
0x284	TX CP Cal Status	D7 = Valid; D4 = Busy	TX CP calibration status
0x287	TX PLL Lock	D1	TX PLL lock
0x1F8	RXBBF Divide LSB	D7:D0	RX BBF divider low 8 bits
0x1F9	RXBBF Divide MSB	D0	RX BBF divider ninth bit
0x1FB	BBBW MHz	D7:D0	Integer MHz part of BBBW
0x1FC	BBBW kHz	D6:D0	kHz part of BBBW
0x0D6	TXBBF Divide LSB	D7:D0	TX BBF divider low 8 bits
0x0D7	TXBBF Divide MSB	D0	TX BBF divider ninth bit
0x169	RX Quad Config	D5:D0	RX quadrature calibration configuration

Translation Notes

These notes record the treatment of issues in the supplied source. RevC is a customer reference revision, not a new silicon qualification report.

[S1] Malformed timing ranges

The source contains joined timing values with missing range separators. These are replaced by TBC in the operational text. No missing separator is inferred. Other illustrative timing estimates are retained as source estimates, not guaranteed limits; use completion indicators and confirm timeout budgets.

[S2] Charge pump Scale behavior

The source cycle expression has been replaced by the dimensionally consistent expression used in its worked example. At Scale = 1, the example yields 921.6 µs per channel at 40 MHz. Non-default Scale table values conflict with that expression and are withheld pending confirmation. This change does not establish the correct hardware Scale semantics.

[S3] RF DC arithmetic

The source incorrectly substituted 1280 for 4 × 256. RevC uses 1024, giving 1289 cycles per average and 21913 cycles per evaluated gain index. For 25 total evaluated indexes, the illustrative time is 547825 / 61.44 MHz, approximately 8.916 ms. The actual number of evaluated indexes, including the extra index in the general formula, remains configuration-dependent.

[S4] TX Monitor counter definition

The source concatenates four bits and eight bits but calls the result 10-bit (0-1023). RevC withholds an authoritative field mapping pending the controlled register definition. Numerical timing examples are retained only as illustrations.

[S5] RX quadrature timing

The source one-shot formula scales with channel count, while its later text claims parallel execution without doubled time. RevC identifies the scheduling/timing as unresolved. The single-channel example is not a dual-channel timing guarantee.

[S6] SXS046 even-divider examples

The SXS046 source explicitly permits clearing divider bit 0. RevC applies this method to odd values in the example tables: RX 31 becomes 30; TX 7 becomes 6. Corresponding tune-clock frequencies and ideal search durations are recalculated from BBPLL/divider and 610 or 355 tune-clock cycles. These are formula-derived examples, not new bench measurements or bandwidth-accuracy guarantees. Do not apply this manual to SXS055 without device-specific confirmation.

ADC equation evaluation order

All 40 configuration equations are retained. data[10] is evaluated before data[9]; writing the completed array still proceeds from 0x200 to 0x227.

End of document.