SXA003

14-Bit, 250 MSPS A/D Converter

14 位 250MSPS A/D 转换器

14-bit | 1 channel | 250 MSPS | QFN48 | Parallel LVDS

14位 | 单通道 | 250MSPS | QFN48 | 并行LVDS

对标 / Cross Reference: AD4149 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXA003 14-Bit 250MSPS A/D Converter — Product Specification & User Manual

SXA003 型 14 位 250MSPS A/D 转换器产品说明书、使用手册

深信科技 / Shenzhen Shenxin Technology Co., Ltd. 版本 / Revision: V1.20260727 对标 / Cross Reference: AD4149 — pin-to-pin compatible alternative

联系方式 / Contact: Felix (Flip) Lai, CEO ｜ 邮箱 / Email: felix@shenxinic.com ｜ 电话 / Tel: +852 51367095 ｜ 官网 / Website: shenxinic.com

版本修订记录 / Revision History

版本号 / Version	发布日期 / Date	更改章节 / Changed Section	更改说明 / Description	备注 / Note
V1.20260727	20260727	——	首次发布 / Initial release	

1. 产品用途及应用范围 / Applications

- 无线、宽带通信 / Wireless and broadband communications
- 接收器 / Receivers
- 通信测试设备 / Communications test equipment

2. 标准 / Standards

- 详细规范及确认号：Q/GC 0222-2026《半导体集成电路 SXA003 型 14 位 250MSPS A/D 转换器详细规范》 Detailed specification and approval ref.: Q/GC 0222-2026, Semiconductor Integrated Circuit — Detailed Specification for SXA003 14-bit 250MSPS A/D Converter
- 质量等级：企标 / Quality grade: Enterprise standard

3. 产品特点 / Features

- 电源电压包括：1.8V / Supply voltage: 1.8V
- 分辨率：14bit / Resolution: 14-bit
- 转换速率：250MSPS / Conversion rate: 250MSPS
- SNR：68dBFS@10M（典型值）/ SNR: 68dBFS @10M (typical)
- SFDR：78dBFS@10M（典型值）/ SFDR: 78dBFS @10M (typical)
- DNL：±0.6LSB（典型值）/ DNL: ±0.6LSB (typical)
- INL：±4LSB（典型值）/ INL: ±4LSB (typical)
- 功耗：≤0.45W / Power dissipation: ≤0.45W

- 输入数据接口：LVDS / Input data interface: LVDS
- ESD 等级：1C 级，HBM 模型：1000V / ESD rating: Class 1C, HBM 1000V
- 产品重量：0.90g±0.09g / Weight: 0.90g±0.09g

4. 产品描述 / Product Description

SXA003 型高速高精度 14 位 250MSPS A/D 转换器是采用 CMOS 工艺制造的单片集成电路，采样率最高可达 250 MSPS。该模数转换器利用新的设计方法在获得高的动态性能的同时，也能在 1.8V 的电源电压下获得超低功耗。它适用于多载波的宽带通信应用。图 1 为 SXA003 型 A/D 转换器的原理图。该电路主要包括多级流水线，输出驱动电路，内部基准产生电路、时钟稳定电路、控制逻辑、数字校正电路以及输出驱动电路等。

The SXA003 is a monolithic, high-speed, high-precision 14-bit 250MSPS A/D converter fabricated in a CMOS process, with a maximum sampling rate of 250 MSPS. Using a new design approach, this analog-to-digital converter achieves high dynamic performance together with ultra-low power consumption at a 1.8V supply voltage. It is suitable for multi-carrier broadband communications applications. Figure 1 is the schematic diagram of the SXA003 A/D converter. The circuit mainly consists of a multi-stage pipeline, an output driver circuit, an internal reference generation circuit, a clock stabilization circuit, control logic, a digital correction circuit, and an output driver circuit.

该产品采用 48 引线塑料片式载体封装（QFN48）。该产品功能框图如图 1 所示。

The device is packaged in a 48-lead plastic chip carrier package (QFN48). The functional block diagram of the device is shown in Figure 1.

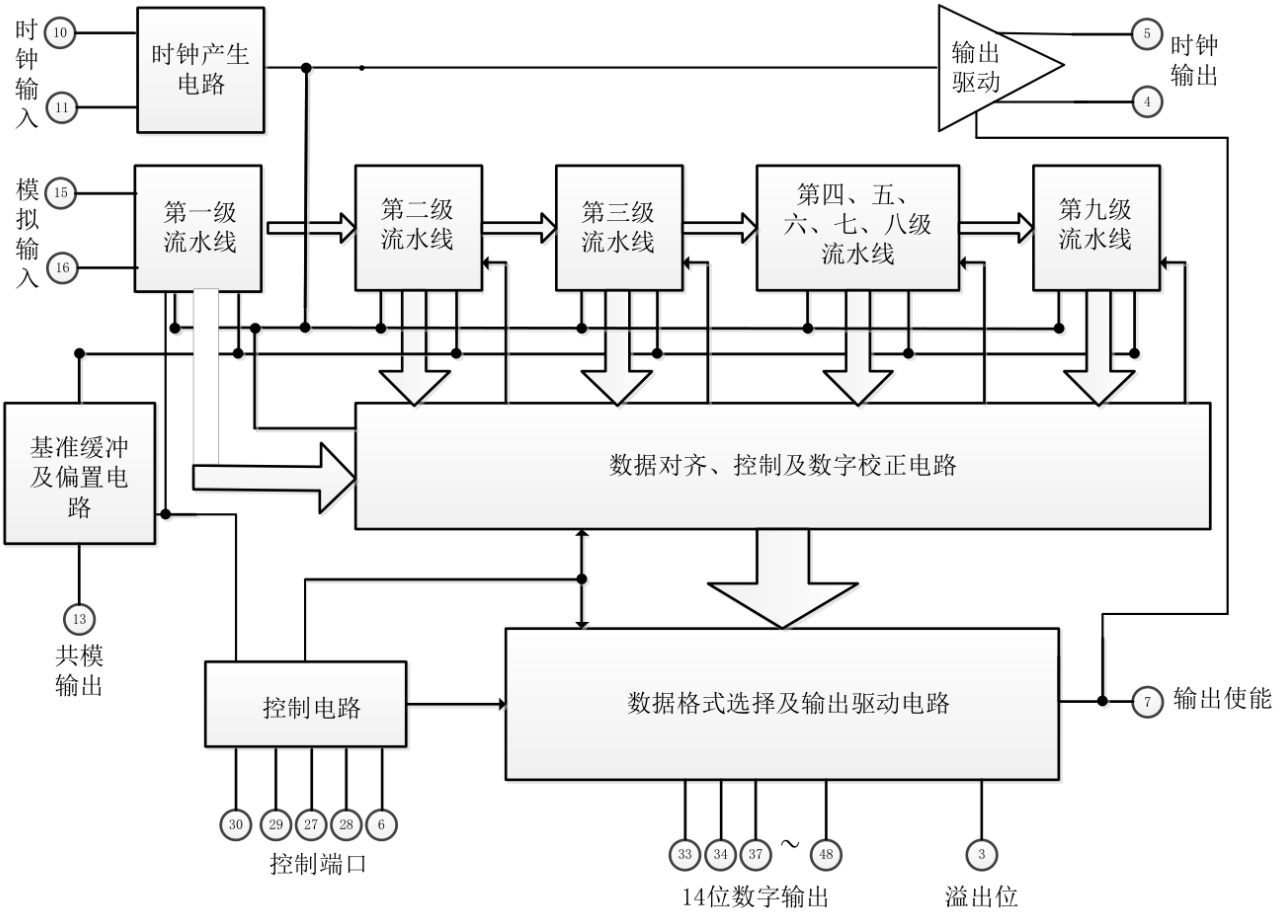


Figure 1: 功能框图

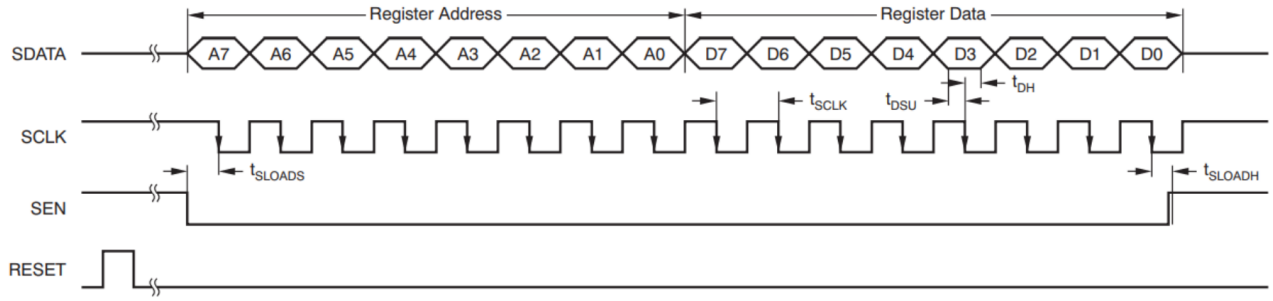


Figure 2: 串行接口时序

5. 产品外形图和实物图片 / Package Outline and Physical Pictures

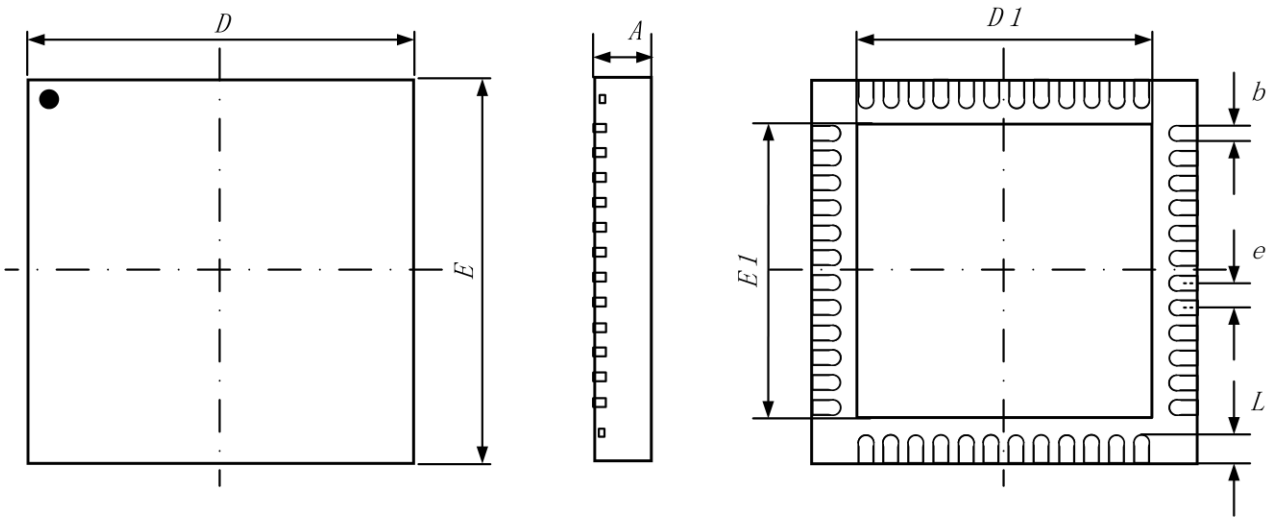


Figure 3: 产品外形尺寸图

产品外形尺寸 / Package Dimensions

单位为毫米 / Dimensions in mm

尺寸符号 / Symbol	数值 / Value			尺寸符号 / Symbol	数值 / Value		
	最小 / Min	公称 / Nom	最大 / Max		最小 / Min	公称 / Nom	最大 / Max
A	0.70	0.85 a	0.90	D	6.90	7.00 a	7.10
b	0.18	0.25 a	0.30	D1	5.20	5.30 a	5.50
e	—	0.50	—	E	6.90	7.00 a	7.10
L	0.35	0.40 a	0.45	E1	5.20	5.30 a	5.50

a 外壳实际公称值，推荐用户参考该尺寸设计使用； a: Actual nominal value of the package; users are recommended to refer to these dimensions for design.

注：推荐焊盘设计详见电装说明。 Note: See the assembly instructions for recommended pad layout.

6. 引出端排列（俯视图）/ Pin Arrangement (Top View)

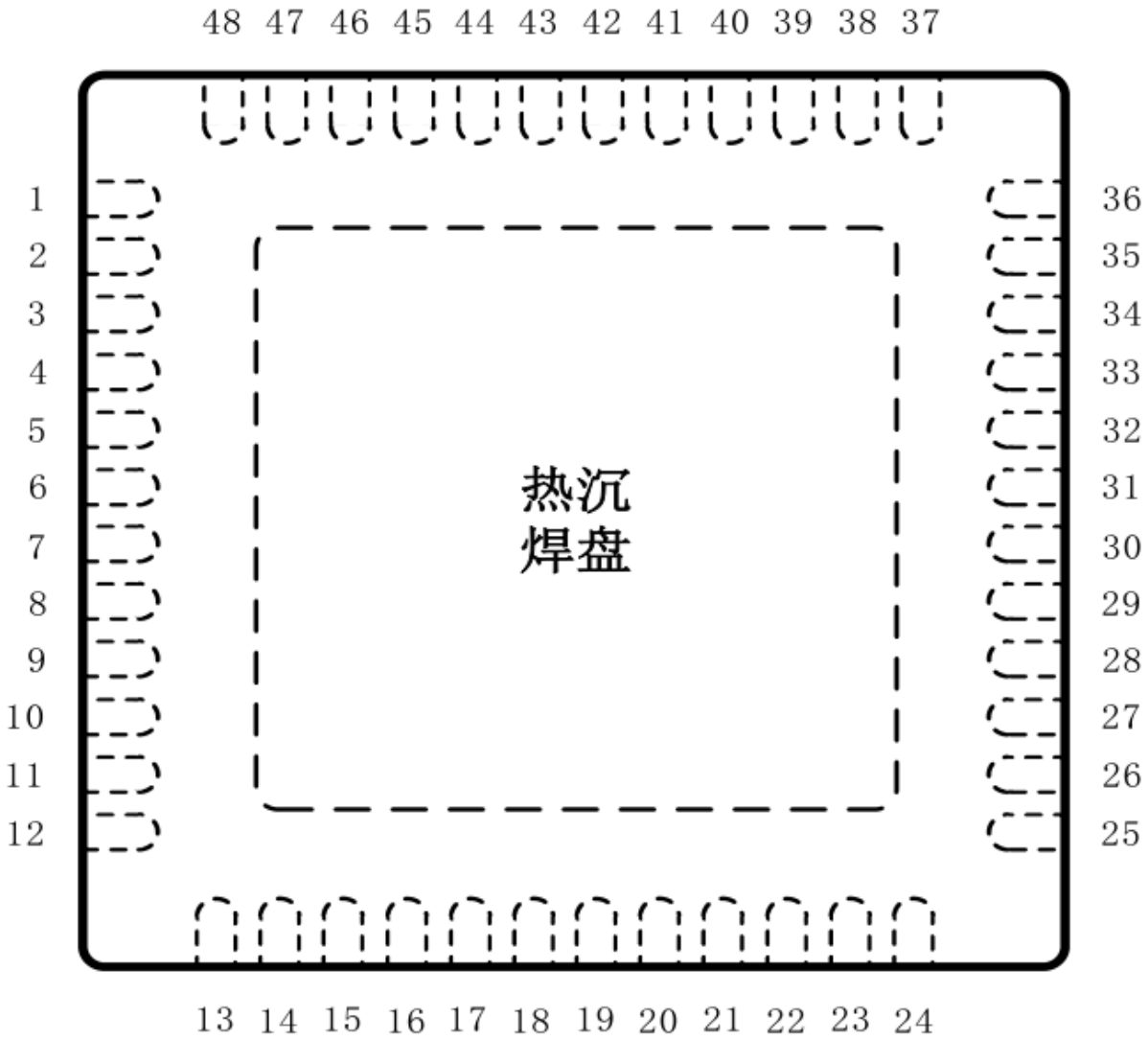


Figure 4: 引出端排列

7. 引出端功能符号表 / Pin Function Table

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
1	GNDD	数字地 / Digital ground	/	25	GNDA	模拟地 / Analog ground	/
2	VDDD	数字电源 / Digital supply	/	26	VDDA	模拟电源 / Analog supply	/
3	QOR	溢出位 / Over-range bit	O	27	SEN	串行接口使能 / Serial interface enable	I
4	QCLK+	时钟输出正 / Clock output, positive	I	28	SDATA	串行接口数据输入 / Serial interface data input	I
5	QCLK-		I	29	SCLK		I

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
		时钟输出负 / Clock output, negative				串行接口时钟输入 / Serial interface clock input	
6	DFS	输出数据格式 / Output data format	I	30	RESET	复位 / Reset	I
7	OE	输出使能 / Output enable	I	31	DNC	悬空 / No connect	/
8	VDDA	模拟电源 / Analog supply	/	32	DNC	悬空 / No connect	/
9	GNDA	模拟地 / Analog ground	/	33	DD0-/DD1-	D0、D1 输出负端 / D0, D1 output, negative	O
10	INCLK+	差分时钟输入正 / Differential clock input, positive	I	34	DD0+/ DD1+	D0、D1 输出正端 / D0, D1 output, positive	O
11	INCLK-	差分时钟输入负 / Differential clock input, negative	I	35	VDDD	数字电源 / Digital supply	/
12	GNDA	模拟地 / Analog ground	/	36	GNDD	数字地 / Digital ground	/
13	VCM	共模输出 / Common-mode output	O	37	DD2-/DD3-	D2、D3 输出负端 / D2, D3 output, negative	O
14	GNDA	模拟地 / Analog ground	/	38	DD2+/ DD3+	D2、D3 输出正端 / D2, D3 output, positive	O
15	IN+	差分模拟输入正 / Differential analog input, positive	I	39	DD4-/DD5-	D4、D5 输出负端 / D4, D5 output, negative	O
16	IN-	差分模拟输入负 / Differential analog input, negative	I	40	DD5+/ DD5+	D4、D5 输出正端 / D4, D5 output, positive	O
17	GNDA	模拟地 / Analog ground	/	41	DD6-/DD7-	D6、D7 输出负端 / D6, D7 output, negative	O
18	VDDA	模拟电源 / Analog supply	/	42	DD6+/ DD7+	D6、D7 输出正端 / D6, D7 output, positive	O
19	GNDA	模拟地 / Analog ground	/	43	DD8-/DD9-	D8、D9 输出负端 / D8, D9 output, negative	O
20	VDDA	模拟电源 / Analog supply	/	44	DD8+/ DD9+	D8、D9 输出正端 / D8, D9 output, positive	O
21	DNC	悬空 / No connect	/	45	DD10-/ DD11-	D10、D11 输出负端 / D10, D11 output, negative	O
22	VDDA	模拟电源 / Analog supply	/	46	DD10+/ DD11+	D10、D11 输出正端 / D10, D11 output, positive	O
23	DNC	备用 / Spare	/	47	DD12-/ DD13-	D12、D13 输出负端 / D12, D13 output, negative	O
24	VDDA	模拟电源 / Analog supply	/	48	DD12+/ DD13+	D12、D13 输出正端 / D12, D13 output, positive	O

注：封装底部的热沉焊盘为模拟地端 GNDA。 Note: The thermal pad at the package bottom is analog ground GNDA.

8. 推荐工作条件 / Recommended Operating Conditions

- 工作频率（fCLK）：80MHz~250MHz / Operating frequency (fCLK): 80MHz–250MHz
- 模拟电源电压（VDDA）：1.75V~1.85V / Analog supply voltage (VDDA): 1.75V–1.85V
- 数字电源电压（VDDD）：1.75V~1.85V / Digital supply voltage (VDDD): 1.75V–1.85V
- 输入信号幅度范围（峰峰值）：≤2V / Input signal amplitude range (peak-to-peak): ≤2V
- 工作环境温度（TA）：-40°C~85°C / Operating ambient temperature (TA): -40°C to 85°C

9. 绝对最大额定值 / Absolute Maximum Ratings

- 模拟电源电压（VDDA）：0.3V~2.1V / Analog voltage (VDDA): 0.3V–2.1V
- 数字电源电压（VDDD）：-0.3V~2.1V / Digital voltage (VDDD): -0.3V–2.1V
- 贮存温度（Tstg）：-65°C~150°C / Storage temperature (Tstg): -65°C to 150°C
- 结温（TJ）：150°C / Junction temperature (TJ): 150°C

---

10. 性能指标 / Performance Specifications

除另有规定外，VDDA=1.8V，VDDD=1.8V，fCLK=250MHz，fIN=10MHz，GNDD=GNDA=0V，模拟输入范围：2VP-P，-40°C≤TA≤85°C。 Unless otherwise specified, VDDA=1.8V, VDDD=1.8V, fCLK=250MHz, fIN=10MHz, GNDD=GNDA=0V, analog input range: 2VP-P, -40°C ≤ TA ≤ 85°C.

参数 / Parameter	符号 / Symbol	条件 / Condition	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
分辨率 / Resolution	RES	fCLK=250MHz，fIN=10MHz	—	14	—	bit
线性误差 / Integral linearity error	EL	fCLK=250MHz，fIN=10MHz	-7	±4	7	LSB
微分误差 / Differential linearity error	EDL	fCLK=250MHz，fIN=10MHz	-1	±0.6	2	LSB
失调误差 / Offset error	EO	—	-15	3	15	mV
增益误差 / Gain error	EG	—	-10	2	+10	%FS
逻辑输入高电平 / Logic input high	VIH	—	1.5	1.5	—	V
逻辑输入低电平 / Logic input low	VIL	—	—	0.3	0.3	V
输入高电平电流 / Input high current	IIH	SDATA 引脚 / SDATA pin	-15	11	15	uA
输入低电平电流 / Input low current	IIL	—	-2	-0.1	2	uA
共模输出电压 / Common-mode output voltage	VCM	—	0.9	0.97	1.05	V
信噪比 / SNR	SNR	fCLK=250MHz，fIN=10MHz； fCLK=250MHz，fIN=170MHz	62	68	—	dB
无杂散动态范围 / SFDR	SFDR	fCLK=250MHz，fIN=10MHz； fCLK=250MHz，fIN=170MHz	65	78	—	dB
信噪失真比 / SINAD	SINAD	fCLK=250MHz，fIN=10MHz； fCLK=250MHz，fIN=170MHz	62	64	—	dB

参数 / Parameter	符号 / Symbol	条件 / Condition	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
有效位数 / ENOB	ENOB	fCLK=250MHz，fIN=10MHz	10	11	—	bit
LVDS 差分输出电压 / LVDS differential output voltage	VOD	LVDS 模式（350mV）/ LVDS mode (350mV)	270	350	430	mV
LVDS 共模输出电压 / LVDS common-mode output voltage	VOS	—	0.85	1	1.25	V
模拟电源电流 / Analog supply current	ICC	LVDS 模式（350mV）/ LVDS mode (350mV)	—	138	150	mA
数字电源电流 / Digital supply current	IDD	—	—	70	80	mA
功耗 / Power dissipation	PD	—	—	0.36	0.45	W
休眠功耗 / Power-down power	PDWN	—	—	5	25	mW
时钟周期 / Clock period	tCLK	80MHz≤fCLK≤250MHz a	4	10	12.5	ns
时钟高脉冲宽度 / Clock high pulse width	tCLKH	80MHz≤fCLK≤250MHz a	2	5	6.25	ns
时钟低脉冲宽度 / Clock low pulse width	tCLKL	80MHz≤fCLK≤250MHz a	2	5	6.25	ns
占空比 / Duty cycle	ODC	LVDS 模式（350mV）/ LVDS mode (350mV)	42	50	58	%

a 原表中该条件为跨行合并单元格，覆盖 tCLK、tCLKH、tCLKL 三行。 a: In the source table this condition is a vertically merged cell spanning the tCLK, tCLKH, and tCLKL rows.

注：典型值为常温测试数据。 Note: Typical values are room-temperature test data.

11. 主要特性曲线图（电特性测试图）/ Typical Performance Curves (Electrical Test Plots)

1. fCLK=250MHz，fin=10MHz 条件下频谱图 / Spectrum at fCLK=250MHz, fin=10MHz

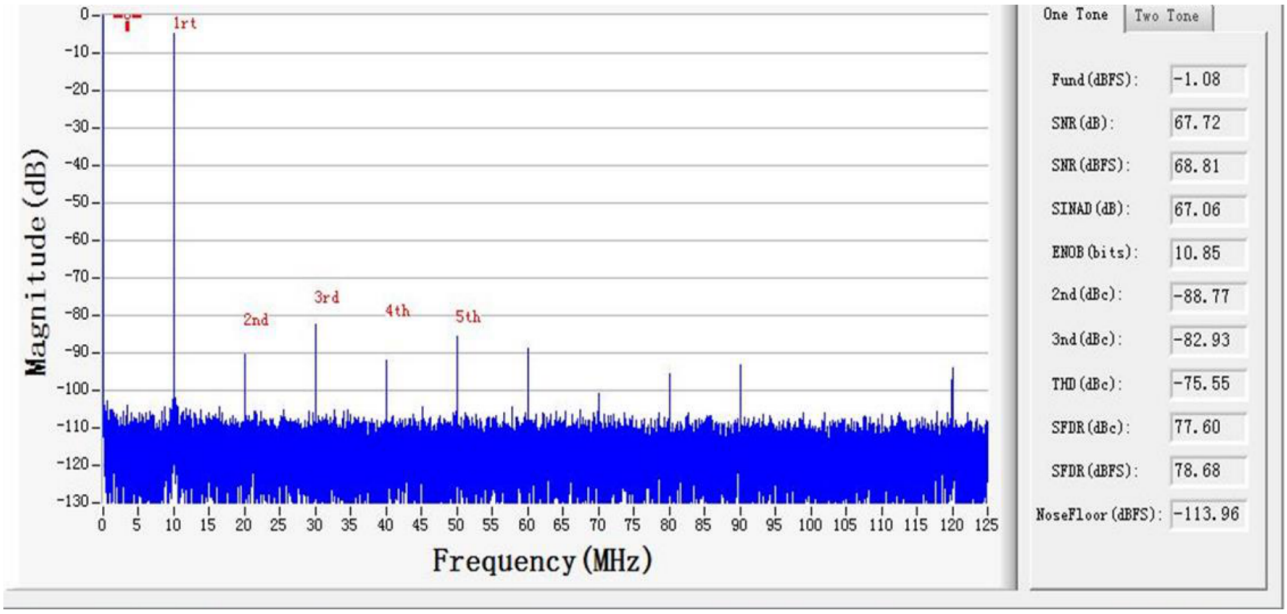


Figure 5: fCLK=250MHz，fin=10MHz FFT 谱线

1. fCLK=250MHz，fin=70MHz 条件下频谱图 / Spectrum at fCLK=250MHz, fin=70MHz

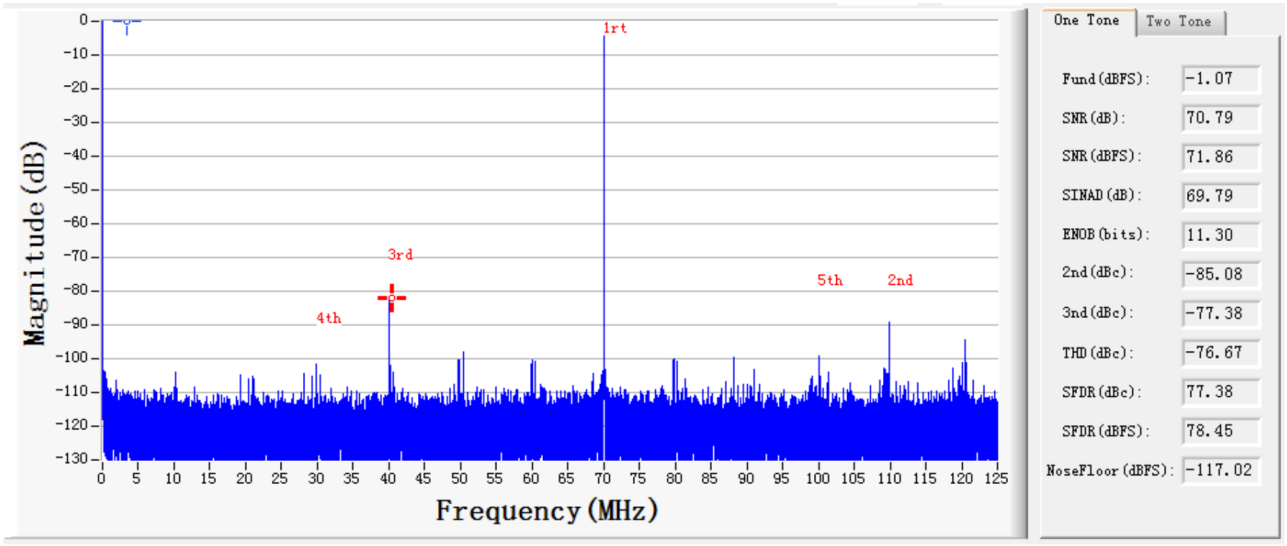


Figure 6: fCLK=250MHz，fin=70MHz FFT 谱线

1. fCLK=250MHz，fin=170MHz 条件下频谱图 / Spectrum at fCLK=250MHz, fin=170MHz

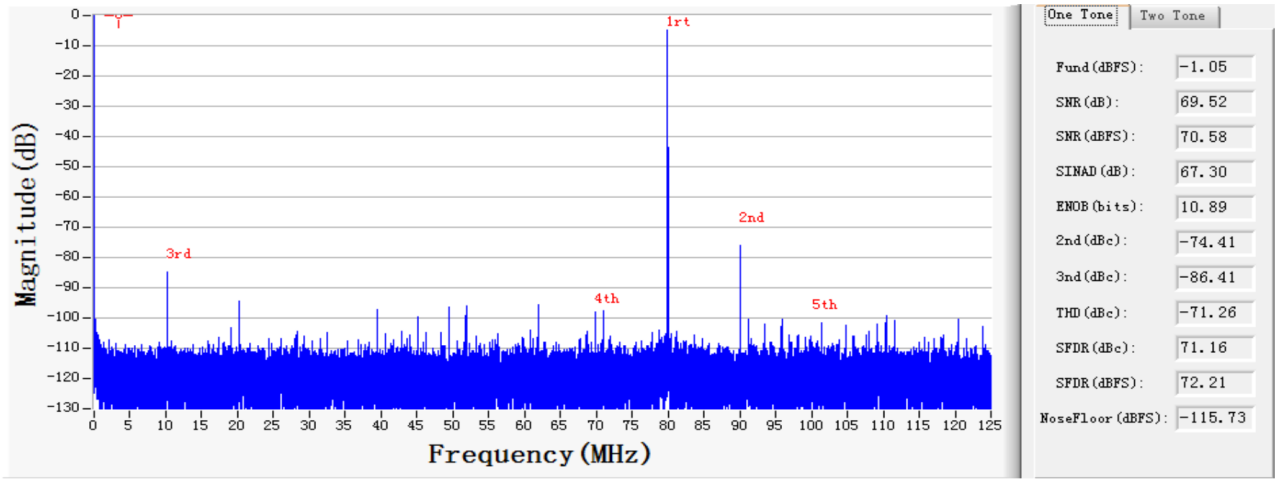


Figure 7: fCLK=250MHz，fin=170MHz FFT 谱线

1. 微分非线性误差和积分非线性误差图 / Differential and integral nonlinearity plots

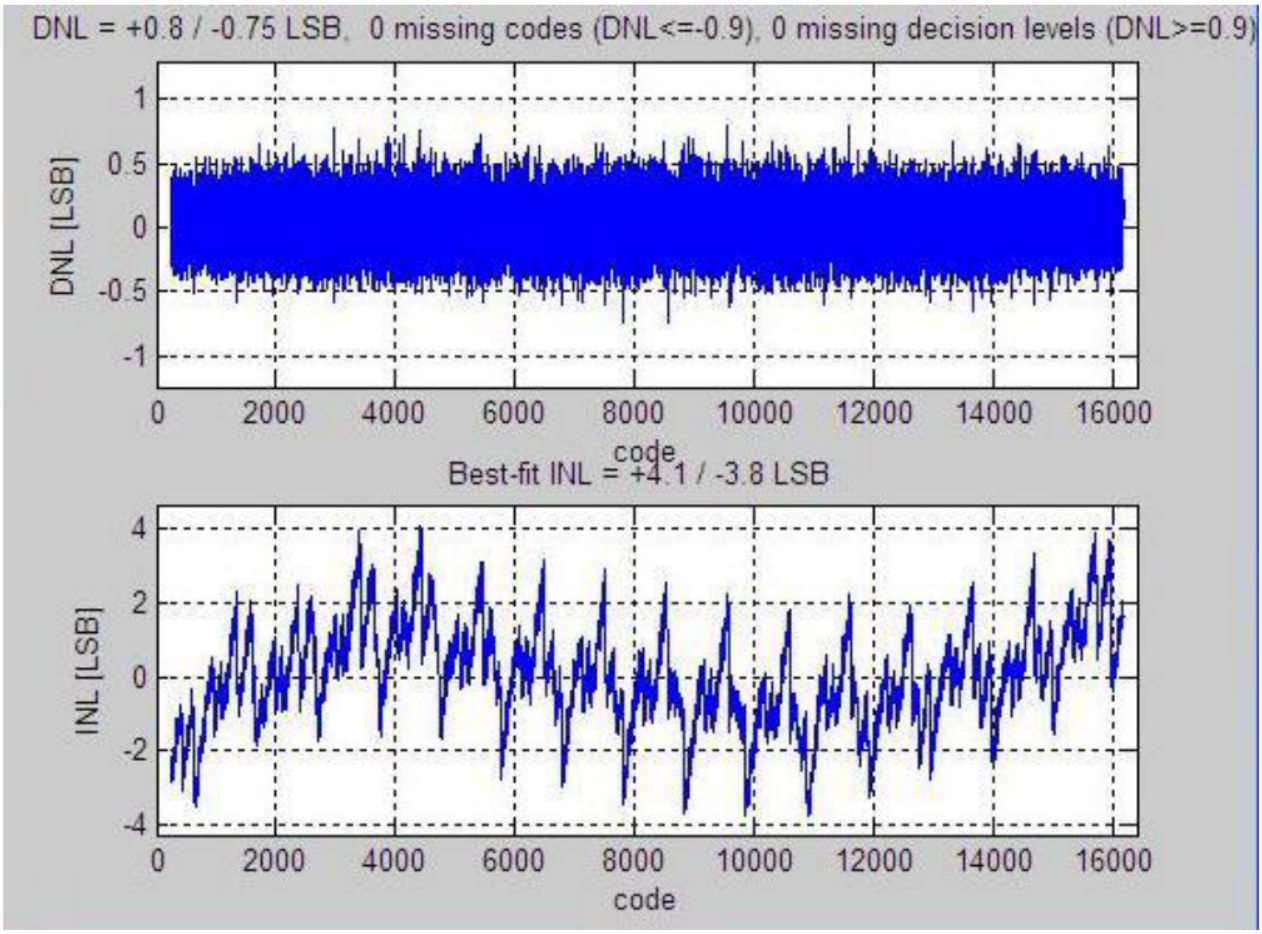


Figure 8: fCLK=250MHz，fin=10MHz DNL 和 INL

12. 典型应用线路图 / Typical Application Circuits

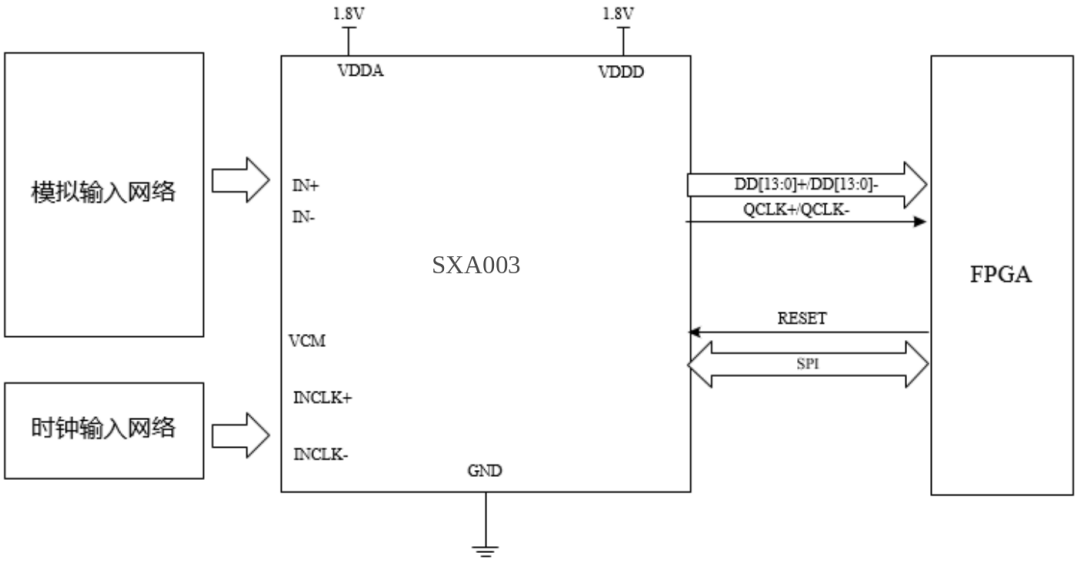


Figure 9: SXA003 典型外围电路图

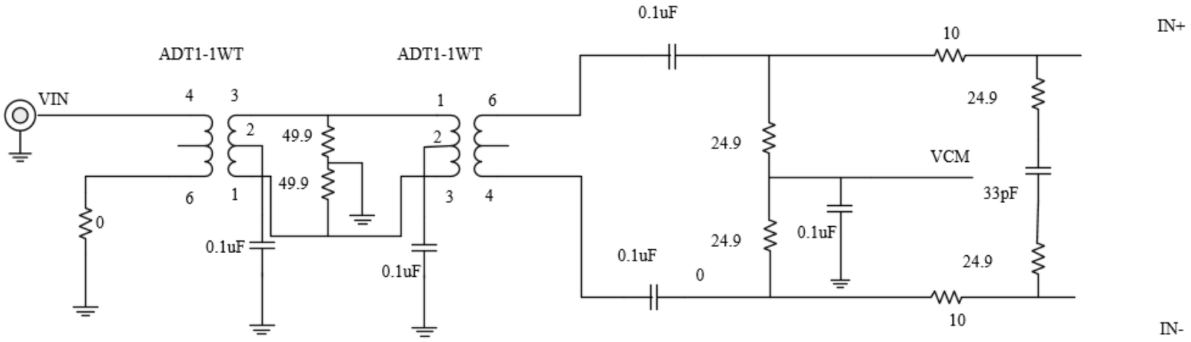


Figure 10: 模拟前端电路

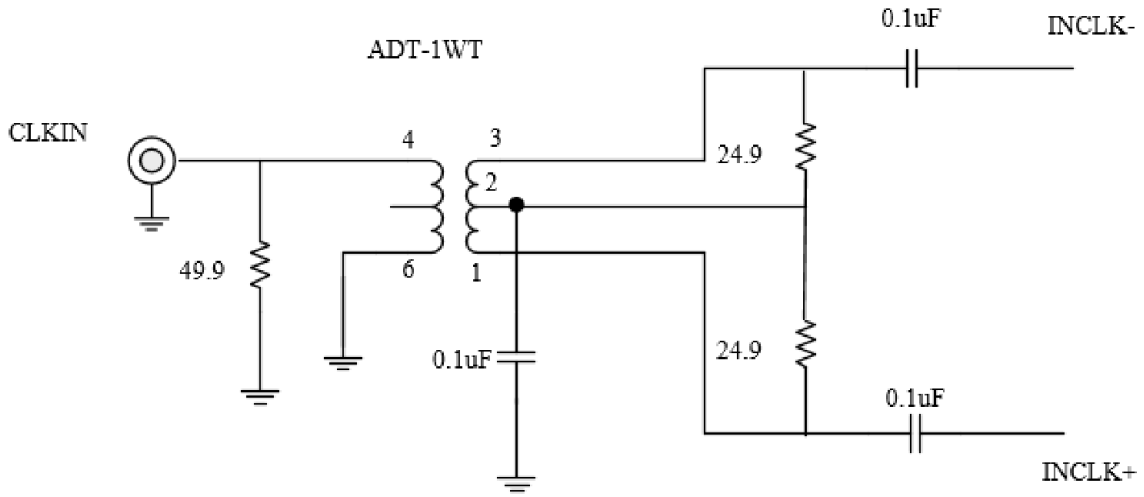


Figure 11: 时钟前端电路

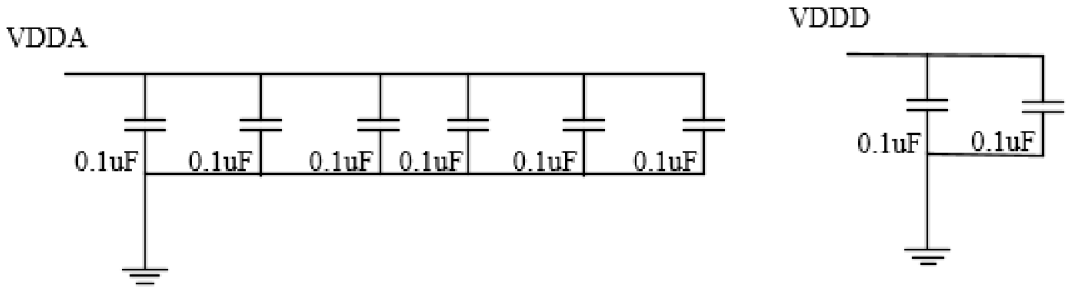


Figure 12: 电源滤波

13. 单元模块及工作原理 / Functional Blocks and Theory of Operation

13.1 原理概述 / Overview

SXA003 型高速高精度 14 位 A/D 转换器是采用 CMOS 工艺制造的半导体集成电路。该产品具有采样率高、线性误差小、失调增益校正和 SPI 接口控制等特点。通过 SPI 接口可对内部电路的工作状态、输入失调和满度输入范围进行配置；模拟输入为差分输入，既可交流耦合输入也可直流耦合输入；时钟输入电路内部设有直流偏置，必须交流耦合输入。

The SXA003 high-speed, high-precision 14-bit A/D converter is a semiconductor integrated circuit fabricated in a CMOS process. The device features a high sampling rate, small linearity error, offset and gain correction, and SPI interface control. The operating state of the internal circuits, the input offset, and the full-scale input range can be configured through the SPI interface. The analog input is a differential

input, which can be either AC-coupled or DC-coupled; the clock input circuit has an internal DC bias and must be AC-coupled.

13.2 模拟输入 / Analog Input

模拟输入包含一个差分的基于开关电容的采样保持结构，如图 13 所示。差分结构在高频输入时有更好的 AC 特性。差分输入 INP 和 INM 的共模电压为 0.95V，由片内引脚 VCM 提供。差分的最大输入摆幅为 2VPP。

The analog input contains a differential switched-capacitor sample-and-hold structure, as shown in Figure 13. The differential structure provides better AC characteristics at high-frequency inputs. The common-mode voltage of the differential inputs INP and INM is 0.95V, provided by the on-chip VCM pin. The maximum differential input swing is 2VPP.

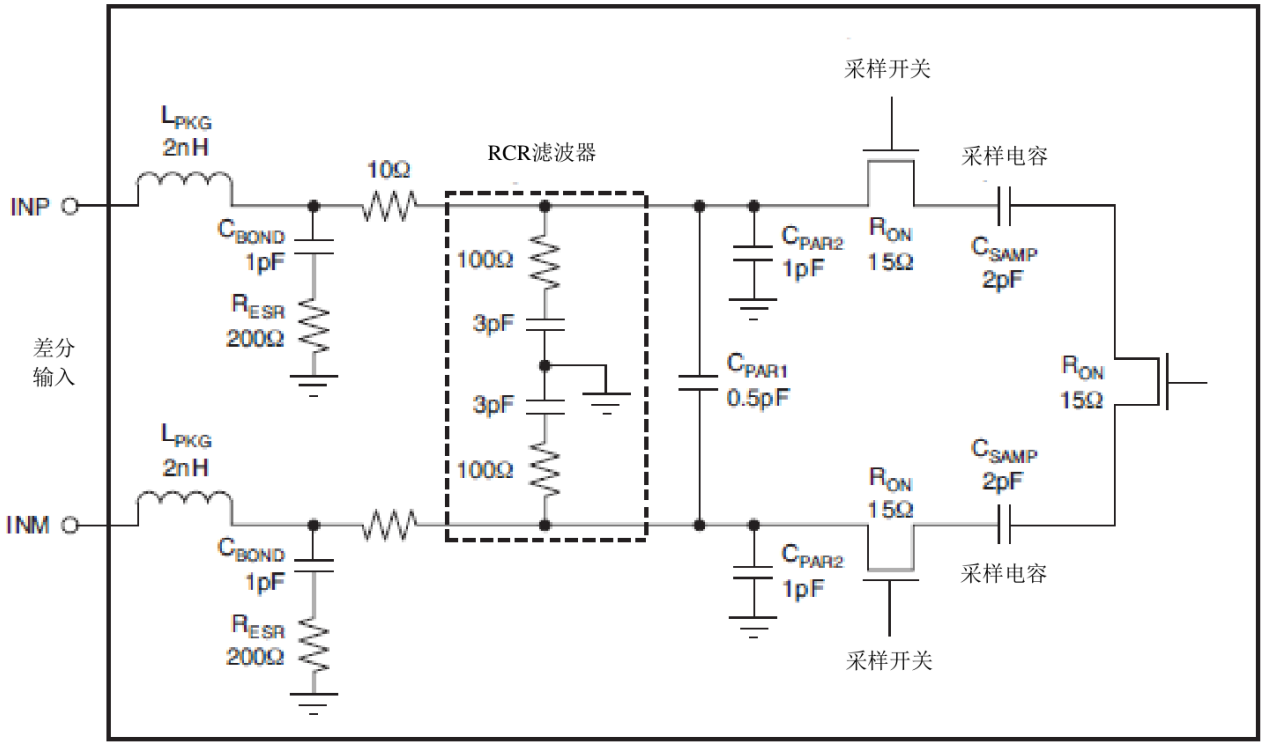


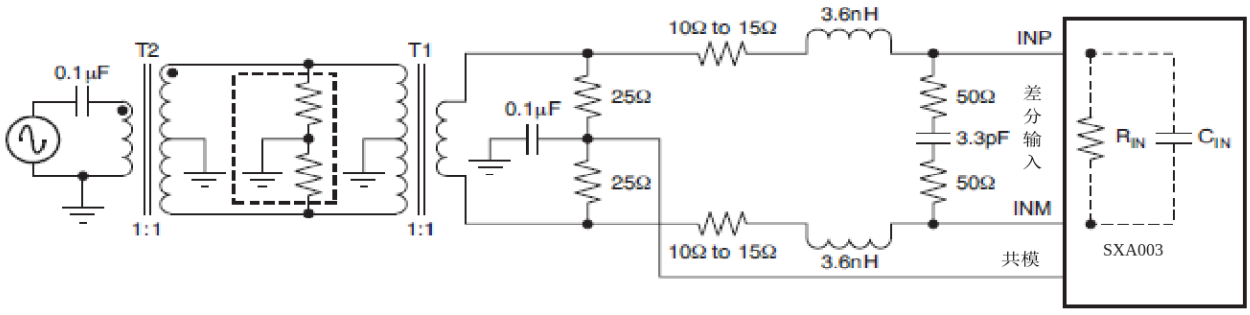
Figure 13: 模拟输入端等效电路

13.3 驱动电路 / Driver Circuit

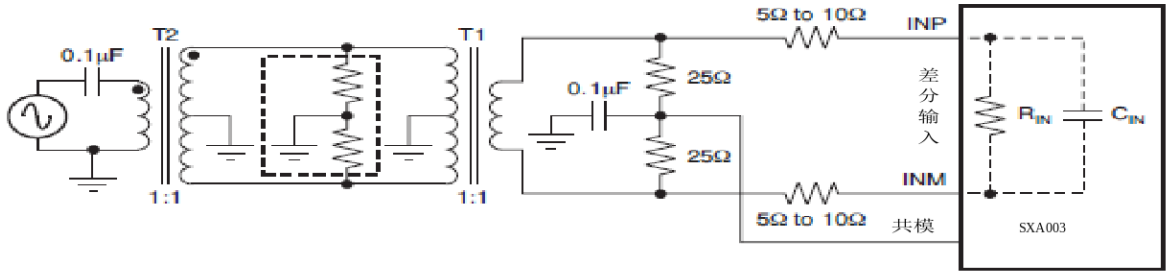
图 14（a）和图 14（b）展示了驱动电路的两种配置情况：一个是从低带宽方面进行优化的，另一个则是从高带宽（以支持高输入频率）方面进行优化的。在图 14（a）中，使用 3.3pF 的外部 R-C-R 滤波器来帮助吸收采样干扰脉冲。R-C-R 滤波器限制了驱动电路的带宽，使其适用于低输入频率（最高 250MHz）。对于更高的输入频率，R-C-R 滤波器下降，与较低的串联电阻（5Ω 到 10Ω）一起，该驱动电路提供更高的带宽，以支持高达 500MHz 的频率，如图 14（b）。

Figure 14(a) and Figure 14(b) show two configurations of the driver circuit: one optimized for low bandwidth, and the other optimized for high bandwidth (to support high input frequencies). In Figure 14(a), an external 3.3pF R-C-R filter is used to help absorb sampling glitch pulses. The R-C-R filter limits the bandwidth of the driver circuit, making it suitable for low input frequencies (up to 250MHz). For higher

input frequencies, the R-C-R filter is reduced, and together with a lower series resistance (5Ω to 10Ω), this driver circuit provides higher bandwidth to support frequencies up to 500MHz, as shown in Figure 14(b).



(a) 低频



(b) 高频

Figure 14: 模拟输入驱动电路

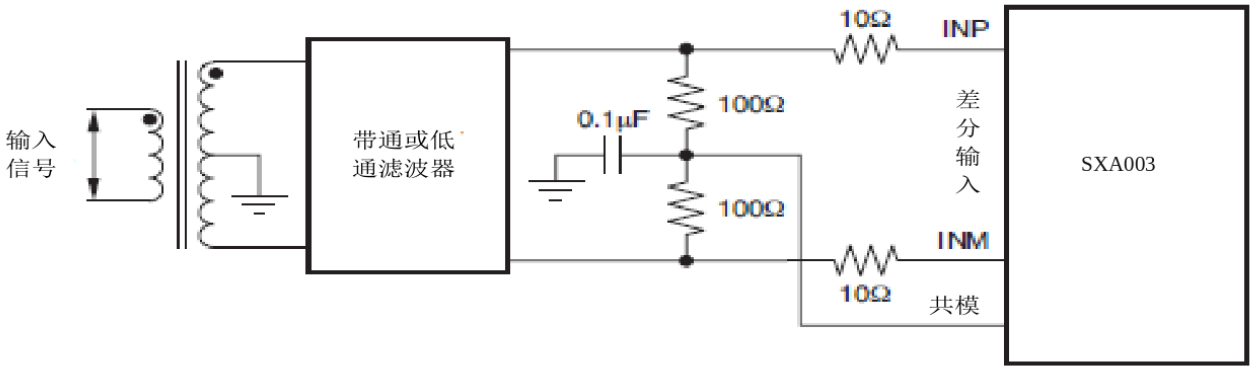


Figure 15: 1：4 的变压器驱动电路

在各种情形下，为获得需要的动态性能，需要有带通或者低通的滤波器辅助，如图 15 所示。这样的一个滤波器在高频时有较低的源阻抗，有利于吸收采用尖峰，同时又不会造成性能的衰减。

In all cases, a band-pass or low-pass filter is needed to assist in obtaining the required dynamic performance, as shown in Figure 15. Such a filter has a low source impedance at high frequencies, which helps absorb sampling spikes without degrading performance.

13.4 时钟输入 / Clock Input

SXA003 的输入时钟可以差分（正弦、LVPECL 或者 LVDS）也可以单端（LVCMOS）驱动。当用正弦时钟信号时，驱动电路可以采用变压器耦合的；当用 LVPECL 或者 LVDS 的时钟信号源时，驱动电路可以采用交流耦合的。输入时钟的等效电路如图 16 所示。

The input clock of the SXA003 can be driven differentially (sine wave, LVPECL, or LVDS) or single-ended (LVCMOS). With a sine-wave clock signal, the driver circuit can be transformer-coupled; with an LVPECL or LVDS clock source, the driver circuit can be AC-coupled. The equivalent circuit of the input clock is shown in Figure 16.

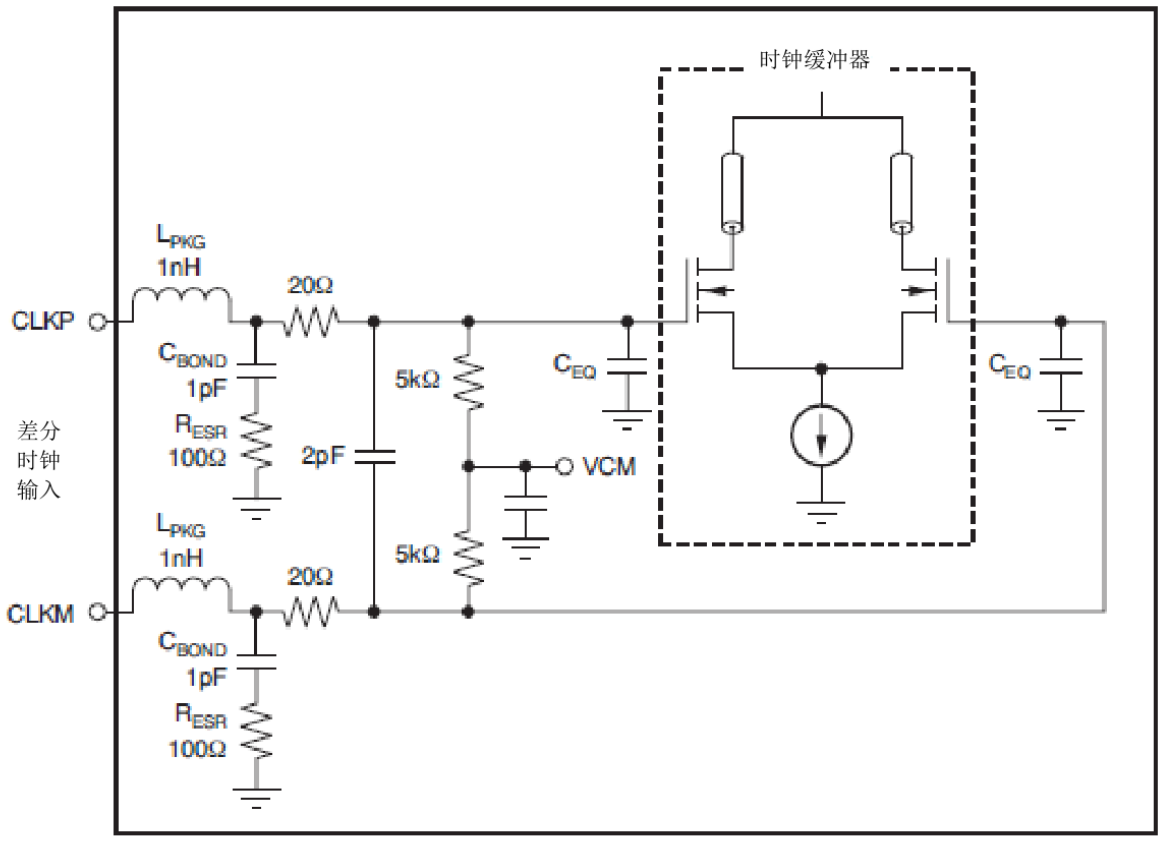


Figure 16: 输入时钟等效电路

单端的时钟驱动电路如图 17 所示。一个单端 CMOS 时钟可以交流耦合到 CLKP 输入，CLKM 通过一个 0.1uF 的电容连接到地。为了获得最佳性能，时钟输入必须采用差分驱动，以降低对共模噪声的敏感性。对于高输入频率采样，建议使用具有非常低抖动的时钟源。时钟源的带通滤波可以帮助减少抖动。非 50% 占空比的时钟输入对性能没有影响。差分的时钟驱动电路如图 18 所示。

The single-ended clock driver circuit is shown in Figure 17. A single-ended CMOS clock can be AC-coupled to the CLKP input, while CLKM is connected to ground through a 0.1uF capacitor. For best performance, the clock input must be driven differentially to reduce sensitivity to common-mode noise. For sampling at high input frequencies, a clock source with very low jitter is recommended. Band-pass filtering of the clock source helps reduce jitter. A clock input with a non-50% duty cycle has no effect on performance. The differential clock driver circuit is shown in Figure 18.

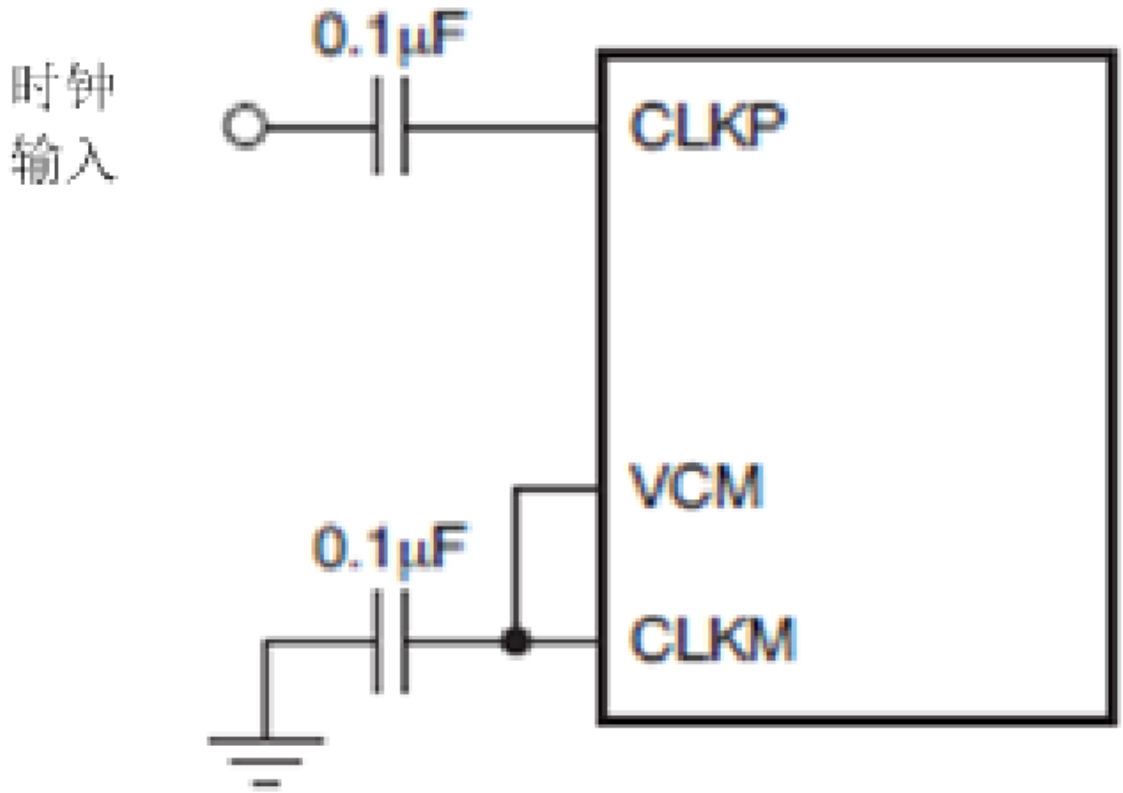


Figure 17: 单端时钟驱动电路

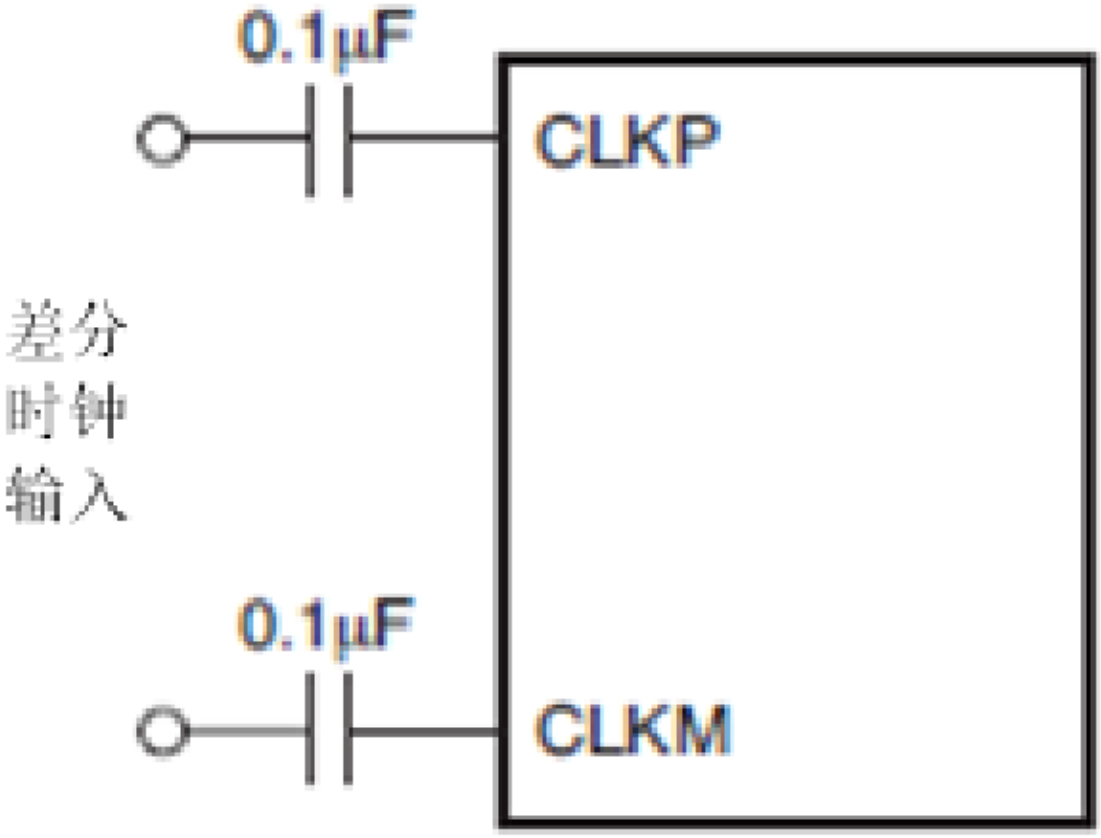


Figure 18: 差分时钟驱动电路

13.5 数字功能 / Digital Functions

器件默认处于低延迟模式，该模式下没有开启任何数字功能。配置"低延迟模式"寄存器为"1"，可以开启的数字功能包含增益校正、失调校正以及测试模式，如图 19 所示。

By default, the device is in low-latency mode, in which no digital functions are enabled. Setting the "low latency mode" register to "1" enables the digital functions, including gain correction, offset correction, and test modes, as shown in Figure 19.



Figure 19: 低延迟模式

13.6 串行接口时序 / Serial Interface Timing

SXA003 有一组内部寄存器，可由串行 SEN（serial interface enable）、SCLK（serial interface clock）和 SDATA（serial interface data）组成的串行接口访问。当 SEN 为低时，位的串行移位进入设备。当 SEN 值激活（低）时，串行数据 SDATA 锁存于 SCLK 的下降沿。当 SEN 为低时，串行数据在每第 16 个 SCLK 的下降沿载入寄存器中。如果字长超过 16 位的倍数，则忽略多余位。数据可以在单个活动 SEN 脉冲中以 16 位字的倍数加载。前 8 位构成寄存器的地址，后 8 位则为寄存器数据。该接口使用 SCLK 的频率可以从 20MHz 下降到很低的速度（几 Hz），也可以使用非 50% 占空比的 SCLK。

The SXA003 has a set of internal registers that can be accessed through a serial interface consisting of SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data). When SEN is low, bits are serially shifted into the device. When SEN is active (low), the serial data SDATA is latched on the falling edge of SCLK. When SEN is low, the serial data is loaded into the registers on every 16th falling edge of SCLK. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first 8 bits form the register address, and the last 8 bits are the register data. The interface can use an SCLK frequency from 20MHz down to very low speeds (a few Hz), and a non-50% duty-cycle SCLK can also be used.

13.7 增益配置中 SFDR/SNR 折中 / SFDR/SNR Trade-Off in Gain Configuration

SXA003 自带有提高 SFDR 的增益设置功能。可以通过上图的增益寄存器设置增益从 0 到 6dB。下表是增益设置对应的模拟输入范围关系。SFDR 的提升来自于 SNR 的折中，对每个增益设置来说，SNR 下降大约 0.5 到 1dB。高频输入时 SNR 下降速度放缓。所以增益配置对于高频输入时非常有效因为 SFDR 提升显著的同时，SNR 下降有限。所以此功能可以用来折中 SFDR 和 SNR。

The SXA003 includes a gain setting function that improves SFDR. The gain can be set from 0 to 6dB through the gain register shown above. The table below shows the analog input range corresponding to each gain setting. The SFDR improvement comes from an SNR trade-off: for each gain setting, the SNR decreases by approximately 0.5 to 1dB. At high-frequency inputs, the SNR decreases more slowly. The gain configuration is therefore very effective for high-frequency inputs, because the SFDR improves significantly while the SNR decrease is limited. This function can thus be used to trade off SFDR and SNR.

复位后，ADC 在低延时模式下，增益配置功能禁用，如果开启，需要以下步骤： After reset, the ADC is in low-latency mode and the gain configuration function is disabled. To enable it, the following steps are required:

1. 禁用低延时模式（DIS LOW LATENCY = 1）。 Disable low-latency mode (DIS LOW LATENCY = 1).
2. 这些设置使能增益并使器件进入 0dB 增益模式。 These settings enable the gain and place the device in 0dB gain mode.
3. 对于其他增益设置，设置寄存器中的增益位。 For other gain settings, set the gain bits in the register.

GAIN（dB）/ Gain (dB)	TYPE / Type	FULL-SCALE (VPP) / Full-Scale (VPP)
0	重置后默认 / Default after reset	2
1	可编程 / Programmable	1.78
2	可编程 / Programmable	1.59
3	可编程 / Programmable	1.42
4	可编程 / Programmable	1.26
5	可编程 / Programmable	1.12
6	可编程 / Programmable	1.00

14. 寄存器 / Registers

14.1 寄存器初始化 / Register Initialization

上电后，内部寄存器必须初始化为默认值，其中 DB 寄存器必须 always write 04。可以通过以下两种方式来初始化：

After power-up, the internal registers must be initialized to their default values; the DB register must always write 04. Initialization can be performed in the following two ways:

（1）通过在 RESET 引脚（宽度大于 10ns）上施加高脉冲进行硬件复位，如图 23 所示。 (1) Hardware reset, by applying a high pulse (width greater than 10ns) on the RESET pin, as shown in Figure 23.

Figure 23: RESET 引脚硬件复位（原件缺图）
[原图待插入。需要详细原图请联系FAE。 / figure to be inserted. Contact FAE for detailed original figures.]

（2）通过软件重置。当使用串行接口时，将 RESET 位（寄存器 0x00 中的 D7）设置为高，此设置将内部寄存器初始化为默认值，然后将 RESET 位自动复位为低。在这种情况下，RESET 引脚将保持低电平。 (2) Software reset. When using the serial interface, setting the RESET bit (D7 in register 0x00) high initializes the internal registers to their default values, after which the RESET bit is automatically reset to low. In this case, the RESET pin remains low.

（3）串行接口时序特点 / Serial interface timing characteristics

表 1 串行接口时序 / Table 1 Serial Interface Timing

参数 / Parameter	说明 / Description	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
fSCLK	SCLK 频率（1/tSCLK）/ SCLK frequency (1/tSCLK)	>DC	—	20	MHz
tSLOADS	SEN 到 SCLK 建立时间 / SEN-to-SCLK setup time	25	—	—	ns
tSLOADH	SCLK 到 SEN 保持时间 / SCLK-to-SEN hold time	25	—	—	ns
tDSU	SDATA 建立时间 / SDATA setup time	25	—	—	ns
tDH	SDATA 保持时间 / SDATA hold time	25	—	—	ns

14.2 寄存器地址 / Register Addresses

工作在高温环境（环境温度高于 50°C）或采样率高于 150M 时，需在器件启动后配置 SPI 相关寄存器，以获得最佳性能。上电后，请先完成寄存器复位操作。

When operating in a high-temperature environment (ambient temperature above 50°C) or at a sampling rate above 150M, the SPI-related registers must be configured after device start-up to obtain the best performance. After power-up, complete the register reset operation first.

寄存器地址 A7:0 / Address	初始值 D7:0 / Initial Value	寄存器数据 / Register Data (D7→D0)
00	00	D7=0，D6=0，D5=0，D4=0，D3=0，D2=0，D1=重置 / Reset，D0=读出 / Readout
01	00	LVDS 摆幅编程（D7~D2）：000000 = LVDS 摆幅默认；±350mV 外接 100Ω 端口；011011 = LVDS 摆幅增加到 ±410mV；110010 = LVDS 摆幅增加到 ±465mV；010100 = LVDS 摆幅增加到 ±570mV；111110 = LVDS 摆幅减小到 ±200mV；001111 = LVDS 摆幅减小到 ±125mV。D1=0，D0=0。 / LVDS swing programming (D7–D2): 000000 = LVDS swing default, ±350mV with 100Ω external termination; 011011 = LVDS swing increased to ±410mV; 110010 = LVDS swing increased to ±465mV; 010100 = LVDS swing increased to ±570mV; 111110 = LVDS swing decreased to ±200mV; 001111 = LVDS swing decreased to ±125mV. D1=0, D0=0.
03	00	0，0，0，0，0，0，高性能模式 1 / High-performance mode 1
25	00	增益编程：0000 = 0dB gain（默认值）；0001 = 0.5dB gain；0010 = 1.0dB gain；0011 = 1.5dB gain；0100 = 2.0dB gain；0101 = 2.5dB gain；0110 = 3.0dB gain；0111 = 3.5dB gain；1000 = 4.0dB gain；1001 = 4.5dB gain；1010 = 5.0dB gain；1011 = 5.5dB gain；1100 = 6.0dB gain。设置增益：0 = gain 使能；如果低延时模式被禁用，则增益仅由 GAIN 位设置；1 = 增益禁用。测试模式：000 = 正常运行；001 = 输出所有为 0；010 = 输出所有为 1；011 = 输出切换模式，在 SXA003 中 D[13:0] 为 01010101010101 和 10101010101010；100 = 输出数字斜坡，在 SXA003 中输出数据在 0 到 16383 中每一个时钟周期增加 1LSB；101 = 输出自定义模式（使用寄存器 0x3F 和 0x40 设置自定义模式）；110 = 未使用；111 = 未使用。 / Gain programming: 0000 = 0dB gain (default); 0001 = 0.5dB gain; 0010 = 1.0dB gain; 0011 = 1.5dB gain; 0100 = 2.0dB gain; 0101 = 2.5dB gain; 0110 = 3.0dB gain; 0111 = 3.5dB gain; 1000 = 4.0dB gain; 1001 = 4.5dB gain; 1010 = 5.0dB gain; 1011 = 5.5dB gain; 1100 = 6.0dB gain. Gain setting: 0 = gain enabled; if low-latency mode is disabled, the gain is set by the GAIN bits only; 1 = gain disabled. Test mode: 000 = normal operation; 001 = output all 0s; 010 = output all 1s; 011 = output toggle mode, in the SXA003 D[13:0] alternates between 01010101010101 and 10101010101010; 100 = output digital ramp, in the SXA003 the output data increments by 1LSB every clock cycle from 0 to 16383; 101 = output user-defined pattern (set the custom pattern using registers 0x3F and 0x40); 110 = unused; 111 = unused.
26	00	0，0，0，0，0，0，LVDS 输出时钟缓冲强度：0 = 100Ω 外部节点（默认强度）；1 = 50Ω 外部节点（2 倍强度）。LVDS 数据缓冲强度：0 = 100Ω 外部节点（默认强度）；1 = 50Ω 外部节点（2 倍强度）。 / 0, 0, 0, 0, 0, 0, LVDS output clock buffer strength: 0 = 100Ω external termination (default strength); 1 = 50Ω external

寄存器地址 A7:0 / Address	初始值 D7:0 / Initial Value	寄存器数据 / Register Data (D7→D0)
		termination (2× strength). LVDS data buffer strength: 0 = 100Ω external termination (default strength); 1 = 50Ω external termination (2× strength).
3D	00	数据格式：00 = DFS 引脚控制数据格式选择；10 = 二补码；11 = 偏移二进制。偏移校正设置：0 = 偏移校正禁用；1 = 启用偏移校正。0，0，0，0，0。 / Data format: 00 = data format selection controlled by the DFS pin; 10 = twos complement; 11 = offset binary. Offset correction setting: 0 = offset correction disabled; 1 = offset correction enabled. 0, 0, 0, 0, 0.
3F	00	传统模式高位 D[13:6]。在 SXA003 中，这些位设置了传统输出模式，输出数据比特 13 到 0 是传统模式 D[13:0]。 / Legacy mode high bits D[13:6]. In the SXA003, these bits set the legacy output mode; output data bits 13 to 0 are the legacy-mode D[13:0].
40	00	传统模式 D[5:0]，0，0。 / Legacy mode D[5:0], 0, 0.
41	00	LVDS CMOS 接口选择：00 = DFS 引脚控制 LVDS 或 CMOS 接口选择；10 = DFS 引脚控制 LVDS 或 CMOS 引脚接口选择；01 = DDR LVDS 接口；11 = 并行 CMOS 接口。CMOS 输出时钟强度控制：00 = 最大强度（推荐并用于指定时序）；01 = 中等强度；10 = 低强度；11 = 非常低强度。启用时钟上升：0 = 禁用输出时钟上升沿；1 = 使能输出时钟上升沿。输出时钟上升控制（控制上升沿位置）：LVDS 接口：00 = 默认位置（时序在此条件下指定）；01 = 建立减少 500ps，保持增加 500ps；10 = 数据转移与上升沿对齐；11 = 建立减少 200ps，保持增加 200ps。使能输出时钟下降沿：0 = 禁用输出时钟下降沿；1 = 使能输出时钟下降沿。 / LVDS/CMOS interface selection: 00 = DFS pin controls LVDS or CMOS interface selection; 10 = DFS pin controls LVDS or CMOS pin interface selection; 01 = DDR LVDS interface; 11 = parallel CMOS interface. CMOS output clock strength control: 00 = maximum strength (recommended and used for the specified timing); 01 = medium strength; 10 = low strength; 11 = very low strength. Enable clock rising edge: 0 = output clock rising edge disabled; 1 = output clock rising edge enabled. Output clock rise control (controls the rising-edge position): LVDS interface: 00 = default position (timing is specified under this condition); 01 = setup reduced by 500ps, hold increased by 500ps; 10 = data transition aligned with the rising edge; 11 = setup reduced by 200ps, hold increased by 200ps. Enable output clock falling edge: 0 = output clock falling edge disabled; 1 = output clock falling edge enabled.
42	00	控制输出时钟下降沿：LVDS 接口：00 = 默认位置（时序在此条件下指定）；01 = 建立减少 400ps，保持增加 400ps；10 = 数据转移跟上升沿一致；11 = 建立减少 200ps，保持增加 200ps。0，0。禁用低延时模式：0 = 低延时模式使能，增益、测试模式和失调修正被禁用；1 = 低延时模式关闭，数字算法功能被启用。待机模式：0 = 正常运行；1 = 只有 ADC 和输出缓冲区断电，内部参考是激活的，待机唤醒时间快。0，0。 / Output clock fall control: LVDS interface: 00 = default position (timing is specified under this condition); 01 = setup reduced by 400ps, hold increased by 400ps; 10 = data transition consistent with the rising edge; 11 = setup reduced by 200ps, hold increased by 200ps. 0, 0. Disable low-latency mode: 0 = low-latency mode enabled, gain, test mode, and offset correction are disabled; 1 = low-latency mode off, digital algorithm functions are enabled. Standby mode: 0 = normal operation; 1 = only the ADC and output buffers are powered down, the internal reference remains active, and standby wake-up is fast. 0, 0.
43	00	0。断电：0 = 正常运行；1 = 全断电，ADC、内部参考、输出缓冲都断电，唤醒时间慢。0。输出缓冲断电：0 = 输出数据和时钟引脚使能；1 = 输出数据和时钟引脚断电。0，0。LVDS 摆幅控制：00 = 使用 LVDS 摆幅寄存器的 LVDS 摆幅控制被禁用；01 = 不使用；10 = 不使用；11 = 使用 LVDS 摆幅寄存器的 LVDS 摆幅控制使能。 / 0. Power-down: 0 = normal operation; 1 = full power-down, the ADC, internal reference, and output buffers are all powered down, and wake-up is slow. 0. Output buffer power-down: 0 = output data and clock pins enabled; 1 = output data and clock pins powered down. 0, 0. LVDS swing control: 00 = LVDS swing control using the LVDS swing register is disabled; 01 = not used; 10 = not used; 11 = LVDS swing control using the LVDS swing register is enabled.
4A	00	0，0，0，0，0，0，0，高性能模式 2：0 = 重置后默认的性能；1 = 高频输入信号时设置最佳性能。 / 0, 0, 0, 0, 0, 0, 0, High-performance mode 2: 0 = default performance after reset; 1 = set for best performance with high-frequency input signals.
BF	00	设置失调底座：当失调校正使能后，失调校正后最终收敛值就是 ADC 中码值。通过对这些位进行编程，可以在最终的收敛值上添加一个底座。SXA003 值 / 底座：011111 / 31LSB；011110 / 30LSB；011101 / 29LSB；- / -；000000 / 0LSB；- / -；111111 / -1LSB；111110 / -2LSB；- / -；100000 / -32LSB。0，0。 / Offset pedestal setting: when offset correction is enabled, the final converged value after offset correction is the ADC mid-

寄存器地址 A7:0 / Address	初始值 D7:0 / Initial Value	寄存器数据 / Register Data (D7→D0)
		code value. By programming these bits, a pedestal can be added to the final converged value. SXA003 value / pedestal: 011111 / 31LSB; 011110 / 30LSB; 011101 / 29LSB; - / -; 000000 / 0LSB; - / -; 111111 / -1LSB; 111110 / -2LSB; - / -; 100000 / -32LSB. 0, 0.
CF	00	冻结失调校正：0 = 失调校正估计不冻结；1 = 失调校正被冻结。0。失调校正时间常数：数值 / 时间常数（周期）：0000 / 1M；0001 / 2M；0010 / 4M；0011 / 8M；0100 / 16M；0101 / 32M；0110 / 64M；0111 / 128M；1000 / 256M；1001 / 512M；1010 / 1G；1011 / 2G。0，0。 / Freeze offset correction: 0 = offset correction estimation not frozen; 1 = offset correction frozen. 0. Offset correction time constant: value / time constant (cycles): 0000 / 1M; 0001 / 2M; 0010 / 4M; 0011 / 8M; 0100 / 16M; 0101 / 32M; 0110 / 64M; 0111 / 128M; 1000 / 256M; 1001 / 512M; 1010 / 1G; 1011 / 2G. 0, 0.
DB	00	Always write 04

15. 电源地间保护 / Power-to-Ground Protection

为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.35V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。

To improve the anti-static capability of the device, ESD protection circuits exist between the various supply pins inside the device, as shown below. The forward conduction voltage drop of each ESD protection diode is approximately 0.35V; prolonged forward conduction of these ESD protection diodes should be avoided during power-up and normal use.

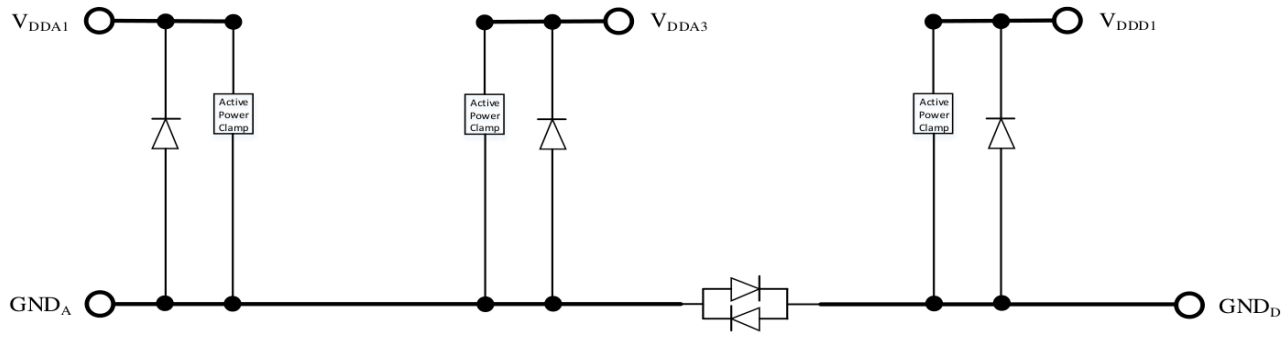


Figure 20: 内部电源间的 ESD 保护电路

16. 注意事项 / Cautions

16.1 产品安装注意事项 / Product Installation Cautions

1) 焊接时请注意器件方向，以免焊错。 Pay attention to the device orientation when soldering to avoid soldering it incorrectly. 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 Instruments and meters used for circuit debugging must have good common grounding. PCB design must maintain good grounding and power-supply decoupling. 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。 Take care not to reverse the power supply or short the inputs/outputs to the power supply, which can easily damage the circuit.

16.2 产品使用注意事项 / Product Usage Cautions

1) 差分输入应尽量靠近且相互平行。 Differential inputs should be routed as close together and as parallel as possible. 2) 输入连线应尽量短以最小化寄生电容和噪声引入。 Input traces should be as short as possible to minimize parasitic capacitance and noise pickup. 3) 为了更好的散热并获得更好的电性能，芯片的底板应焊接到 PCB 板的一个大的地端，从而最大限度发挥封装的热性能。 For better heat dissipation and electrical performance, the die paddle of the chip should be soldered to a large ground area on the PCB to maximize the thermal performance of the package. 4) 很重要的是，芯片的地应该通过尽量多的渠道和足够多的面积与 PCB 板的地层相连。 It is important that the ground of the chip be connected to the ground layer of the PCB through as many vias and as large an area as possible. 5) 该产品工作在高温环境（环境温度高于 50°C）或采样率高于 150M 时，需在器件启动后配置 SPI 相关寄存器。具体为：SPI 中配置，地址 DB，数据 04。 When this product operates in a high-temperature environment (ambient temperature above 50°C) or at a sampling rate above 150M, the SPI-related registers must be configured after device start-up. Specifically: in the SPI configuration, address DB, data 04. 6) 推荐上电后首先对电路进行复位，再进行使用。 It is recommended to reset the circuit first after power-up before use.

16.3 产品防护注意事项 / Product Protection Cautions

1) 该电路所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 All pins of this circuit are designed with ESD protection structures; however, large-energy electrical pulses may still damage the circuit. ESD protection must therefore be observed during testing, handling, and storage. 2) 超出绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。 Exceeding absolute maximum ratings may cause permanent device damage. These are rating limits only and do not imply that the device will operate normally under these conditions or any other conditions beyond those shown in this manual. 3) 在避免雨、雪直接影响的条件下，装有产品的包装箱可以用安全的运输工具运输。但不能和带有酸性、碱性和其它腐蚀性物体堆放在一起。包装应是安全的，可以采用现有的运输工具。 Provided direct exposure to rain and snow is avoided, cartons containing the product may be transported by safe means of transport. They must not be stacked together with acidic, alkaline, or other corrosive materials. The packaging shall be safe, and existing means of transport may be used. 4) 包装好的产品贮存环境应满足 Q/W 657A 第 8.1 规定的 I 类库房条件要求（温度：15°C~25°C，湿度：25%~65%），周围没有酸、碱或其它腐蚀性气体，通风良好，且具备相应防静电措施。 The storage environment for the packaged product shall meet the Class I warehouse conditions specified in Q/W 657A, Section 8.1 (temperature: 15°C–25°C, humidity: 25%–65%), with no acidic, alkaline, or other corrosive gases in the surroundings, good ventilation, and appropriate ESD protection measures in place.

16.4 电装说明 / Assembly Instructions

1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； This product has a moisture sensitivity level of MSL3. After removing the product from the moisture-barrier bag, dry storage, or baking, the allowable exposure time to the ambient environment before reflow soldering is: ≤30°C/60RH%, 168h. 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； If device storage conditions cannot be controlled or traced, bake at 125°C for 8h strictly before assembly. 3) 若电装环境温湿度无法保证 ≤30°C/60RH%，请在烘烤后 12h 内完成焊接； If the assembly environment cannot be guaranteed at ≤30°C/60RH%, complete soldering within 12h after baking. 4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； After baking, the product is highly susceptible to static electricity; ESD protection must be observed throughout all

handling. 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C–235°C, with maximum peak temperature not exceeding 235°C; dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60–90s, ramp-up rate 2–4°C/s, ramp-down rate 2–6°C/s. 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C； For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C–245°C, with maximum peak temperature not exceeding 260°C; dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60–90s, ramp-up rate 2–4°C/s, ramp-down rate 2–6°C. 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）； If a mixed assembly process requires higher temperatures, ensure the device body temperature does not exceed 260°C (measured at the top surface of the device during reflow).

16.5 热阻 / Thermal Resistance

表 2 热阻信息汇总 / Table 2 Thermal Resistance Summary

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard & Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)	28.05 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2 natural-convection thermal test environmental requirements and test method for integrated circuits
Rthjt（结到器件顶面的热阻）/ Rthjt (junction-to-top thermal resistance)	3.596 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14 one-dimensional heat-flow-path two-interface separation method
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-bottom thermal resistance)	2.825 K/W	JESD51-14 拐点理论器件内部结构分层得到 / JESD51-14 inflection-point theory, obtained by layering the internal device structure

17. 常见故障及处理办法 / Common Faults and Troubleshooting

1. 无信号输出：检查电源电压、输入信号、时钟是否正确加载。 No signal output: check that supply voltage, input signal, and clock are correctly applied.
2. 器件功能不正常：明确器件工作模式，确认配置是否正确。 Device functions abnormally: clarify the device operating mode and confirm that the configuration is correct.
3. 器件工作不稳定：检查电源，保证电源电压稳定。 Device operates unstably: check the power supply to ensure stable supply voltage.

18. 联系方式 / Contact

深圳市深信科技有限公司 / Shenzhen Shenxin Technology Co., Ltd.

- 联系人 / Contact: Felix (Flip) Lai, CEO
- 邮箱 / Email: felix@shenxinic.com

- 电话 / Tel: +852 51367095
- 官网 / Website: shenxinic.com

---

19. 附加说明 / Additional Notes

1. 本说明书首次发布日期：2026 年 6 月。 First publication date of this manual: June 2026.
2. 本产品状态：☑生产（该产品型号目前已在生产，可以提供正式产品）☐预发布（该产品型号尚未投入正式生产，可以提供样品） Product status: ☑Production (this model is currently in production; formal product available) ☐Pre-release (this model is not yet in formal production; samples available)
3. 替代进口器件情况说明 / Notes on substitution of imported devices:

1）绝对最大额定值对比 / Absolute maximum ratings comparison

附表 1 绝对最大额定值对比 / Appendix Table 1 — Absolute Maximum Ratings Comparison

参数 / Parameter	SXA003 规范要求 / SXA003 Specification	进口器件手册 / Imported Device Datasheet	比对结果 / Comparison
模拟电源电压（VAVDD）/ Analog supply voltage (VAVDD)	-0.3V~2.1V	-0.3V~2.1V	一致 / Consistent
数字电源电压（VDRVDD）/ Digital supply voltage (VDRVDD)	-0.3V~2.1V	-0.3V~2.1V	一致 / Consistent
贮存温度（Tstg）/ Storage temperature (Tstg)	-65°C~150°C	-65°C~150°C	一致 / Consistent
结温（TJ）/ Junction temperature (TJ)	175°C	125°C	不一致 / Different

2）推荐工作条件对比 / Recommended operating conditions comparison

附表 2 推荐工作条件对比 / Appendix Table 2 — Recommended Operating Conditions Comparison

参数 / Parameter	SXA003 规范要求 / SXA003 Specification	进口器件手册 / Imported Device Datasheet	比对结果 / Comparison
工作频率（fCLK）/ Operating frequency (fCLK)	80MHz~250MHz	80MHz~250MHz	一致 / Consistent
模拟电源电压（VAVDD）/ Analog supply voltage (VAVDD)	1.75V~1.85V	1.75V~1.85V	一致 / Consistent
数字电源电压（VDRVDD）/ Digital supply voltage (VDRVDD)	1.75V~1.85V	1.75V~1.85V	一致 / Consistent
输入信号幅度范围（峰峰值）/ Input signal amplitude range (peak-to-peak)	≤2V	≤2V	一致 / Consistent
工作环境温度（TA）/ Operating ambient temperature (TA)	-40°C~85°C	-40°C~85°C	一致 / Consistent

3）电特性对比 / Electrical characteristics comparison

附表 3 电特性对比 / Appendix Table 3 — Electrical Characteristics Comparison

参数 / Parameter	符号 / Symbol	条件 / Condition	SXA003 参考值 / SXA003 Reference			进口器件手册参考值 / Imported Device Reference			说明 / Note	单位 / Unit
			最小值 / Min	典型值 / Typ	最大值 / Max	最小值 / Min	典型值 / Typ	最大值 / Max		
分辨率 / Resolution	RES	fCLK=250MHz，fIN=10MHz	14			14			一致 / Consistent	bit
线性误差 / Integral linearity error	EL	fCLK=250MHz，fIN=10MHz	-7	±3	7	-5	±2	5	偏大 / Larger	LSB
微分误差 / Differential linearity error	EDL	fCLK=250MHz，fIN=10MHz	-1	±0.8	2	-0.95	±0.5		偏小 / Smaller	LSB
失调误差 / Offset error	EO	—	-15	3	15	-15	2.5	15	一致 / Consistent	mV
增益误差 / Gain error	EG	—	-10	2	+10	-2		2	偏大 / Larger	%FS
逻辑输入高电平 / Logic input high	VIH	—	1.5	1.5	—	1.3			偏大 / Larger	V
逻辑输入低电平 / Logic input low	VIL	—	—	0.3	0.3			0.4	偏小 / Smaller	V
输入高电平电流 / Input high current	IIH	SDATA 引脚 / SDATA pin	-15	0	15		10		偏大 / Larger	uA
输入低电平电流 / Input low current	IIL	—	-2	0	2		0		一致 / Consistent	uA
共模输出电压 / Common-mode output voltage	VCM	—	0.9	1	1.05		0.95		偏大 / Larger	V
信噪比 / SNR	SNR	fCLK=250MHz，fIN=10MHz；fCLK=250MHz，fIN=170MHz	62	68	—		67.5 / 70.6		偏小 / Smaller	dB
	SFDR		65	78	—	72	84			dB

参数 / Parameter	符号 / Symbol	条件 / Condition	SXA003 参考值 / SXA003 Reference			进口器件手册参考值 / Imported Device Reference			说明 / Note	单位 / Unit
无杂散动态范围 / SFDR		fCLK=250MHz，fIN=10MHz；fCLK=250MHz，fIN=170MHz							偏小 / Smaller	
信噪失真比 / SINAD	SINAD	fCLK=250MHz，fIN=10MHz；fCLK=250MHz，fIN=170MHz	62	64	—	66	69.4		偏小 / Smaller	dB
有效位数 / ENOB	ENOB	fCLK=250MHz，fIN=10MHz	10	11	—		11.3		偏小 / Smaller	bit
LVDS 差分输出电压 / LVDS differential output voltage	VOD	LVDS 模式（350mV）/ LVDS mode (350mV)	270	350	430	270	350	430	一致 / Consistent	mV
LVDS 共模输出电压 / LVDS common-mode output voltage	VOS	—	0.85	1	1.25	0.85	1.05	1.25	偏小 / Smaller	V
模拟电源电流 / Analog supply current	ICC	LVDS 模式（350mV）/ LVDS mode (350mV)	—	130	150		99	113	偏大 / Larger	mA
数字电源电流 / Digital supply current	IDD	—	—	70	80		47		偏大 / Larger	mA
功耗 / Power dissipation	PD	—	—	0.36	0.45		0.26		偏大 / Larger	W
休眠功耗 / Power-down power	PDWN	—	—	20	25		10	25	偏大 / Larger	mW
时钟周期 / Clock period	tCLK	80MHz≤fCLK≤250MHz	4	10	12.5	4	10	12.5	一致 / Consistent	ns
时钟高脉冲宽度 / Clock high pulse width	tCLKH	80MHz≤fCLK≤250MHz	2	5	6.25	2	5	6.25	一致 / Consistent	ns
时钟低脉冲宽度 / Clock low pulse width	tCLKL	—	2	5	6.25	2	5	6.25	一致 / Consistent	ns

参数 / Parameter	符号 / Symbol	条件 / Condition	SXA003 参考值 / SXA003 Reference			进口器件手册参考值 / Imported Device Reference			说明 / Note	单位 / Unit
占空比 / Duty cycle	ODC	LVDS 模式（350mV）/ LVDS mode (350mV)	42	50	58	42	48	54	偏大 / Larger	%

4）其它指标对比 / Other parameters comparison

附表 4 其它指标对比 / Appendix Table 4 — Other Parameters Comparison

参数 / Parameter	SXA003	进口器件 / Imported Device	比对结果 / Comparison
封装形式 / Package	QFN48	QFN48	一致 / Consistent
质量等级 / Quality grade	企标 / Enterprise standard	工业级 / Industrial	有差异 / Different
尺寸 / Dimensions	7mm×7mm×0.9mm	7mm×7mm×0.9mm	一致 / Consistent
替代建议 / Substitution recommendation	□直接替代 □有效替代 ☑功能替代 / □Drop-in □Effective ☑Functional alternative		

© 2026 深圳市深信科技有限公司 / Shenzhen Shenxin Technology Co., Ltd.