SXA006

Dual-Channel 8-Bit, 1.5 GSPS A/D Converter

双路 8 位 1.5GSPS A/D 转换器

8-bit | 2 channels | 1.5 GSPS | eLQFP128 | Parallel LVDS

8位 | 双通道 | 1.5GSPS | eLQFP128 | 并行LVDS

对标 / Cross Reference: ADC08D1500 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXA006 Dual-Channel 8-Bit 1.5GSPS A/D Converter — Product Specification & User Manual

SXA006 型双路 8 位 1.5GSPS A/D 转换器产品说明书、使用手册

深信科技 / Shenzhen Shenxin Technology Co., Ltd. 版本 / Revision: V1.20260727 对标 / Cross Reference: ADC08D1500 — pin-to-pin compatible alternative

联系方式 / Contact: Felix (Flip) Lai, CEO ｜ 邮箱 / Email: felix@shenxinic.com ｜ 电话 / Tel: +852 51367095 ｜ 官网 / Website: shenxinic.com

版本修订记录 / Revision History

版本号 / Version	发布日期 / Date	更改章节 / Changed Section	更改说明 / Description	备注 / Note
V1.20260727	20260727	——	——	首次发布 / Initial release

1. 产品用途及应用范围 / Applications

- 数字示波器 / Digital oscilloscopes
- 通信接收机 / Communications receivers
- 直接 RF 下变频转换器 / Direct RF down-conversion converters
- 高速数字采集 / High-speed digital acquisition

2. 产品特点 / Features

- 双通道超高速 A/D 转换器 / Dual-channel ultra-high-speed A/D converter
- 8 位分辨率 / 8-bit resolution
- 模拟电源：1.95V～2.05V / Analog supply: 1.95V–2.05V
- 输出驱动电源：1.95V～2.05V / Output driver supply: 1.95V–2.05V
- 功耗：≤2.6W / Power dissipation: ≤2.6W
- 模拟输入范围：570mVpp～1100mVpp / Analog input range: 570mVpp–1100mVpp
- 最大转换速率：1.5GSPS / Maximum conversion rate: 1.5GSPS
- SDR 或 DDR 输出时钟选择 / SDR or DDR output clock selection
- 每通道采样率 1.5GSPS，采用时间交替模式可达到 2 倍采样率 / 1.5GSPS per channel; 2× sample rate achievable in time-interleaved mode
- 多路 ADC 同步性能 / Multi-ADC synchronization capability
- 时钟占空比校正 / Clock duty-cycle correction
- 扩展控制为串行接口：4 位地址，16 位数据 / Extended control via serial interface: 4-bit address, 16-bit data

- 输入满刻度范围数字调节 / Digital adjustment of input full-scale range
- 电路接口：并行 LVDS / Interface: parallel LVDS
- ESD 等级：2 级，HBM 模型，2000V / ESD rating: Class 2, HBM model, 2000V
- 产品重量：4.9g±0.5g / Weight: 4.9g±0.5g
- 封装形式：eLQFP128 / Package: eLQFP128

3. 产品描述 / Product Description

SXA006 型双路 8 位 1.5GSPS A/D 转换器是采用 CMOS 工艺制造的单片集成电路。该产品采用折叠/插值结构，电路内部包含采样/保持放大器、折叠放大器、带隙电压基准、时钟电路和 LVDS 输出等电路。

The SXA006 dual-channel 8-bit 1.5GSPS A/D converter is a monolithic integrated circuit fabricated in a CMOS process. It uses a folding/interpolating architecture and integrates a sample-and-hold amplifier, folding amplifiers, a bandgap voltage reference, clock circuitry, and LVDS outputs.

本器件采用暴露焊盘的塑料 128 引线扁平封装（LQFP128），外形尺寸为 20mm×20mm×1.6（max）mm。也可根据用户实际需要，提供芯片及其它封装形式。

The device is housed in a plastic 128-lead flat package with an exposed pad (LQFP128), with outline dimensions of 20mm×20mm×1.6 (max) mm. Bare die and other package options can also be provided according to user requirements.

本产品数据输出、溢出输出和数据时钟输出的同相/反相引出端与国外产品不一致，与国外产品是相反的，但不影响使用。

The in-phase/inverted pins of the data outputs, overflow output, and data clock output of this product are interchanged relative to the foreign product; this does not affect use.

该产品功能框图如下： The functional block diagram of the product is shown below:

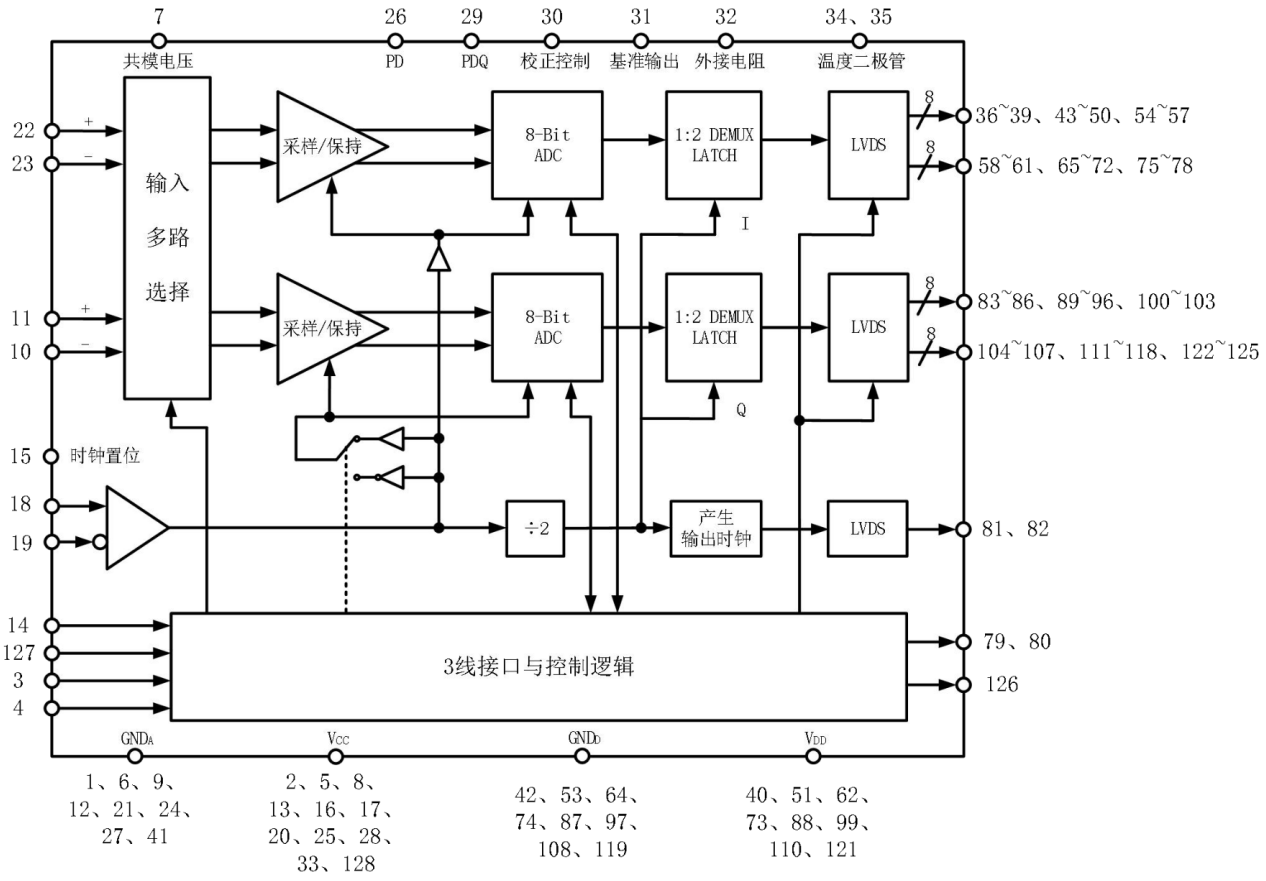


Figure 1: 功能框图

产品工作时序如下： The operating timing of the product is shown below:

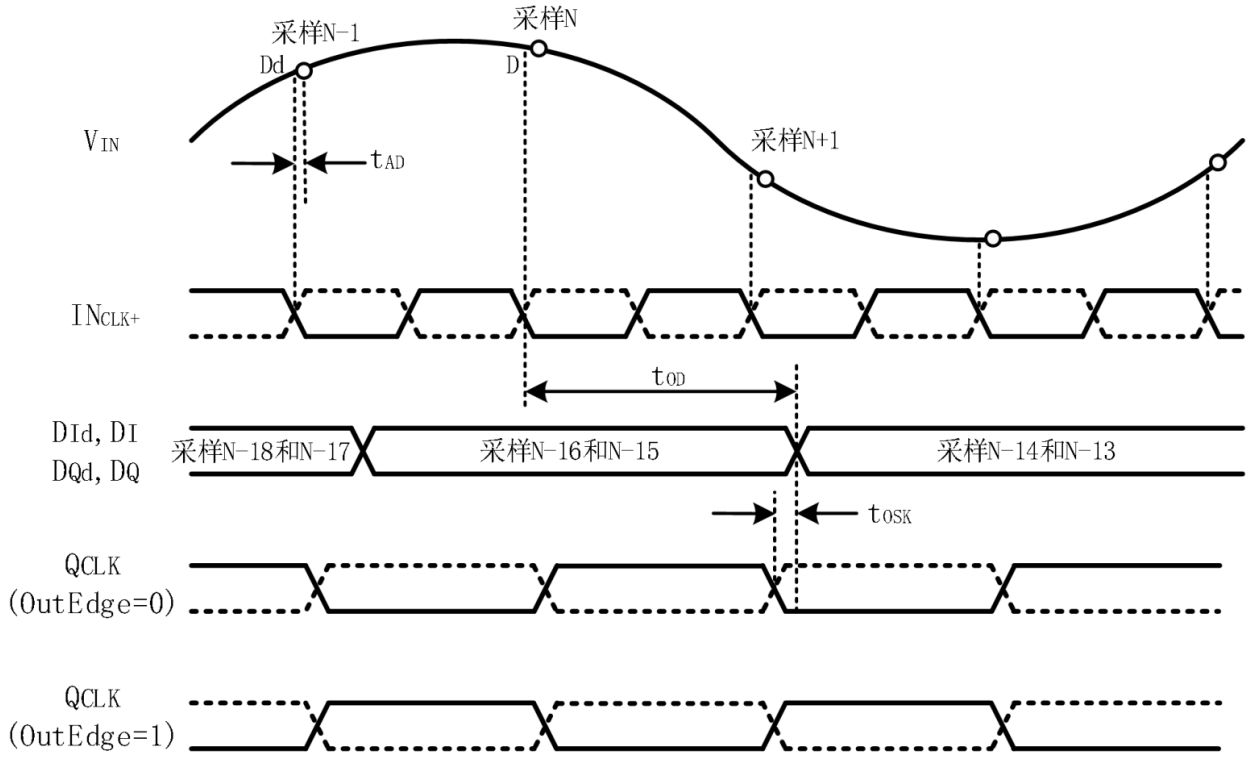


Figure 2: 单数据速率（SDR）时序（OutEdge 为高或低）

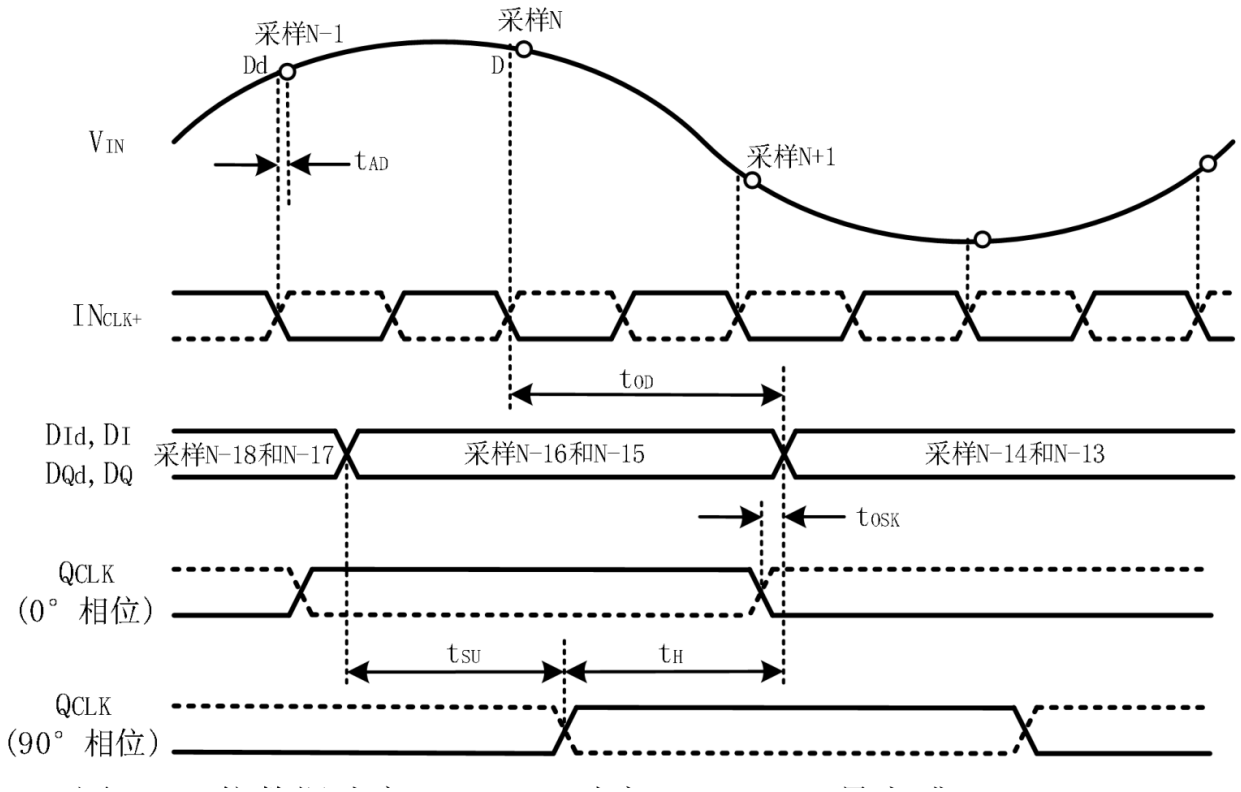


Figure 3: 双倍数据速率（DDR）时序（OutEdge 悬空或 VCC/2）

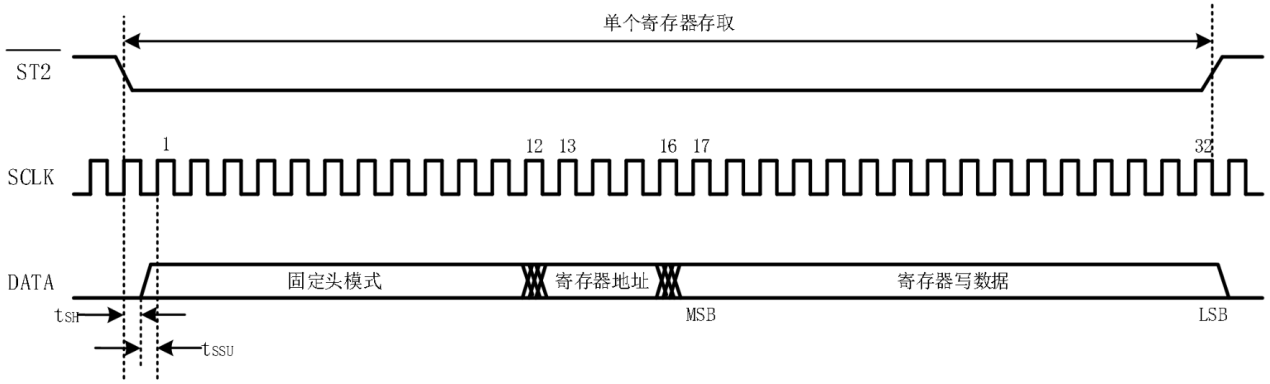


Figure 4: 串行接口时序

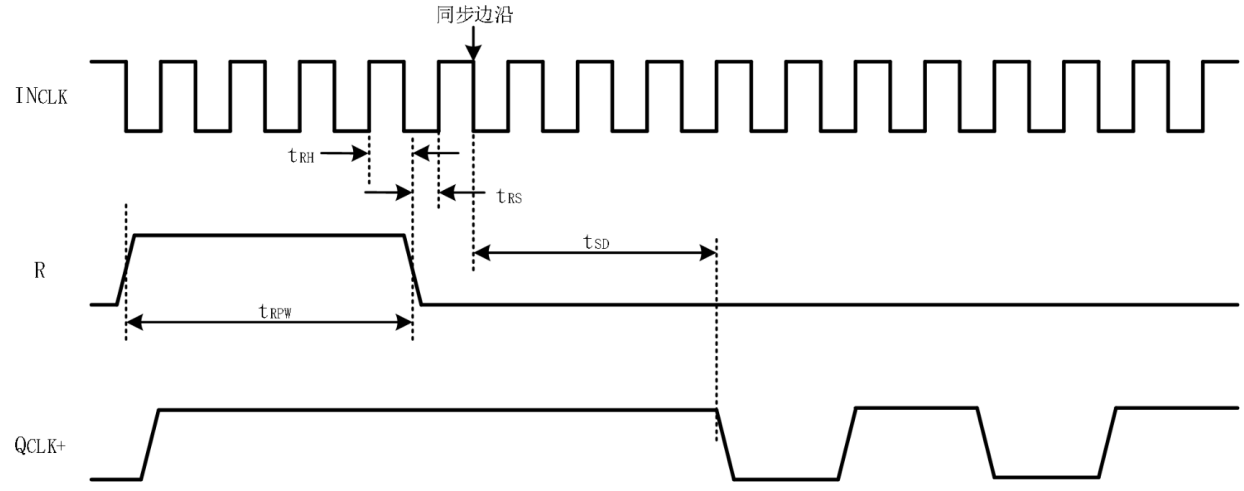


Figure 5: DDR 模式输出时钟（QCLK）置位时序（OutEdge 悬空或 VCC/2）

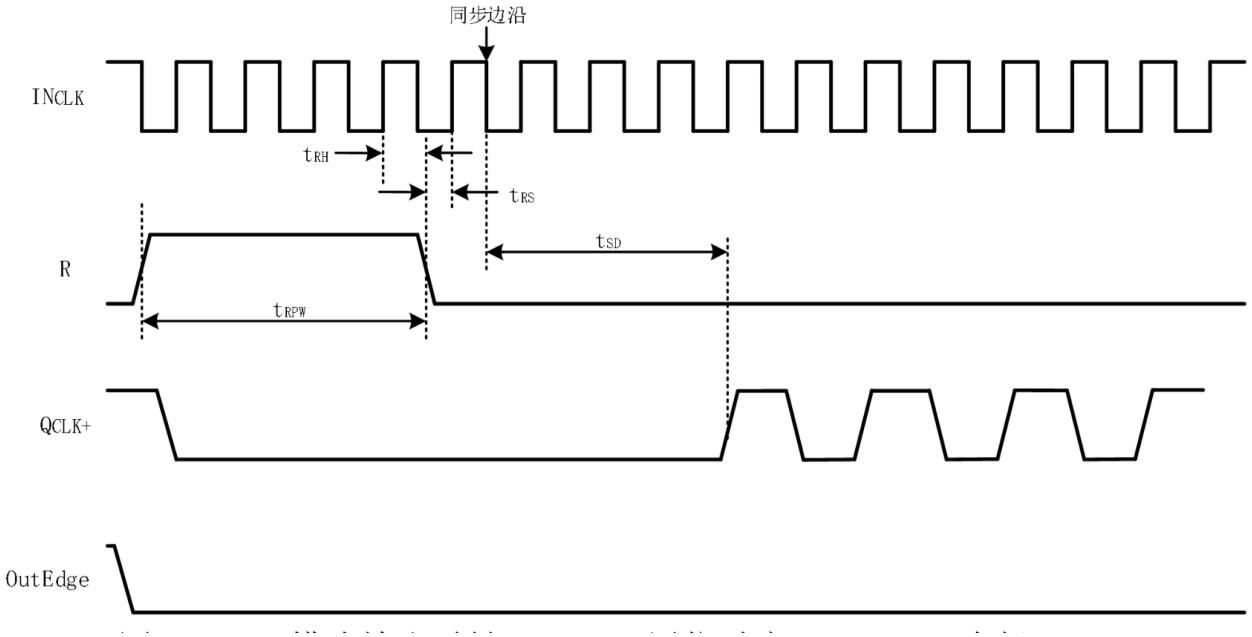


Figure 6: SDR 模式输出时钟（QCLK）置位时序（OutEdge 为低）

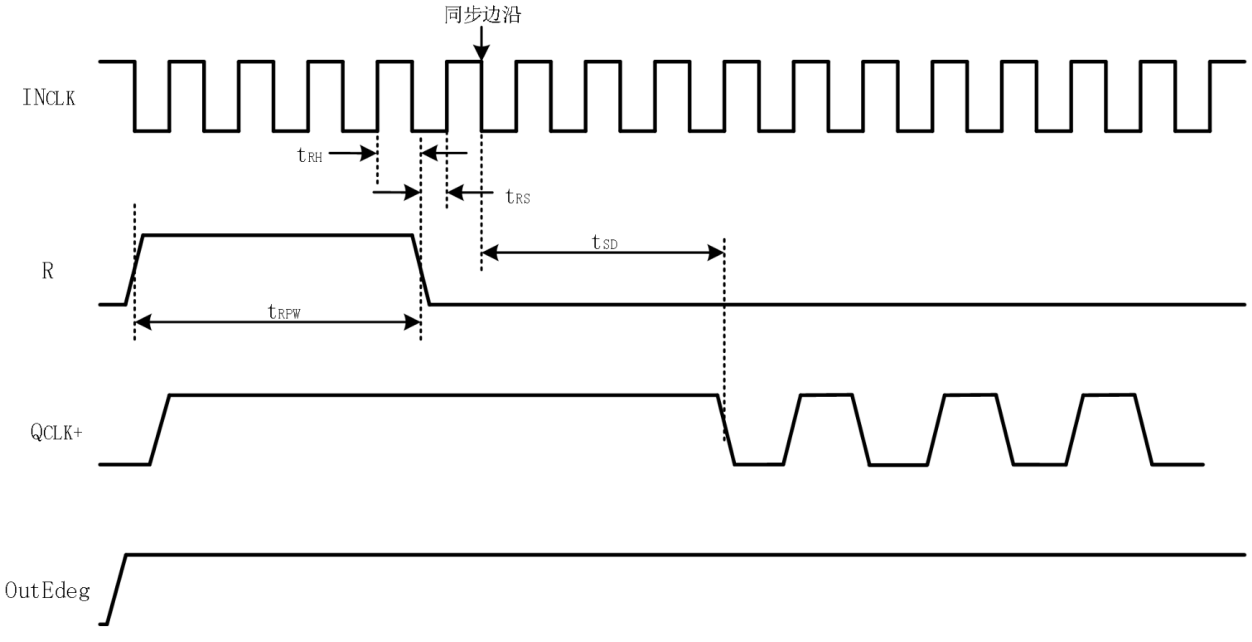


Figure 7: SDR 模式输出时钟（QCLK）置位时序（OutEdge 为高）

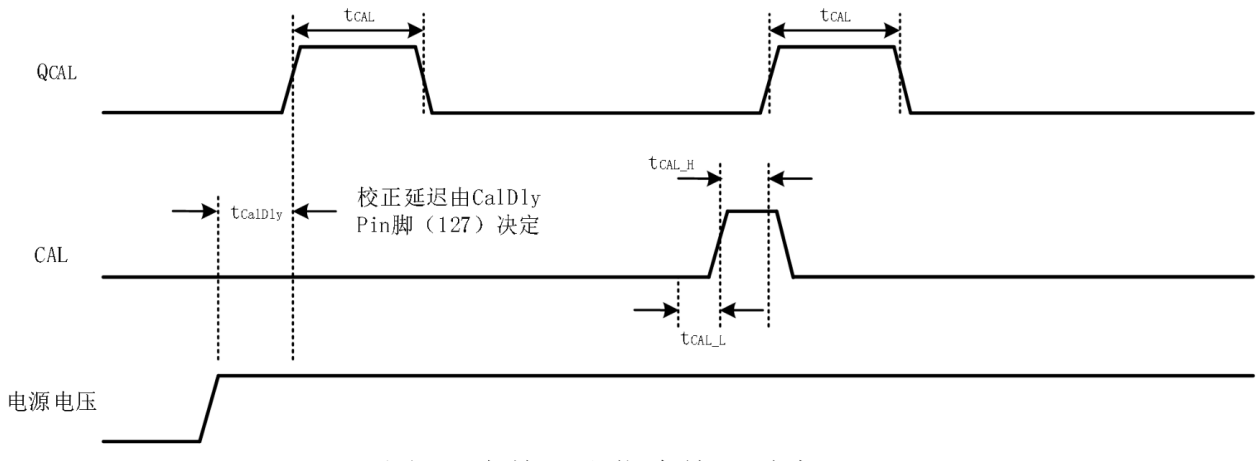


Figure 8: 自校正和指令校正时序

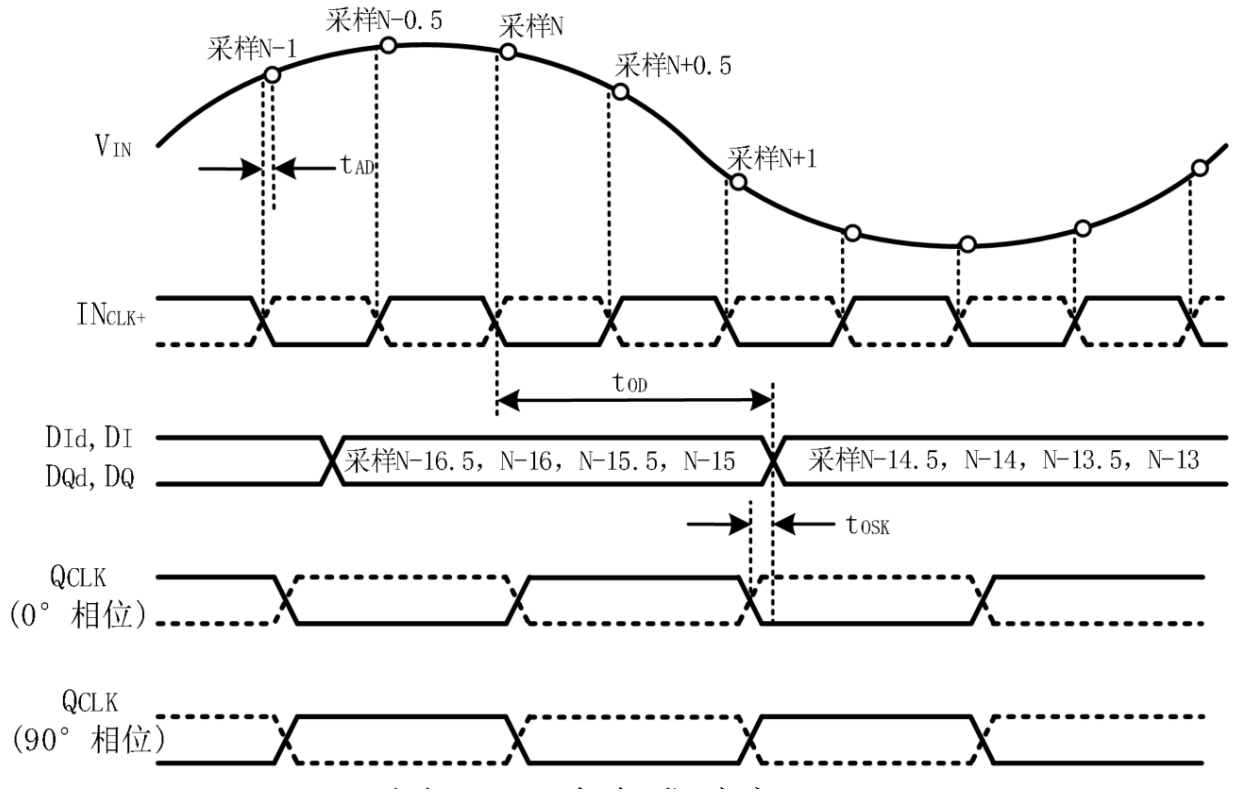


Figure 9: 双路合成时序

表1 时间参数表 / Table 1 Timing Parameters

符号 / Symbol	参数 / Parameter	数值 / Value	单位 / Unit
tCAL_L	CAL 引脚低电平时间 / CAL pin low-level time	⩾80	Clock Cycles
tCAL_H	CAL 引脚高电平时间 / CAL pin high-level time	⩾80	Clock Cycles
tCAL	校准时间 / Calibration time	典型值 1.4×10^5 / Typ 1.4×10^5	Clock Cycles

符号 / Symbol	参数 / Parameter	数值 / Value	单位 / Unit
tRPW	复位脉宽 / Reset pulse width	≥4	Clock Cycles
tRPW_H	复位脉宽高电平时间 / Reset pulse width, high-level time	≥4	Clock Cycles
tRPW_L	复位脉宽低电平时间 / Reset pulse width, low-level time	≥40	Clock Cycles
tCalDly	校准延迟时间（Pin 127 高）/ Calibration delay time (Pin 127 high)	≤231	Clock Cycles
tCalDly	校准延迟时间（Pin 127 低）/ Calibration delay time (Pin 127 low)	≥225	Clock Cycles

表2 输出码（标准模式，FSR 为高）/ Table 2 Output Codes (Standard Mode, FSR High)

等效十进制 / Equivalent Decimal	VIN+－VIN-	电压电平 / Voltage Level	二进制码 / Binary Code	溢出位 / Overflow Bit
255	＞460mV	>正满度范围＋1/2LSB / >positive full-scale range +1/2 LSB	11111111	1
255	460mV	正满度范围＋1/2LSB / Positive full-scale range +1/2 LSB	11111111	0
254	458mV	正满度范围－1/2LSB / Positive full-scale range −1/2 LSB	11111110	0
…	…	…	…	…
128	1.8mV	双极 0＋1/2LSB / Bipolar 0 +1/2 LSB	10000000	0
127	-1.8mV	双极 0－1/2LSB / Bipolar 0 −1/2 LSB	01111111	0
…	…	…	…	…
1	-458mV	负满度范围＋1/2LSB / Negative full-scale range +1/2 LSB	00000001	0
0	-460mV	负满度范围－1/2LSB / Negative full-scale range −1/2 LSB	00000000	0
0	＜-460mV	＜负满度范围－1/2LSB / <negative full-scale range −1/2 LSB	00000000	1

4. 标准 / Standards

- 详细规范及确认号：Q/GC 0225-2026《半导体集成电路 SXA006 型双路 8 位 1.5GSPS A/D 转换器详细规范》 Detailed specification and approval ref.: Q/GC 0225-2026, Semiconductor Integrated Circuit — Detailed Specification for SXA006 Dual-Channel 8-bit 1.5GSPS A/D Converter
- 质量等级：企标 / Quality grade: Enterprise standard

5. 产品外形图和实物图片 / Package Outline and Physical Pictures

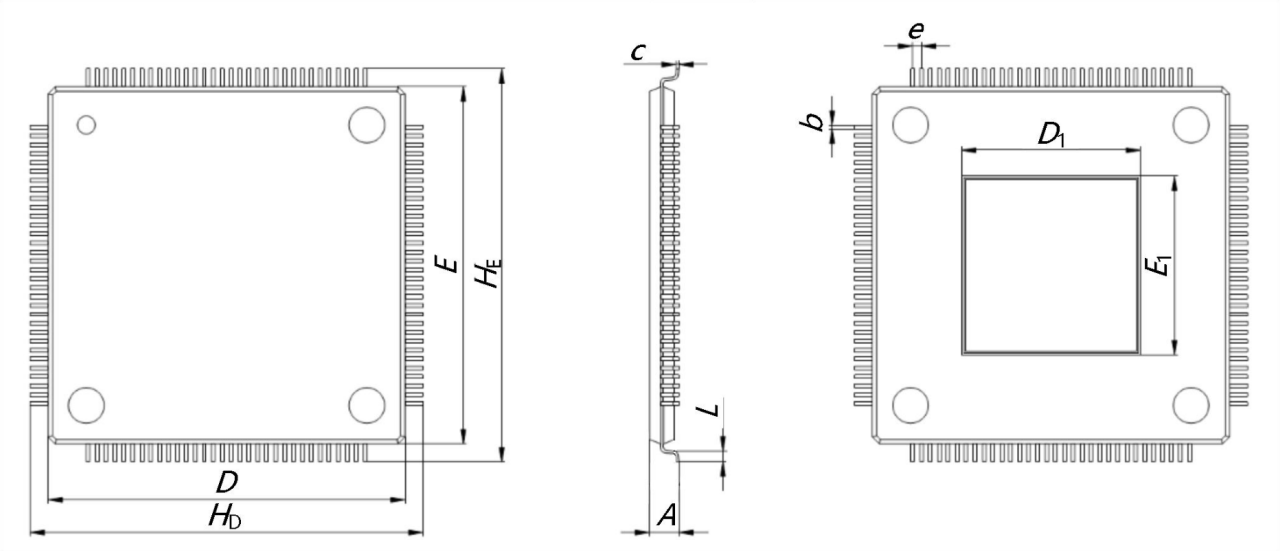


Figure 10: 产品外形尺寸图

产品外形尺寸 / Package Dimensions

单位为毫米 / Dimensions in mm

尺寸符号 / Symbol	数值 / Value			尺寸符号 / Symbol	数值 / Value		
	最小 / Min	公称 / Nom	最大 / Max		最小 / Min	公称 / Nom	最大 / Max
A	——	——	1.80	c	0.13	0.15 a	0.18
D	19.70	20.0 a	20.30	e	——	0.50	——
D1	9.80	10.0 a	10.20	E	19.70	20.0 a	20.30
HD	21.60	22.0 a	22.40	E1	9.80	10.0 a	10.20
HE a	21.60	22.0 a	22.40	L	0.45	0.60 a	0.75
b	0.18	0.22 a	0.27				

a 外壳实际公称值，推荐用户参考该尺寸设计使用； a: Actual nominal value of the package; users are recommended to refer to these dimensions for design.

注：推荐焊盘设计详见电装说明。 Note: See the assembly instructions for recommended pad layout.

6. 引出端排列（俯视图）/ Pin Arrangement (Top View)

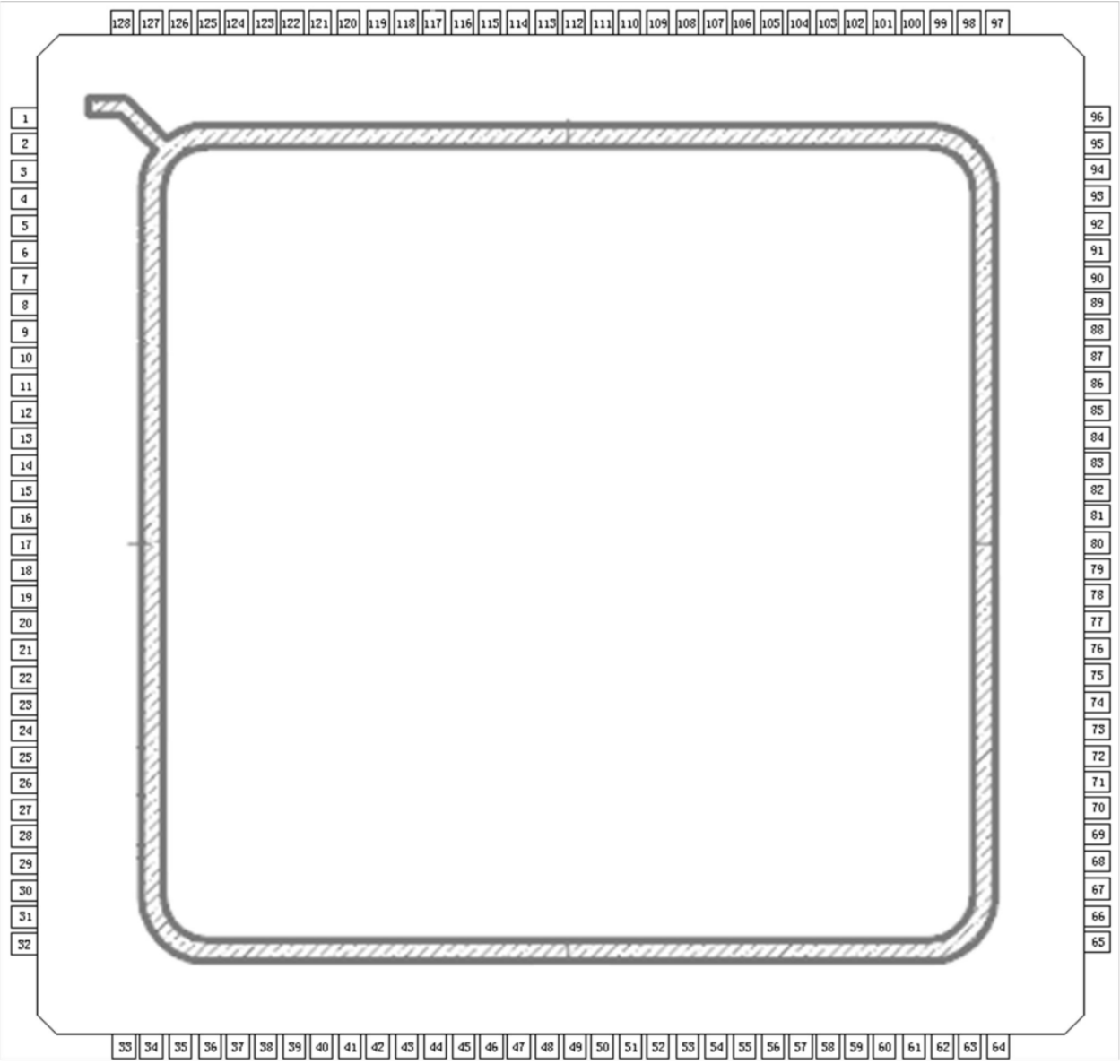


Figure 11: 引出端排列

7. 引出端功能符号表 / Pin Function Table

注：原符号带上划线者为反相输出，下表在符号后以（反相）标注；I/O 栏中的"/"（电源/地引脚）。 Note: Symbols overlined in the source are inverted outputs, marked "(inverted)" after the symbol below; "/" in the I/O column is reproduced from the source (supply/ground pins).

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
1	GNDA	模拟地 / Analog ground	/	65			O

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
					DQ2（反相）/ DQ2 (inverted)	Q 路数据输出位 DQ2（反相）/ Q-channel data output bit DQ2 (inverted)	
2	VCC	模拟电源 / Analog supply	/	66	DQ2	Q 路数据输出位 DQ2 / Q-channel data output bit DQ2	O
3	Outv/SCLK	输出电压幅度控制/串行接口时钟输入 / Output voltage amplitude control / serial interface clock input	I	67	DQ3（反相）/ DQ3 (inverted)	Q 路数据输出 DQ3（反相）/ Q-channel data output DQ3 (inverted)	O
4	OutEdge/ DDR/DATA	输出时钟沿选择/双数据速率控制/串行数据输入 / Output clock edge select / double data rate control / serial data input	I	68	DQ3	Q 路数据输出位 DQ3 / Q-channel data output bit DQ3	O
5	VCC	模拟电源 / Analog supply	/	69	DQ4（反相）/ DQ4 (inverted)	Q 路数据输出位 DQ4（反相）/ Q-channel data output bit DQ4 (inverted)	O
6	GNDA	模拟地 / Analog ground	/	70	DQ4	Q 路数据输出位 DQ4 / Q-channel data output bit DQ4	O
7	VCMO	共模电压 / Common-mode voltage	O	71	DQ5（反相）/ DQ5 (inverted)	Q 路数据输出位 DQ5（反相）/ Q-channel data output bit DQ5 (inverted)	O
8	VCC	模拟电源 / Analog supply	/	72	DQ5	Q 路数据输出位 DQ5 / Q-channel data output bit DQ5	O
9	GNDA	模拟地 / Analog ground	/	73	VDD	输出驱动电源 / Output driver supply	/
10	INI-	I 路模拟输入负 / I-channel analog input, negative	I	74	GNDD	输出驱动地 / Output driver ground	/
11	INI+	I 路模拟输入正 / I-channel analog input, positive	I	75	DQ6（反相）/ DQ6 (inverted)	Q 路数据输出位 DQ6（反相）/ Q-channel data output bit DQ6 (inverted)	O
12	GNDA	模拟地 / Analog ground	/	76	DQ6	Q 路数据输出位 DQ6 / Q-channel data output bit DQ6	O
13	VCC	模拟电源 / Analog supply	/	77	DQ7（反相）/ DQ7 (inverted)	Q 路数据输出位 DQ7（反相）（最高位）/ Q-channel data output bit DQ7 (inverted) (MSB)	O
14	FSR/ST1	满刻度范围选/扩展控制模式选择 / Full-scale range select / extended control mode select	I	78	DQ7	Q 路数据输出位 DQ7（最高位）/ Q-channel data output bit DQ7 (MSB)	O
15	R	时钟置位控制输入 / Clock reset control input	I	79	DOR（反相）/ DOR (inverted)	溢出反相输出 / Overflow inverted output	O
16	VCC	模拟电源 / Analog supply	/	80	DOR	溢出同相输出 / Overflow in-phase output	O
17	VCC	模拟电源 / Analog supply	/	81	QCLK	数据时钟同相输出 / Data clock in-phase output	O

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
18	INCLK+	时钟输入正 / Clock input, positive	I	82	QCLK（反相）/ QCLK (inverted)	数据时钟反相输出 / Data clock inverted output	O
19	INCLK-	时钟输入负 / Clock input, negative	I	83	DI7	I 路数据输出位 DI7（最高位）/ I-channel data output bit DI7 (MSB)	O
20	VCC	模拟电源 / Analog supply	/	84	DI7（反相）/ DI7 (inverted)	I 路数据输出位 DI7（反相）（最高位）/ I-channel data output bit DI7 (inverted) (MSB)	O
21	GNDA	模拟地 / Analog ground	/	85	DI6	I 路数据输出位 DI6 / I-channel data output bit DI6	O
22	INQ+	Q 路模拟输入正 / Q-channel analog input, positive	I	86	DI6（反相）/ DI6 (inverted)	I 路数据输出位 DI6（反相）/ I-channel data output bit DI6 (inverted)	O
23	INQ-	Q 路模拟输入负 / Q-channel analog input, negative	I	87	GNDD	输出驱动地 / Output driver ground	/
24	GNDA	模拟地 / Analog ground	/	88	VDD	输出驱动电源 / Output driver supply	/
25	VCC	模拟电源 / Analog supply	/	89	DI5	I 路数据输出位 DI5 / I-channel data output bit DI5	O
26	PD	省电模式控制 / Power-down mode control	I	90	DI5（反相）/ DI5 (inverted)	I 路数据输出位 DI5（反相）/ I-channel data output bit DI5 (inverted)	O
27	GNDA	模拟地 / Analog ground	/	91	DI4	I 路数据输出位 DI4 / I-channel data output bit DI4	O
28	VCC	模拟电源 / Analog supply	/	92	DI4（反相）/ DI4 (inverted)	I 路数据输出位 DI4（反相）/ I-channel data output bit DI4 (inverted)	O
29	PDQ	Q 路省电模式控制 / Q-channel power-down mode control	I	93	DI3	I 路数据输出位 DI3 / I-channel data output bit DI3	O
30	CAL	校正控制 / Calibration control	I	94	DI3（反相）/ DI3 (inverted)	I 路数据输出位 DI3（反相）/ I-channel data output bit DI3 (inverted)	O
31	VREF	基准输出 / Reference output	O	95	DI2	I 路数据输出位 DI2 / I-channel data output bit DI2	O
32	Rext	外接电阻 / External resistor	O	96	DI2（反相）/ DI2 (inverted)	I 路数据输出位 DI2（反相）/ I-channel data output bit DI2 (inverted)	O
33	VCC	模拟电源 / Analog supply	/	97	GNDD	输出驱动地 / Output driver ground	/
34	Tdiode_p	温度二极管正级 / Temperature diode, positive	/	98	NC	空 / No connect	/
35	Tdiode_n	温度二极管负级 / Temperature diode, negative	/	99	VDD	输出驱动电源 / Output driver supply	/
36		Q 路数据输出位 DQd0（反相）（最低位）/ Q-channel data	O	100	DI1	I 路数据输出位 DI1 / I-channel data output bit DI1	O

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
	DQd0（反相）/ DQd0 (inverted)	output bit DQd0 (inverted) (LSB)					
37	DQd0	Q 路数据输出位 DQd0（最低位）/ Q-channel data output bit DQd0 (LSB)	O	101	DI1（反相）/ DI1 (inverted)	I 路数据输出位 DI1（反相）/ I-channel data output bit DI1 (inverted)	O
38	DQd1（反相）/ DQd1 (inverted)	Q 路数据输出位 DQd1（反相）/ Q-channel data output bit DQd1 (inverted)	O	102	DI0	I 路数据输出位 DI0（最低位）/ I-channel data output bit DI0 (LSB)	O
39	DQd1	Q 路数据输出位 DQd1 / Q-channel data output bit DQd1	O	103	DI0（反相）/ DI0 (inverted)	I 路数据输出位 DI0（反相）（最低位）/ I-channel data output bit DI0 (inverted) (LSB)	O
40	VDD	输出驱动电源 / Output driver supply	/	104	DId7	I 路数据输出位 DId7（最高位）/ I-channel data output bit DId7 (MSB)	O
41	GNDA	模拟地 / Analog ground	/	105	DId7（反相）/ DId7 (inverted)	I 路数据输出位 DId7（反相）（最高位）/ I-channel data output bit DId7 (inverted) (MSB)	O
42	GNDD	输出驱动地 / Output driver ground	/	106	DId6	I 路数据输出位 DId6 / I-channel data output bit DId6	O
43	DQd2（反相）/ DQd2 (inverted)	Q 路数据输出位 DQd2（反相）/ Q-channel data output bit DQd2 (inverted)	O	107	DId6（反相）/ DId6 (inverted)	I 路数据输出位 DId6（反相）/ I-channel data output bit DId6 (inverted)	O
44	DQd2	Q 路数据输出位 DQd2 / Q-channel data output bit DQd2	O	108	GNDD	输出驱动地 / Output driver ground	/
45	DQd3（反相）/ DQd3 (inverted)	Q 路数据输出位 DQd3（反相）/ Q-channel data output bit DQd3 (inverted)	O	109	NC	空 / No connect	/
46	DQd3	Q 路数据输出位 DQd3 / Q-channel data output bit DQd3	O	110	VDD	输出驱动电源 / Output driver supply	/
47	DQd4（反相）/ DQd4 (inverted)	Q 路数据输出位 DQd4（反相）/ Q-channel data output bit DQd4 (inverted)	O	111	DId5	I 路数据输出位 DId5 / I-channel data output bit DId5	O
48	DQd4	Q 路数据输出位 DQd4 / Q-channel data output bit DQd4	O	112	DId5（反相）/ DId5 (inverted)	I 路数据输出位 DId5（反相）/ I-channel data output bit DId5 (inverted)	O
49	DQd5（反相）/ DQd5 (inverted)	Q 路数据输出位 DQd5（反相）/ Q-channel data output bit DQd5 (inverted)	O	113	DId4	I 路数据输出位 DId4 / I-channel data output bit DId4	O
50	DQd5	Q 路数据输出位 DQd5 / Q-channel data output bit DQd5	O	114	DId4（反相）/ DId4 (inverted)	I 路数据输出位 DId4（反相）/ I-channel data output bit DId4 (inverted)	O
51	VDD	输出驱动电源 / Output driver supply	/	115	DId3	I 路数据输出位 DId3 / I-channel data output bit DId3	O

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
52	NC	空 / No connect	/	116	DId3（反相）/ DId3 (inverted)	I 路数据输出位 DId3（反相）/ I-channel data output bit DId3 (inverted)	O
53	GNDD	输出驱动地 / Output driver ground	/	117	DId2	I 路数据输出位 DId2 / I-channel data output bit DId2	O
54	DQd6（反相）/ DQd6 (inverted)	Q 路数据输出位 DQd6（反相）/ Q-channel data output bit DQd6 (inverted)	O	118	DId2（反相）/ DId2 (inverted)	I 路数据输出位 DId2（反相）/ I-channel data output bit DId2 (inverted)	O
55	DQd6	Q 路数据输出位 DQd6 / Q-channel data output bit DQd6	O	119	GNDD	输出驱动地 / Output driver ground	/
56	DQd7（反相）/ DQd7 (inverted)	Q 路数据输出位 DQd7（反相）（最高位）/ Q-channel data output bit DQd7 (inverted) (MSB)	O	120	NC	空 / No connect	/
57	DQd7	Q 路数据输出位 DQd7（最高位）/ Q-channel data output bit DQd7 (MSB)	O	121	VDD	输出驱动电源 / Output driver supply	/
58	DQ0（反相）/ DQ0 (inverted)	Q 路数据输出位 DQ0（反相）（最低位）/ Q-channel data output bit DQ0 (inverted) (LSB)	O	122	DId1	I 路数据输出位 DId1 / I-channel data output bit DId1	O
59	DQ0	Q 路数据输出位 DQ0（最低位）/ Q-channel data output bit DQ0 (LSB)	O	123	DId1（反相）/ DId1 (inverted)	I 路数据输出位 DId1（反相）/ I-channel data output bit DId1 (inverted)	O
60	DQ1（反相）/ DQ1 (inverted)	Q 路数据输出位 DQ1（反相）/ Q-channel data output bit DQ1 (inverted)	O	124	DId0	I 路数据输出位 DId0 / I-channel data output bit DId0	O
61	DQ1	Q 路数据输出位 DQ1 / Q-channel data output bit DQ1	O	125	DId0（反相）/ DId0 (inverted)	I 路数据输出位 DId0（反相）/ I-channel data output bit DId0 (inverted)	O
62	VDD	输出驱动电源 / Output driver supply	/	126	QCAL	校正运行指示输出 / Calibration-running indicator output	O
63	NC	空 / No connect	/	127	CalDly/DES/ST2（反相）/ CalDly/DES/ST2 (inverted)	上电校正延迟选择/双沿采样控制/串行接口选通 / Power-up calibration delay select / dual-edge sampling control / serial interface strobe	I
64	GNDD	输出驱动地 / Output driver ground	/	128	VCC	模拟电源 / Analog supply	/

注：本产品数据输出（DI、DId、DQ、DQd）、溢出输出（DOR）和数据时钟输出（QCLK）的同相/反相引出端与国外产品不一致，与进口器件是相反的，但不影响使用。 Note: The in-phase/inverted pins of the data outputs (DI, DId, DQ, DQd), overflow output (DOR), and data clock output (QCLK) of this product are interchanged relative to the imported device; this does not affect use.

8. 推荐工作条件 / Recommended Operating Conditions

- 模拟电源电压（VCC）： 1.95V～2.05V / Analog supply voltage (VCC): 1.95V–2.05V
- 输出驱动电源电压（VDD）： 1.95V～2.05V / Output driver supply voltage (VDD): 1.95V–2.05V
- 模拟输入共模电压（VCM）： 1.2V～1.33V / Analog input common-mode voltage (VCM): 1.2V–1.33V
- 差分模拟输入范围（VIN）： 570～1100mVpp / Differential analog input range (VIN): 570–1100mVpp
- 串行接口时钟输入频率（fSCLK）： 100MHz / Serial interface clock input frequency (fSCLK): 100MHz
- 时钟频率范围（fclk）： 200MHz～1500MHz / Clock frequency range (fclk): 200MHz–1500MHz
- 时钟输入占空比（QC）： 典型 50% / Clock input duty cycle (QC): typ 50%
- 差分时钟输入幅度（VID）： 0.5～2.0VPP，典型 0.6 VPP / Differential clock input amplitude (VID): 0.5–2.0VPP, typ 0.6 VPP
- 工作温度（TA）： -40°C～85°C / Operating temperature (TA): -40°C to 85°C

9. 绝对最大额定值 / Absolute Maximum Ratings

- 模拟电源电压（VCC）： 2.2V / Analog supply voltage (VCC): 2.2V
- 输出驱动电源电压（VDD）： 2.2V / Output driver supply voltage (VDD): 2.2V
- 电源差 VDD-VCC：0V～100mV / Supply difference VDD–VCC: 0V–100mV
- 任一引脚的输入电流：±25mA / Input current at any pin: ±25mA
- 引线耐焊接温度 TH（10s）： 300°C / Lead soldering temperature TH (10s): 300°C
- 贮存温度 TS：-65°C～150°C / Storage temperature TS: -65°C to 150°C

---

10. 性能指标 / Performance Specifications

除另有规定外，VCC=VDD=2.0V，GNDA=GNDD=0V，-40°C≤TA≤85°C，模拟输入交流耦合，时钟交流耦合输入，占空比 50%；外接电阻 Rext=3300Ω±0.1%。 Unless otherwise specified, VCC=VDD=2.0V, GNDA=GNDD=0V, -40°C ≤ TA ≤ 85°C, AC-coupled analog input, AC-coupled clock input, 50% duty cycle; external resistor Rext=3300Ω±0.1%.

特性 / Characteristic	符号 / Symbol	条件 / Condition	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
分辨率 / Resolution	RES	—	—	8	—	Bits
模拟电源电流 / Analog supply current	ICC	fclk=1.5GHz，VPD=VPDQ=0.3V	—	948	1000	mA
数字电源电流 / Digital supply current	IDD	fclk=1.5GHz，VPD=VPDQ=0.3V	—	248	300	mA
功耗 / Power dissipation	PD	fclk=1.5GHz，VPD=VPDQ=0.3V	—	2.4	2.6	W
积分非线性误差 / Integral nonlinearity error	EL	DC 耦合，1MHz 正弦波，数据输出单数据速率（见图 2）/ DC-coupled, 1MHz sine wave, single-data-rate output (see Figure 2)	-1.2	±0.7	1.2	LSB
微分非线性误差 / Differential nonlinearity error	EDL	DC 耦合，1MHz 正弦波，数据输出单数据速率（见图 2）/ DC-coupled, 1MHz sine wave, single-data-rate output (see Figure 2)	-0.9	±0.5	1.0	LSB
失调误差 / Offset error	EO	数据输出双倍数据速率（见图 3）/ Double-data-rate output (see Figure 3)	-2.5	±0.2	2.5	LSB

特性 / Characteristic	符号 / Symbol	条件 / Condition	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
正满刻度误差 / Positive full-scale error	EFS+	—	-40	20	40	mV
负满刻度误差 / Negative full-scale error	EFS-	—	-40	20	40	mV
带隙基准输出电压 / Bandgap reference output voltage	VREF	IREF=±100μA	1.2	1.28	1.33	V
模拟差分输入电压 / Analog differential input voltage	VID1(pp)	FSR（14 脚）接地 / FSR (pin 14) grounded	570	685	900	mV
		FSR（14 脚）接 VCC / FSR (pin 14) at VCC	790	905	1100	mV
模拟差分输入电阻 / Analog differential input resistance	RI	—	94	102	106	Ω
时钟差分输入电压 / Clock differential input voltage	VID2(pp)	—	0.5	1.2	2	V
逻辑输入高电平 / Logic input high level	VIH	测试 Outv，R，PD，PDQ 脚 / Tested at Outv, R, PD, PDQ pins	1.6	—	—	V
逻辑输入低电平 / Logic input low level	VIL	—	—	—	0.3	V
数字输出高电平 / Digital output high level	VOH	测试 QCAL（126 脚）/ Tested at QCAL (pin 126)	1.5	1.8	—	V
数字输出低电平 / Digital output low level	VOL	测试 QCAL（126 脚）/ Tested at QCAL (pin 126)	—	0.1	0.3	V
LVDS 差分输出电压 / LVDS differential output voltage	VOD(PP)	VOutv=1.6V，VREF 脚悬空 / VOutv=1.6V, VREF pin floating	400	700	1000	mV
		VOutv=0.3V，VREF 脚悬空 / VOutv=0.3V, VREF pin floating	280	500	800	mV
溢出输出码 / Overflow output code	OROC	(VIN+-VIN-)＞正满度 / >positive full scale	255	—	—	
		(VIN+-VIN-)＜负满度 / <negative full scale	—	—	0	
增益平坦度 / Gain flatness	ΔA	fclk=1.5GHz，fIN=99MHz、199MHz、299MHz、399MHz、499MHz，TA=25°C	-1	0.7	1	dBFS
信噪比 / SNR	SNR	fclk=1.5GHz，fIN=373MHz	42	46.1	—	dB
有效位 / ENOB	ENOB	ENOB=(SNR-1.76)/6.02	6.6	7.3	—	Bits
信噪失真比 / SINAD	SINAD	fclk=1.5GHz，fIN=373MHz	41.5	45.4	—	dB
无杂散动态范围 / SFDR	SFDR	fclk=1.5GHz，fIN=373MHz	45	57.1	—	dB
总谐波失真 / THD	THD	fclk=1.5GHz，fIN=373MHz	—	-57.2	-45	dB
双路合成信噪比 / Interleaved (DES) SNR	SNRDS	fclk=1.5GHz，fIN=373MHz，TA=25°C，见图 9 时序 / see Figure 9 timing	34	41.0	—	dB
最大转换速率 / Maximum conversion rate	SRmax	fIN=373MHz	1.5	—	—	GSPS
	QDC	—	45	50	55	%

特性 / Characteristic	符号 / Symbol	条件 / Condition	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
输出时钟占空比 / Output clock duty cycle						
时钟置位脉冲宽度 / Clock reset pulse width	tRPW	见图 5～图 7 时序 / See Figures 5–7 timing	4	—	—	Clock Cycles
校正控制低电平时间 / Calibration control low-level time	tCAL_L	见图 8 时序 / See Figure 8 timing	80	—	—	Clock Cycles
校正控制高电平时间 / Calibration control high-level time	tCAL_H	见图 8 时序 / See Figure 8 timing	80	—	—	Clock Cycles

注：典型值为常温测试数据。 Note: Typical values are room-temperature test data.

11. 主要特性曲线图（电特性测试图）/ Typical Performance Curves (Electrical Test Plots)

1、fclk=1.5GSPS，模拟输入 373MHz 条件下 FFT 谱线 / FFT spectrum at fclk=1.5GSPS with 373MHz analog input

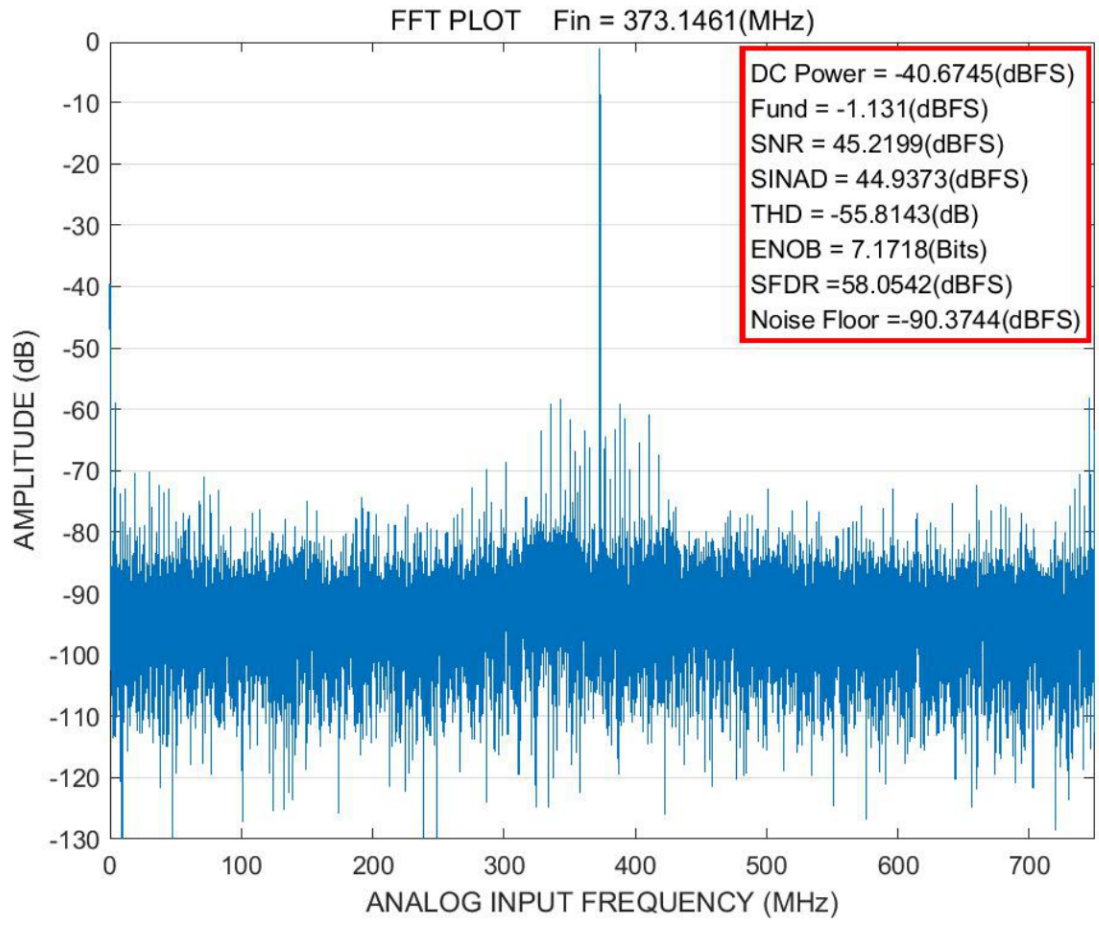


Figure 12: fclk=1.5GSPS，fIN=373MHz 谱线，TA=25°C

2、fclk=1.5GSPS，微分非线性误差（EDL）和积分非线性误差（EL）曲线 / DNL (EDL) and INL (EL) curves at fclk=1.5GSPS

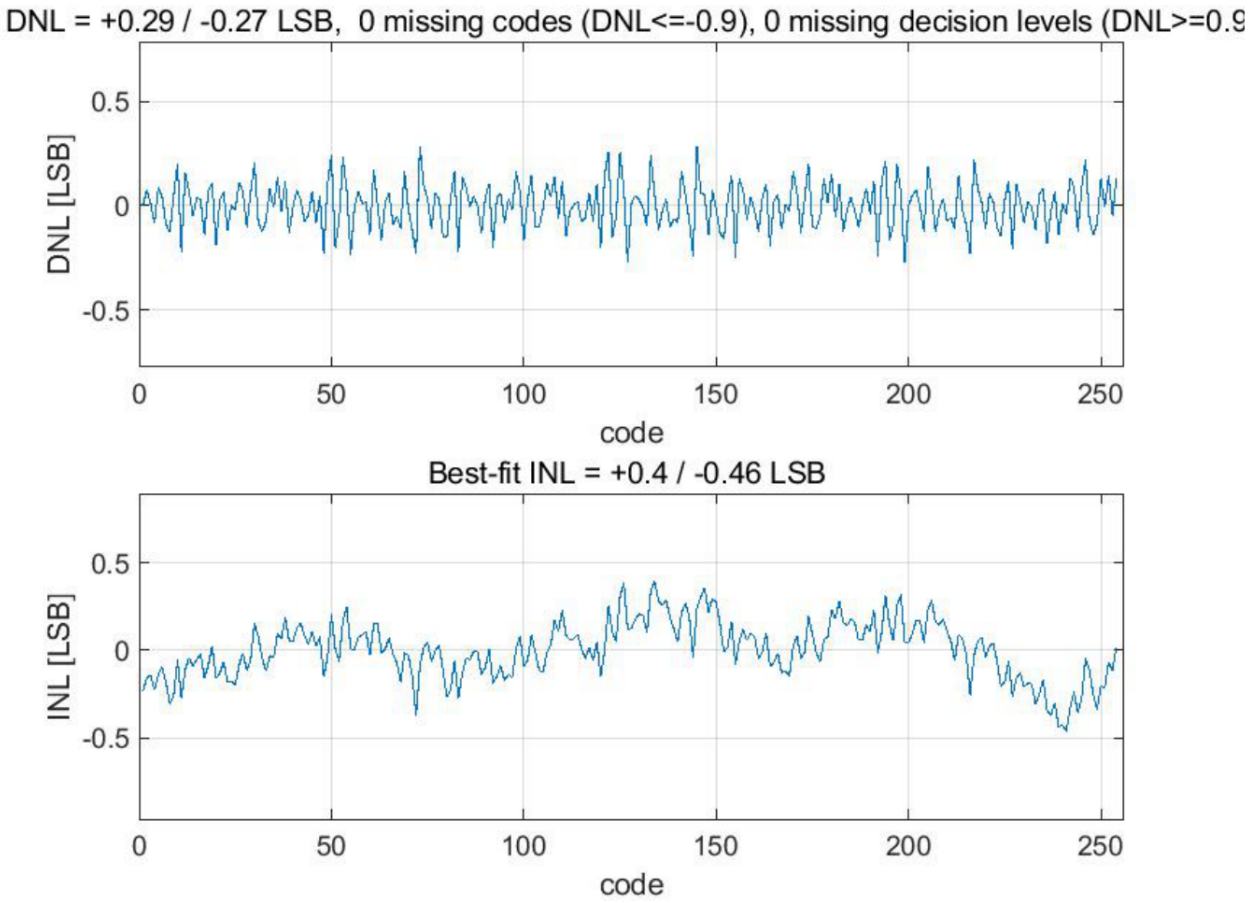


Figure 13: 微分非线性误差（EDL）和积分非线性误差（EL）测试曲线，fclk=1.5GSPS，TA=25°C

12. 典型应用线路图 / Typical Application Circuits

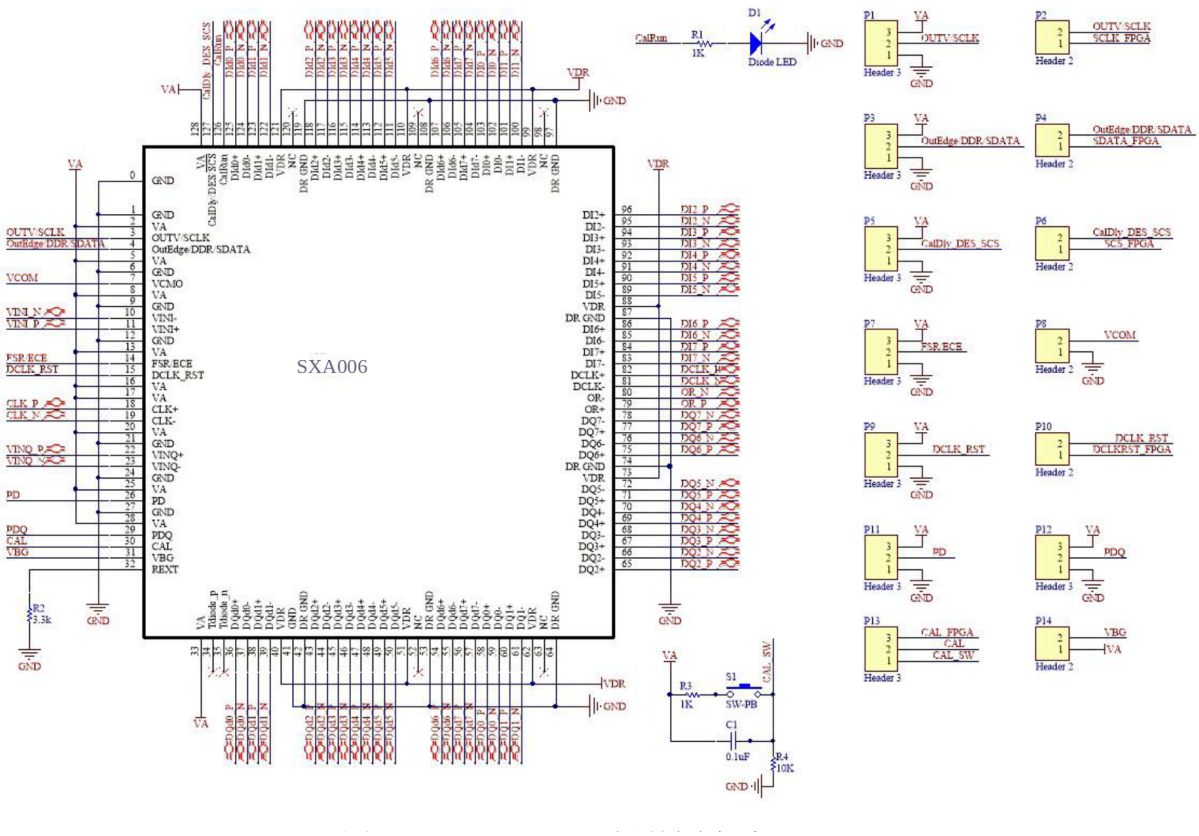


Figure 14: SXA006 PCB 板外围电路

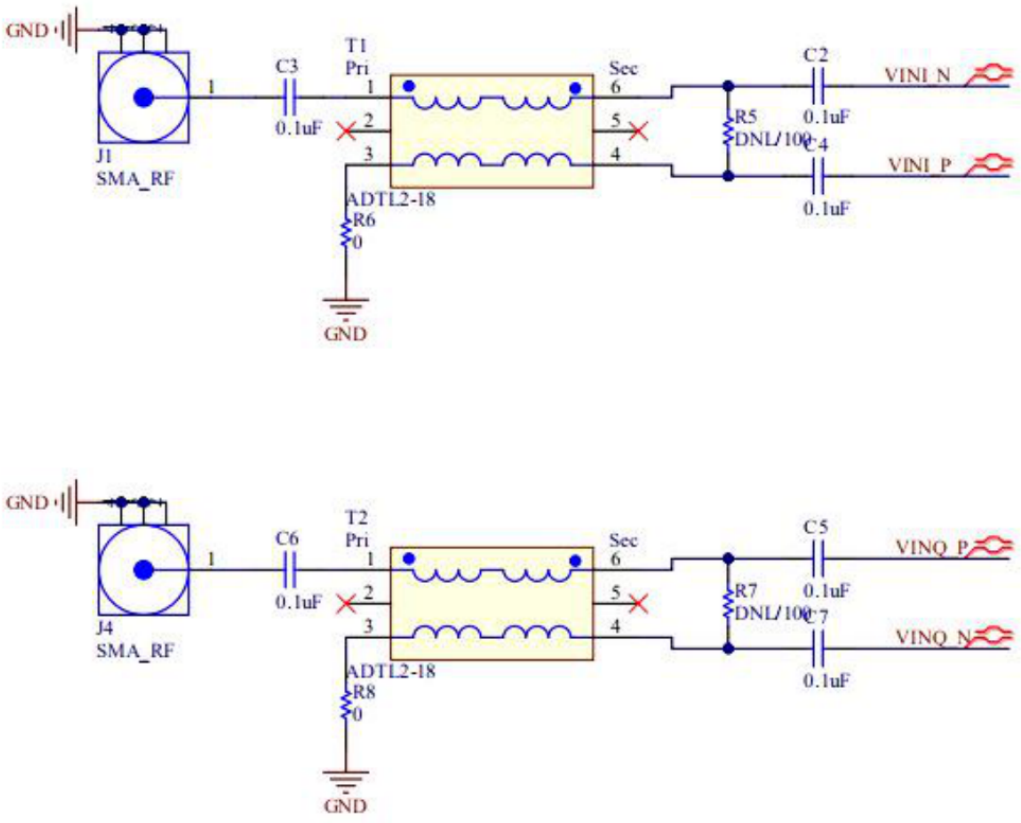


Figure 15: SXA006 PCB 板模拟输入前端电路

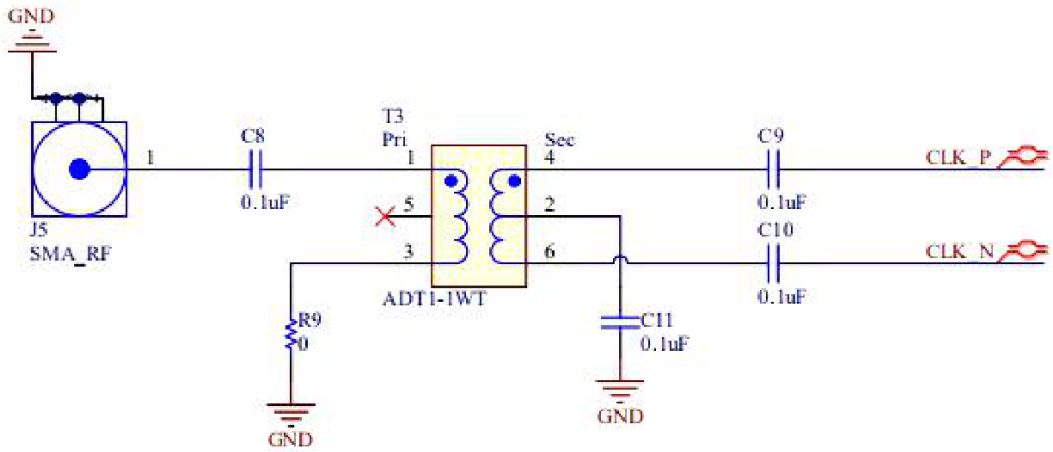


Figure 16: SXA006 PCB 板时钟输入前端电路

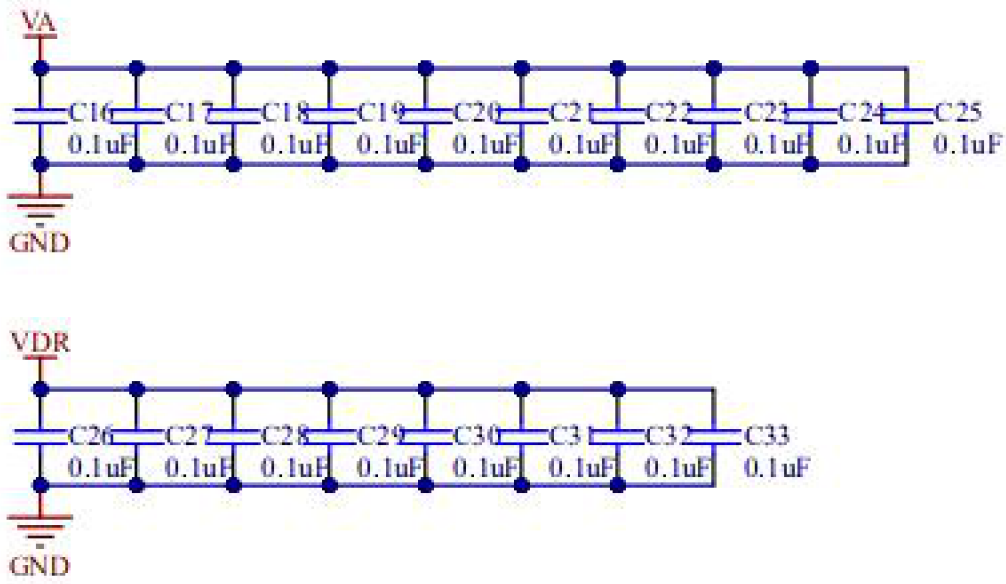


Figure 17: SXA006 PCB 板电源滤波电路

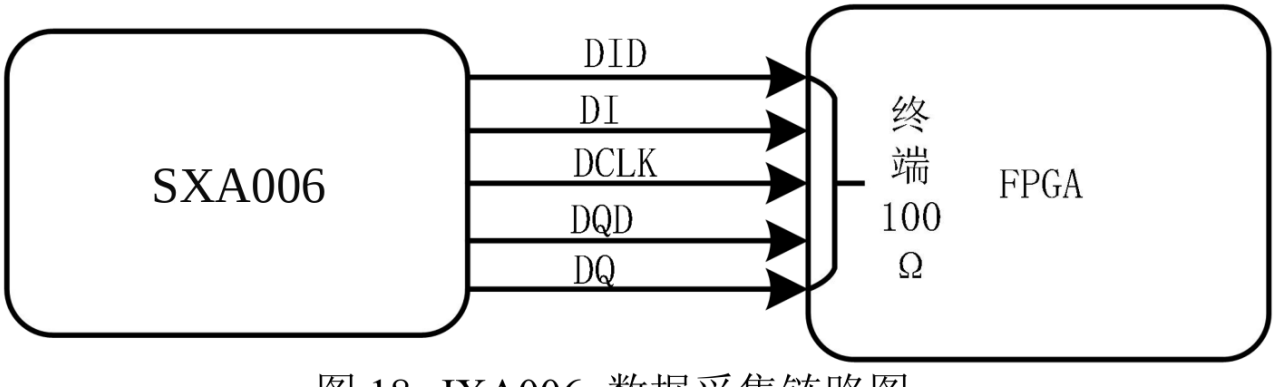


Figure 18: SXA006 数据采集链路图

AD 供电：电源 VCC、VDD 建议同时上电或先上电 VCC 再上电 VDD；电源滤波按照上图 20 所示，每组电源均需加滤波电容进行滤波。 AD power supplies: VCC and VDD should preferably be powered up simultaneously, or VCC first and then VDD; for power-supply filtering, refer to Figure 20 above, and each supply group requires a filter capacitor.

AD 工作原理和工作模式：主要包含时钟输入，作为 ADC 的采样时钟，模拟输入端的模拟信号进行 AD 转换，通过 LVDS 接口传输至接收端进行数字处理；工作模式分为 Pin 模式和扩展模式，具体见表 6 控制模式表。 AD operating principle and modes: the clock input serves as the ADC sampling clock; the analog signal at the analog input is A/D-converted and transmitted via the LVDS interface to the receiver for digital processing. The operating modes are the pin mode and the extended mode; see Table 6, the control mode table.

注意事项： 本产品数据输出（DI、DId、DQ、DQd）、溢出输出（DOR）和数据时钟输出（QCLK）的同相/反相引出端与国外产品不一致，相位与进口器件相比是相反的。即在同一引出端下本器件为同相输出，进口器件为反相输出；反之，本器件为反相输出，进口器件为同相输出，这不影响使用。除这 3 类输出端外，其余与进口器件相同。 Cautions: The in-phase/inverted pins of the data outputs (DI, DId, DQ, DQd), overflow output

(DOR), and data clock output (QCLK) of this product are interchanged relative to the imported device, i.e., the phases are opposite to those of the imported device. At the same pin, where this device provides an in-phase output the imported device provides an inverted output, and vice versa; this does not affect use. Apart from these three classes of outputs, all other pins are the same as the imported device.

如果要求本器件输出端与进口器件输出一致，可以通过以下两种方式进行调整： （1）在本器件 SXA006 的输出端（数据输出、溢出输出和数据时钟输出）接一个反相器，使数据相位在使用时与进口器件一致； （2）在采集输出端（数据输出、溢出输出和数据时钟输出）数据时，先通过 FPGA 在软件上先进行一个反相操作，使数据在使用时与进口器件一致。 If the outputs of this device are required to match those of the imported device, either of the following two adjustments can be used: (1) Connect an inverter at the outputs of the SXA006 (data outputs, overflow output, and data clock output) so that the data phase in use matches the imported device; (2) When acquiring data at the output side (data outputs, overflow output, and data clock output), first perform an inversion in software in the FPGA so that the data in use matches the imported device.

---

13. 单元模块及工作原理 / Functional Blocks and Theory of Operation

1 功能描述 / Functional Description

1.1 概述 / Overview

SXA006 采用了带校正的折叠内插结构，可以达到 7.3bit 的有效位。折叠运放的应用极大地减少了比较器的数量和功耗。内插结构减少了前置运放的数量，同时减少了输入信号的负载电容，更进一步降低了功耗。除此以外，器件集成校正降低了因折叠结构引起的 INL 弓形。通过这些技术实现了超高速、高性能、低功耗的转换器。

The SXA006 uses a folding and interpolating architecture with calibration, achieving an effective resolution of 7.3 bits. Folding amplifiers greatly reduce the number of comparators and the power consumption. The interpolating structure reduces the number of preamplifiers and the load capacitance on the input signal, further reducing power consumption. In addition, integrated calibration reduces the INL bow caused by the folding structure. These techniques realize an ultra-high-speed, high-performance, low-power converter.

在转换器输入电压范围内的模拟输入信号被数字化为 8 位码值输出，转换速率为 200MSPS～1.5GSPS。典型情况下差分输入电压低于负的满刻度值将使输出码值全为 0；差分输入电压高于正的满刻度值将使输出码值全为 1。"I"或"Q"通道出现上面两个中任一种情况将会溢出输出范围，这些单个的输出码值超出范围指的是从一个通道或两个通道输出的码值低于负的满刻度值或超出正的满刻度值。两通道转换器都有一个满足两路 LVDS 输出总线的 1:2 多路信号分离器，这些输出总线上的数据在每条总线上以采样率一半的速率输出，同时使用者可以选择隔行扫描来达到采样率的速率输出。

Analog input signals within the converter input voltage range are digitized into 8-bit output codes at conversion rates from 200MSPS to 1.5GSPS. Typically, a differential input voltage below the negative full-scale value makes all output codes 0, and a differential input voltage above the positive full-scale value makes all output codes 1. If either case occurs in the "I" or "Q" channel, the output over-ranges; these individual out-of-range output codes are codes from one or both channels that fall below the negative full-scale value or exceed the positive full-scale value. Each of the two channel converters has a 1:2 demultiplexer feeding two LVDS output buses; data on each bus is output at half the sample rate, and the user can select interleaved operation to obtain output at the full sample rate.

输出幅度可以选择普通模式或者低幅度模式。采用低幅度模式可以降低功耗但会造成一些或所有的数据采集，特别是在高采样率和边界设计系统下。

The output amplitude can be selected as normal mode or low-amplitude mode. The low-amplitude mode reduces power consumption but may compromise some or all data acquisition, especially at high sample rates and in marginally designed systems.

a. 自校正 / Self-Calibration

上电和用户指令都可以启动自校正。自校正主要用来修调 100Ω 模拟输入差分终端电阻，同时最小化满刻度误差、失调误差、DNL 和 INL，最大化 SNR、THD、SINAD 和 ENOB，同样内部偏置电流也是通过自校正过程来进行设置。上电自校正和用户指令启动自校正都可以实现这些目的。自校正是器件功能的一个重要组成部分，其目的是使器件达到更好的性能。自校正除了在上电启动外，只要 FSR 引脚（14 脚）的控制发生变化就要重新启动自校正。为了达到更好的性能，我们建议在上电之后和器件工作温度相对与系统性能要求的温度差别很大时，让自校正运行 20 秒或更长时间。更详细的可参考 2.4）.b.②指令校正。当器件处于省电模式（PD 或 PDQ 为高）时，自校正不能初始化或者运行。更详细的信息可参考 1.1）.g 省电模式自校正与省电模式的关系。

Self-calibration can be initiated at power-up or by a user command. It primarily trims the 100Ω analog input differential termination resistance, minimizes full-scale error, offset error, DNL, and INL, and maximizes SNR, THD, SINAD, and ENOB; the internal bias currents are also set through the self-calibration process. Both power-up self-calibration and user-commanded self-calibration achieve these purposes. Self-calibration is an important part of the device function, intended to bring the device to its best performance. In addition to running at power-up, self-calibration must be re-run whenever the control state of the FSR pin (pin 14) changes. For best performance, it is recommended to let self-calibration run for 20 seconds or longer after power-up and when the device operating temperature differs greatly from the temperature required by the system performance. See 2.4).b.② for details on commanded calibration. When the device is in power-down mode (PD or PDQ high), self-calibration cannot be initialized or run. See 1.1).g for the relationship between self-calibration and power-down mode.

在普通工作模式下，器件上电和输入一个有效的校正指令，自校正都会工作。校正指令保持 CAL 引脚（30 脚）为低至少一个 tCAL_L 时钟周期，接着保持 CAL 引脚为高至少另个 tCAL_H 时钟周期，其中 tCAL_L 和 tCAL_H 在转换器电特性中定义的，见图 8。自校正所占有的时间为转换器电特性中定义的 tCAL。在上电之后保持 CAL 引脚为高将阻止自校正过程运行，直到 CAL 引脚出现前面提到的 tCAL_L 时钟周期紧跟着是 tCAL_H 时钟周期。

In normal operating mode, self-calibration runs both at power-up and upon a valid calibration command. A calibration command holds the CAL pin (pin 30) low for at least one tCAL_L clock cycle and then high for at least another tCAL_H clock cycle, where tCAL_L and tCAL_H are defined in the converter electrical characteristics; see Figure 8. Self-calibration occupies the time tCAL defined in the converter electrical characteristics. Holding the CAL pin high after power-up prevents the self-calibration process from running until the CAL pin sees the aforementioned tCAL_L clock cycles followed by tCAL_H clock cycles.

CalDly（引脚 127）用来选择在上电之后到自校正开始运行时的 2 个延迟时间之中的 1 个，自校正的延迟时间由 CalDly 引脚设置，在转换器电特性中定义为 tCalDly，见表 3 所示。这些延迟时间的长度为电源电压上电并稳定到自校正工作这段时间。在上电之后如果 PD（26 脚）这个引脚为高，自校正延迟计算器将会无效，直到 PD 引脚重新为低。因此，在上电后保持 PD 引脚为高，将进一步延迟上电后自校正周期的开始。CalDly 引脚最好的设置依赖于电源电压的上电设置时间。

CalDly (pin 127) selects one of the two delay times between power-up and the start of self-calibration. The self-calibration delay time is set by the CalDly pin and is defined as tCalDly in the converter electrical

characteristics; see Table 3. These delays are the time allowed for the supply voltage to power up and stabilize before self-calibration works. If the PD pin (pin 26) is high after power-up, the self-calibration delay counter is disabled until the PD pin returns low. Therefore, holding the PD pin high after power-up further delays the start of the power-up self-calibration cycle. The best CalDly setting depends on the supply voltage power-up settling time.

表3 上电延迟时间控制功能表（PD 为低电平）/ Table 3 Power-Up Delay Control (PD Low)

CalDly（引脚 127）/ CalDly (pin 127)	上电延迟选择（tCalDly）/ Power-Up Delay Selection (tCalDly)
H	231 个输入时钟周期 / 231 input clock cycles
L	225 个输入时钟周期 / 225 input clock cycles
DES（双沿采样模式）/ DES (dual-edge sampling mode)	225 个输入时钟周期 / 225 input clock cycles

自校正工作注意事项：●在自校正周期期间，溢出（QOR）输出可能是校正算法的一个有用结果。在校正期间，所有数据输出和溢出输出的数据是无效的。●在上电校正期间和指令校正期间，所有时钟都停止，包括内部时钟和输出时钟 QCLK；这时输入终端电阻阻值被修调到 Rext/33。在校正周期中校正输入电阻是校正期间的一部分，目的是为了减少噪声。参考 2.4）.b.自校正。这个外接电阻位于引脚 32 与地之间，Rext 必须精确等于 3300Ω±0.1%。利用这个值，输入终端电阻阻值被修调为 100Ω。因为 Rext 还用来为采样/保持运放、前置放大器和比较器设置适当的偏置电流，所以 Rext 的其它值不能采用。●只要校正在运行，无论是上电自校正还是用户指令启动自校正，CalRun 输出都为高。 Notes on self-calibration operation: ● During a self-calibration cycle, the overflow (QOR) output may be a useful result of the calibration algorithm. During calibration, all data outputs and overflow outputs are invalid. ● During power-up calibration and commanded calibration, all clocks stop, including the internal clock and the output clock QCLK; at this time the input termination resistance is trimmed to Rext/33. Calibrating the input resistance during the calibration cycle is part of the calibration, intended to reduce noise. See 2.4).b. This external resistor is located between pin 32 and ground, and Rext must be exactly 3300Ω±0.1%. With this value, the input termination resistance is trimmed to 100Ω. Because Rext is also used to set the proper bias currents for the sample-and-hold amplifier, preamplifiers, and comparators, no other value of Rext may be used. ● Whenever calibration is running, whether power-up self-calibration or user-commanded self-calibration, the CalRun output is high.

b. 输出数据的捕获 / Output Data Capture

在时钟 INCLK+（引脚 18）的下降沿数据输出，即在 13 个输入时钟周期后 DI 和 DQ 端输出的数据和在 14 个输入时钟周期后 DId 和 DQd 端输出的数据有效。输出数据在输出获得之前，有另外的内部延迟叫 tOD，见时序图。只要有输入时钟信号，SXA006 就会进行数据转换工作。全差分比较器设计和创新的采样保持放大器设计，以及自校正技术，在 1.5GHz 以下获得了一个非常平坦的 SINAD/ENOB 响应。SXA006 输出数据信号是 LVDS，输出格式是二进制偏移码。

Data is output on the falling edge of the clock INCLK+ (pin 18): the data at the DI and DQ outputs is valid after 13 input clock cycles, and the data at the DId and DQd outputs is valid after 14 input clock cycles. Before the output data is obtained there is an additional internal delay called tOD; see the timing diagrams. As long as an input clock signal is present, the SXA006 performs data conversion. The fully differential comparator design, the innovative sample-and-hold amplifier design, and the self-calibration

technique provide a very flat SINAD/ENOB response below 1.5GHz. The SXA006 output data signals are LVDS, in offset binary format.

c. 控制模式 / Control Modes

提供的多个控制引脚实现了用户控制的多种模式。例如包括校正循环的初始化，省电模式和满刻度范围设置控制。然而，SXA006 也提供一个扩展控制模式，通过扩展控制模式，一个串行接口被用来访问基于寄存器的许多高级特性的控制。这个扩展控制模式不能自动被使用，而使用者希望在所有时间都能用普通控制模式或者扩展控制模式。当器件处于扩展控制模式时，基于引脚控制的许多特性就会被基于寄存器控制的特性所取代，那些基于引脚的控制将无效。这些引脚是 Outv（引脚 3），OutEdge/DDR（引脚 4），FSR（引脚 14）和 CalDly/DES（引脚 127），见表 4 所示。关于扩展控制模式更详细的信息请参考 1.2）普通/扩展控制模式。

Multiple control pins provide various user-controlled modes, including calibration cycle initialization, power-down mode, and full-scale range setting control. However, the SXA006 also provides an extended control mode, through which a serial interface accesses register-based control of many advanced features. The extended control mode is not engaged automatically; the user is expected to use either the normal control mode or the extended control mode at all times. When the device is in extended control mode, many pin-based control features are replaced by register-based control features, and those pin-based controls become ineffective. These pins are Outv (pin 3), OutEdge/DDR (pin 4), FSR (pin 14), and CalDly/DES (pin 127); see Table 4. For more information on the extended control mode, see 1.2).

表4 控制模式表 / Table 4 Control Mode Table

控制输入 / Control Input	FSR/ST1（14 引脚）/ FSR/ST1 (pin 14)	CalDly/DES/ST2（127 引脚）/ CalDly/DES/ST2 (pin 127)	OutEdge/DDR/DATA（4 引脚）/ OutEdge/DDR/DATA (pin 4)	Outv/SCLK（3 引脚）/ Outv/SCLK (pin 3)
控制模式：普通模式（FSR/ST1 为 H 或 L（VCC 或 GND））/ Normal mode (FSR/ST1 = H or L (VCC or GND))	——	上电校正延迟选择：H 时延迟 231 个时钟周期；L 时延迟 225 个时钟周期 / Power-up calibration delay select: 231 clock cycles when H; 225 clock cycles when L	双沿采样：悬空或 0.5VCC；单数据速率模式（SDR）：为 H 或 L；双倍数据速率模式（DDR）：悬空或 0.5VCC / Dual-edge sampling: floating or 0.5VCC; SDR mode: H or L; DDR mode: floating or 0.5VCC	控制 LVDS 输出幅度：H 时输出正常幅度；L 时输出幅度降低 / LVDS output amplitude control: normal amplitude when H; reduced amplitude when L
控制模式：扩展模式（FSR/ST1 悬空或 VCC/2）/ Extended mode (FSR/ST1 floating or VCC/2)	——	选通扩展模式串行接口的时钟和数据 / Strobes the extended-mode serial interface clock and data	H 时串行数据输入被封锁；L 时串行数据输入 / Serial data input blocked when H; serial data input when L	H 时串行时钟输入被封锁；L 时串行时钟输入 / Serial clock input blocked when H; serial clock input when L

d. 模拟输入 / Analog Input

SXA006 必须由一个差分输入信号驱动，单端信号工作不是推荐的。交流耦合输入时，VCMO（7 引脚）接地；当直流耦合输入时，VCMO 引脚悬空，但输入共模电压必须等于 VCMO 的输出电压。

The SXA006 must be driven by a differential input signal; single-ended operation is not recommended. With AC-coupled input, VCMO (pin 7) is grounded; with DC-coupled input, the VCMO pin is left floating, but the input common-mode voltage must equal the VCMO output voltage.

引脚 14（FSR）提供了 2 个满刻度范围设置，在普通模式下，由 FSR 设置来控制输入满刻度范围，通过转换器电特性中参数模拟输入范围来定义的，满刻度范围设置时对两个 ADC 都有效。在扩展控制模式，输入满刻度范围由串行接口的数据输入进行调节，在 1.4）和 2.2）中进行叙述。模拟输入满刻度范围控制见表 5。

Pin 14 (FSR) provides two full-scale range settings. In normal mode, the FSR setting controls the input full-scale range, defined by the analog input range parameter in the converter electrical characteristics; the full-scale range setting applies to both ADCs. In extended control mode, the input full-scale range is adjusted by serial interface data input, as described in 1.4) and 2.2). See Table 5 for analog input full-scale range control.

表5 模拟输入满刻度范围控制表 / Table 5 Analog Input Full-Scale Range Control

FSR	模拟差分输入满刻度范围 / Analog Differential Input Full-Scale Range
H	790～1100mVpp，典型 910 mVpp / 790–1100mVpp, typ 910 mVpp
L	570～900 mVpp，典型 695 mVpp / 570–900 mVpp, typ 695 mVpp
悬空或 VCC/2 / Floating or VCC/2	串行接口的 9 位二进制码输入控制，560～840 mVpp，默认 700 mVpp / Controlled by 9-bit binary code input via the serial interface, 560–840 mVpp, default 700 mVpp

e. 时钟输入/输出 / Clock Input/Output

SXA006 必须由一个差分时钟信号通过交流耦合连接来驱动，2.3）描述了时钟输入引脚的用法。一个差分 LVDS 输出时钟用来锁存 ADC 输出数据，便于后续器件接收数据。

The SXA006 must be driven by a differential clock signal through an AC-coupled connection; 2.3) describes the use of the clock input pins. A differential LVDS output clock is used to latch the ADC output data for reception by subsequent devices.

SXA006 提供了两种输出时钟选择，一种是选择输出数据在输出时钟 QCLK 的上沿转换还是在输出时钟的下沿转换，另一种选择是单数据速率（SDR）输出，还是双数据速率（DDR）输出，见表 6，时序见图 2、图 3。

The SXA006 provides two output clock selections: whether the output data transitions on the rising edge or the falling edge of the output clock QCLK, and whether the output is single data rate (SDR) or double data rate (DDR); see Table 6, and Figures 2 and 3 for timing.

表6 输出时钟选择（FSR 为 H 或 L）/ Table 6 Output Clock Selection (FSR = H or L)

OutEdge/DDR（4 引脚）/ OutEdge/DDR (pin 4)	模式 / Mode	输出时钟 / Output Clock
H	SDR	频率为 1/2 输入频率，输出数据在该时钟的上沿转换 / Frequency is 1/2 the input frequency; output data transitions on the rising edge of this clock
L	SDR	频率为 1/2 输入频率，输出数据在该时钟的下沿转换 / Frequency is 1/2 the input frequency; output data transitions on the falling edge of this clock
悬空或 VCC/2 / Floating or VCC/2	DDR	频率为 1/4 输入频率，输出数据在该时钟的上下沿转换 / Frequency is 1/4 the input frequency; output data transitions on both edges of this clock

SXA006 时钟输入内部有一个占空比调节器，以改善内部时钟性能，可通过扩展模式（地址码 0001）进行选择，使占空比调节器是否工作，默认设置是工作的。占空比调节器允许 ADC 的时钟可以是一个占空比为 20～80%（最差情况）的信号源。

The SXA006 clock input contains an internal duty-cycle adjuster to improve internal clock performance. It can be selected via extended mode (address code 0001) whether the duty-cycle adjuster operates; the default setting is operating. The duty-cycle adjuster allows the ADC clock to be a source with a duty cycle of 20–80% (worst case).

① 双沿采样（DES）功能 / Dual-Edge Sampling (DES)

DES 模式允许 SXA006 中的一个输入（I 或 Q 通道）被两个 ADC 所采样。一个 ADC 在输入时钟的正边沿采样输入信号，另一个 ADC 在输入时钟的负边沿采样输入。因此信号输入在每个时钟周期被采样两次，所以一个完整的采样率是输入时钟频率的两倍，或者对于 1.5GHz 的输入时钟采样率为 3GSPS。

The DES mode allows one input of the SXA006 (I or Q channel) to be sampled by both ADCs. One ADC samples the input signal on the positive edge of the input clock and the other ADC samples it on the negative edge. The signal input is therefore sampled twice per clock cycle, so the full sample rate is twice the input clock frequency — for example, a 3GSPS sample rate for a 1.5GHz input clock.

在这个模式，交替存取的输出数据被一个多路选择器转换为 1:4。由于采样率是二倍，在 1.5GHz 输入时钟下，4 路数据输出中的任一路都以 750MHz 的速率输出，所有数据都是并行输出。每个时钟输出的 4 路并行数据是紧跟着采样顺序的，从最早到最后依次是：DQd，DId，DQ，DI；这表示可以提供不同采样率的可能性。

In this mode, the interleaved output data is converted by a multiplexer to 1:4. Because the sample rate is doubled, at a 1.5GHz input clock each of the four data outputs is output at a 750MHz rate, and all data is output in parallel. The four parallel data outputs of each clock follow the sampling order, from earliest to latest: DQd, DId, DQ, DI; this makes different sample rates possible.

SXA006 包括一个自动时钟相位后台校正特性，这个特性能在 DES 模式下自动的连续用来调节 I 通道和 Q 通道的时钟相位。这个特性免除了手动设置时钟相位的需要，同时提供最佳的双边沿采样 ENOB 性能。

The SXA006 includes an automatic clock phase background calibration feature, which in DES mode automatically and continuously adjusts the clock phases of the I and Q channels. This feature eliminates the need to set the clock phase manually and provides the best dual-edge sampling ENOB performance.

特别注意：在 DES 模式下的后台校正特性不能代替在进入 DES 模式之前要运行的指令校正，或如果芯片工作环境温度出现大的变化时所需要的指令校正。 Special note: The background calibration feature in DES mode does not replace the commanded calibration that must be run before entering DES mode, or when the chip operating ambient temperature changes significantly.

表7 输出数据对应的输入通道采样时间 / Table 7 Input-Channel Sampling Times Corresponding to Data Outputs

数据输出（总是对应 QCLK 的下降沿）/ Data Output (always referenced to the QCLK falling edge)	普通采样模式 / Normal Sampling Mode	双沿采样模式（DES）选择 I 通道输入 / DES Mode, I-Channel Input Selected	双沿采样模式（DES）选择 Q 通道输入* / DES Mode, Q-Channel Input Selected*
DI	"I"输入采样对应输出前 13 个 INCLK 周期的下降沿 / "I" input sampled on the falling edge 13 INCLK cycles before the output	"I"输入采样对应输出前 13 个 INCLK 周期的下降沿 / "I" input sampled on the falling edge 13 INCLK cycles before the output	"Q"输入采样对应输出前 13 个 INCLK 周期的下降沿 / "Q" input sampled on the falling edge 13 INCLK cycles before the output

数据输出（总是对应 QCLK 的下降沿）/ Data Output (always referenced to the QCLK falling edge)	普通采样模式 / Normal Sampling Mode	双沿采样模式（DES）选择 I 通道输入 / DES Mode, I-Channel Input Selected	双沿采样模式（DES）选择 Q 通道输入* / DES Mode, Q-Channel Input Selected*
DId	"I"输入采样对应输出前 14 个 INCLK 周期的下降沿 / "I" input sampled on the falling edge 14 INCLK cycles before the output	"I"输入采样对应输出前 14 个 INCLK 周期的下降沿 / "I" input sampled on the falling edge 14 INCLK cycles before the output	"Q"输入采样对应输出前 14 个 INCLK 周期的下降沿 / "Q" input sampled on the falling edge 14 INCLK cycles before the output
DQ	"Q"输入采样对应输出前 13 个 INCLK 周期的下降沿 / "Q" input sampled on the falling edge 13 INCLK cycles before the output	"I"输入采样对应输出前 13.5 个 INCLK 周期的上升沿 / "I" input sampled on the rising edge 13.5 INCLK cycles before the output	"Q"输入采样对应输出前 13.5 个 INCLK 周期的上升沿 / "Q" input sampled on the rising edge 13.5 INCLK cycles before the output
DQd	"Q"输入采样对应输出前 14 个 INCLK 周期的下降沿 / "Q" input sampled on the falling edge 14 INCLK cycles before the output	"I"输入采样对应输出前 14.5 个 INCLK 周期的上升沿 / "I" input sampled on the rising edge 14.5 INCLK cycles before the output	"Q"输入采样对应输出前 14.5 个 INCLK 周期的上升沿 / "Q" input sampled on the rising edge 14.5 INCLK cycles before the output

*在 DES 普通模式下，只有 I 通道进行采样。在 DES 的扩展模式下，I 或 Q 通道都可以进行采样。 *In DES normal mode, only the I channel is sampled. In DES extended mode, either the I or the Q channel can be sampled.

② OutEdge 引脚设置 / OutEdge Pin Setting

为了使在 SDR 模式数据采样变得容易，输出数据可以在输出数据时钟（QCLK）的正沿或负沿进行转换。这可以通过 OutEdge 输入（引脚 4）来选择。OutEdge 输入为高时输出数据在 QCLK 上升沿转换；OutEdge 输入为低时输出数据在 QCLK 下降沿转换，见表 8。参考 2.4）.c 输出沿同步。

To make data sampling easy in SDR mode, the output data can transition on the positive or negative edge of the output data clock (QCLK). This is selected by the OutEdge input (pin 4). When the OutEdge input is high, output data transitions on the QCLK rising edge; when it is low, output data transitions on the QCLK falling edge; see Table 8. See 2.4).c for output edge synchronization.

③ 双倍数据速率 / Double Data Rate

提供了单倍数据率（SDR）或双倍数据率（DDR）输出的选择。如果是 SDR，输出时钟（QCLK）频率与两路输出总线的数据速率一样。如果是 DDR，QCLK 频率是数据速率的一半，数据在 QCLK 的两个沿被送到输出端。DDR 时钟通过让引脚 4 悬空或 VCC/2 来控制，在 FSR（引脚 14）普通控制模式有效，见表 6 和表 8。

A choice of single data rate (SDR) or double data rate (DDR) output is provided. In SDR, the output clock (QCLK) frequency equals the data rate of the two output buses. In DDR, the QCLK frequency is half the data rate, and data is sent to the outputs on both QCLK edges. The DDR clock is controlled by leaving pin 4 floating or at VCC/2, effective in the FSR (pin 14) normal control mode; see Tables 6 and 8.

f. LVDS 输出 / LVDS Outputs

数据输出、溢出输出（DOR）和时钟输出（QCLK）都是 LVDS。当 Outv 输入（引脚 3）为高时，输出电流源将提供 3mA 的输出电流到 100Ω 的差分电阻负载；当 Outv 输入（引脚 3）为低时，输出电流源将提供 2.2mA 的输

出电流到 100Ω 的差分电阻负载，见表 10。为了缩短 LVDS 线长和降低系统噪声，Outv 输入（引脚 3）为低会获得满意的性能，同时降低功耗。如果 LVDS 路线太长或 SXA006 系统噪声太大，把 Outv 输入接高电平是很有必要的。

The data outputs, overflow output (DOR), and clock output (QCLK) are all LVDS. When the Outv input (pin 3) is high, the output current source provides 3mA of output current into a 100Ω differential resistive load; when the Outv input (pin 3) is low, it provides 2.2mA into a 100Ω differential resistive load. With short LVDS traces and low system noise, setting the Outv input (pin 3) low gives satisfactory performance while reducing power consumption. If the LVDS routing is too long or the SXA006 system noise is too large, connecting the Outv input high is necessary.

当 VREF（引脚 31）未连接或悬空时，LVDS 数据输出有一个 800mV 的共模电压。如果要求更高的共模电压，可以通过把 VREF 引脚与 VCC 相连使共模电压增加到 1.2V，见表 11。 特别注意：连接 VREF 引脚到 VCC 也会增加差分 LVDS 输出电压 40mV。

When VREF (pin 31) is unconnected or floating, the LVDS data outputs have an 800mV common-mode voltage. If a higher common-mode voltage is required, connecting the VREF pin to VCC increases the common-mode voltage to 1.2V. Special note: Connecting the VREF pin to VCC also increases the differential LVDS output voltage by 40mV.

表8 LVDS 输出幅度控制 / Table 8 LVDS Output Amplitude Control

Outv 输入（引脚 3）/ Outv Input (pin 3)	LVDS 输出幅度 / LVDS Output Amplitude
H	400～1000mVpp，典型 700 mVpp / 400–1000mVpp, typ 700 mVpp
L	280～800mVpp，典型 500 mVpp / 280–800mVpp, typ 500 mVpp

表9 LVDS 输出共模电压（VOS）/ Table 9 LVDS Output Common-Mode Voltage (VOS)

VREF（引脚 31）/ VREF (pin 31)	LVDS 输出共模 / LVDS Output Common-Mode
H	典型 1.2 V / Typ 1.2 V
悬空 / Floating	典型 800 mV / Typ 800 mV

g. 省电模式（Power Down）/ Power-Down Mode

当 PD（引脚 26）为低时，SXA006 处于正常工作状态。当 PD 引脚为高时，器件处于省电模式。在省电模式，数据输出引脚（正和负）都是三态，同时器件功耗被降低到最小。时钟输出（QCLK 和 QCLK（反相））和溢出输出（DOR 和 DOR（反相））不是三态，他们在内部被拉到地。因此，当 I 和 Q 都是省电模式时，时钟输出和溢出输出不能接到一个直流电压。

When PD (pin 26) is low, the SXA006 is in normal operation. When the PD pin is high, the device is in power-down mode. In power-down mode, the data output pins (positive and negative) are all tri-stated and the device power consumption is reduced to a minimum. The clock outputs (QCLK and QCLK (inverted)) and overflow outputs (DOR and DOR (inverted)) are not tri-stated; they are pulled to ground internally. Therefore, when both I and Q are in power-down mode, the clock outputs and overflow outputs must not be connected to a DC voltage.

PDQ 引脚为高或悬空时将使"Q"通道处于省电模式，"I"通道处于正常工作状态，不受 PDQ 的控制，见表 10。再回到普通工作模式，通道中将包含无意义的信息。

When the PDQ pin is high or floating, the "Q" channel is in power-down mode while the "I" channel remains in normal operation, unaffected by PDQ; see Table 10. On returning to normal operation, the channel will contain meaningless information.

如校正在运行期间 PD 置为高，器件不会进入省电工作，仍然正常工作，直至校正时序完成。然而，如果在已经上电和 PD 已为高的情况下，器件进入省电工作，不进行校正，直到 PD 变为低。如果器件处于省电模式要求手动校正，校正根本就不会启动。那就是说，手动校正输入完全被省电状态封锁了。但如果 PDQ 为高"Q"通道处于省电模式，"I"通道校正仍会运行，"Q"通道将不能被校正。如果"Q"通道是后来被使用，在 PDQ 为低后进行一次校正是必须的。

If PD is set high while calibration is running, the device does not enter power-down and continues normal operation until the calibration sequence completes. However, if the device has powered up with PD already high, the device enters power-down without performing calibration until PD goes low. If manual calibration is requested while the device is in power-down mode, calibration will not start at all — that is, the manual calibration input is completely blocked by the power-down state. But if PDQ is high and the "Q" channel is in power-down mode, "I" channel calibration still runs, while the "Q" channel cannot be calibrated. If the "Q" channel is used later, a calibration must be performed after PDQ goes low.

表10 省电模式控制 / Table 10 Power-Down Mode Control

PD	PDQ	I 路 / I Channel	Q 路 / Q Channel
H	H 或 L / H or L	省电模式 / Power-down mode	省电模式 / Power-down mode
L	H 或悬空 / H or floating	正常工作 / Normal operation	省电模式 / Power-down mode
L	L	正常工作 / Normal operation	正常工作 / Normal operation

1.2 普通/扩展控制 / Normal / Extended Control

SXA006 可以工作在这两种模式中任一种。普通的标准控制模式，使用者可以通过几个引脚来设置和控制器件的工作状态；"扩展控制模式"是通过一个串行接口和对 9 个寄存器的设置来实现另外的配置和控制选择。两种控制模式通过引脚 14（FSR/ST1：满刻度范围选择和扩展控制模式选择）来选择。控制模式的选择必须是一个固定的选择，当器件工作时不能随意转换这两种模式。表 11 显示了器件特性受控制模式选择的影响。

The SXA006 can operate in either of these two modes. In the normal standard control mode, the user sets and controls the device operating state through several pins; the "extended control mode" provides additional configuration and control options through a serial interface and the settings of 9 registers. The control mode is selected by pin 14 (FSR/ST1: full-scale range select and extended control mode select). The control mode selection must be a fixed selection and must not be switched arbitrarily while the device is operating. Table 11 shows how device features are affected by the control mode selection.

表11 器件特性和模式 / Table 11 Device Features and Modes

特性 / Feature	普通控制模式 / Normal Control Mode	扩展控制模式 / Extended Control Mode
SDR 或 DDR 模式时钟 / SDR or DDR mode clock	引脚 4 悬空或 VCC/2 选择 DDR 时钟，为高或低选择 SDR 时钟 / Pin 4 floating or VCC/2	在配置寄存器（1h；D10）中用 nDE 选择。当器件处于 DDR 模式，设置地址 1h，bit-8 必须为 0。/ Selected by nDE in

特性 / Feature	普通控制模式 / Normal Control Mode	扩展控制模式 / Extended Control Mode
	selects the DDR clock; high or low selects the SDR clock	the configuration register (1h; D10). When the device is in DDR mode and address 1h is set, bit-8 must be 0.
DDR 模式时钟相位 / DDR mode clock phase	没有选择，只有 0°相位 / No selection; 0° phase only	在配置寄存器（1h；D11）中，用 DCP 选择。/ Selected by DCP in the configuration register (1h; D11).
SDR 模式，数据转换在 QCLK 上升或下降沿 / SDR mode, data transitions on QCLK rising or falling edge	当引脚 4 为高时，SDR 数据在 QCLK+ 上升沿转换；当引脚 4 为低时，下降沿转换 / When pin 4 is high, SDR data transitions on the QCLK+ rising edge; when pin 4 is low, on the falling edge	在配置寄存器（1h；D8）中，用 OE 选择 / Selected by OE in the configuration register (1h; D8)
LVDS 输出幅度 / LVDS output amplitude	引脚 3 为高，正常的差分数据和 QCLK 输出幅度；为低时，减小幅度。/ Pin 3 high: normal differential data and QCLK output amplitude; low: reduced amplitude.	在配置寄存器（1h；D9）中，用 OV 选择 / Selected by OV in the configuration register (1h; D9)
上电校正延迟 / Power-up calibration delay	当引脚 127 为低，选择短的延迟；为高，选择长的延迟。/ Pin 127 low selects the short delay; high selects the long delay.	只能短的延迟 / Short delay only
满刻度范围 / Full-scale range	当引脚 14 为高时，正常的输入满刻度范围；为低时，减小范围。范围的选择对两个通道均有效。/ Pin 14 high: normal input full-scale range; low: reduced range. The range selection applies to both channels.	在 1.4 寄存器描述中，整个正常满刻度范围内多达 512 步长的调节。选择用输入满刻度范围调节寄存器（3h；D7～D15）/ Adjustment of up to 512 steps over the whole normal full-scale range, per the register description in 1.4. Selected with the input full-scale range adjustment register (3h; D7–D15)
输入失调调节 / Input offset adjustment	不能调节 / Not adjustable	用输入失调寄存器（2h；D7～D15）调节，多达 512 步长 / Adjusted with the input offset register (2h; D7–D15), up to 512 steps
双边沿采样选择 / Dual-edge sampling selection	引脚 127 悬空或 VCC/2 / Pin 127 floating or VCC/2	通过 DES 使能寄存器来控制 / Controlled by the DES enable register
双边沿采样输入通道选择 / Dual-edge sampling input channel selection	只有 I 通道输入可用 / I-channel input only	I 或 Q 通道输入都可以被 2 个 ADC 采样 / Either I- or Q-channel input can be sampled by the two ADCs
DES 采样时钟调节 / DES sampling clock adjustment	时钟相位是自动调节 / Clock phase is automatically adjusted	在 DES 中设置 D14 使能寄存器（Dh）来选择自动时钟相位控制。时钟相位也可以通过粗和细寄存器（Eh 和 Fh）来进行手动调节。/ Set the D14 enable register (Dh) in DES to select automatic clock phase control. The clock phase can also be manually adjusted through the coarse and fine registers (Eh and Fh).

扩展控制模式的默认状态由上电复位进行设置，如表 12 所示。 The default state of the extended control mode is set by power-on reset, as shown in Table 12.

表12 扩展控制模式工作（14 脚悬空或 VCC/2）/ Table 12 Extended Control Mode Operation (Pin 14 Floating or VCC/2)

特性 / Feature	扩展控制模式默认状态 / Extended Control Mode Default State
SDR 或 DDR 模式时钟 / SDR or DDR mode clock	DDR 模式时钟 / DDR mode clock
DDR 模式时钟相位 / DDR mode clock phase	QCLK 边沿（0°相位）数据变化 / Data changes on the QCLK edge (0° phase)
LVDS 输出幅度 / LVDS output amplitude	正常幅度（700m Vpp） / Normal amplitude (700m Vpp)

特性 / Feature	扩展控制模式默认状态 / Extended Control Mode Default State
上电校正延迟 / Power-up calibration delay	缩短的延迟 / Shortened delay
模拟输入满刻度范围 / Analog input full-scale range	两个通道都是 700mVpp / 700mVpp for both channels
输入失调调节 / Input offset adjustment	两个通道都没有失调调节 / No offset adjustment on either channel
双边沿采样（DES）/ Dual-edge sampling (DES)	不用此模式 / Not used

1.3 串行接口 / Serial Interface

只有当器件工作在扩展控制模式下，3 线串行接口才能被激活。这些串行接口的引脚是串行时钟（SCLK）、串行数据（DATA）和串行接口选择（ST2（反相）），八个只写寄存器通过串行接口获取信号。

The 3-wire serial interface can only be activated when the device operates in extended control mode. The serial interface pins are the serial clock (SCLK), serial data (DATA), and serial interface select (ST2 (inverted)); eight write-only registers are accessed through the serial interface.

ST2（反相）：通过串行接口访问一个寄存器时，这个信号应该为低。相对于 SCLK 的建立时间和保持时间必须满足要求。 SCLK：串行数据输入在这个信号的上升沿获得，对 SCLK 没有最小频率要求。 DATA：每个寄存器存取要求这个输入端为一个明确的 32 位组合格式。这个格式由头模式、寄存器地址和寄存器值组成，寄存器值由 MSB 位开始。相对于 SCLK 的建立时间和保持时间必须满足要求，看时序图。 ST2 (inverted): When a register is accessed through the serial interface, this signal should be low. The setup and hold times relative to SCLK must be met. SCLK: Serial data input is acquired on the rising edge of this signal; there is no minimum frequency requirement for SCLK. DATA: Each register access requires a defined 32-bit combined format at this input. The format consists of a header pattern, a register address, and a register value, with the register value starting from the MSB. The setup and hold times relative to SCLK must be met; see the timing diagram.

每个寄存器访问由 32 位组成，如图 4 所示的时序图。固定头模式为 0000 0000 0001（11 个 0，1 个 1），写入次序是 0 最先写入，这 12 位组成头模式。接下来写入 4 位寄存器的地址，最后 16 位数据被写入到寄存器，不同寄存器的地址详细表述如表 15 所示。

Each register access consists of 32 bits, as shown in the timing diagram of Figure 4. The fixed header pattern is 0000 0000 0001 (eleven 0s and one 1); the write order writes 0 first, and these 12 bits form the header pattern. Next, the 4-bit register address is written, and finally the 16-bit data is written to the register. The addresses of the different registers are detailed in Table 13.

当 ST2（反相）永久保持为低电平时，从第 33 个 SCLK 开始后面的寄存器存取能直接完成，在寄存器地址之间不再进行选通。虽然这种用法不推荐，但那是可能的。

When ST2 (inverted) is held low permanently, subsequent register accesses can be performed directly starting from the 33rd SCLK, with no further strobing between register addresses. Although this usage is not recommended, it is possible.

重要提示：当校正 ADC 的时候，串行接口不要使用，如果使用会降低器件的性能，除非再进行正确的校正。寄存器存取期间进行串行接口寄存器操作也会降低 ADC 的动态特性。 Important: Do not use the serial interface while the ADC is calibrating; using it will degrade device performance unless a correct calibration is performed again. Performing serial interface register operations during register access will also degrade the ADC dynamic performance.

表13 寄存器地址 / Table 13 Register Addresses

地址写入顺序：A3 在 H0（固定头模式的最后位，即"1"）后锁存，A0 在最后锁存 / Address write order: A3 is latched after H0 (the last bit of the fixed header pattern, i.e., "1"), and A0 is latched last

A3	A2	A1	A0	Hex	寄存器地址 / Register
0	0	0	0	0h	保留 / Reserved
0	0	0	1	1h	状态配置 / Status configuration
0	0	1	0	2h	I 通道输入失调调节 / I-channel input offset adjustment
0	0	1	1	3h	I 通道满刻度电压调节 / I-channel full-scale voltage adjustment
0	1	0	0	4h	保留 / Reserved
0	1	0	1	5h	保留 / Reserved
0	1	1	0	6h	保留 / Reserved
0	1	1	1	7h	保留 / Reserved
1	0	0	0	8h	保留 / Reserved
1	0	0	1	9h	保留 / Reserved
1	0	1	0	Ah	Q 通道输入失调调节 / Q-channel input offset adjustment
1	0	1	1	Bh	Q 通道满刻度电压调节 / Q-channel full-scale voltage adjustment
1	1	0	0	Ch	保留 / Reserved
1	1	0	1	Dh	DES 使能 / DES enable
1	1	1	0	Eh	DES 粗调节 / DES coarse adjustment
1	1	1	1	Fh	DES 细调节 / DES fine adjustment

1.4 寄存器描述 / Register Descriptions

在扩展控制模式 8 个只写寄存器提供了许多控制和配置选择，当器件处于普通控制模式时，这些寄存器对器件没有影响。下面每个寄存器的描述介绍了每个控制位的上电复位状态（POR）。 In extended control mode, the eight write-only registers provide many control and configuration options; when the device is in normal control mode, these registers have no effect on the device. The description of each register below gives the power-on reset (POR) state of each control bit.

寄存器配置 / Configuration Register

地址：1h（0001b），只写。默认值：（0xB2FF） Address: 1h (0001b), write-only. Default value: (0xB2FF)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	DCS	DCP	nDE	OV	OE	1	1	1	1	1	1	1	1

- Bit 15 必须设置为 1b / Bit 15 must be set to 1b
- Bit 14 必须设置为 0b / Bit 14 must be set to 0b
- Bit 13 必须设置为 1b / Bit 13 must be set to 1b
- Bit 12 DCS：占空比稳定器。当这个位设置为 1b，一个占空比稳定器电路就被应用于时钟输入。当这个位设置为 0b，占空比稳定器电路取消。POR 状态：1b Bit 12 DCS: Duty-cycle stabilizer. When this bit is

set to 1b, a duty-cycle stabilizer circuit is applied to the clock input. When set to 0b, the duty-cycle stabilizer circuit is disabled. POR state: 1b

- Bit 11 DCP：DDR 模式时钟相位。这个位只能在 DDR 模式下才有影响。当这个位为 0b，QCLK 边沿与数据边沿（0°相位）一致。当这个位为 1b，QCLK 边沿位于数据二进制单元中间（90°相位），利用了 QCLK 一半的速度。参考图 3 相位。POR 状态：0b Bit 11 DCP: DDR mode clock phase. This bit has an effect only in DDR mode. When 0b, the QCLK edge coincides with the data edge (0° phase). When 1b, the QCLK edge is located in the middle of the data binary cell (90° phase), using half the QCLK rate. See Figure 3 for the phase. POR state: 0b
- Bit 10 nDE：DDR 或 SDR 模式选择。当这个位设为 0b，数据总线时钟遵循 DDR 模式（双数据率），这样 QCLK 时钟每个上升和下降沿都输出一个数据字节。当这个位为 1b，数据总线时钟遵循 SDR 模式（单倍数据率），这样 QCLK 时钟的上升沿或下降沿输出一个数据字节，由 OutEdge 位决定。POR 状态：0b Bit 10 nDE: DDR or SDR mode selection. When 0b, the data bus clock follows DDR mode (double data rate), so a data byte is output on each rising and falling edge of the QCLK clock. When 1b, the data bus clock follows SDR mode (single data rate), so a data byte is output on the rising or falling edge of the QCLK clock, as determined by the OutEdge bit. POR state: 0b
- Bit 9 OV：输出电压幅度。这个位决定 LVDS 输出电压幅度，它还与用在普通控制模式的 OutV 引脚有一样的功能。当这个位为 1b，输出标准幅度 800mVpp。当这个位为 0b，输出减小的幅度 600mVpp。POR 状态：1b Bit 9 OV: Output voltage amplitude. This bit determines the LVDS output voltage amplitude and has the same function as the OutV pin used in normal control mode. When 1b, the output is the standard amplitude of 800mVpp. When 0b, the output is the reduced amplitude of 600mVpp. POR state: 1b
- Bit 8 OE：SDR 模式输出时钟沿选择。这个位选择 SDR 模式下数据转换的 QCLK 边沿，它还与在普通控制模式下 OutEdge 引脚一样的功能。当这个位为 1，数据输出在 QCLK+ 的上升沿转变；当这个位为 0，数据输出在 QCLK+ 的下降沿转变。POR 状态：0b Bit 8 OE: SDR mode output clock edge selection. This bit selects the QCLK edge on which data transitions in SDR mode and has the same function as the OutEdge pin in normal control mode. When 1, data output transitions on the rising edge of QCLK+; when 0, on the falling edge of QCLK+. POR state: 0b
- Bits 7:0 必须设为 1b。/ Bits 7:0 must be set to 1b.

I 通道失调调节 / I-Channel Offset Adjustment

地址：2h（0010b），只写。默认值：（0x007F） Address: 2h (0010b), write-only. Default value: (0x007F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	失调值 / Offset value						LSB	符号 / Sign	1	1	1	1	1	1	1

- Bits 15:8 失调值。I 通道 ADC 的输入失调在这里被线性和单调的调节。00h 提供一个普通的零失调，FFh 提供一个 45mV 的失调。因此，每个码步有 0.176mV 的失调。POR 状态：0000 0000 b Bits 15:8 Offset value. The input offset of the I-channel ADC is adjusted linearly and monotonically here. 00h provides a nominal zero offset, and FFh provides a 45mV offset. Each code step therefore has 0.176mV of offset. POR state: 0000 0000 b
- Bits 7 符号位。0b 给正的失调，1b 给负的失调。POR 状态：0b Bit 7 Sign bit. 0b gives a positive offset, 1b gives a negative offset. POR state: 0b
- Bit 6:0 必须设为 1b / Bits 6:0 must be set to 1b

I 通道满刻度电压调节 / I-Channel Full-Scale Voltage Adjustment

地址：3h（0011b），只写。默认值：（0x807F） Address: 3h (0011b), write-only. Default value: (0x807F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	调节值 / Adjustment value							LSB	1	1	1	1	1	1	1

- Bit 15:7 满刻度电压调节值。I 通道 ADC 的输入满刻度电压或增益被以 9 位数据值进行线性和单调地调节。调节范围是正常 700mVpp 差分值的 ±20%。 Bit 15:7 Full-scale voltage adjustment value. The input full-scale voltage or gain of the I-channel ADC is adjusted linearly and monotonically with a 9-bit data value. The adjustment range is ±20% of the nominal 700mVpp differential value.
- 0000 0000 0 → 560 mVpp
- 1000 0000 0 → 700 mVpp（默认值 / default）
- 1111 1111 1 → 840 mVpp
- 为了达到最好的性能，建议这个值限制在 0110 0000 0b 到 1110 0000 0b 之间。例如，限制调节的幅度为 ±15%，保留 ±5% 的余量来允许 ADC 自己满刻度变化。增益调节的时候不能同时进行 ADC 再校正。POR 状态：1000 0000 0b（不调节） For best performance, it is recommended to limit this value between 0110 0000 0b and 1110 0000 0b. For example, limit the adjustment to ±15%, reserving ±5% of margin for the ADC's own full-scale variation. ADC re-calibration must not be performed at the same time as gain adjustment. POR state: 1000 0000 0b (no adjustment)
- Bits 6:0 必须设为 1b / Bits 6:0 must be set to 1b

Q 通道失调调节 / Q-Channel Offset Adjustment

地址：Ah（1010b）；只写。默认值：（0x007F） Address: Ah (1010b); write-only. Default value: (0x007F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	失调值 / Offset value						LSB	符号 / Sign	1	1	1	1	1	1	1

- Bits 15:8 失调值。Q 通道 ADC 的输入失调在这里被线性和单调地调节。00h 提供一个普通的零失调，FFh 提供一个 45mV 的失调。因此，每个码步有 0.176mV 的失调。POR 状态：0000 0000 b Bits 15:8 Offset value. The input offset of the Q-channel ADC is adjusted linearly and monotonically here. 00h provides a nominal zero offset, and FFh provides a 45mV offset. Each code step therefore has 0.176mV of offset. POR state: 0000 0000 b
- Bits 7 符号位。0b 给正的失调，1b 给负的失调。POR 状态：0b Bit 7 Sign bit. 0b gives a positive offset, 1b gives a negative offset. POR state: 0b
- Bit 6:0 必须设为 1b / Bits 6:0 must be set to 1b

Q 通道满刻度电压调节 / Q-Channel Full-Scale Voltage Adjustment

地址：Bh（1011b）；只写。默认值：（0x807F） Address: Bh (1011b); write-only. Default value: (0x807F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	调节值 / Adjustment value							LSB	1	1	1	1	1	1	1

- Bit 15:7 满刻度电压调节值。Q 通道 ADC 的输入满刻度电压或增益被以 9 位数据值进行线性和单调的调节。调节范围是正常 700m VP-P 差分值的 ±20%。 Bit 15:7 Full-scale voltage adjustment value. The

input full-scale voltage or gain of the Q-channel ADC is adjusted linearly and monotonically with a 9-bit data value. The adjustment range is ±20% of the nominal 700m VP-P differential value.

- 0000 0000 0 → 560 mVpp
- 1000 0000 0 → 700 mVpp（默认值 / default）
- 1111 1111 1 → 840 mVpp
- 为了达到最好的性能，建议这个值范围限制在 0110 0000 0b 到 1110 0000 0b 之间。例如，限制调节的幅度为 ±15%。保留 ±5% 的余量来允许 ADC 自己满刻度变化。增益调节的时候不能同时进行 ADC 再校正。POR 状态：1000 0000 0b（不调节） For best performance, it is recommended to limit this value between 0110 0000 0b and 1110 0000 0b. For example, limit the adjustment to ±15%, reserving ±5% of margin for the ADC's own full-scale variation. ADC re-calibration must not be performed at the same time as gain adjustment. POR state: 1000 0000 0b (no adjustment)
- Bits 6:0 必须设为 1b / Bits 6:0 must be set to 1b

DES 使能配置 / DES Enable Configuration

地址：Dh（1101b）；只写。默认值：（0x3FFF） Address: Dh (1101b); write-only. Default value: (0x3FFF)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DEN	ACP	1	1	1	1	1	1	1	1	1	1	1	1	1	1

- Bit 15 DES 使能。设置这个位为 1b，进入双边沿采样模式，在这个模式器件以时间交替方式工作，模拟输入被双路 ADC 采样和转换，获得输入时钟频率两倍的采样速率。当这个位设为 0b 时，器件工作在普通的双通道模式。POR 状态：0b Bit 15 DES enable. Setting this bit to 1b enters dual-edge sampling mode, in which the device works in a time-interleaved manner and the analog input is sampled and converted by both ADCs, obtaining a sample rate of twice the input clock frequency. When set to 0b, the device works in the normal dual-channel mode. POR state: 0b
- Bit 14 自动时钟相位控制（ACP）。设置这个位为 1b，进入自动时钟相位控制，在这个模式，DES 粗和细手动控制无效，一个相位检测电路连续地调节 I 和 Q 采样边沿为超出 180 度相位。当这个位为 0b，I 和 Q 通道间的采样时钟延迟设为手动调节方式，用 DES 粗和细调节寄存器。（参考 2.4）.e）。推荐用 ACP 控制来设置 DES，而不是手动设置。POR 状态：0b Bit 14 Automatic clock phase control (ACP). Setting this bit to 1b enters automatic clock phase control; in this mode the DES coarse and fine manual controls are ineffective, and a phase detection circuit continuously adjusts the I and Q sampling edges to a phase difference of 180 degrees. When 0b, the sampling clock delay between the I and Q channels is set to manual adjustment using the DES coarse and fine adjustment registers. (See 2.4).e.) Using ACP control to set up DES is recommended rather than manual setting. POR state: 0b
- Bit 13:0 必须设为 1b / Bits 13:0 must be set to 1b

DES 粗调节 / DES Coarse Adjustment

地址：Eh（1110b）；只写。默认值：（0x07FF） Address: Eh (1110b); write-only. Default value: (0x07FF)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IS	ADS	CAM			1	1	1	1	1	1	1	1	1	1	1

- Bit 15 模拟输入选择。当这个位设为 0b 时，I 通道的模拟输入通过两个 ADC 工作。当这个位设为 1b 时，Q 通道的输入通过两个 ADC 工作。POR 状态：0b Bit 15 Analog input selection. When 0b, the I-

channel analog input works through both ADCs. When 1b, the Q-channel input works through both ADCs. POR state: 0b

- Bit 14 延迟调节方向选择。当这个位设为 0b，程序延迟用于 I 通道采样时钟，而 Q 通道采样时钟保持固定不变。当这个位设为 1b 时，程序延迟用于 Q 通道采样时钟，而 I 通道采样时钟保持固定不变。POR 状态：0b Bit 14 Delay adjustment direction selection. When 0b, the programmed delay is applied to the I-channel sampling clock while the Q-channel sampling clock remains fixed. When 1b, the programmed delay is applied to the Q-channel sampling clock while the I-channel sampling clock remains fixed. POR state: 0b
- Bits 13:11 延迟粗调节。这里的每个码值延迟 I 通道或 Q 通道采样时钟（由 ADS 位定义）近 20ps。在这里 000b 的一个值产生 0 调节。POR 状态：000b Bits 13:11 Delay coarse adjustment. Each code value here delays the I- or Q-channel sampling clock (as defined by the ADS bit) by approximately 20ps. A value of 000b here produces zero adjustment. POR state: 000b
- Bits 10:0 必须设为 1b / Bits 10:0 must be set to 1b

DES 细调节 / DES Fine Adjustment

地址：Fh（1111b）；只写。默认值：（0x007F） Address: Fh (1111b); write-only. Default value: (0x007F)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
(MSB) FAM (LSB)									1	1	1	1	1	1	1

- Bits 15:7 延迟细调节。在这里每个码值延迟 I 通道和 Q 通道（由 DES 粗调节的 ADS 位决定）采样时钟近 0.1ps。这里 0000 0000 0b 为零调节。注意，每个码值能够调节的大小随器件工作环境和粗调节值的选择而变化。POR 状态：0000 0000 0b Bits 15:7 Delay fine adjustment. Each code value here delays the I- and Q-channel sampling clocks (as determined by the ADS bit of DES coarse adjustment) by approximately 0.1ps. A value of 0000 0000 0b here is zero adjustment. Note that the amount of adjustment per code varies with the device operating environment and the coarse adjustment value selected. POR state: 0000 0000 0b
- Bit 6:0 必须设为 1b / Bits 6:0 must be set to 1b

关于扩展模式失调校正的说明： 当用 I 或 Q 通道失调调节寄存器时，请注意下面的信息。 对于 +0000 0000 和 -0000 0000 的失调值，实际情况两者失调值并不一样。只需要改变这种情况的符号位，两者将有 1/10 个 LSB 的数字输出码值。下面的图 24 表示更清楚。 Note on extended-mode offset correction: When using the I- or Q-channel offset adjustment registers, note the following information. For offset values of +0000 0000 and -0000 0000, the two offset values are actually not the same. Merely changing the sign bit in this case gives a difference of 1/10 LSB in the digital output code value between the two. Figure 19 below illustrates this more clearly.

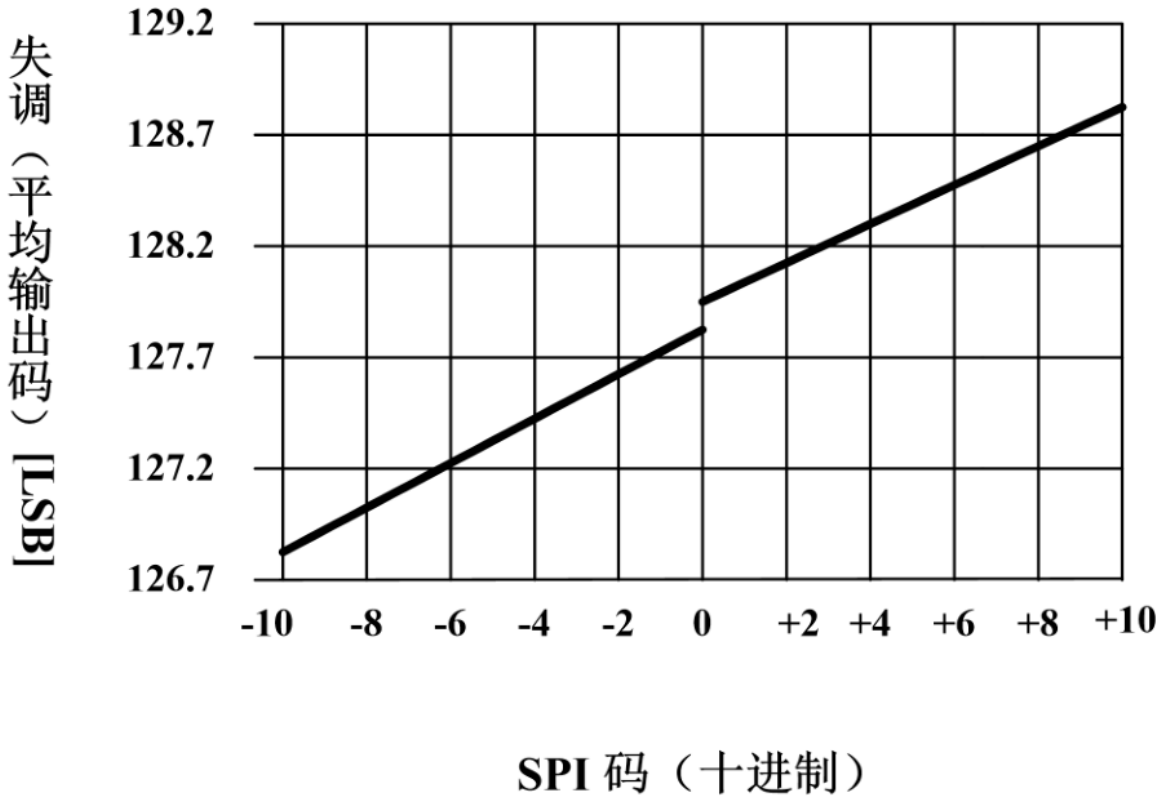


Figure 19: 扩展模式失调性能

1.5 多个 ADC 同步 / Synchronizing Multiple ADCs

SXA006 有这样一个功能，用户可以输入一个置位脉冲 R（15 脚）来精确重置器件采样时钟输入到 QCLK 输出的关系。这允许多个 ADC 在一个系统中有它们自己的 QCLK（和数据）输出转换，并在同样的时间共享输入时钟 INCLK，这个时钟用于所有 ADC 采样。

The SXA006 has a feature whereby the user can input a reset pulse R (pin 15) to precisely reset the relationship between the device sampling clock input and the QCLK output. This allows multiple ADCs in a system to have their own QCLK (and data) output transitions at the same time while sharing the input clock INCLK used for sampling by all ADCs.

置位输入 R 必须满足图 5、图 6 和图 7 的时序关系，置位脉冲 R 必须有一个最小宽度，相对于输入时钟 INCLK 上升沿，它的下降沿必须满足建立和保持时间要求，这些时间是在转换器电特性中的 tRH，tRS 和 tRPW。

The reset input R must satisfy the timing relationships of Figures 5, 6, and 7. The reset pulse R must have a minimum width, and its falling edge must meet the setup and hold time requirements relative to the rising edge of the input clock INCLK; these times are tRH, tRS, and tRPW in the converter electrical characteristics.

置位（R）信号与输入时钟异步。如果 R 是异步的，QCLK 输出被保持在一个设定的状态。在重置期间 QCLK 保持的状态由工作模式（SDR/DDR）和 OutvEdge 配置引脚或配置位设置来决定（参考图 5、图 6 和图 7）。因此，当置位（R）信号异步时，在重置期间在 QCLK 时序上可能有一个窄脉冲。当 R 信号与 INCLK 上升沿不同

步，下一个 INCLK 下降沿与 QCLK 输出和系统中其它 SXA006 的输出同步，在一个固定延迟后（相对于输入时钟频率）QCLK 输出再次使能，即时钟输入 INCLK 到输出时钟 QCLK 的延迟（tSD）。在正常工作下器件总表现出这些延迟特性。

The reset (R) signal is asynchronous to the input clock. If R is asynchronous, the QCLK output is held in a set state. The state in which QCLK is held during reset is determined by the operating mode (SDR/DDR) and the OutvEdge configuration pin or configuration bit setting (see Figures 5, 6, and 7). Therefore, when the reset (R) signal is asynchronous, there may be a narrow pulse on QCLK during reset. When the R signal is not synchronous with the INCLK rising edge, the next INCLK falling edge synchronizes with the QCLK output and the outputs of other SXA006 devices in the system, and after a fixed delay (relative to the input clock frequency) the QCLK output is enabled again — this is the delay from clock input INCLK to output clock QCLK (tSD). The device always exhibits these delay characteristics in normal operation.

当校正过程正进行时（当 CalRun 为高），置位（R）引脚不应该设置为高。这样做将在数字电路中引起一个数字脉冲，这将导致校正的错误和失效。 When a calibration process is in progress (when CalRun is high), the reset (R) pin should not be set high. Doing so will cause a digital pulse in the digital circuitry, which will cause calibration errors and failure.

---

2 应用信息 / Application Information

2.1 参考电压 / Reference Voltage

SXA006 的电压参考由一个 1.254V 的带缓冲器的带隙基准提供，为了用户方便，可以在引脚 31 获得 VREF。这个输出有 ±100μA 的电流输出能力，如果需要比这更大的电流应加缓冲器。内部带隙基准参考电压有一个对应于普通的模拟输入值 VID1，由 FSR 引脚定义并在 1.1）.d 模拟输入中有描述。

The voltage reference of the SXA006 is provided by a buffered 1.254V bandgap reference, available at pin 31 as VREF for user convenience. This output has a current output capability of ±100μA; if a larger current is needed, a buffer should be added. The internal bandgap reference voltage corresponds to the nominal analog input value VID1, defined by the FSR pin and described in 1.1).d Analog Input.

本产品不提供外部参考电压的应用，但满刻度输入电压在扩展控制模式能通过一个配置寄存器进行调节，如在 1.2）普通/扩展控制描述。 This product does not provide for the use of an external reference voltage, but the full-scale input voltage can be adjusted in extended control mode through a configuration register, as described in 1.2).

差分输入信号在选择的满刻度输入范围内将被数字转换为 8 位数字码，信号超出满刻度范围的部分在输出将不出现，在信号超出满刻度范围时激活溢出输出 DOR，参考 2.2).b 溢出范围指示。 A differential input signal within the selected full-scale input range is digitally converted to 8-bit digital codes; any part of the signal exceeding the full-scale range does not appear at the output, and the overflow output DOR is activated when the signal exceeds the full-scale range; see 2.2).b Overflow Range Indication.

VREF 引脚的一个额外的特性是它可以用来提升 LVDS 输出共模电压，当 VREF 引脚被作为输出或没有连接时，输出共模电压（VOS）典型值为 800mV。为了将 LVDS 失调电压提升到一个典型值 1200mV，VREF 引脚可以直接接到电源线上。 An additional feature of the VREF pin is that it can be used to raise the LVDS output common-mode voltage. When the VREF pin is used as an output or is not connected, the output common-mode voltage (VOS) is typically 800mV. To raise the LVDS offset voltage to a typical value of 1200mV, the VREF pin can be connected directly to the supply rail.

2.2 模拟输入 / Analog Input

模拟输入是一个差分信号，这个信号既可交流耦合连接也可直流耦合连接。在普通模式，满刻度输入范围用 FSR 引脚来选择。在扩展控制模式，满刻度输入范围通过串行接口由满刻度电压调节寄存器来进行选择。当在扩展模式调节输入满刻度范围时，为达到最好的性能，参考 1.4）寄存器描述作为指导关于调节的大小限制。

The analog input is a differential signal, which can be connected either AC-coupled or DC-coupled. In normal mode, the full-scale input range is selected with the FSR pin. In extended control mode, the full-scale input range is selected through the serial interface by the full-scale voltage adjustment register. When adjusting the input full-scale range in extended mode, refer to the register description in 1.4) as a guide on the adjustment magnitude limits for best performance.

表 14 给出了在普通模式下 SFR 为高时输入到输出的关系，SFR 为低时幅度减少为 75%。在扩展模式这个幅度由控制寄存器的满刻度输入范围和失调设置确定。 Table 14 gives the input-to-output relationship in normal mode when FSR is high; when FSR is low the amplitude is reduced to 75%. In extended mode this amplitude is determined by the full-scale input range and offset settings of the control registers.

带缓冲器的模拟输入简化了驱动这些输入的情况，通常情况采样 ADC 输入的 RC 极点是不需要的。如要求在 ADC 前用一个放大器电路，注意选择一个足够好的噪声和失调性能及在应用频率有足够增益的放大器。 The buffered analog input simplifies driving these inputs; usually the RC pole at the sampling ADC input is not needed. If an amplifier circuit is required in front of the ADC, take care to select one with sufficiently good noise and offset performance and sufficient gain at the application frequency.

注意：一个精确的直流共模电压必须施加于 ADC 的模拟输入，当交流耦合输入时这个共模电压 VCMO 由器件内部提供，模拟信号交流耦合到 ADC 输入。 Note: A precise DC common-mode voltage must be applied to the analog input of the ADC. With AC-coupled input, this common-mode voltage VCMO is provided internally by the device, and the analog signal is AC-coupled to the ADC input.

当输入被交流耦合连接时，VCMO 输出必须接地，如图 20 所示。器件内部的 VCMO 电压通过片内 50KΩ 电阻连接到模拟输入。 When the input is AC-coupled, the VCMO output must be grounded, as shown in Figure 20. The internal VCMO voltage of the device is connected to the analog input through an on-chip 50KΩ resistor.

表14 差分输入到输出的关系（FSR 为高，非扩展模式）/ Table 14 Differential Input-to-Output Relationship (FSR High, Non-Extended Mode)

VIN+	VIN-	输出码 / Output Code
VCMO-230mV	VCMO+230mV	00000000
VCMO-115mV	VCMO+115mV	01000000
VCMO	VCMO	01111111 / 10000000
VCMO+115mV	VCMO-115mV	11000000
VCMO+230mV	VCMO-230mV	11111111

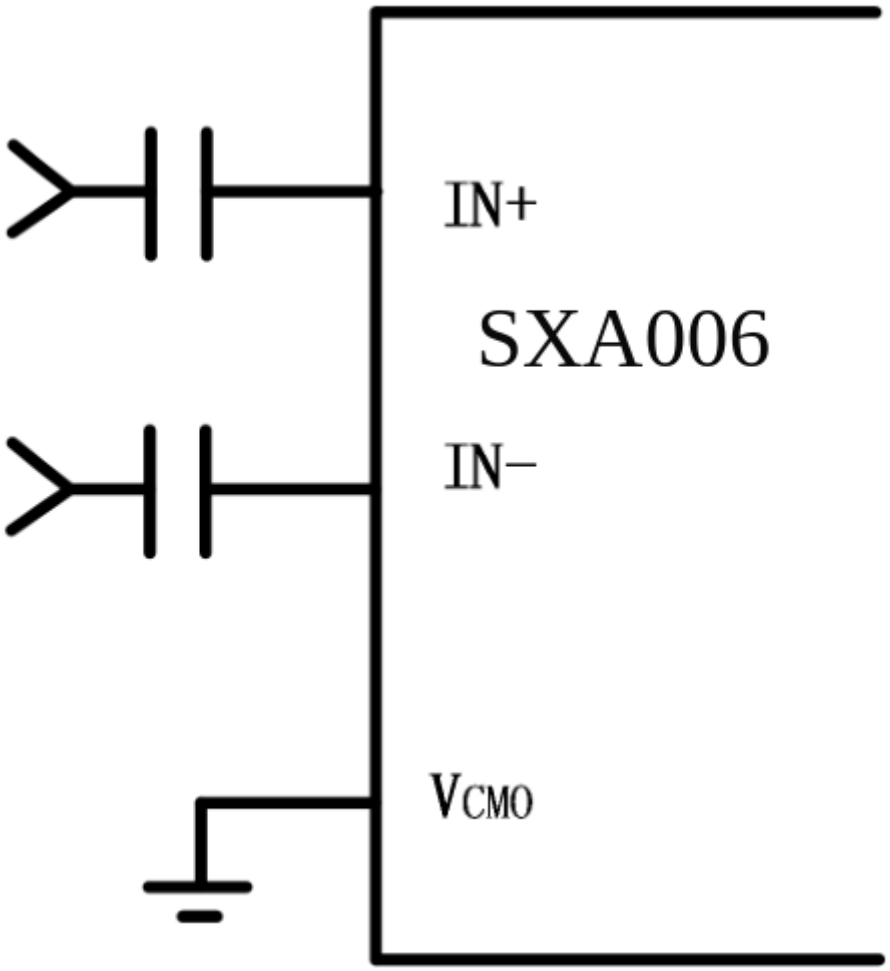


Figure 20: 差分输入驱动

重要提示：当模拟输入是交流耦合连接时，没有用的模拟输入通道（如在 DES 模式）应该悬空，没有用的模拟输入不要连接到地。 Important: When the analog input is AC-coupled, unused analog input channels (e.g., in DES mode) should be left floating; do not connect unused analog inputs to ground.

当模拟输入直流耦合连接模式时，在差分输入必须提供共模电压。这个共模电压应该跟踪 VCMO 输出引脚，并注意到 VCMO 输出电压将随温度变化，驱动电路的共模电压输出应当跟踪这个变化。 When the analog input is DC-coupled, a common-mode voltage must be provided at the differential input. This common-mode voltage should track the VCMO output pin; note that the VCMO output voltage varies with temperature, and the common-mode voltage output of the driving circuit should track this variation.

重要提示：当模拟输入直流耦合连接时，没有用的模拟输入通道（如在 DES 模式）应该连接到 VCMO 电压，没有用的模拟输入不要连接到地。 Important: When the analog input is DC-coupled, unused analog input channels (e.g., in DES mode) should be connected to the VCMO voltage; do not connect unused analog inputs to ground.

当输入共模电压偏离 VCMO 时，满刻度失真性能下降极快，这是因为用了一个非常低的电源电压来降低功耗的直接结果，因此，应保持输入共模电压在 VCMO±50mV 以内。 When the input common-mode voltage deviates from VCMO, the full-scale distortion performance degrades very rapidly, which is a direct result of

using a very low supply voltage to reduce power consumption; therefore, the input common-mode voltage should be kept within VCMO±50mV.

SXA006 的直流耦合连接模式的性能与交流耦合连接模式的性能一样好，但提供的输入共模电压在两个模式下应保持在 VCMO±50mV 以内。 The DC-coupled connection mode of the SXA006 performs as well as the AC-coupled connection mode, but the provided input common-mode voltage should be kept within VCMO±50mV in both modes.

a. 单端输入信号处理 / Single-Ended Input Signal Handling

由于 SXA006 内部没有对单端信号处理的电路，因而不提供处理单端输入信号。处理单端信号最好的方式是在输入到 ADC 之前把信号转换成差分信号，最容易的单端信号转换为差分信号的方式是用一个适当的不平衡连接的变压器，如图 21 所示。

Because the SXA006 has no internal circuitry for single-ended signal handling, it does not provide single-ended input signal handling. The best way to handle a single-ended signal is to convert it to a differential signal before it is input to the ADC; the easiest way to convert a single-ended signal to a differential signal is to use a suitably unbalanced-connected transformer, as shown in Figure 21.

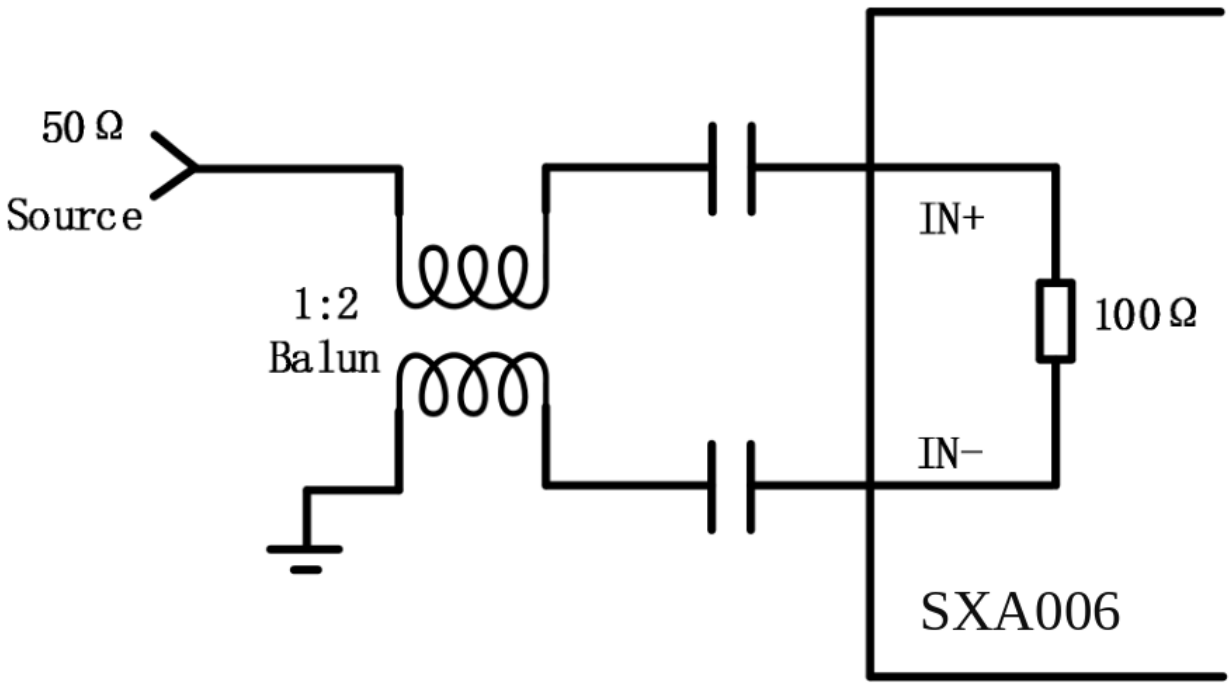


Figure 21: 单端到差分信号转换

① 交流耦合输入 / AC-Coupled Input

最容易的单端交流输入转差分交流输入的方式是用一个适当的不平衡连接的变压器，如图 23 所示。图 23 [同前注 / see previous note] 是用变压器将单端信号转为差分信号的一个简图。变压器的特性依赖于变压器类型的选择和整个板子的布局。建议系统设计师和变压器制造师交流，他们可以帮助选择出最好的单端转差分用的特殊变压器。

The easiest way to convert a single-ended AC input to a differential AC input is to use a suitably unbalanced-connected transformer, as shown in Figure 21. That figure is a simplified diagram of

converting a single-ended signal to a differential signal with a transformer. The characteristics of the transformer depend on the choice of transformer type and the layout of the whole board. System designers are advised to communicate with transformer manufacturers, who can help select the best special transformer for single-ended-to-differential conversion.

当选择一个变压器，了解 ADC 的输入结构是非常重要的。系统设计师应当注意这些特殊的变压器参数。它们的模拟输入源到 SXA006 器件内部的 100Ω 差分输入终端电阻的阻抗应该匹配。这个终端电阻的范围在电特性表中描述为 RIN。

When selecting a transformer, it is very important to understand the input structure of the ADC. System designers should pay attention to these special transformer parameters. The impedance from the analog input source to the 100Ω differential input termination resistance inside the SXA006 device should be matched. The range of this termination resistance is described as RIN in the electrical characteristics table.

作为 ADC 结构的结果，相位和幅度的平衡也变得重要。当选择一个变压器时，相位不平衡要求不超过 ±2.5°，在希望输入的频率范围内幅度不平衡应该限制不超过 1dB。最后，应该考虑这个变压器的 VSWR（电压驻波比）、带宽和插入损失。当连接到 ADC 输入时，VSWR 帮助决定变压器的整个传输线终端电容。插入损失应该被考虑，以便在变压器输出的信号在电特性中要求的 ADC 输入范围 VID1 内。

As a result of the ADC structure, phase and amplitude balance also become important. When selecting a transformer, the phase imbalance is required to be no more than ±2.5°, and the amplitude imbalance should be limited to no more than 1dB over the desired input frequency range. Finally, the transformer's VSWR (voltage standing wave ratio), bandwidth, and insertion loss should be considered. When connected to the ADC input, the VSWR helps determine the transformer's overall transmission line termination capacitance. Insertion loss should be considered so that the signal at the transformer output is within the ADC input range VID1 required by the electrical characteristics.

② 直流耦合输入 / DC-Coupled Input

当要求直流耦合到 SXA006 模拟输入，单端到差分转换采用图 22 所示。在这个应用中，放大器 A1 的作用是实现单端到差分的转换，同时传输低失调和低噪声信号，也实现输出平衡，提供 SXA006 工作的信号。连接 SXA006 的 VCMO 引脚到放大器 A1 的 VCM_REF 引脚，通过恰当的缓冲器，将确保 SXA006 共模输入电压是 SXA006 最优化性能所需要的，见图 22。图中放大器 A2 作为具有低压工作和合理失调电压的缓冲器。

When DC coupling to the SXA006 analog input is required, the single-ended-to-differential conversion shown in Figure 22 is used. In this application, amplifier A1 performs the single-ended-to-differential conversion while transmitting a low-offset, low-noise signal and achieving output balance, providing the signal for the SXA006 to work with. Connecting the VCMO pin of the SXA006 to the VCM_REF pin of amplifier A1, through a suitable buffer, ensures that the SXA006 common-mode input voltage is what the SXA006 needs for optimized performance; see Figure 22. Amplifier A2 in the figure serves as a buffer with low-voltage operation and reasonable offset voltage.

确保从 SXA006 VCMO 引脚输出的电流不超过 100μA。 Ensure that the current output from the SXA006 VCMO pin does not exceed 100μA.

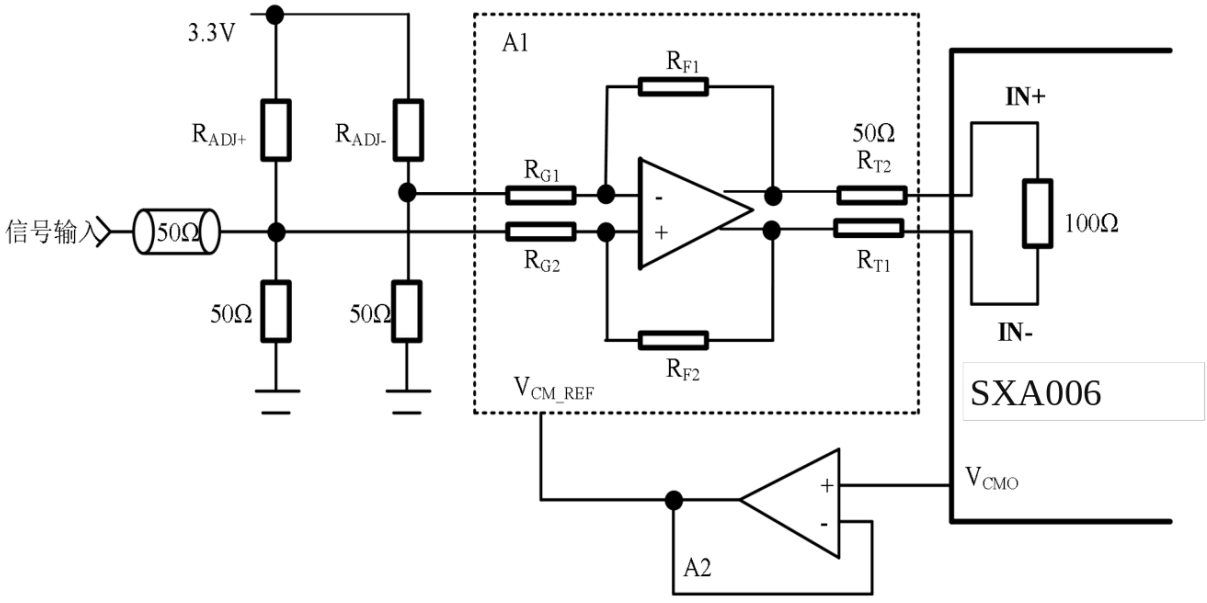


Figure 22: 用 VCMO 模拟输入的例子

图中 RADJ- 和 RADJ+ 被用来调节差分失调，这个失调可以从 ADC 输入 IN+/IN- 测量。关于一个 VIN- 超过丨15mV丨 未调节的正失调，应该通过在 RADJ- 位置的电阻来减小。同样地，一个关于 VIN- 超过 丨15mV丨 未调节的负失调，应该通过在 RADJ+ 位置的电阻来减小。要用未调节的差分失调将 VIN+/VIN- 的差分失调减小到丨15mV丨 以内，给定的 RADJ- 和 RADJ+ 值是不同的，参见表 15。 In the figure, RADJ- and RADJ+ are used to adjust the differential offset, which can be measured at the ADC inputs IN+/IN-. For an unadjusted positive offset of VIN- exceeding |15mV|, it should be reduced by the resistor in the RADJ- position. Similarly, an unadjusted negative offset of VIN- exceeding |15mV| should be reduced by the resistor in the RADJ+ position. To reduce the VIN+/VIN- differential offset to within |15mV| using the unadjusted differential offset, the given RADJ- and RADJ+ values differ; see Table 15.

表15 直流耦合失调调节 / Table 15 DC-Coupled Offset Adjustment

未调节失调读取 / Unadjusted Offset Reading	电阻值 / Resistance Value
0mV 到 10mV / 0mV to 10mV	不需要电阻 / No resistor required
11mV 到 30mV / 11mV to 30mV	20.0kΩ
31mV 到 50mV / 31mV to 50mV	10.0 kΩ
51mV 到 70mV / 51mV to 70mV	6.81 kΩ
71mV 到 90mV / 71mV to 90mV	4.75 kΩ
91mV 到 110mV / 91mV to 110mV	3.92 kΩ

b. 溢出范围（DOR）指示 / Overflow Range (DOR) Indication

当转换结果被截去一部分时，溢出输出被激活，结果 DOR 为高，DOR（反相）为低。只要在一条或两条总线上的正确数据在 00h～FFh 范围外，这个输出就被激活。 When the conversion result is clipped, the overflow output is activated, with DOR high and DOR (inverted) low. This output is activated whenever the correct data on one or both buses falls outside the range 00h–FFh.

c. 满刻度输入范围 / Full-Scale Input Range

对于所有 A/D 转换器，输入范围都是由 ADC 参考电压值来决定。SXA006 的参考电压由一个内部带隙参考驱动，其有效的参考电压值由 FSR 引脚控制，所以，当 FSR 引脚为高时模拟输入的差分满刻度范围为普通幅度；当 FSR 引脚为低时为减小的幅度，在电特性表中进行了定义。最好的 SNR 是在 FSR 为高时，但更好的失真和 SFDR 是在 FSR 为低时获得的。 For all A/D converters, the input range is determined by the ADC reference voltage value. The reference voltage of the SXA006 is driven by an internal bandgap reference, and its effective reference voltage value is controlled by the FSR pin. Therefore, when the FSR pin is high, the differential full-scale range of the analog input is the normal amplitude; when the FSR pin is low, it is the reduced amplitude, as defined in the electrical characteristics table. The best SNR is obtained with FSR high, but better distortion and SFDR are obtained with FSR low.

2.3 时钟输入 / Clock Input

SXA006 有差分 LVDS 时钟输入 INCLK+ 和 INCLK-，时钟输入必须采用差分信号交流耦合驱动。SXA006 是采用一个差分 1.5GHz 时钟来测试和保证它的性能，电特性表中用这个频率来表征典型功能。时钟输入内部设有直流偏置，输入时钟信号必须电容耦合到时钟引脚，如图 23 所示。

The SXA006 has differential LVDS clock inputs INCLK+ and INCLK-. The clock input must be driven by an AC-coupled differential signal. The SXA006 is tested and its performance guaranteed using a differential 1.5GHz clock, and this frequency is used in the electrical characteristics table to characterize typical functions. The clock input has internal DC bias, and the input clock signal must be capacitively coupled to the clock pins, as shown in Figure 23.

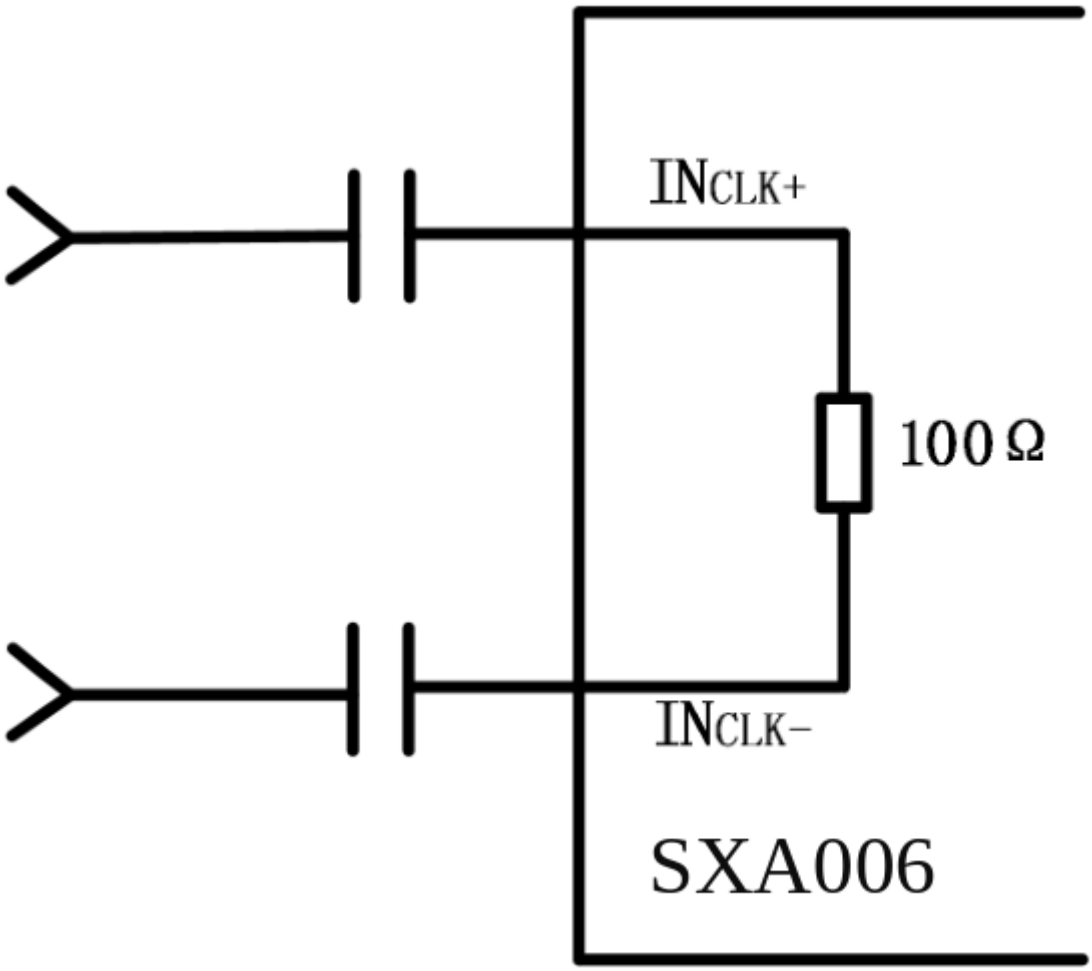


Figure 23: 差分（LVDS）输入时钟连接

如果最高环境温度不超出给定范围，工作在转换特性定义的采样率是没有问题的。如果在给定的环境温度下，工作采样率超过转换特性给定的值，可能会降低器件动态性能。这是因为在高采样率下会造成很高的功耗和芯片温度，在可靠性方面适当的热处理也是重要的，看 2.6）.b 热处理部分描述。 If the maximum ambient temperature does not exceed the given range, operating at the sample rates defined in the conversion characteristics is not a problem. If the operating sample rate exceeds the value given in the conversion characteristics at a given ambient temperature, the device dynamic performance may be reduced. This is because high sample rates cause high power consumption and chip temperature, and proper thermal treatment is also important for reliability; see the thermal treatment description in 2.6).b.

时钟输入差分对应该有一个 100Ω 的特征电阻，当用一个变压器时应在时钟源端接一个特征电阻（100Ω）。输入时钟线应尽可能的短和走直线，SXA006 时钟输入有一个未修调过的 100Ω 电阻。 The clock input differential pair should have a 100Ω characteristic resistance; when a transformer is used, a characteristic resistance (100Ω) should be terminated at the clock source. The input clock lines should be as short as possible and routed straight; the SXA006 clock input has an untrimmed 100Ω resistor.

输入时钟幅度不足将导致差的动态性能，输入时钟幅度过高会造成模拟输入失调电压的变化。为了避免这些问题，务必保持时钟幅度在电特性给定的范围内 VID2。 An insufficient input clock amplitude will result in poor dynamic performance, and an excessive input clock amplitude will cause changes in the analog input

offset voltage. To avoid these problems, be sure to keep the clock amplitude within the VID2 range given in the electrical characteristics.

输入时钟信号的高低时间会影响任何 A/D 转换器的性能。SXA006 有一个时钟占空比校正电路来保证在整个温度范围的性能。如果输入时钟高和低时间保持在电特性给定的占空比范围内，ADC 将会满足性能要求。 The high and low times of the input clock signal affect the performance of any A/D converter. The SXA006 has a clock duty-cycle correction circuit to guarantee performance over the entire temperature range. If the input clock high and low times are kept within the duty-cycle range given in the electrical characteristics, the ADC will meet the performance requirements.

SXA006 这样的高速高性能 ADC 要求一个非常稳定的具有最小相位噪声或抖动的输入时钟信号。ADC 抖动由 ADC 精度（位数）、最大输入频率和相对于输入满刻度范围的输入信号幅度决定。下面公式可以得到为防止抖动引起 SNR 减小的最大抖动（所有信号源抖动的和）： A high-speed, high-performance ADC such as the SXA006 requires a very stable input clock signal with minimum phase noise or jitter. The ADC jitter is determined by the ADC accuracy (number of bits), the maximum input frequency, and the input signal amplitude relative to the input full-scale range. The following formula gives the maximum jitter (the sum of the jitter of all signal sources) that prevents jitter from reducing the SNR:

$$tJ(MAX) = [1 / (2^{(N+1)} \times \pi \times fIN)] \times (VINFSR / VIN(PP))$$

这里 tJ(MAX) 是所有抖动源的二阶均方根和，VIN(PP) 是模拟输入信号峰峰值，VINFSR 是 ADC 的满刻度范围，"N" 是 ADC 分辨率，fIN 是 ADC 最大模拟输入频率。 Here tJ(MAX) is the root-sum-square of all jitter sources, VIN(PP) is the peak-to-peak analog input signal, VINFSR is the full-scale range of the ADC, "N" is the ADC resolution, and fIN is the maximum analog input frequency of the ADC.

注意到上面提到的最大抖动是所有源抖动的 RSS（平方和的平方根）之和，包括 ADC 输入时钟，加上系统到输入时钟和输入信号，再加上 ADC 自身的抖动。由于 ADC 自身抖动影响不受设计者控制，设计者能做的最好是保证输入时钟抖动和模拟电路到模拟信号的抖动相加达到最小。 Note that the maximum jitter mentioned above is the RSS (root-sum-square) sum of all source jitter, including the ADC input clock, plus the system contributions to the input clock and input signal, plus the ADC's own jitter. Because the effect of the ADC's own jitter is not under the designer's control, the best the designer can do is to ensure that the sum of the input clock jitter and the jitter contributed by the analog circuitry to the analog signal is minimized.

输入时钟幅度大于电特性表给定的值会导致输入失调电压的增加，当两个模拟输入引脚接在同一电位时会造成转换器产生一个不是预期的 127/128 的输出码。 An input clock amplitude greater than the value given in the electrical characteristics table will cause an increase in the input offset voltage; when the two analog input pins are connected to the same potential, it will cause the converter to produce an unexpected 127/128 output code.

2.4 控制引脚 / Control Pins

6 个控制引脚（不包括串行接口的使用）提供了很多 SXA006 可能的工作模式和帮助对器件的使用。这些控制引脚提供了满刻度输入范围设置、自校正、校正延迟、输出沿同步选择、LVDS 输出电平选择和一个省电工作模式。 Six control pins (not including the serial interface usage) provide many of the SXA006's possible operating modes and assist in using the device. These control pins provide full-scale input range setting, self-calibration, calibration delay, output edge synchronization selection, LVDS output level selection, and a power-down operating mode.

a. 满刻度输入范围设置 / Full-Scale Input Range Setting

在普通工作模式下，满刻度输入范围由 FSR 控制脚（14 脚）来选择，在电特性表中进行了定义。在扩展控制模式（SPI 模式）满刻度输入范围由 SPI 编程控制。 In normal operating mode, the full-scale input range is selected by the FSR control pin (pin 14), as defined in the electrical characteristics table. In extended control mode (SPI mode), the full-scale input range is controlled by SPI programming.

b. 自校正 / Self-Calibration

SXA006 必须运行自校正才能达到保证的性能，校正过程是上电自动运行，同时也可通过指令校正在任何时候运行。无论是上电就有输入时钟还是上电一段时间之后有时钟，校正过程都是一样的。当校正正在运行时 CalRun 输出指示为高。注意到在校正周期 QCLK 输出是无效的，因此不推荐其作为系统时钟。 The SXA006 must run self-calibration to achieve its guaranteed performance. The calibration process runs automatically at power-up and can also be run at any time by commanded calibration. The calibration process is the same whether the input clock is present at power-up or starts some time after power-up. While calibration is running, the CalRun output indicates high. Note that the QCLK output is invalid during the calibration cycle, so its use as a system clock is not recommended.

① 上电校正 / Power-Up Calibration

在上电延迟一段时间后校正过程自动完成，这个延迟时间由 CalDly 设置决定，将在下面的校正延迟选择部分描述。 The calibration process completes automatically after a power-up delay; this delay is determined by the CalDly setting, as described in the calibration delay selection part below.

上电时，如果 CAL 引脚为高电平，则校正过程不能完成，但 SXA006 仍会工作，只是校正过程不能执行而已，这时性能也会变差，不推荐使用。这种情况下可采用指令校正的方式来实现校正，详细描述见 2.4）.b.②指令校正部分。 At power-up, if the CAL pin is at a high level, the calibration process cannot complete, but the SXA006 still works — only the calibration process cannot be executed, and the performance will be worse; this is not recommended. In this case, commanded calibration can be used to achieve calibration; see 2.4).b.② for details.

如果输入时钟在上电后没有运行，且上电校正电路处于活动状态，这时内部上电校正电路处于一个未知的逻辑状态。模拟电路将保持在省电状态，典型功耗将不超过 200mW。在时钟开始运行后功耗将正常。 If the input clock does not run after power-up and the power-up calibration circuit is active, the internal power-up calibration circuit is in an unknown logic state. The analog circuitry will remain in the power-down state, and the typical power consumption will not exceed 200mW. After the clock starts running, the power consumption will become normal.

② 指令校正 / Commanded Calibration

指令校正可在任何时候运行。为了启动指令校正，在 CAL 为低电平保持最小 tCAL_L 输入时钟周期之后，再让 CAL 引脚为高电平保持一个最小 tCAL_H 输入时钟周期。如在上电时 CAL 引脚为高电平将阻止上电校正的运行，这时要采用指令校正的方式来使校正运行，即 CAL 引脚必须为低电平保持最小 tCAL_L 输入时钟周期之后，接着为高电平保持最小 tCAL_H 输入时钟周期，CAL 引脚在这个高电平 tCAL_H 输入时钟周期之后校正运行才开始。为了确定校正运行什么时候完成，应该监测 CalRun 信号。 Commanded calibration can be run at any time. To start commanded calibration, hold CAL low for at least the minimum tCAL_L input clock cycles, and then hold the CAL pin high for at least the minimum tCAL_H input clock cycles. If the CAL pin is high at power-up, it prevents power-up calibration from running; in that case, commanded calibration must be

used to run calibration, i.e., the CAL pin must be held low for at least the minimum tCAL_L input clock cycles and then high for at least the minimum tCAL_H input clock cycles, after which the calibration run starts. To determine when the calibration run is complete, the CalRun signal should be monitored.

当不需要校正时，为了保证随机噪声不引起校正开始，最小的 tCAL_H 和 tCAL_L 输入时钟周期时序是必须的。像在 1.1）.a 自校正提到的为了最好的性能，在上电之后自校正应该运行 20 秒或更长时间，根据实际系统性能要求当工作温度变化太大时校正要重启。ENOB 随结温增加而轻微降低，运行一个新的自校正周期可以从根本上消除这个变化。 When calibration is not needed, the minimum tCAL_H and tCAL_L input clock cycle timing is necessary to ensure that random noise does not start a calibration. As mentioned in 1.1).a, for best performance self-calibration should run for 20 seconds or longer after power-up, and calibration should be restarted when the operating temperature changes greatly, according to actual system performance requirements. ENOB decreases slightly as the junction temperature increases; running a new self-calibration cycle can fundamentally eliminate this variation.

在一个上电校正周期期间，两个 ADC 和输入终端电阻都被校正，当 ENOB 随结温度轻微变化时，执行一个指令校正可以使 ADC 性能变得一致。 During a power-up calibration cycle, both ADCs and the input termination resistance are calibrated; when the ENOB varies slightly with junction temperature, performing a commanded calibration can make the ADC performance consistent.

③ 校正延迟 / Calibration Delay

在上电应用后到校正开始，CalDly 输入（引脚 127）是用来选择二个延迟时间中的一个，如 1.1）.a 自校正所述。校正延迟时间值是在校正开始前使电源电压上电并达到稳定。没有延迟或延迟不够，这样将使在电源电压还没有稳定在工作值时，校正就开始工作，将导致不能达到最好校正结果。如果上电后 PD 引脚为高，校正延迟计数器将失效直到 PD 引脚为低。因此，在上电期间保持 PD 引脚为高将使上电校正开始的延迟更大。CalDly 引脚的最好设置取决于电源电压上电设置时间。 Between power-up application and the start of calibration, the CalDly input (pin 127) is used to select one of two delay times, as described in 1.1).a. The calibration delay value allows the supply voltage to power up and stabilize before calibration starts. With no delay or insufficient delay, calibration starts working before the supply voltage has stabilized at its operating value, which will prevent the best calibration result. If the PD pin is high after power-up, the calibration delay counter is disabled until the PD pin goes low. Therefore, holding the PD pin high during power-up will make the delay before power-up calibration starts even longer. The best CalDly setting depends on the supply voltage power-up settling time.

注意：在扩展控制模式校正延迟选择是不可用的，且延迟时间被缩短。 Note: In extended control mode, the calibration delay selection is not available, and the delay time is shortened.

c. 输出沿同步 / Output Edge Synchronization

QCLK 信号可用来帮助锁存转换器输出数据到外部电路，输出数据能与这些 QCLK 信号的任何一个沿同步。这就是说，输出数据转换可被设定发生在 QCLK 信号的上升沿或下降沿，因此 QCLK 信号的两个沿都能被用来锁存输出数据到接收电路。 The QCLK signal can be used to help latch the converter output data into external circuitry; the output data can be synchronized to either edge of these QCLK signals. That is, output data transitions can be set to occur on the rising or falling edge of the QCLK signal, so both edges of the QCLK signal can be used to latch output data into the receiving circuit.

当 OutEdge（引脚 4）为高，输出数据转换与 QCLK+（引脚 82） 的上升沿同步变化；当 OutEdge（引脚 4）为低，输出数据转换与 QCLK+（引脚 82）的下降沿同步变化。 When OutEdge (pin 4) is high, output data

transitions are synchronized with the rising edge of QCLK+ (pin 82); when OutEdge (pin 4) is low, output data transitions are synchronized with the falling edge of QCLK+ (pin 82).

在 SXA006 所能承受的非常高的速度下，QCLK 和数据线长度细微的差别都能造成数据捕获的正确和错误。OutEdge 引脚被用来设置在 QCLK 边沿捕获数据，这最适合于应用电路和布版。 At the very high speeds the SXA006 can sustain, minute differences in QCLK and data line lengths can make the difference between correct and incorrect data capture. The OutEdge pin is used to set data capture at the QCLK edge that best suits the application circuit and layout.

重要提示：为了获得正确的数据，当 OutEdge（引脚 4）为高时，最好用 QCLK+ 的下降沿捕获数据；当 OutEdge（引脚 4）为低时，最好用 QCLK+ 的上升沿捕获数据。 Important: To obtain correct data, when OutEdge (pin 4) is high, it is best to capture data on the falling edge of QCLK+; when OutEdge (pin 4) is low, it is best to capture data on the rising edge of QCLK+.

d. LVDS 输出电平控制 / LVDS Output Level Control

输出电平可以用 Outv（引脚 3）来设置为二个电平之中的一个。当 Outv 为高时，输出驱动能力非常强；Outv 为低时，输出驱动功耗较低，但是较小的输出电平意味着减少了抗噪声能力。 The output level can be set to one of two levels with Outv (pin 3). When Outv is high, the output drive capability is very strong; when Outv is low, the output drive power is lower, but the smaller output level means reduced noise immunity.

对于短的 LVDS 线和低噪声系统，Outv 输入为低可以得到满意的性能。如果 LVDS 线很长或使用 SXA006 的系统是有噪声的，把 Outv 接为高是必须的。 For short LVDS lines and low-noise systems, setting the Outv input low gives satisfactory performance. If the LVDS lines are long or the system using the SXA006 is noisy, connecting Outv high is necessary.

e. 双边沿采样 / Dual-Edge Sampling

双边沿采样（DES）特性使两对模拟输入中的一对被送入到两通道 ADC，另一对输入无效。一通道的 ADC 在输入时钟的一个沿（占空比校正）采样输入信号，另一通道在输入时钟的另一个沿（占空比校正）采样输入信号，结果是一个 1：4 的多路选择器输出数据，采样率是输入时钟频率的两倍。 The dual-edge sampling (DES) feature routes one of the two pairs of analog inputs into the two-channel ADC, with the other pair of inputs disabled. One channel's ADC samples the input signal on one edge of the input clock (with duty-cycle correction) and the other channel samples the input signal on the other edge of the input clock (with duty-cycle correction); the result is a 1:4 multiplexer output data stream at a sample rate of twice the input clock frequency.

为了在非扩展控制模式下使用这个特性，让引脚 127 悬空，在 I 通道输入的信号被两个转换器采样，那么校正延迟将是只有一个短的延迟。 To use this feature in non-extended control mode, leave pin 127 floating; the signal at the I-channel input is sampled by both converters, and the calibration delay will be only a single short delay.

在扩展控制模式，每一个输入都可被用作双边沿采样，参考 1.1）.e.① 部分。 In extended control mode, either input can be used for dual-edge sampling; see 1.1).e.①.

重要提示： 1）对于扩展控制模式，当在双边沿采样模式下采用自动时钟相位控制特性时，在 ADC 上电前自动相位控制要设置为无效（设置 DES 使能寄存器 Dh 的 14 位为 0）这个非常重要。如果不这样做可能造成芯片不能从省电状态转换到正常工作状态来。 2）对于非扩展控制模式，当 SXA006 已上电，且 DES 模式是必须时，在上电序列期间或之后确保引脚 127（CalDly/DES/ST2（反相））最初为低，然后这个引脚可以被悬空或接到 VCC/

2，进入 DES 模式，这将确保这部分正确地进入 DES 模式。 3）如果输入时钟因为某个原因被中断或停止，自动相位控制应该也是无效。如果输入时钟频率发生一个大的突变，也是出现这种情况的一个事例。 4）在自动 DES 模式下，如果 ADC 的校正是必须的，在完成一个校正周期前器件必须返回到普通模式工作。一旦校正完成，器件能重返回到自动 DES 模式，并且重新开始工作。 Important: 1) For extended control mode, when the automatic clock phase control feature is used in dual-edge sampling mode, it is very important that automatic phase control be set to disabled before the ADC is powered up (set bit 14 of the DES enable register Dh to 0). Failure to do so may cause the chip to be unable to transition from the power-down state to normal operation. 2) For non-extended control mode, when the SXA006 has powered up and DES mode is required, ensure that pin 127 (CalDly/DES/ST2 (inverted)) is initially low during or after the power-up sequence; this pin can then be left floating or connected to VCC/2 to enter DES mode, which will ensure this part correctly enters DES mode. 3) If the input clock is interrupted or stopped for any reason, automatic phase control should also be disabled. A large sudden change in the input clock frequency is an example of this situation. 4) In automatic DES mode, if ADC calibration is required, the device must return to normal mode operation before completing a calibration cycle. Once calibration is complete, the device can return to automatic DES mode and resume operation.

f. 省电（Power Down）特性 / Power-Down Feature

省电引脚（PD 和 PDQ）允许 SXA006 两通道完全处于省电模式（PD）或 Q 通道进入省电而 I 通道仍然正常工作，见表 12，关于省电特性更详细的介绍请看 1.1).g 部分。 The power-down pins (PD and PDQ) allow both channels of the SXA006 to be fully in power-down mode (PD), or the Q channel to enter power-down while the I channel still operates normally; see Table 10. For a more detailed introduction to the power-down feature, see 1.1).g.

当省电引脚（PD 和 PDQ）对各自通道为高时，数据（+/-）输出引脚处于高阻状态。从省电模式再回到普通模式工作，通路中将包含无意义的信息，必须清除。 When the power-down pins (PD and PDQ) are high for their respective channels, the data (+/-) output pins are in a high-impedance state. On returning from power-down mode to normal operation, the path will contain meaningless information, which must be cleared.

在校正正在运行时，即使 PD 输入为高，器件也不能进入省电模式，直到校正过程完成。然而，如果已上电，同时 PD 已经为高，器件将不会进入校正过程，直到 PD 输入为低。在器件处于省电模式时，即使使用手动校正，校正也根本不会运行，这就是说，当器件处于省电模式时手动校正不起作用，完全被封锁了。 While calibration is running, even if the PD input is high, the device cannot enter power-down mode until the calibration process completes. However, if the device has powered up with PD already high, the device will not enter the calibration process until the PD input goes low. When the device is in power-down mode, calibration will not run at all even with manual calibration — that is, manual calibration has no effect and is completely blocked when the device is in power-down mode.

2.5 数据输出 / Data Output

在器件内部，SXA006 中 I 或 Q 通道的输出数据到两条 LVDS 输出总线上。两路 LVDS 总线中的一路在输入时钟（INCLK+）引脚的奇数下降沿开始连续获得输出数据，与此同时，另一路输出数据在输入时钟（INCLK+）的偶数下降沿开始连续获得。这意味着，每个 LVDS 总线的数据速率为输入时钟频率的二分之一，同时两路总线必须被多路转换合并后才能获得完整的 1.5GSPS 转换结果。

Inside the device, the output data of the I or Q channel of the SXA006 goes onto two LVDS output buses. One of the two LVDS buses begins to continuously obtain output data on the odd falling edges of the input

clock (INCLK+) pin, while the other bus begins to continuously obtain output data on the even falling edges of the input clock (INCLK+). This means that the data rate of each LVDS bus is one half of the input clock frequency, and the two buses must be multiplexed together to obtain the complete 1.5GSPS conversion result.

由于这个器件推荐的输入时钟频率最小值为 200MHz（普通模式，非 DES 模式），则有效的输出数据速率低到 100MSPS。 Because the recommended minimum input clock frequency of this device is 200MHz (normal mode, non-DES mode), the effective output data rate goes as low as 100MSPS.

这里有一个 LVDS 输出时钟对（QCLK）可用于锁存所有总线上的 LVDS 输出数据。数据是在 QCLK 的上升沿还是下降沿被输出是由 OutEdge 引脚的状态所决定的，见 2.4）.c 部分描述。 An LVDS output clock pair (QCLK) is available to latch the LVDS output data on all buses. Whether data is output on the rising or falling edge of QCLK is determined by the state of the OutEdge pin; see 2.4).c.

DDR（双倍数据率）时钟也可以使用，在这个模式下，以 QCLK 的每个沿输出一组数据，QCLK 频率是输入时钟频率 1/4，更详细的看时序图部分。 A DDR (double data rate) clock can also be used; in this mode, a set of data is output on each edge of QCLK, and the QCLK frequency is 1/4 of the input clock frequency; see the timing diagram section for details.

Outv 引脚被用来设置 LVDS 差分输出幅度，看 2.4）.d 部分。 The Outv pin is used to set the LVDS differential output amplitude; see 2.4).d.

输出格式是偏移二进制码。因此，一个相对于 IN- 的 IN+ 正满刻度输入将产生一个全为 1 的输出码，一个相对于 IN+ 的 IN- 满刻度输入将产生一个全为 0 的输出码，当 IN+ 与 IN- 相等时，输出码在 127 和 128 之间变化。 The output format is offset binary code. Therefore, a positive full-scale input at IN+ relative to IN- produces an output code of all 1s, a full-scale input at IN- relative to IN+ produces an output code of all 0s, and when IN+ and IN- are equal, the output code toggles between 127 and 128.

2.6 功耗考虑 / Power Consumption Considerations

如果 A/D 转换器没有用充分地旁路来泄放大的瞬态电流，将破坏内部的电源电路。在 A/D 转换器电源引脚 2.5cm 之内放置一个 33μF 的电容，而另一个 0.1μF 的电容应该放置在每个 VCC 引脚尽可能近的地方，最好在 0.5 厘米之内，无铅片式电容是首选，因为有低的引线电感。 If the A/D converter is not adequately bypassed to shunt large transient currents, the internal supply circuitry will be damaged. Place a 33μF capacitor within 2.5cm of the A/D converter supply pins, and another 0.1μF capacitor as close as possible to each VCC pin, preferably within 0.5 cm; leadless chip capacitors are preferred because of their low lead inductance.

VCC 和 VDD 电源引脚应该隔离，以阻止数字噪声耦合到 ADC 的模拟部分。当它们共用一个电源时，推荐在这些电源线间放置一个铁氧体扼流圈。 The VCC and VDD supply pins should be isolated to prevent digital noise from coupling into the analog section of the ADC. When they share a single supply, it is recommended to place a ferrite choke between these supply lines.

作为所有高速转换器的一个例子，假设 SXA006 有很小的电源电压噪声抑制，在一个消耗许多数字功耗的系统中，任何一个用于数字电路的电源都不能作为 SXA006 的电源。如果没有一个专用电源的话，ADC 电源应该使用与其他模拟电路一样的电源。 As is the case with all high-speed converters, assume that the SXA006 has very small supply voltage noise rejection; in a system that consumes a lot of digital power, no supply used for digital circuitry can serve as the SXA006 supply. If no dedicated supply is available, the ADC supply should use the same supply as other analog circuitry.

a. 电源电压 / Supply Voltage

SXA006 指定的工作电源电压是 1.95V～2.05V。注意这点非常重要，当器件工作在稍微高点的电源电压时，这些较高的电源电压可能会降低工作寿命。 The specified operating supply voltage of the SXA006 is 1.95V–2.05V. Note that this is very important: when the device operates at a slightly higher supply voltage, these higher supply voltages may reduce the operating life.

任何引脚的电压都不能超过电源电压或低于地超过 150mV，更不能接一个瞬态偏置，否则，在电源上电或断电的时候可能会出现问题。为了确保驱动任何输入引脚的电压，模拟或数字输入端都不能出现任何一个比 SXA006 电源引脚电压更快的电压。 The voltage at any pin must not exceed the supply voltage or go below ground by more than 150mV, and a transient bias must not be applied; otherwise, problems may occur at power-up or power-down. To ensure the voltage driving any input pin, neither the analog nor the digital input must see any voltage faster than the voltage at the SXA006 supply pins.

即使在电源上电和断电期间，都应严格遵守绝对最大额定值。在电源开启或关断时会产生一个电压尖峰损坏 SXA006。图 27 提供了一个电源过冲保护电路。 The absolute maximum ratings must be strictly observed even during power-up and power-down. A voltage spike generated when the supply is switched on or off can damage the SXA006. Figure 24 provides a power-supply overshoot protection circuit.

除有一个最低负载供给外，许多调节器都提供了上电输出尖峰，而有源器件吸收非常小的电流，这个尖峰电压能达到几百毫伏。这个结果就是一个上电尖峰，能损坏 SXA006，除非电源供给的是最低负载。为了确保没有上电尖峰，在调节器输出端接 100Ω 电阻，给上电期间提供一个最小的输出电流。 Unless a minimum load is provided, many regulators produce a power-up output spike, while active devices draw very small current; this spike voltage can reach several hundred millivolts. The result is a power-up spike that can damage the SXA006 unless the supply provides the minimum load. To ensure there is no power-up spike, connect a 100Ω resistor at the regulator output to provide a minimum output current during power-up.

在图 24 中，如果电源电压是 4V～5V，一个 LM317 线性调节器可以满足要求；如果用一个 3.3V 电源，推荐使用 LM1086 线性调节器。 In Figure 24, if the supply voltage is 4V–5V, an LM317 linear regulator meets the requirements; if a 3.3V supply is used, an LM1086 linear regulator is recommended.

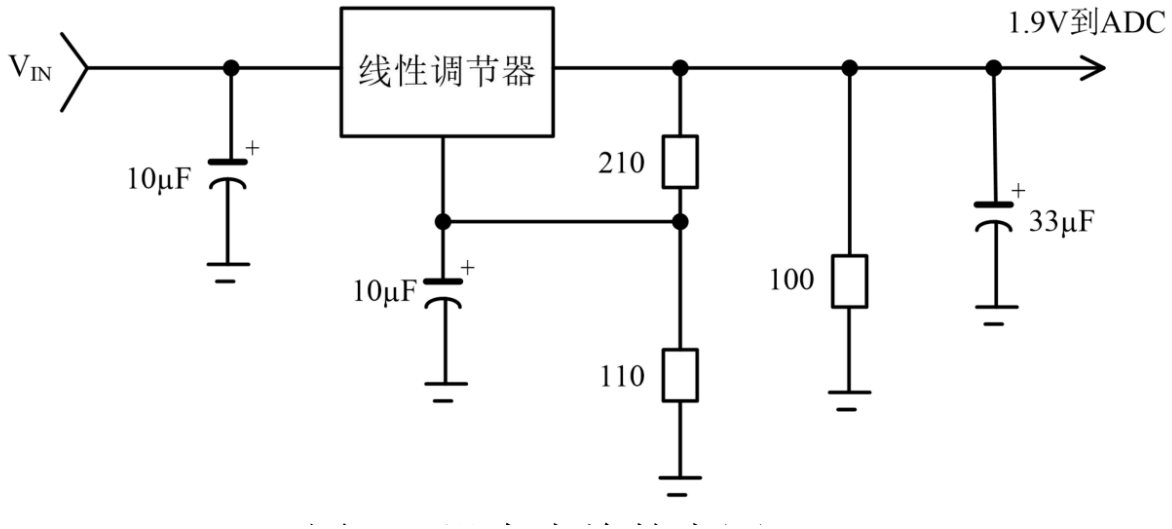


Figure 24: 没有尖峰的电源

输出驱动有一个电源电压 VDD，其值应在工作额定值规定的范围内，这个电压不能超过模拟电源电压 VCC，其电压尖峰决不能超过 VCC+100mV。 The output driver has a supply voltage VDD, whose value should be within the range specified by the operating ratings; this voltage must not exceed the analog supply voltage VCC, and its voltage spike must never exceed VCC+100mV.

器件上电后，如果没有时钟信号输入，器件的电流可能会小于 200mA，这是因为 SXA006 复位是通过时钟逻辑来控制的，因此它的初始状态是未知的。如果复位逻辑在"导通"状态到来，这将导致大部分模拟电路进入省电（power down）模式，这样电源电流不超过 100mA。这个电流大于省电模式电流，这是因为不是 ADC 的所有部分都处于省电状态，在输入时钟建立后器件电流将正常。 After power-up, if there is no clock signal input, the device current may be less than 200mA, because the SXA006 reset is controlled through clock logic and its initial state is therefore unknown. If the reset logic arrives in the "on" state, this will cause most of the analog circuitry to enter power-down mode, so that the supply current does not exceed 100mA. This current is greater than the power-down mode current because not all parts of the ADC are in the power-down state; once the input clock is established, the device current will become normal.

b. 散热处理 / Thermal Treatment

对于 SXA006 具有这样的超高速和高性能功耗是很低的。但是就单纯功耗来讲仍然是很大，需要注意其散热处理。因可靠性原因，芯片最大温度不应超过 160°C。 For the SXA006, such ultra-high speed and high performance are achieved with low power consumption. However, in absolute terms the power consumption is still large, and attention must be paid to its thermal treatment. For reliability reasons, the maximum chip temperature should not exceed 160°C.

作为给用户使用提供方便，SXA006 内含一个热二极管辅助进行温度测量。但热二极管的特性没有表征，工艺没有提供有关的准确信息。 For user convenience, the SXA006 contains a thermal diode to assist temperature measurement. However, the characteristics of the thermal diode have not been characterized, and the process provides no accurate information about it.

请注意下面是推荐在 PCB 板上安装器件。应该考虑在 PCB 上的开始点和开发装配过程。推荐按基于过去封装安装的经验进行。SXA006 封装的底部有一个镀金焊盘，提供一个主要的散热通道，具有非常好的到印制电路板的接地效果。焊接到 PCB 板的引线图形设计与普通的 CQFP 一样，但封装的底部镀金焊盘必须焊接到印制板上，以最大程度移走封装上的热量，同时确保最好的产品性能。 Note the following recommendations for mounting the device on a PCB. The starting point on the PCB and the development assembly process should be considered. It is recommended to proceed based on past package mounting experience. The bottom of the SXA006 package has a gold-plated pad that provides a primary heat dissipation path and a very good ground connection to the printed circuit board. The lead pattern design for soldering to the PCB is the same as a normal CQFP, but the gold-plated pad at the bottom of the package must be soldered to the printed board to remove the package heat to the maximum extent and ensure the best product performance.

为了最大程度地移走封装上的热量，在封装区域内一个热连接图形必须内嵌在 PC 板上。器件的底部必须焊接，直到能确保在封装区域外有足够的热传导。这个外露焊盘的引线图形设计应与封装底部一样大，尺寸为 14.1×14.1mm2，位于器件的底部，并完全覆盖热引线图形，且这个热引线图形应连接到地。 To remove the package heat to the maximum extent, a thermal connection pattern must be embedded in the PC board within the package area. The bottom of the device must be soldered so that sufficient heat conduction outside the package area is ensured. The lead pattern design of this exposed pad should be the same size as the package bottom, 14.1×14.1mm2, located at the bottom of the device and completely covering the thermal lead pattern, and this thermal lead pattern should be connected to ground.

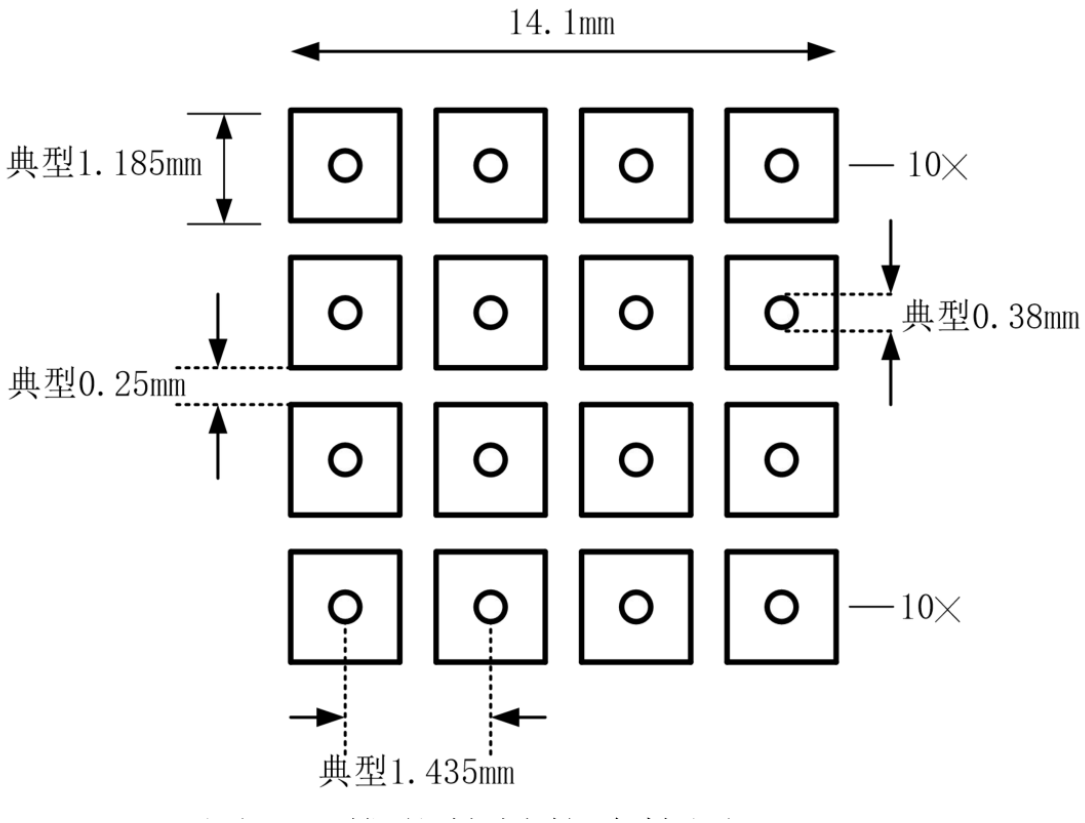


Figure 25: 推荐的封装连接图形

由于用一个大孔开口可能会导致接触不良，因此孔开口应再细分为小孔阵列，类似于图 28 的连接图形。
Because a single large hole opening may cause poor contact, the hole opening should be subdivided into an array of small holes, similar to the connection pattern of Figure 25.

为了最小化结温度，推荐在 PCB 板上安装一个简单的散热片，这就是在 PCB 板的对边制作一个大约 14.5 平方厘米面积的铜区域，这个铜区域可以是镀金的或涂上一层焊锡以防止腐蚀，但不应有保形涂料，它可能提供某些热绝缘。应该用热孔来实现顶部和底部铜区域的连接。这些热孔扮演"热管道"的角色，把热能从器件 PCB 板的一边传递到对面的一边，利于更有效地释放热量，推荐使用近 100 个热孔。 To minimize the junction temperature, it is recommended to install a simple heat sink on the PCB, that is, to make a copper area of approximately 14.5 square centimeters on the opposite side of the PCB. This copper area can be gold-plated or coated with a layer of solder to prevent corrosion, but it should not have conformal coating, which may provide some thermal insulation. Thermal vias should be used to connect the top and bottom copper areas. These thermal vias act as "heat pipes," transferring heat energy from one side of the device PCB to the other side to release heat more effectively; using nearly 100 thermal vias is recommended.

这些热孔间的典型距离为 1.435mm，孔的典型直径 0.38mm，这些孔应是一个柱体镀金的，以避免在焊接过程中焊接材料掉入孔中，因为这些焊接材料在 PCB 和封装暴露焊盘之间会形成气孔。这些气孔会增加器件和板上热焊盘之间的热阻，这会导致器件工作变热。 The typical spacing between these thermal vias is 1.435mm, and the typical hole diameter is 0.38mm. These holes should be cylindrical and gold-plated to prevent solder material from falling into the holes during soldering, because such solder material would form voids between the PCB and the package exposed pad. These voids increase the thermal resistance between the device and the board thermal pad, causing the device to operate hotter.

2.7 版图和接地 / Layout and Grounding

合适的接地和所有信号走线从根本上保证了正确的转换，应使用单一的地平面来代替模拟和数字区域分离的地平面。 Proper grounding and the routing of all signals fundamentally guarantee correct conversion; a single ground plane should be used instead of separate ground planes for the analog and digital regions.

由于数字开关瞬态由大量的高频成分组成，表面效应告诉我们一个整体的地平面对逻辑产生的噪声影响很小，总的表面面积比总的地平面体积更重要。典型的有噪声数字电路与敏感模拟电路之间的耦合导致性能差，这是不可能隔离和修复的，解决办法是让模拟电路与数字电路分离。 Because digital switching transients consist of many high-frequency components, the skin effect tells us that a single integral ground plane has very little effect on logic-generated noise; the total surface area is more important than the total ground plane volume. The typical coupling between noisy digital circuitry and sensitive analog circuitry leads to poor performance, which cannot be isolated and repaired; the solution is to separate the analog circuitry from the digital circuitry.

高功耗数字部分不能位于这些部分之上或紧邻，这些部分为：任何线性元件、电源路径、用于模拟或混合信号的平面。因为这些公共回路电流通路会引起回到 ADC 的模拟输入地波动，给转换结果造成额外的噪声。 High-power digital sections must not be located above or immediately adjacent to the following sections: any linear components, power supply paths, and planes used for analog or mixed signals. Because these common return current paths will cause fluctuations in the analog input ground returning to the ADC, causing additional noise in the conversion results.

为了避免数字噪声进入模拟通道中，通常采取模拟信号线和数字信号线彼此以 90°十字交叉方式。然而在高频系统，应避免模拟信号线和数字信号线完全十字交叉，输入时钟信号线应与所有模拟和数字线隔离，一般公认的是应避免 90°交叉，因为在高频下即使一点点耦合都会引起问题，因此，在高频下采用直线信号通路将获得最好的性能。 To avoid digital noise entering the analog channel, analog signal lines and digital signal lines are usually crossed at 90° to each other. However, in high-frequency systems, complete crossing of analog and digital signal lines should be avoided; the input clock signal line should be isolated from all analog and digital lines. It is generally accepted that 90° crossings should be avoided, because at high frequencies even a tiny amount of coupling can cause problems; therefore, straight signal paths at high frequencies will give the best performance.

模拟输入应与噪声信号路径隔离，避免伪信号耦合到输入，这对 SXA006 以低电平信号驱动时特别重要。在转换器的输入与地之间连接的任何外部元件（例如滤波电容）应连接到模拟地平面的一个非常干净的点上，所有模拟电路（输入放大器、滤波器等）应与任何数字元件隔离。 The analog input should be isolated from noisy signal paths to avoid spurious signals coupling into the input; this is particularly important when the SXA006 is driven with low-level signals. Any external component connected between the converter input and ground (e.g., a filter capacitor) should be connected to a very clean point on the analog ground plane, and all analog circuitry (input amplifiers, filters, etc.) should be isolated from any digital components.

2.8 动态性能 / Dynamic Performance

SXA006 是采用交流测试的，它的动态性能是可保证的。为了满足技术要求和避免抖动引入噪声，驱动 INCLK 输入的时钟源必须具备低的均方根抖动，可容许的抖动是输入频率和输入信号电平的一个函数，如 2.3）部分描述的。 The SXA006 is AC-tested, and its dynamic performance is guaranteed. To meet the technical requirements and avoid jitter-introduced noise, the clock source driving the INCLK input must have low RMS jitter; the allowable jitter is a function of the input frequency and input signal level, as described in 2.3).

实际应用中，让 ADC 输入时钟线尽可能的短，让他足够远离其他任何信号线，视其为一个传输线，这些是一个非常好的习惯。其他信号线可能引入抖动到输入时钟信号，如果不与这些路径隔离开的话，时钟信号也能引入噪声到模拟路径。 In practical applications, it is a very good habit to keep the ADC input clock line as short as possible, keep it far enough away from all other signal lines, and treat it as a transmission line. Other signal lines may introduce jitter into the input clock signal, and if not isolated from these paths, the clock signal can also introduce noise into the analog path.

将封装背面的外露焊盘良好地连接到地时，获得最好的动态性能。这是因为这个从芯片到地的通路是一个低阻的，比封装脚提供的通路还低。 The best dynamic performance is obtained when the exposed pad on the back of the package is well connected to ground. This is because this path from the chip to ground is a low-resistance one, lower than the path provided by the package pins.

2.9 串行接口使用 / Serial Interface Usage

SXA006 可能工作在非扩展控制模式（无串行接口）或扩展控制模式，表 17 和表 18 分别描述了 Pin3、4、14 和 127 在非扩展控制模式和扩展控制模式的功能。 The SXA006 may work in non-extended control mode (no serial interface) or extended control mode. Tables 16 and 17 describe the functions of Pins 3, 4, 14, and 127 in non-extended control mode and extended control mode, respectively.

a. 普通（非扩展）控制模式工作 / Normal (Non-Extended) Control Mode Operation

普通控制模式工作意思是串行接口无效以及所有控制功能都是由各种 pin 脚设置来控制，即满刻度范围、上电校正延迟、输出电压和输入耦合（a.c 或 d.c），通过设置 pin 脚 14 为高或低来选择非扩展控制模式，相反让其悬空。 Normal control mode operation means the serial interface is inactive and all control functions are controlled by the various pin settings — namely full-scale range, power-up calibration delay, output voltage, and input coupling (a.c. or d.c.). The non-extended control mode is selected by setting pin 14 high or low; making it floating selects the opposite.

表16 普通控制模式（Pin 14 为高或低）/ Table 16 Normal Control Mode (Pin 14 High or Low)

PIN	低电平 / Low Level	高电平 / High Level	悬空 / Floating
3	减小的输出幅度 / Reduced output amplitude	正常输出幅度 / Normal output amplitude	正常输出幅度 / Normal output amplitude
4	输出时钟下沿 / Output clock falling edge	输出时钟上沿 / Output clock rising edge	DDR 模式 / DDR mode
127	短的上电延迟 / Short power-up delay	长的上电延迟 / Long power-up delay	不用 / Not used
14	减小的输入幅度 / Reduced input amplitude	正常的输入幅 / Normal input amplitude	扩展控制模式 / Extended control mode

在扩展控制模式：Pin 脚 3 也可以为高或低；Pin 脚 14 必须悬空或 VCC/2；更多的信息看 1.2）普通/扩展控制。Pin 脚 4 在普通控制模式可以为高或为低或让其悬空；在普通控制模式，Pin 脚 4 高或低定义输出数据在输出时钟的那个边沿转换，更多信息看 2.4）.c 输出沿同步。如果这个 Pin 脚 4 悬空，输出时钟（QCLK）是一个 DDR（双数据率）时钟（看 1.1）.e.③双数据率），由于数据在 QCLK 的两个沿都输出，数据输出与输出时钟不同步。 In extended control mode: Pin 3 can also be high or low; Pin 14 must be floating or VCC/2; see 1.2) for more information. Pin 4 in normal control mode can be high, low, or floating; in normal control mode, Pin 4 high or low defines on which edge of the output clock the output data transitions; see 2.4).c for more

information. If Pin 4 is floating, the output clock (QCLK) is a DDR (double data rate) clock (see 1.1).e.③); because data is output on both edges of QCLK, the data output is not synchronized with the output clock.

Pin 脚 127 在普通控制模式设置校正延迟，此时 Pin 脚 127 不能悬空。 Pin 127 sets the calibration delay in normal control mode; at this time Pin 127 must not be floating.

表17 扩展控制模式（Pin 14 悬空或 VCC/2）/ Table 17 Extended Control Mode (Pin 14 Floating or VCC/2)

PIN	功能 / Function
3	SCLK（串行时钟）/ SCLK (serial clock)
4	DATA（串行数据）/ DATA (serial data)
127	ST2（反相）（串行接口选通）/ ST2 (inverted) (serial interface strobe)

2.10 通常应用容易犯的错误 / Common Application Mistakes

为了器件得可靠性，驱动输入（模拟或数字）不能远离电源电压。任何输入都不能低于地引脚 150mV 或高于电源电压引脚 150mV，即使是瞬态偏置也不能超出这些限制，否则不仅会造成器件性能变化，而且会降低器件的可靠性，对于高速数字电路低于地的过冲也是不行的。 For device reliability, the driving inputs (analog or digital) must not be far from the supply voltage. No input may be lower than 150mV below the ground pin or higher than 150mV above the supply voltage pin; even transient bias must not exceed these limits, otherwise it will not only cause device performance changes but also reduce device reliability. Undershoot below ground is also not acceptable for high-speed digital circuits.

在它们的特征阻抗中高速线的阻抗控制和这些线终端的阻抗都应控制其过冲。 The impedance control of high-speed lines in their characteristic impedance and the impedance of the terminations of these lines should both control their overshoot.

应该注意 SXA006 的输入驱动不要过压，否则会导致转换不正确，甚至导致器件损坏。 Care should be taken that the input drive of the SXA006 is not overvoltage; otherwise it will cause incorrect conversion, or even device damage.

在直流耦合模式错误的模拟输入共模电压。如 1.1）.d 模拟输入和 2.2）模拟输入部分描述，输入共模电压必须保持在 VCMO 输出的 50mV 内，且必须要跟踪随温度的变化，如果输入共模电压超过 VCMO±50mV，性能将会降低。 Incorrect analog input common-mode voltage in DC-coupled mode. As described in 1.1).d and 2.2), the input common-mode voltage must be kept within 50mV of the VCMO output and must track the variation with temperature; if the input common-mode voltage exceeds VCMO±50mV, performance will degrade.

用一个不适当的放大器驱动模拟输入。当选择一个高速放大器来驱动 SXA006 时要小心，因为许多高速放大器比 SXA006 的失真还高，会导致整个系统性能的降低。 Driving the analog input with an unsuitable amplifier. Care must be taken when selecting a high-speed amplifier to drive the SXA006, because many high-speed amplifiers have higher distortion than the SXA006, which will reduce the performance of the whole system.

过驱动 VREF 脚会改变参考电压。与在 2.1）参考电压中提到的一样，参考电压通过 FSR 脚固定或满刻度电压调节寄存器设置，过驱动这个脚虽不会改变满刻度值，但会使器件不正常工作。 Overdriving the VREF pin will change the reference voltage. As mentioned in 2.1), the reference voltage is fixed through the FSR pin or

set by the full-scale voltage adjustment register; although overdriving this pin will not change the full-scale value, it will cause the device to operate abnormally.

以一个非常高的电压信号驱动时钟输入。ADC 时钟输入电平不能超过推荐工作条件所描述的电平，也不能改变输入偏置。 Driving the clock input with a very high voltage signal. The ADC clock input level must not exceed the level described in the recommended operating conditions, and the input bias must not be changed.

不恰当的时钟输入电平。如 2.3）时钟输入描述，过低的时钟输入电平会导致性能变差，过高的时钟输入电平会引入输入失调。 Improper clock input level. As described in 2.3), an excessively low clock input level will cause performance to degrade, and an excessively high clock input level will introduce input offset.

用一个有过多抖动的时钟源，用一个非常长的输入时钟信号路径，或有其他信号耦合到输入时钟信号线上。这会导致采样间隔变化，导致过多输出噪声，降低 SNR 性能。 Using a clock source with excessive jitter, a very long input clock signal path, or other signals coupled onto the input clock signal line. This will cause sampling interval variation, resulting in excessive output noise and reduced SNR performance.

不能提供足够的散热。如 2.6）.b 热处理所描述，提供足够的散热对确保器件可靠性是很重要的，这可以通过足够的空气流动或用放在板上的一个简单散热装置来实现。为达到最好的性能，背面的焊盘应该接地。 Failure to provide sufficient heat dissipation. As described in 2.6).b, providing sufficient heat dissipation is important to ensure device reliability; this can be achieved by sufficient air flow or by a simple heat dissipation device placed on the board. For best performance, the pad on the back should be grounded.

---

14. 电源地间保护 / Power-to-Ground Protection

为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.6V，结构示意图如图 26 所示，上电及正常使用中应避免这些 ESD 保护管长时间正向导通，建议在使用时电源电压 VCC、VDD 同时上电或先上电 VCC 再上电 VDD。

To improve the anti-static capability of the device, ESD protection circuits exist between the various supply pins inside the device, as shown below. The forward conduction voltage drop of each ESD protection diode is approximately 0.6V; the structure is shown in Figure 26. Prolonged forward conduction of these ESD protection diodes should be avoided during power-up and normal use. It is recommended that, in use, the supply voltages VCC and VDD be powered up simultaneously, or VCC first and then VDD.

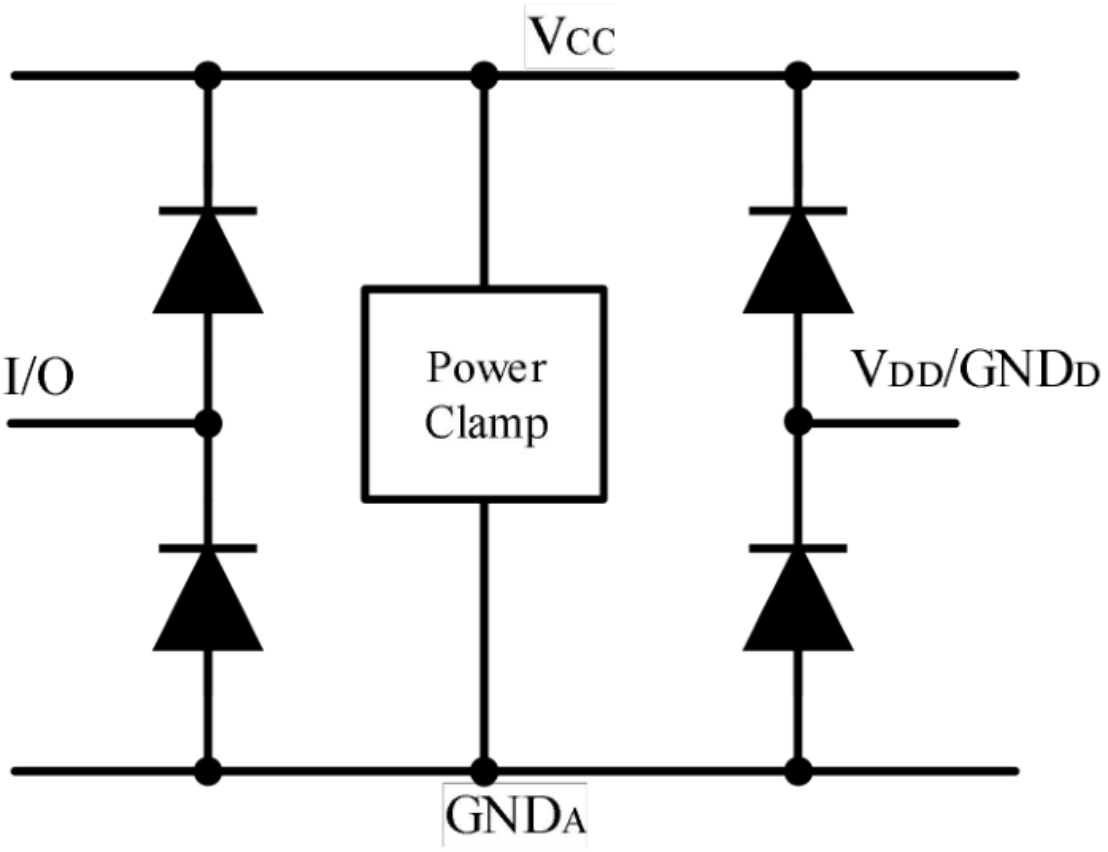


Figure 26: 内部电源间的 ESD 保护电路

15. 注意事项 / Cautions

1 产品安装注意事项 / Product Installation Cautions

1）上电要求：推荐模拟电源、输出驱动电源同时上电。 Power-up requirement: it is recommended that the analog supply and the output driver supply be powered up simultaneously. 2）安装时引线耐焊接温度不超过 300°C，10 秒钟。 During installation, the lead soldering temperature must not exceed 300°C for 10 seconds. 3）引脚间距小，注意不要焊接短路。 The pin pitch is small; take care to avoid solder shorts. 4）使用时推荐切脚长度 1～1.5 毫米，引脚太长后使动态性能下降。 In use, a trimmed lead length of 1–1.5 mm is recommended; excessively long pins degrade the dynamic performance.

2 产品使用注意事项 / Product Usage Cautions

1）引脚 32 外接电阻 Rext 必须精确等于 3300Ω±0.1%，其它值不能采用，1.1）.a 描述。 The external resistor Rext at pin 32 must be exactly 3300Ω±0.1%; no other value may be used. See 1.1).a. 2）应用中，建议 PCB 大面积接地。这样可以消除由于接地点的不同而可能存在的电位不同，同时可以降低电路板产生的电容对电路的影响。 In applications, a large-area PCB ground is recommended. This eliminates potential differences that may exist due to different ground points and reduces the influence of board-generated capacitance on the circuit. 3）使用时，切忌电路插反，否则可能导致电路损坏。 In use, never insert the circuit reversed; otherwise the circuit may be damaged. 4）每个电源引脚需要就近接 1 个 0.1μF 和 33μF 的电容。 Each supply pin requires one 0.1μF and one 33μF capacitor connected nearby. 5）差分模拟输入部分

走线必须等长。 The differential analog input routing must be of equal length. 6）数字电源和模拟电源需要分开。 The digital supply and analog supply must be separated. 7）本产品数据输出（DI、DId、DQ、DQd）、溢出输出（DOR）和数据时钟输出（QCLK）的同相/反相引出端与国外产品不一致，与进口器件是相反的。即在同一引出端下本器件为同相输出，进口器件为反相输出；反之，本器件为反相输出，进口器件为同相输出，这不影响使用。除这 3 类输出端外，其余与进口器件相同。如果要求输出端与进口器件 PIN 一致，则在本器件 SXA006 的输出端（数据输出、溢出输出和数据时钟输出）需接一个反相器，或者在 PFGA 中通过软件操作将接收的数据反相。 The in-phase/inverted pins of the data outputs (DI, DId, DQ, DQd), overflow output (DOR), and data clock output (QCLK) of this product are interchanged relative to the imported device. That is, at the same pin, where this device provides an in-phase output the imported device provides an inverted output, and vice versa; this does not affect use. Apart from these three classes of outputs, all others are the same as the imported device. If the outputs are required to be pin-identical to the imported device, an inverter must be connected at the outputs of the SXA006 (data outputs, overflow output, and data clock output), or the received data must be inverted by a software operation in the FPGA.

3 产品防护注意事项 / Product Protection Cautions

1）该电路所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 All pins of this circuit are designed with electrostatic protection structures; however, large-energy electric pulses may still damage the circuit, so electrostatic protection must be observed during testing, handling, and storage. 2）电路未剪短引脚时需用专用包装保存每一只电路，防止破坏电路外观 Before the leads are trimmed, each circuit must be stored in dedicated packaging to prevent damage to the circuit appearance.

4 电装说明 / Assembly Instructions

1）本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； This product has a moisture sensitivity level of MSL3. After removing the product from the moisture-barrier bag, dry storage, or baking, the allowable exposure time to the ambient environment before reflow soldering is: ≤30°C/60RH%, 168h. 2）若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； If device storage conditions cannot be controlled or traced, bake at 125°C for 8h strictly before assembly. 3）若电装环境温湿度无法保证 ≤30°C/60RH%，请在烘烤后 12h 内完成焊接； If the assembly environment cannot be guaranteed at ≤30°C/60RH%, complete soldering within 12h after baking. 4）产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； After baking, the product is highly susceptible to static electricity; ESD protection must be observed throughout all handling. 5）板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C–235°C, with maximum peak temperature not exceeding 235°C; dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60–90s, ramp-up rate 2–4°C/s, ramp-down rate 2–6°C/s. 6）板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C； For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C–245°C, with maximum peak temperature not exceeding 260°C; dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60–90s, ramp-up rate 2–4°C/s, ramp-down rate 2–6°C/s. 7）若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）； If a mixed assembly process requires higher temperatures, ensure the

device body temperature does not exceed 260°C (measured at the top surface of the device during reflow).
8）本产品引脚表面处理方式为电镀纯锡。 The pin surface finish of this product is electroplated pure tin.

---

16. 常见故障及处理办法 / Common Faults and Troubleshooting

1. 无输出信号：检查时钟引出端是否有时钟输入，检查电源、地信号连接是否正常，保证输入电压、基准电压准确； No output signal: check whether there is a clock input at the clock pin, check that the supply and ground signal connections are normal, and ensure the input voltage and reference voltage are accurate.
2. 输出数据抖动：检查外部电路和连接，保证基准电压稳定。 Output data jitter: check the external circuitry and connections, and ensure the reference voltage is stable.
3. 器件工作不稳定：检查电源，保证电源电压稳定。 Device operates unstably: check the power supply to ensure stable supply voltage.

---

17. 联系方式 / Contact

深圳市深信科技有限公司 / Shenzhen Shenxin Technology Co., Ltd.

- 联系人 / Contact: Felix (Flip) Lai, CEO
- 邮箱 / Email: felix@shenxinic.com
- 电话 / Tel: +852 51367095
- 官网 / Website: shenxinic.com

---

18. 附加说明 / Additional Notes

1. 本说明书首次发布日期：2026 年 7 月。 First publication date of this manual: July 2026.
2. 本产品状态：☑生产（该产品型号目前已在生产，可以提供正式产品）☐预发布（该产品型号尚未投入正式生产，可以提供样品） Product status: ☑Production (this model is currently in production; formal product available) ☐Pre-release (this model is not yet in formal production; samples available)
3. 引出端对比说明 / Pin comparison note:

本产品数据输出（DI、DId、DQ、DQd）、溢出输出（DOR）和数据时钟输出（QCLK）的同相/反相引出端与国外产品不一致，与进口器件是相反的。即在同一引出端下本器件为同相输出，进口器件为反相输出；反之，本器件为反相输出，进口器件为同相输出。其余引出端与国外产品相同，不影响使用。如果要求输出端与进口器件 PIN 一致，则在本器件 SXA006 的输出端（数据输出、溢出输出和数据时钟输出）需接一个反相器。 The in-phase/inverted pins of the data outputs (DI, DId, DQ, DQd), overflow output (DOR), and data clock output (QCLK) of this product are interchanged relative to the foreign product, i.e., opposite to the imported device. At the same pin, where this device provides an in-phase output the imported device provides an inverted output, and vice versa. All other pins are the same as the foreign product, and use is not affected. If the outputs are required to be pin-identical to the imported device, an inverter must be connected at the outputs of the SXA006 (data outputs, overflow output, and data clock output).

1. 替代进口器件情况说明 / Notes on substitution of imported devices:

1）绝对最大额定值对比 / Absolute maximum ratings comparison

附表1 绝对最大额定值对比 / Appendix Table 1 — Absolute Maximum Ratings Comparison

参数 / Parameter	SXA006	国外产品 / Foreign Product	比对结果 / Comparison
模拟电源电压 VCC / Analog supply voltage VCC	2.2V	2.2V	一致 / Consistent
输出驱动电压 VDD / Output driver voltage VDD	2.2V	2.2V	一致 / Consistent
电源电压差（VDD-VCC）/ Supply voltage difference (VDD−VCC)	0V～100mV	0V～100mV	一致 / Consistent
地电压差（|GNDA-GNDD|）/ Ground voltage difference (|GNDA−GNDD|)	0V～100mV	0V～100mV	一致 / Consistent
任一引脚的输入电流 / Input current at any pin	±25mA	±25mA	一致 / Consistent
任一引脚的输入电压 / Input voltage at any pin	-0.15V～VCC+0.15V，不能超过 2.2V / −0.15V to VCC+0.15V, not to exceed 2.2V	-0.15V～VCC+0.15V，不能超过 2.2V / −0.15V to VCC+0.15V, not to exceed 2.2V	一致 / Consistent
封装输入电流（除电源引脚外）/ Package input current (except supply pins)	±50mA	±50mA	一致 / Consistent
最大结温（TJ）/ Maximum junction temperature (TJ)	130°C	130°C	一致 / Consistent
ESD	2000V	2500V	有差异 / Different
贮存温度（Tstg）/ Storage temperature (Tstg)	-65°C~150°C	-65°C~150°C	一致 / Consistent
引线耐焊接温度（Th）（10s）/ Lead soldering temperature (Th) (10s)	300°C	300°C	一致 / Consistent
功耗 / Power dissipation	2.6W	2.2W	有差异 / Different

2）推荐工作条件对比 / Recommended operating conditions comparison

附表2 推荐工作条件对比 / Appendix Table 2 — Recommended Operating Conditions Comparison

参数 / Parameter	SXA006	国外产品 / Foreign Product	比对结果 / Comparison
模拟电源电压（VCC）/ Analog supply voltage (VCC)	1.95V～2.05V	1.8V~2.0V	有差异 / Different
输出驱动电压（VDD）/ Output driver voltage (VDD)	1.95～2.05V	1.8V~2.0V	有差异 / Different
模拟共模输入电压 / Analog common-mode input voltage	1.2V～1.33V	1.2V～1.33V	一致 / Consistent

参数 / Parameter	SXA006	国外产品 / Foreign Product	比对结果 / Comparison
模拟差分输入幅度（FSR 接地）/ Analog differential input amplitude (FSR grounded)	570～900mVpp	570～730mVpp	一致有差异
模拟差分输入幅度（FSR 接 VCC）/ Analog differential input amplitude (FSR at VCC)	790～1100mVpp	790～950mVpp	有差异 / Different
串行接口时钟输入频率 / Serial interface clock input frequency	100MHz	100MHz	一致 / Consistent
差分时钟输入幅度 / Differential clock input amplitude	0.5～2.0VPP	0.5～2.0VPP	一致 / Consistent
时钟输入占空比 / Clock input duty cycle	50%	50%	一致 / Consistent
工作环境温度 / Operating ambient temperature	-40°C～+85°C	-40°C～+85°C	有差异
|GNDA-GNDD|	0mV	0mV	一致 / Consistent

3）电特性对比 / Electrical characteristics comparison

附表3 电特性对比 / Appendix Table 3 — Electrical Characteristics Comparison

特性参数 / Characteristic	SXA006 最小 / Min	SXA006 典型 / Typ	SXA006 最大 / Max	国外产品最小 / Foreign Min	国外产品典型 / Foreign Typ	国外产品最大 / Foreign Max	单位 / Unit	对比结果 / Comparison
分辨率 / Resolution	—	8	—		8		Bits	一致 / Consistent
模拟电源电流 / Analog supply current	—	948	1000	—	770	870	mA	不一致 / Different
输出驱动电源电流 / Output driver supply current	—	248	300	—	207	290	mA	不一致 / Different
功耗 / Power dissipation	—	2.4	2.6	—	1.8	2.2	W	不一致 / Different
积分非线性误差 / INL	-1.2	±0.7	1.2	-0.9	±0.3	0.9	LSB	不一致 / Different
微分非线性误差 / DNL	-0.9	±0.5	1.0	-0.6	±0.15	0.6	LSB	不一致 / Different
失调误差 / Offset error	-2.5	±0.2	2.5	-1.5	-0.45	1.0	LSB	不一致 / Different
正满刻度误差 / Positive full-scale error	-40	20	40	-25	-0.60	25	mV	不一致 / Different
负满刻度误差 / Negative full-scale error	-40	20	40	-25	-1.31	25	mV	不一致 / Different
带隙基准输出电压 / Bandgap reference output voltage	1.2	1.28	1.33	1.2	1.26	1.33	V	一致 / Consistent
模拟差分输入电压（FSR(14 脚）接地）/ Analog differential input voltage (FSR (pin 14) grounded)	570	685	900	570	650	730	mV	不一致 / Different
模拟差分输入电压（FSR(14 脚）接 VCC）/ Analog differential input voltage (FSR (pin 14) at VCC)	790	905	1100	790	870	950	mV	不一致 / Different
模拟差分输入电阻 / Analog differential input resistance	94	102	106	94	102	106	Ω	一致 / Consistent
时钟差分输入电压 / Clock differential input voltage	0.5	1.2	2	0.5	1.2	2	V	一致 / Consistent
逻辑输入高电平 / Logic input high level	1.6	—	—	1.6	—	—	V	一致 / Consistent
逻辑输入低电平 / Logic input low level	—	—	0.3	—	—	0.3	V	一致 / Consistent
数字输出高电平 / Digital output high level	1.5	1.8	—	1.5	1.8	—	V	一致 / Consistent
数字输出低电平 / Digital output low level	—	0.1	0.3	—	0.1	0.3	V	一致 / Consistent
LVDS 差分输出电压（VOutv=1.6V，VREF 脚悬空）/ LVDS differential output voltage (VOutv=1.6V, VREF pin floating)	400	700	1000	400	710	920	mV	不一致 / Different
LVDS 差分输出电压（VOutv=0.3V，VREF 脚悬空）/ LVDS differential output voltage (VOutv=0.3V, VREF pin floating)	280	500	800	280	510	720	mV	不一致 / Different
溢出输出码（(VIN+-VIN-)＞正满度）/ Overflow output code ((VIN+−VIN−) > positive full scale)	255	—	—	255	—	—	—	一致 / Consistent
溢出输出码（(VIN+-VIN-)＜负满度）/ Overflow output code ((VIN+−VIN−) < negative full scale)	—	—	0	—	—	0	—	一致 / Consistent
增益平坦度 / Gain flatness	-1	0.7	1	-1	-	1	dBFS	一致 / Consistent
信噪比 / SNR	42	46.1	—	44.5	47	—	dB	不一致 / Different
有效位 / ENOB	6.6	7.3	—	7.0	7.4	—	Bits	不一致 / Different
信噪失真比 / SINAD	41.5	45.4	—	43.9	46.3	—	dB	不一致 / Different
无杂散动态范围 / SFDR	45	57.1	—	48.5	56	—	dB	不一致 / Different
总谐波失真 / THD	—	-57.2	-45	-	-54.5	-45	dB	不一致 / Different
双路合成信噪比 /								

Interleaved (DES) SNR | 34 | 41.0 | — | - | 45.5 | - | dB | 不一致 / Different | | 最大转换速率 / Maximum conversion rate | 1.5 | — | — | 1.5 | — | — | GSPS | 一致 / Consistent | | 输出时钟占空比 / Output clock duty cycle | 45 | 50 | 55 | 45 | 50 | 55 | % | 一致 / Consistent | | 时钟置位脉冲宽度 / Clock reset pulse width | 4 | — | — | 4 | — | — | Clock Cycles | 一致 / Consistent | | 校正控制低电平时间 / Calibration control low-level time | 80 | — | — | 80 | — | — | Clock Cycles | 一致 / Consistent | | 校正控制高电平时间 / Calibration control high-level time | 80 | — | — | 80 | — | — | Clock Cycles | 一致 / Consistent | | 校正周期时间 / Calibration cycle time | 80 | — | — | 80 | — | — | Clock Cycles | 一致 / Consistent | | 上电到开始校正延迟时间（CalDly = L） / Power-up to calibration-start delay (CalDly = L) | 225 | — | — | 225 | — | — | Clock Cycles | 一致 / Consistent | | 上电到开始校正延迟时间（CalDly = H） / Power-up to calibration-start delay (CalDly = H) | — | — | 231 | — | — | 231 | Clock Cycles | 一致 / Consistent | | 流水线延迟（DI 输出） / Pipeline latency (DI output) | — | 13 | — | — | 13 | — | Clock Cycles | 一致 / Consistent | | 流水线延迟（DId 输出） / Pipeline latency (DId output) | — | 14 | — | — | 14 | — | Clock Cycles | 一致 / Consistent | | 流水线延迟（DQ 输出，双通道） / Pipeline latency (DQ output, dual-channel) | — | 13 | — | — | 13 | — | Clock Cycles | 一致 / Consistent | | 流水线延迟（DQ 输出，DES 模式） / Pipeline latency (DQ output, DES mode) | — | 13.5 | — | — | 13.5 | — | Clock Cycles | 一致 / Consistent | | 流水线延迟（DQd 输出，双通道） / Pipeline latency (DQd output, dual-channel) | — | 14 | — | — | 14 | — | Clock Cycles | 一致 / Consistent | | 流水线延迟（DQd 输出，DES 模式） / Pipeline latency (DQd output, DES mode) | — | 14.5 | — | — | 14.5 | — | Clock Cycles | 一致 / Consistent |

4）寄存器对比 / Register comparison

附表4 寄存器对比表 / Appendix Table 4 — Register Comparison

参数 / Register	SXA006	国外产品 / Foreign Product	比对结果 / Comparison
0h	保留 / Reserved	保留 / Reserved	一致 / Consistent
1h	状态配置 / Status configuration	状态配置 / Status configuration	一致 / Consistent
2h	I 通道输入失调调节 / I-channel input offset adjustment	I 通道输入失调调节 / I-channel input offset adjustment	一致 / Consistent
3h	I 通道满刻度电压调节 / I-channel full-scale voltage adjustment	I 通道满刻度电压调节 / I-channel full-scale voltage adjustment	一致 / Consistent
4h	保留 / Reserved	保留 / Reserved	一致 / Consistent
5h	保留 / Reserved	保留 / Reserved	一致 / Consistent
6h	保留 / Reserved	保留 / Reserved	一致 / Consistent
7h	保留 / Reserved	保留 / Reserved	一致 / Consistent
8h	保留 / Reserved	保留 / Reserved	一致 / Consistent
9h	保留 / Reserved	保留 / Reserved	一致 / Consistent
Ah	Q 通道输入失调调节 / Q-channel input offset adjustment	Q 通道输入失调调节 / Q-channel input offset adjustment	一致 / Consistent
Bh	Q 通道满刻度电压调节 / Q-channel full-scale voltage adjustment	Q 通道满刻度电压调节 / Q-channel full-scale voltage adjustment	一致 / Consistent
Ch	保留 / Reserved	保留 / Reserved	一致 / Consistent
Dh	DES 使能 / DES enable	DES 使能 / DES enable	一致 / Consistent
Eh	DES 粗调节 / DES coarse adjustment	DES 粗调节 / DES coarse adjustment	一致 / Consistent

参数 / Register	SXA006	国外产品 / Foreign Product	比对结果 / Comparison
Fh	DES 细调节 / DES fine adjustment	DES 细调节 / DES fine adjustment	一致 / Consistent

5）其它指标对比 / Other parameters comparison

附表5 其它指标对比 / Appendix Table 5 — Other Parameters Comparison

参数 / Parameter	SXA006	国外产品 / Foreign Product	比对结果 / Comparison
封装形式 / Package	LQFP128，塑封 / LQFP128, plastic	LQFP，塑封 / LQFP, plastic	不一致 / Different
质量等级 / Quality grade	企标 / Enterprise standard	工业级 / Industrial	不一致 / Different
尺寸 / Dimensions	20mm×20mm×1.6mm	20mm×20mm×1.4mm	不一致 / Different
替代建议 / Substitution recommendation	□直接替代 □有效替代 ☑功能替代 / □Drop-in □Effective ☑Functional alternative		

© 2026 深圳市深信科技有限公司 / Shenzhen Shenxin Technology Co., Ltd.