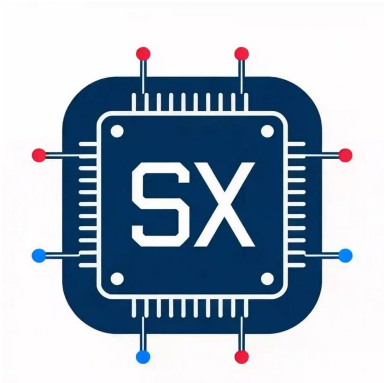


SXA009

Quad 16-Bit, 125 MSPS A/D Converter

四通道 16 位 125MSPS A/D 转换器

16-bit | 4 channels | 125 MSPS | QFN56 | JESD204B

16位 | 四通道 | 125MSPS | QFN56 | JESD204B

对标 / Cross Reference: AD9656 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXA009 Datasheet / 数据手册

Shenzhen Shenxin Technology Co., Ltd. / 深圳市深信科技有限公司

SXA009 16-bit Quad 125MSPS A/D Converter — Product Datasheet / User Manual

SXA009 型四通道 16 位 125MSPS A/D 转换器产品说明书、使用手册

- **Model / 型号**: SXA009
- **Revision / 版本**: V1.20260727
- **Cross Reference / 对标型号**: AD9656 — pin-to-pin compatible alternative
- **Contact / 联系方式**: Felix (Flip) Lai, CEO — felix@shenxinic.com — +852 51367095 — shenxinic.com

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- Additional Notes / 附加说明

Revision History / 版本修订记录

Version / 版本号	Release Date / 发布日期	Changed Sections / 更改章节	Description of Change / 更改说明	Remarks / 备注
V1.20260727	20260727	——	Initial release / 首次发布	

Product Applications and Scope / 产品用途及应用范围

- Medical imaging / 医疗成像
- High-speed imaging / 高速成像
- Radio receivers / 无线电接受机
- Portable measurement equipment / 便携式测量设备

Standards / 标准

- Detailed specification and approval number: Q/GC 0217-2026, 《半导体集成电路 SXA009 型四通道 16 位 125MSPS A/D 转换器详细规范》 (Detailed Specification for SXA009 4-Channel 16-bit 125MSPS A/D Converter Semiconductor Integrated Circuit)
- 详细规范及确认号：Q/GC 0217-2026《半导体集成电路 SXA009 型四通道 16 位 125MSPS A/D 转换器详细规范》
- Quality grade: Enterprise standard / 质量等级：企标

Features / 产品特点

- Supply voltage: 1.8V / 电源电压包括：1.8V
- Resolution: 16bit / 分辨率：16bit
- Number of channels: 4 / 通道数：4 通道
- Conversion rate: 125MSPS / 转换速率：125MSPS
- SNR: 76dBFS@9.7M (typical) / SNR：76dBFS@9.7M（典型值）
- SFDR: 88dBc@9.7M (typical) / SFDR：88dBc@9.7M（典型值）
- DNL: ±0.5LSB (typical) / DNL：±0.5LSB（典型值）
- INL: ±6LSB (typical) / INL：±6LSB（典型值）
- Power consumption: ≤0.839W (typical 0.71W) / 功耗：≤0.839W（典型值 0.71W）
- Input data interface: JESD204B / 输入数据接口：JESD204B
- ESD rating: Class 1C, HBM model: 1000V / ESD 等级：1C 级，HBM 模型：1000V
- Product weight: 0.17g±0.04g / 产品重量：0.17g±0.04g

Product Description / 产品描述

SXA009 is a 4-channel, 16-bit, 125 MSPS analog-to-digital converter (ADC), developed and designed specifically for low power consumption, small size and application flexibility. The device supports conversion rates up to 125 MSPS, with excellent dynamic performance and ultra-low power consumption, suitable for a wide range of application scenarios.

SXA009 是一款 4 通道，16 位，125 MSPS 采样率的模数转换器(Analog-to-Digital Converter，ADC)，专门针对低功耗、小尺寸和使用灵活性进行开发设计。该产品转换速率最高可达到 125 MSPS，具有优异的动态性能和超低功耗特性，适用多种应用场景。

The ADC operates from a single 1.8 V supply with LVPECL/CMOS/LVDS-compatible sampling clock signals. No external reference voltage source or driver is required.

该 ADC 采用 1.8 V 单电源供电和 LVPECL/CMOS/LVDS 兼容型采样时钟信号。无需外部基准电压源和驱动器即可满足需求。

It supports independently powering down each internal channel; with all channels disabled, typical power consumption is less than 14mW. The ADC integrates multiple functions, including programmable clock output, data alignment, and digital test pattern generation. Available digital test patterns include: built-in fixed test patterns and pseudo-random test patterns, and user-defined test patterns via the serial port interface (SPI).

支持独立关闭内部各通道功能；禁用全部通道后，典型功耗小于 14mW。该 ADC 内置多种功能，包括可编程时钟输出、数据对齐、生成数字测试码等。可获得的数字测试码包括：内置固定测试码和伪随机测试码，也支持用户通过串行端口接口(SPI)自定义测试码的方式。

The device is offered in a 56-pin package (QFN56).

该产品采用 56 引脚封装（QFN56）。

The functional block diagram of the device is shown in Figure 1.

该产品功能框图如图 1 所示。

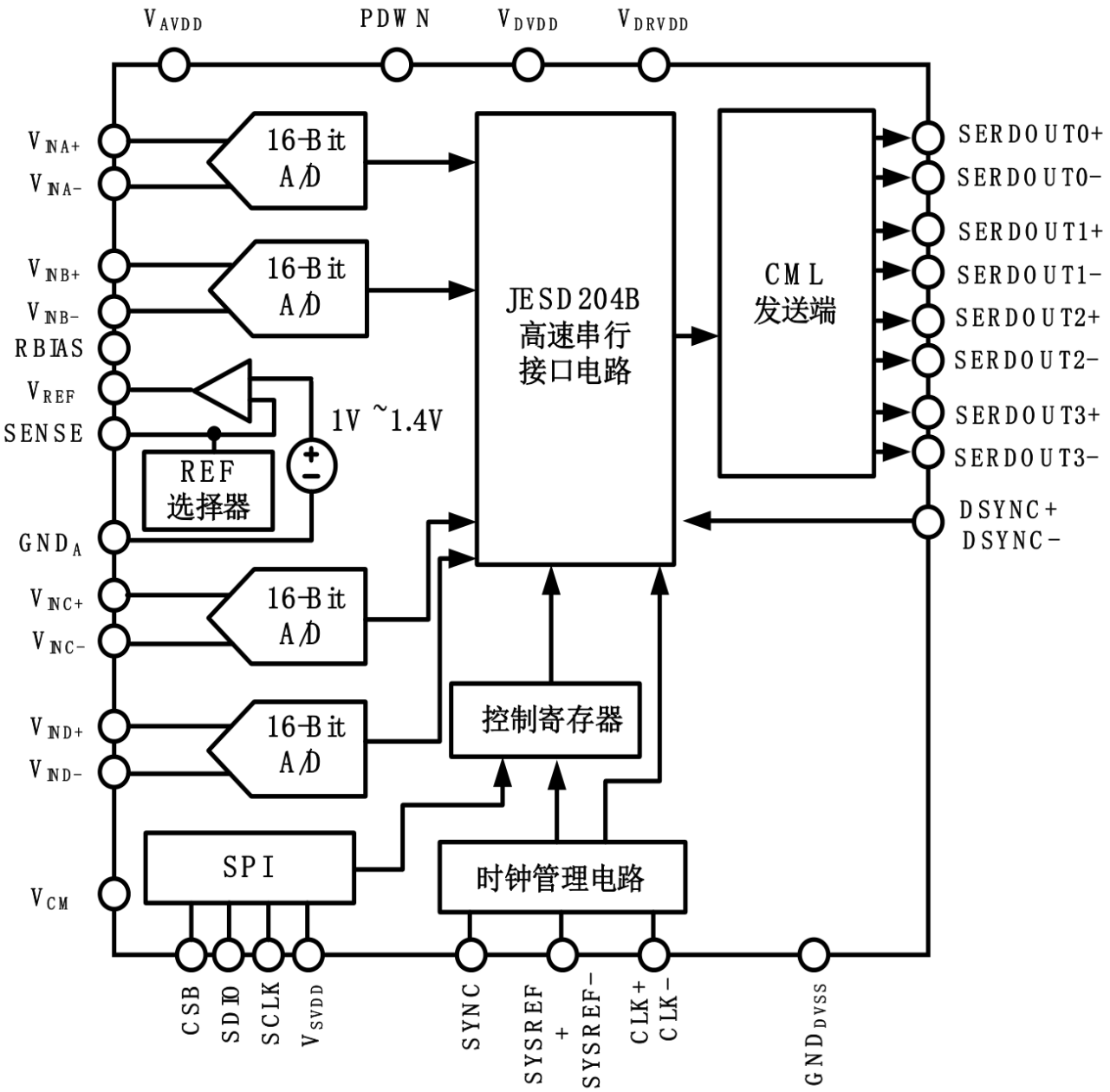


Figure 1: SXA009 functional block diagram

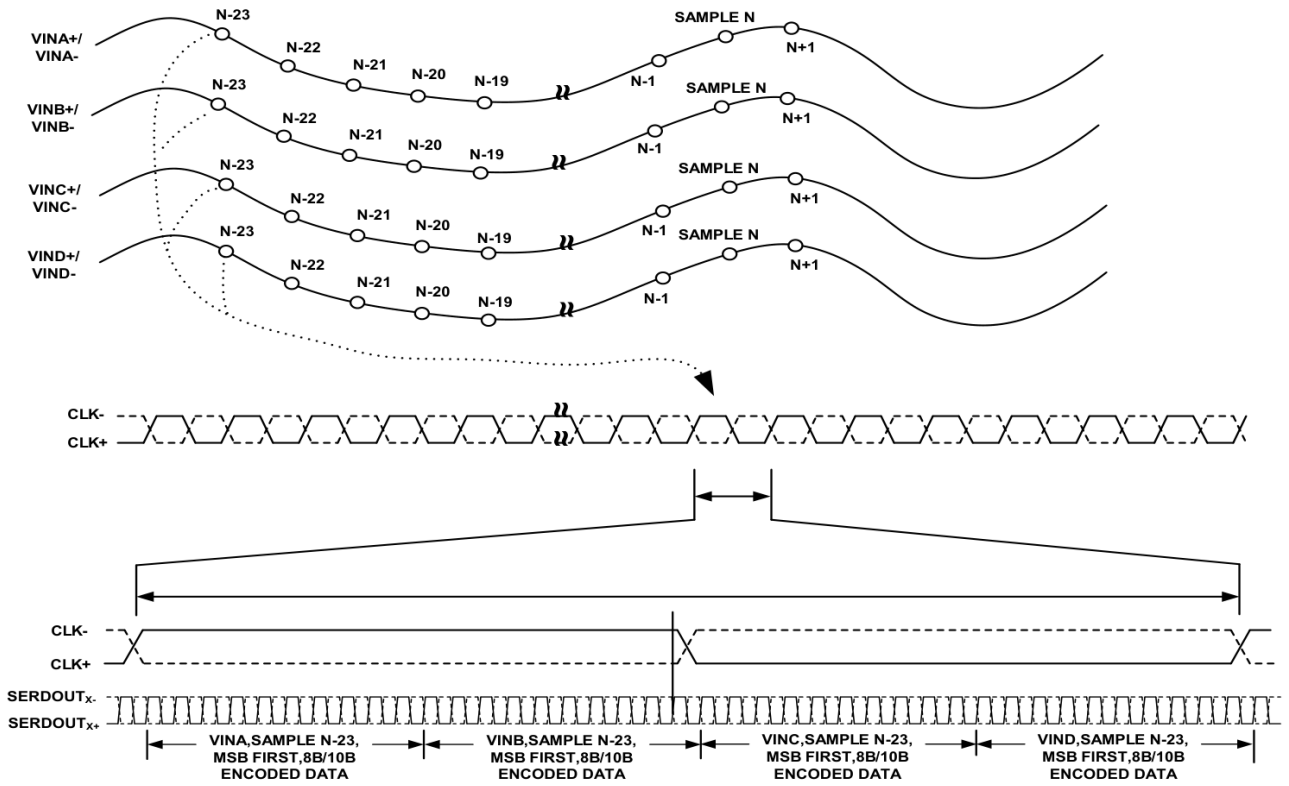


Figure 2: Serial interface timing

Package Outline and Physical Picture / 产品外形图和实物图片

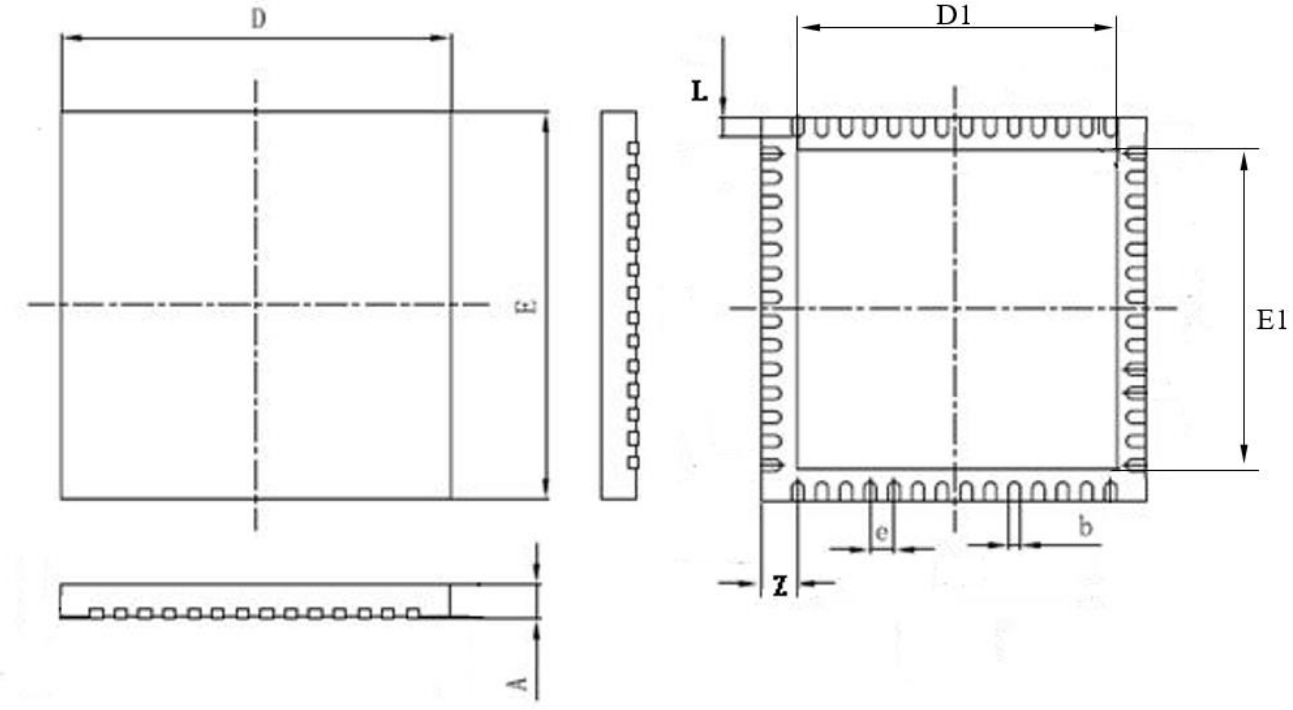


Figure 3: Package outline dimension drawing

Dimensions in millimeters. / 单位为毫米

Dimension Symbol / 尺寸符号	Value / 数值			Dimension Symbol / 尺寸符号	Value / 数值		
	Min / 最小	Nom / 公称	Max / 最大		Min / 最小	Nom / 公称	Max / 最大
A	0.70	0.75a	0.80	E	7.90	8.00a	8.10
b	0.18	0.25a	0.30	D	7.90	8.00a	8.10
e	—	0.50a	—	L	0.35	0.40a	0.45
D1	6.55	6.65a	6.75	Z	—	0.75a	0.80
E1	6.55	6.65a	6.75				

a: Actual nominal package value; users are recommended to refer to these dimensions for design. / a 外壳实际公称值，推荐用户参考该尺寸设计使用；

Note: For recommended pad layout, see the assembly instructions. / 注：推荐焊盘设计详见电装说明。

Pin Arrangement (Top View) / 引出端排列（俯视图）

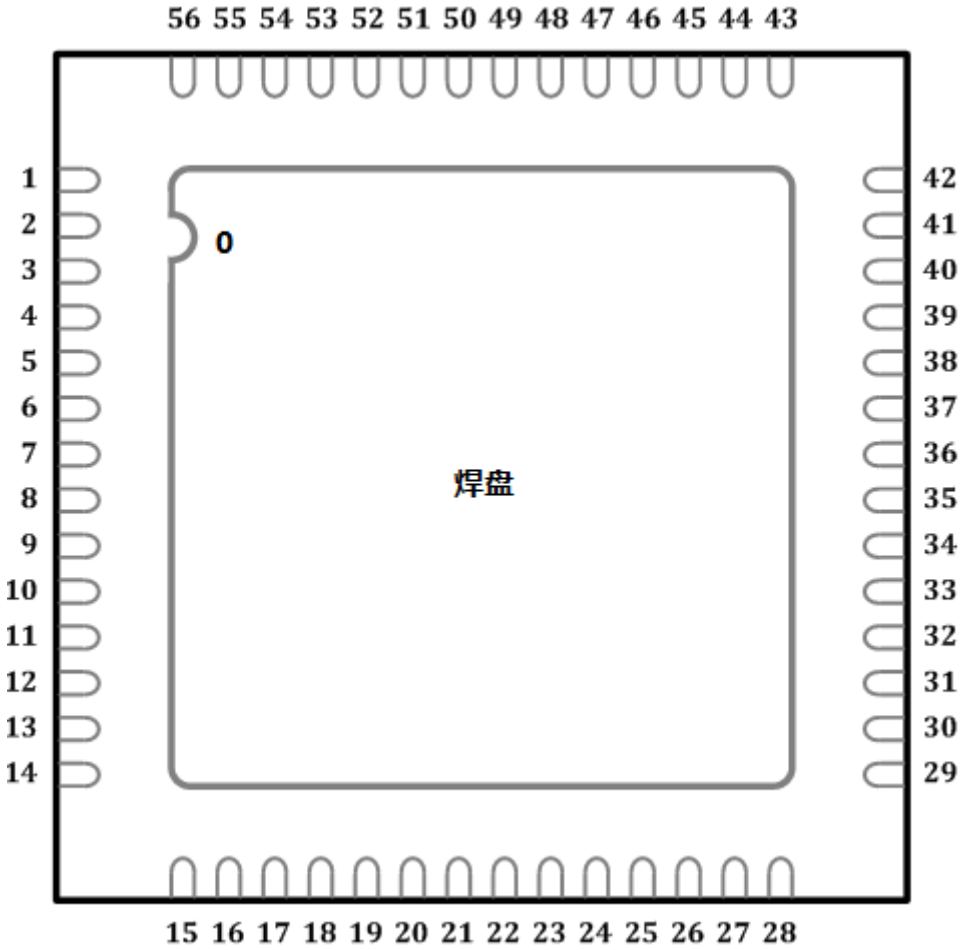


Figure 4: Pin arrangement

Pin Function Symbol Table / 引出端功能符号表

Pin No. / 引出端号	Symbol / 符号	Name / 名称	I/O
0	GNDA	Analog ground / 模拟地	/
1	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
2	VIND+	ADC channel D analog input (+) / ADC D 通道模拟输入(+)	I
3	VIND-	ADC channel D analog input (−) / ADC D 通道模拟输入(−)	I
4	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
5	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
6	CLK−	Differential clock (−) / 差分时钟(−)	I
7	CLK+	Differential clock (+) / 差分时钟(+)	I
8	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
9	DSYSREF+	JESD204B LVDS SYSREF low-level input active (+) / JESD204B LVDS SYSREF 低电平输入有效(+)	I
10	DSYSREF−	JESD204B LVDS SYSREF low-level input active (−) / JESD204B LVDS SYSREF 低电平输入有效(−)	I
11	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
12	VDVDD	Digital supply pin / 数字电源引脚	/
13	GNDDVSS	Digital ground pin / 数字地引脚	/
14	NIC	No connect / 空	/
15	NIC	No connect / 空	/
16	DSYNC+	JESD204B LVDS SYNC low-level input active (+) / JESD204B LVDS SYNC 低电平输入有效(+)	I
17	DSYNC−	JESD204B LVDS SYNC low-level input active (−) / JESD204B LVDS SYNC 低电平输入有效(−)	I
18	VDRVDD	Digital output driver supply pin / 数字输出驱动电源引脚	/
19	SEROUT3−	Lane3 digital output (−) / Lane3 数字输出(−)	O
20	SEROUT3+	Lane3 digital output (+) / Lane3 数字输出(+)	O
21	SEROUT2+	Lane2 digital output (+) / Lane2 数字输出(+)	O
22	SEROUT2−	Lane2 digital output (−) / Lane2 数字输出(−)	O
23	VDRVDD	Digital output driver supply pin / 数字输出驱动电源引脚	/
24	SEROUT1−	Lane1 digital output (−) / Lane1 数字输出(−)	O
25	SEROUT1+	Lane1 digital output (+) / Lane1 数字输出(+)	O
26	SEROUT0+	Lane0 digital output (+) / Lane0 数字输出(+)	O
27	SEROUT0−	Lane0 digital output (−) / Lane0 数字输出(−)	O
28	VDRVDD	Digital output driver supply pin / 数字输出驱动电源引脚	/
29	NIC	No connect / 空	/
30	NIC	No connect / 空	/
31	GNDDVSS	Digital ground pin / 数字地引脚	/
32	VDVDD	Digital supply pin / 数字电源引脚	/

Pin No. / 引出端号	Symbol / 符号	Name / 名称	I/O
33	VSVDD	SPI supply pin / SPI 电源引脚	/
34	DNC	Do not connect; do not connect this pin / 不连接，请勿连接该引脚	/
35	SCLK	SPI clock input / SPI 时钟输入	I
36	SDIO	SPI data input and output / SPI 数据输入和输出	I
37	CSB	SPI chip select, active low, with internal 30kΩ pull-up resistor / SPI 片选信号，低电平有效使能，内置 30kΩ 上拉电阻	I
38	PDWN	Digital input (high level = power-down; low level = operating) / 数字输入(高电平=关断；低电平=工作)	I
39	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
40	VINA−	ADC channel A analog input (−) / ADC A 通道模拟输入(−)	I
41	VINA+	ADC channel A analog input (+) / ADC A 通道模拟输入(+)	I
42	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
43	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
44	VINB+	ADC channel B analog input (+) / ADC B 通道模拟输入(+)	I
45	VINB−	ADC channel B analog input (−) / ADC B 通道模拟输入(−)	I
46	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
47	RBIAS	Analog circuit bias / 模拟电路偏置	I
48	SENSE	Reference voltage mode select / 基准电压模式选择	I
49	VREF	Reference voltage input and output pin / 基准电压输入和输出引脚	O
50	VCM	Analog input common-mode voltage / 模拟输入共模电压	O
51	SYNC	Digital input, synchronization input for clock divider / 数字输入，时钟分频器的同步输入	I
52	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
53	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/
54	VINC−	ADC channel C analog input (−) / ADC C 通道模拟输入(−)	I
55	VINC+	ADC channel C analog input (+) / ADC C 通道模拟输入(+)	I
56	VAVDD	1.8V analog supply pin / 1.8V 模拟电源引脚	/

Note: The thermal pad at the bottom of the package is analog ground GNDA. / 注：封装底部的热沉焊盘为模拟地端 GNDA。

Absolute Maximum Ratings / 绝对最大额定值

- Analog supply voltage (VAVDD): 2V / 模拟电源电压（VAVDD）：2V
- Digital supply voltage (VDVDD): 2V / 数字电源电压（VDVDD）：2V
- Storage temperature (Tstg): −65°C~150°C / 贮存温度（Tstg）：-65°C~150°C
- Junction temperature (TJ): 150°C / 结温（TJ）：150°C

Recommended Operating Conditions / 推荐工作条件

- Operating frequency (fCLK): 40MHz~125MHz / 工作频率（fCLK）：40MHz~125MHz
- Analog supply voltage (VAVDD): 1.75V~1.9V / 模拟电源电压（VAVDD）：1.75V~1.9V
- Digital supply voltage (VDVDD): 1.75V~1.9V / 数字电源电压（VDVDD）：1.75V~1.9V
- Input signal amplitude range (peak-to-peak): ≤2V / 输入信号幅度范围（峰峰值）：≤2V
- Analog input common-mode voltage (VCM): 0.5V~1.3V / 模拟输入共模电压（VCM）：0.5V~1.3V
- Operating ambient temperature (TA): −40°C~85°C / 工作环境温度（TA）：-40°C~85°C

Performance Specifications / 性能指标

Test conditions (unless otherwise specified): VPP=2.0V, VAVDD=VDVDD=VSVDD=VDRVDD=1.8V, GNDA=GNDDVSS=0V, −40°C≤TA≤85°C.

条件（除另有规定外，VPP=2.0V，VAVDD=VDVDD=VSVDD=VDRVDD=1.8V，GNDA=GNDDVSS=0V，-40°C≤TA≤85°C。）

Parameter / 参数	Symbol / 符号	Conditions / 条件	Min / 最小值	Typ / 典型值	Max / 最大值	Unit / 单位
Resolution / 分辨率	RES			16		bits
Number of channels / 通道数	—			4		—
Differential nonlinearity error / 微分线性误差	EDL	fIN=10MHz	−0.99	−0.5/+0.5	+0.99	LSB
Integral nonlinearity error / 积分非线性误差	EIL	fIN=10MHz	−11	−6/+6	+11	LSB
Power consumption / 功耗	PW	Four channels / 四通道	—	710	839	mW
Conversion rate / 转换率	SR		40 a	125	125	MSPS
Signal-to-noise ratio / 信噪比	SNR	−1dBFS, fIN=10MHz	72	76	—	dBFS
		−1dBFS, fIN=128MHz	69	72	—	dBFS
Signal-to-noise and distortion ratio / 信噪失真比	SINAD	−1dBFS, fIN=10MHz	71	75	—	dBFS
		−1dBFS, fIN=128MHz	68	71	—	dBFS
Effective number of bits / 有效位	ENOB	−1dBFS, fIN=10MHz	11.5	12.3		bits
		−1dBFS, fIN=128MHz	11	11.6		bits
Spurious-free dynamic range / 无杂散动态范围	SFDR	−1dBFS, fIN=10MHz	78	88	—	dBFS
		−1dBFS, fIN=128MHz	74	80	—	dBFS

a: The 40MSPS conversion rate is only sampled in Group A inspection 3(0) during initial qualification and when design or process changes. / a 转换率 40MSPS 仅在首次鉴定和设计、工艺发生更改时在 A 组检验中抽测 3（0）。

Note: Typical values are room-temperature test data. / 注：典型值为常温测试数据

Typical Performance Curves / 主要特性曲线图（电特性测试图）

VREF = 1.4 V

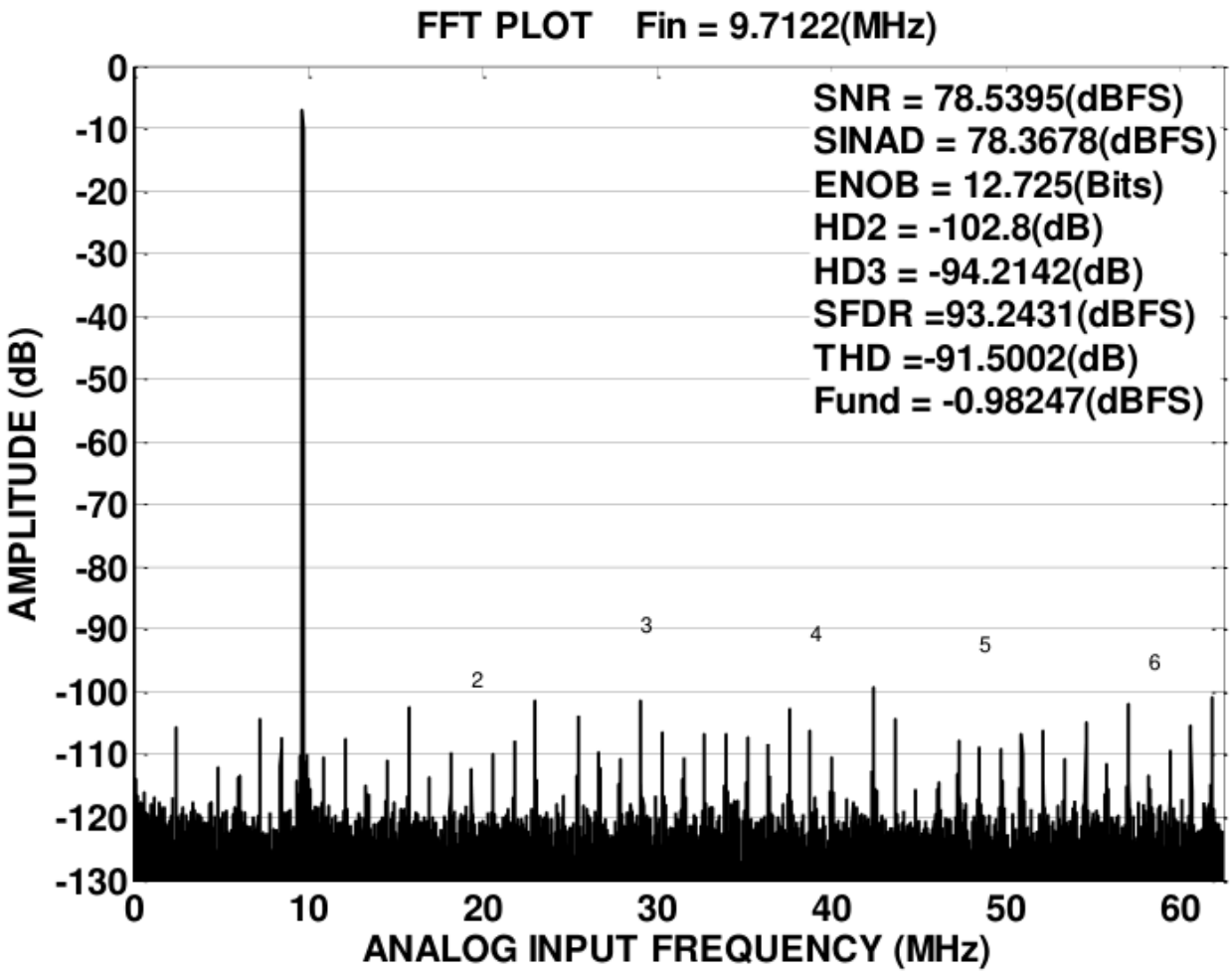


Figure 5: Single-tone 32K FFT plot (fIN=9.7MHz, fS=125MSPS), SNR=78.5395dBFS, SINAD=78.3678dBFS, ENOB=12.725Bits, SFDR=93.2431dBFS

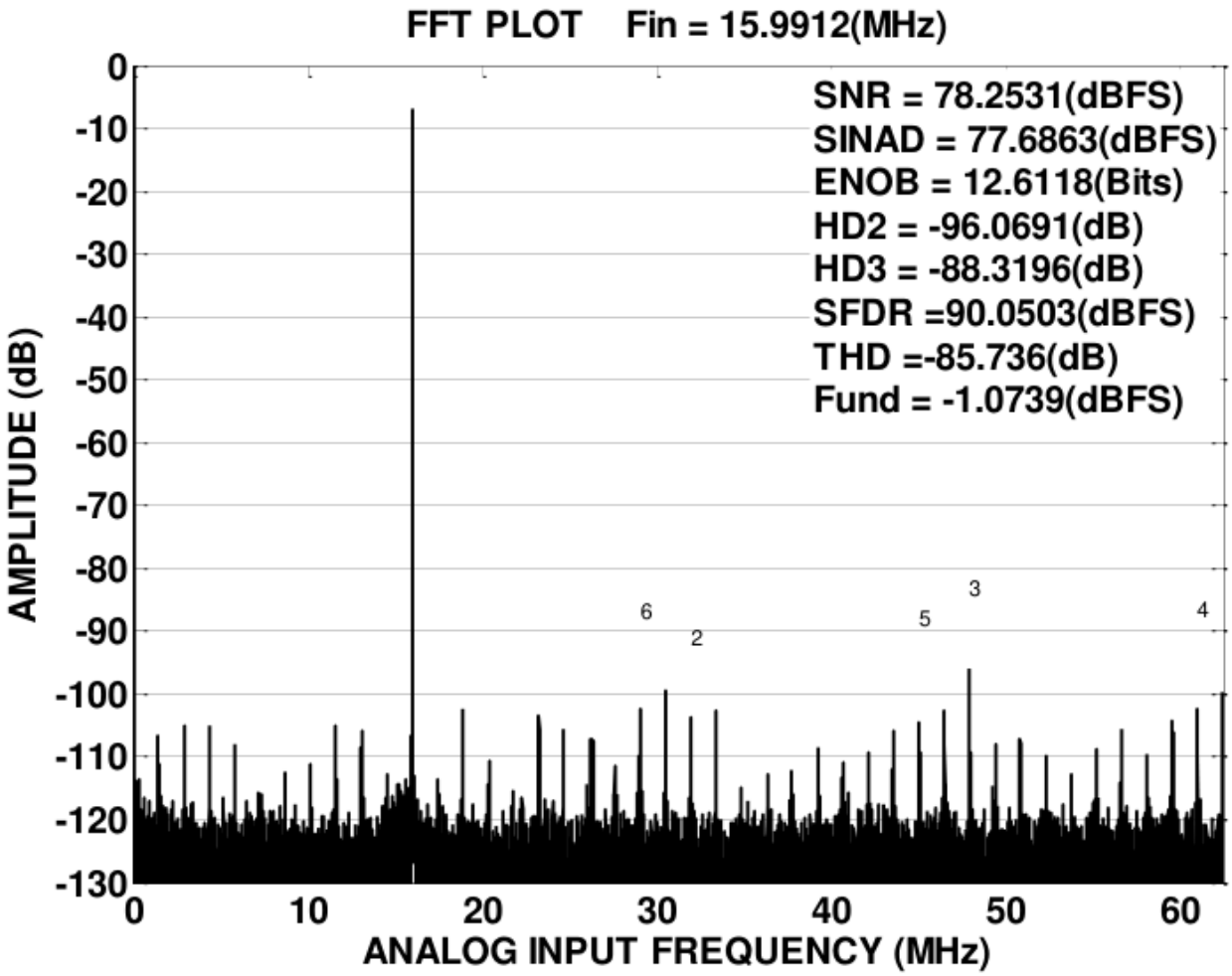


Figure 6: Single-tone 32K FFT plot (fIN=16MHz, fS=125MSPS), SNR=78.2531dBFS, SINAD=77.6863dBFS, ENOB=12.6118Bits, SFDR=90.0503dBFS

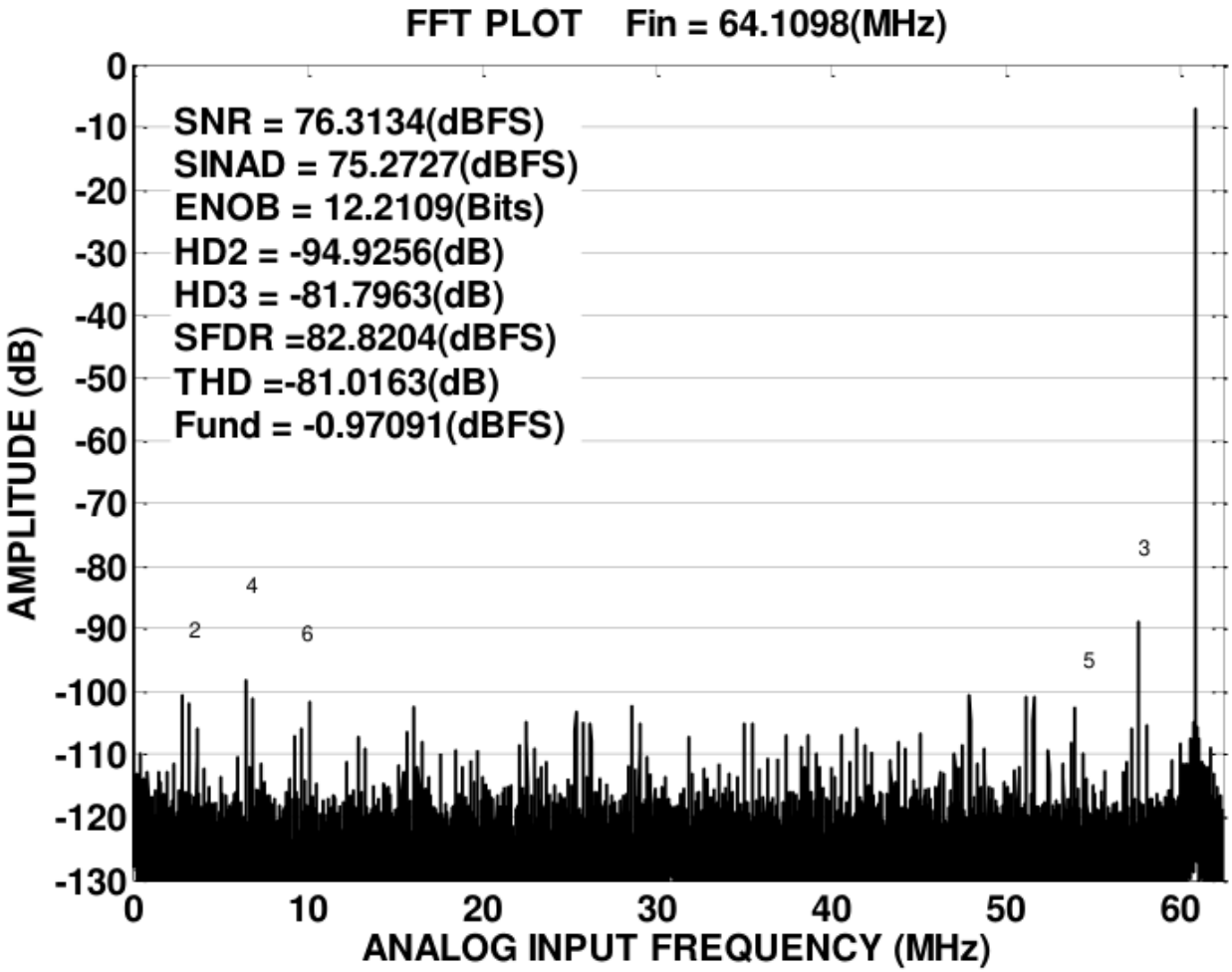


Figure 7: Single-tone 32K FFT plot (fIN=64MHz, fS=125MSPS), SNR=76.3134dBFS, SINAD=75.2727dBFS, ENOB=12.2109Bits, SFDR=82.8204dBFS

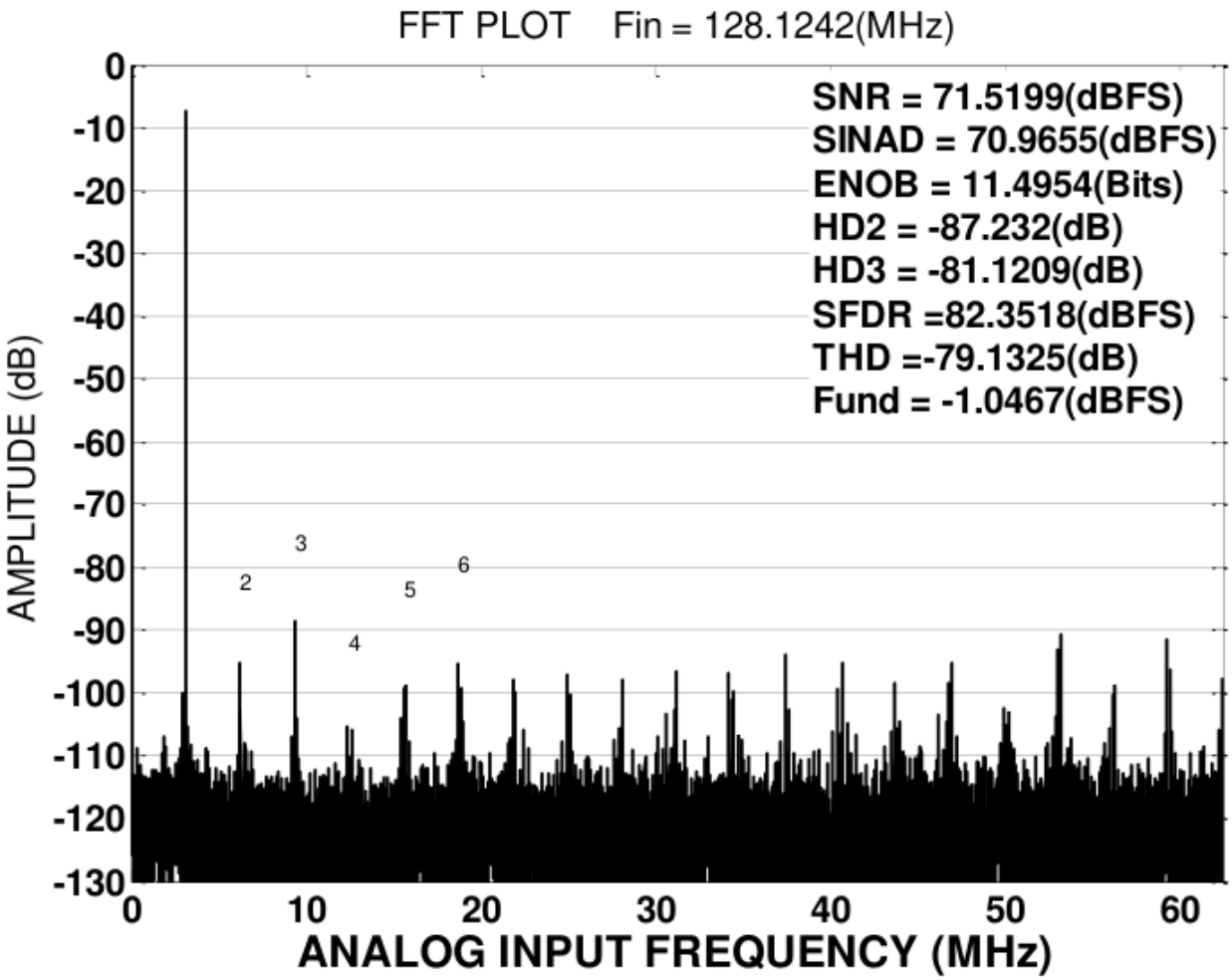


Figure 8: Single-tone 32K FFT plot (fIN=128MHz, fS=125MSPS), SNR=71.5199dBFS, SINAD=70.9653dBFS, ENOB=11.4954Bits, SFDR=82.3518dBFS

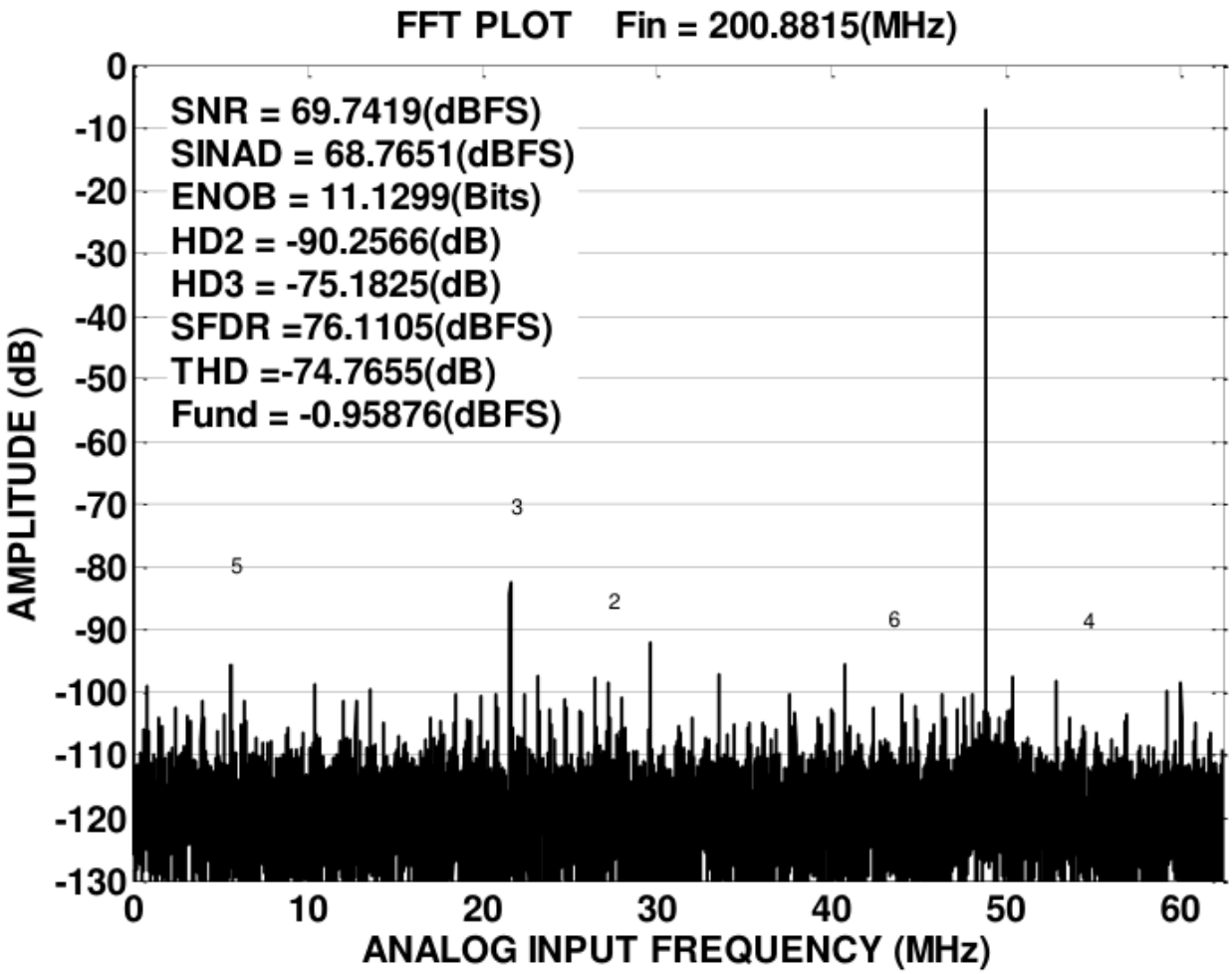


Figure 9: Single-tone 32K FFT plot (fIN=201MHz, fS=125MSPS), SNR=69.7419dBFS, SINAD=68.7651dBFS, ENOB=11.1299Bits, SFDR=76.1105dBFS

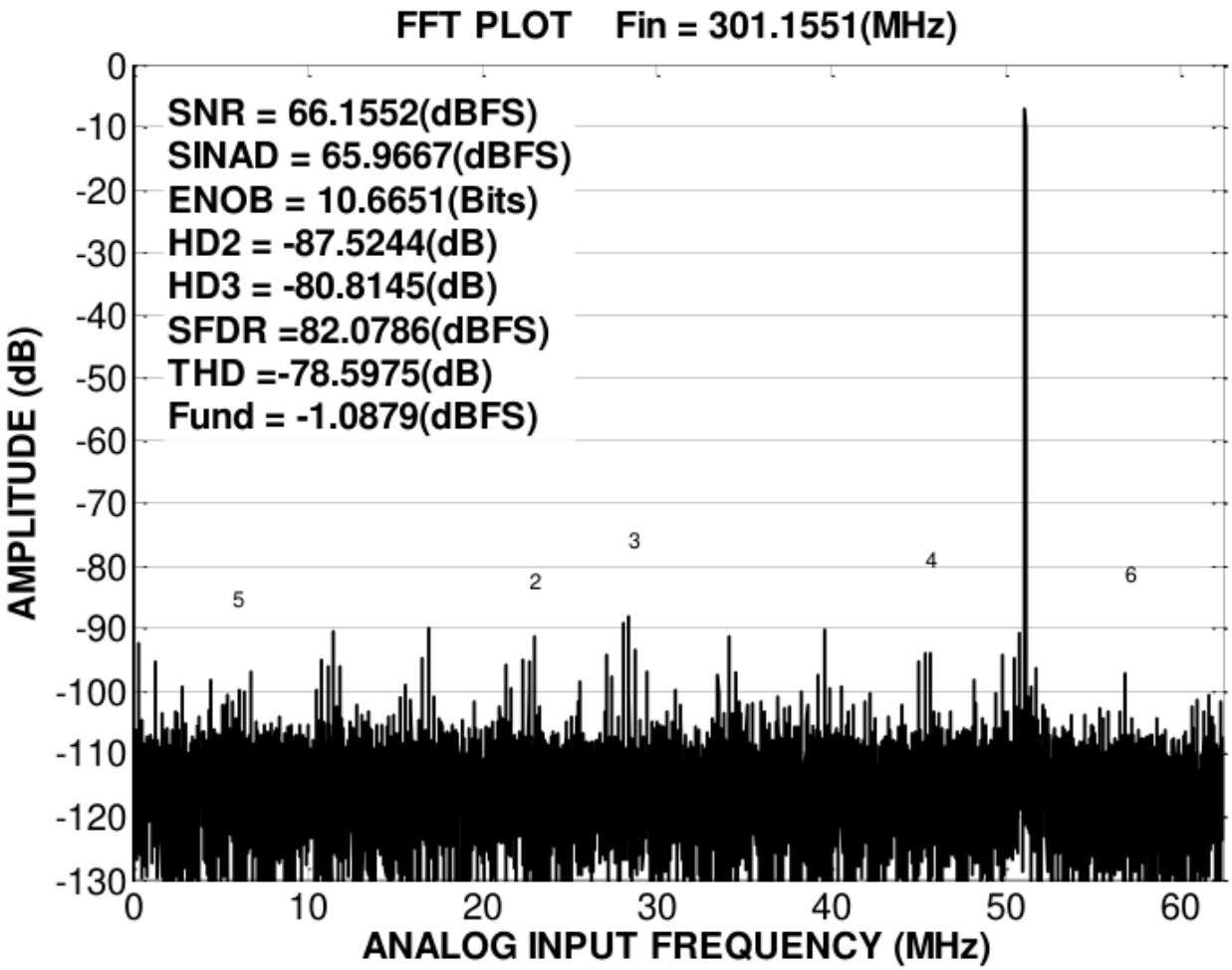


Figure 10: Single-tone 32K FFT plot (fIN=301MHz, fS=125MSPS), SNR=66.1552dBFS, SINAD=65.9667dBFS, ENOB=10.6651Bits, SFDR=82.0786dBFS

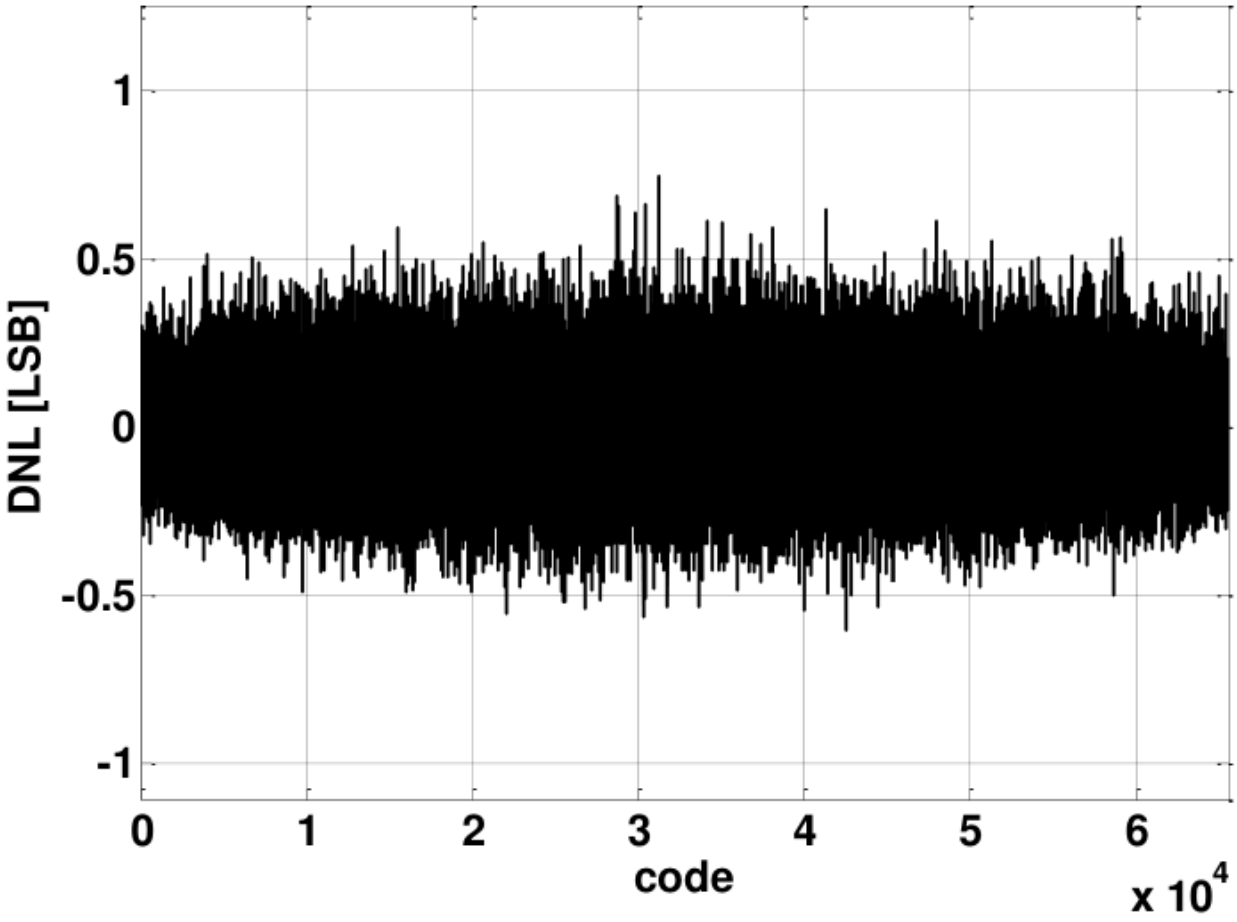


Figure 11: Differential nonlinearity DNL (fIN=9.7MHz, fS=125MSPS)

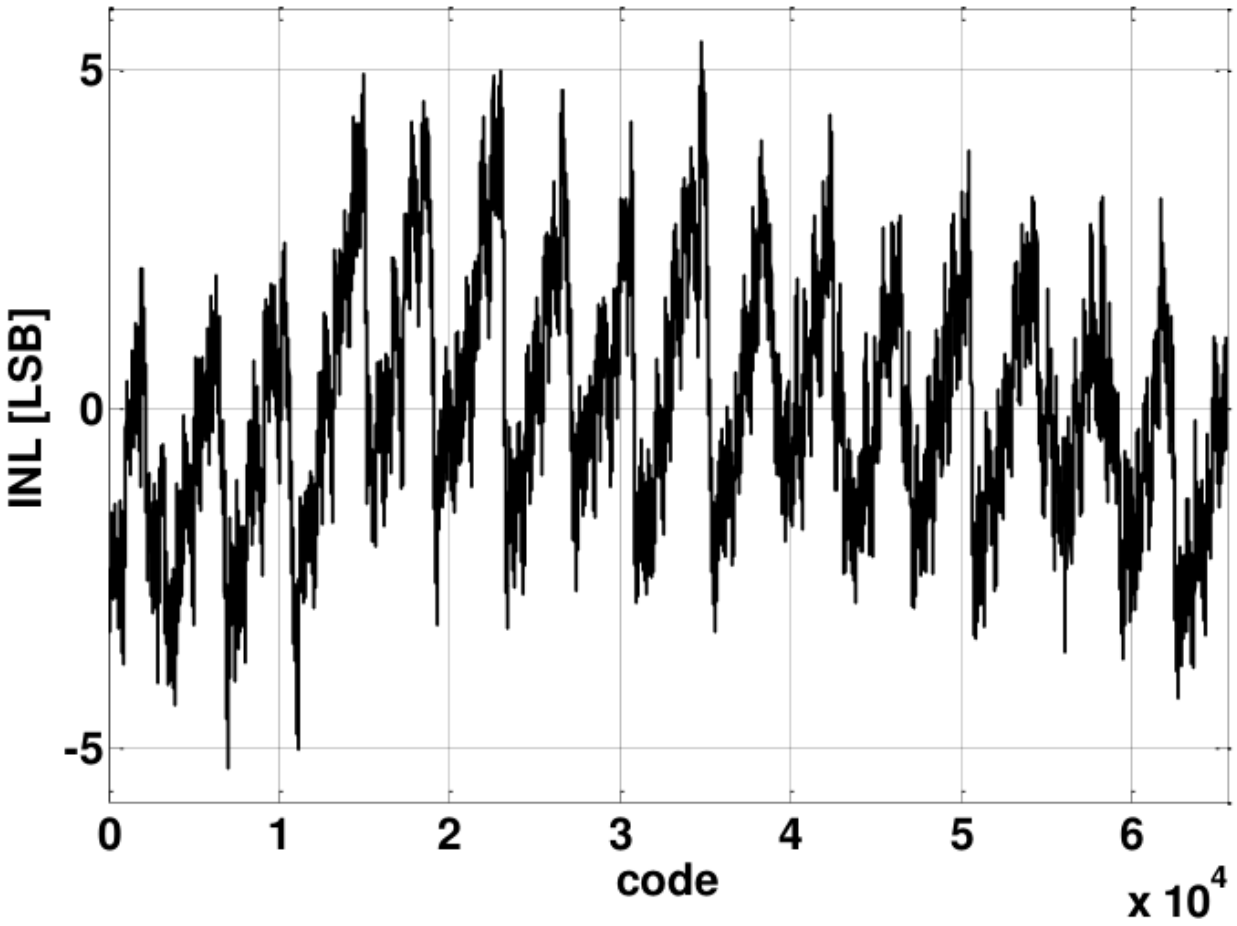


Figure 12: Integral nonlinearity INL (fIN=9.7MHz, fS=125MSPS)

VREF = 1.0 V

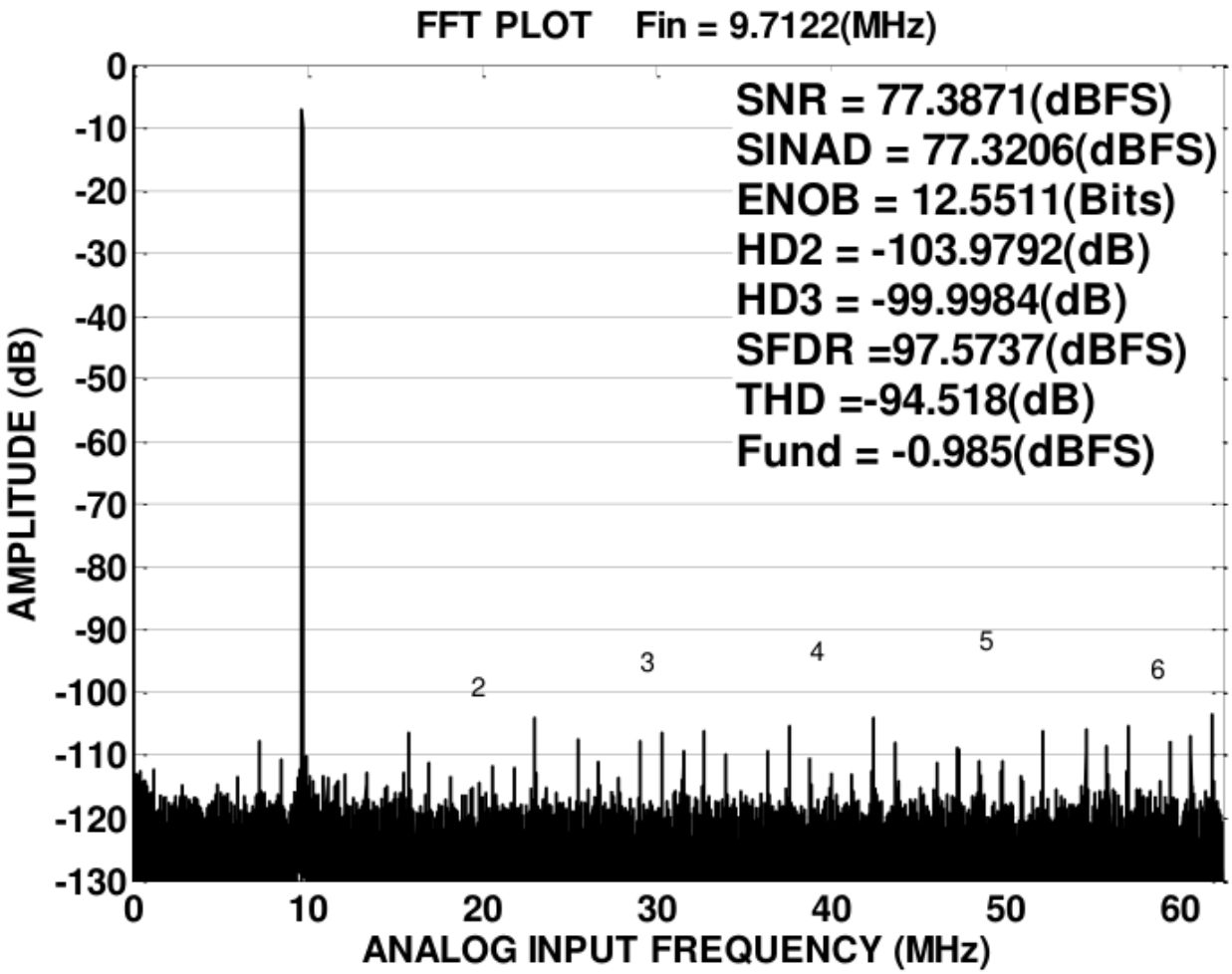


Figure 13: Single-tone 32K FFT plot (fIN=9.7MHz, fS=125MSPS), SNR=77.3871dBFS, SINAD=77.3206dBFS, ENOB=12.5511Bits, SFDR=97.5737dBFS

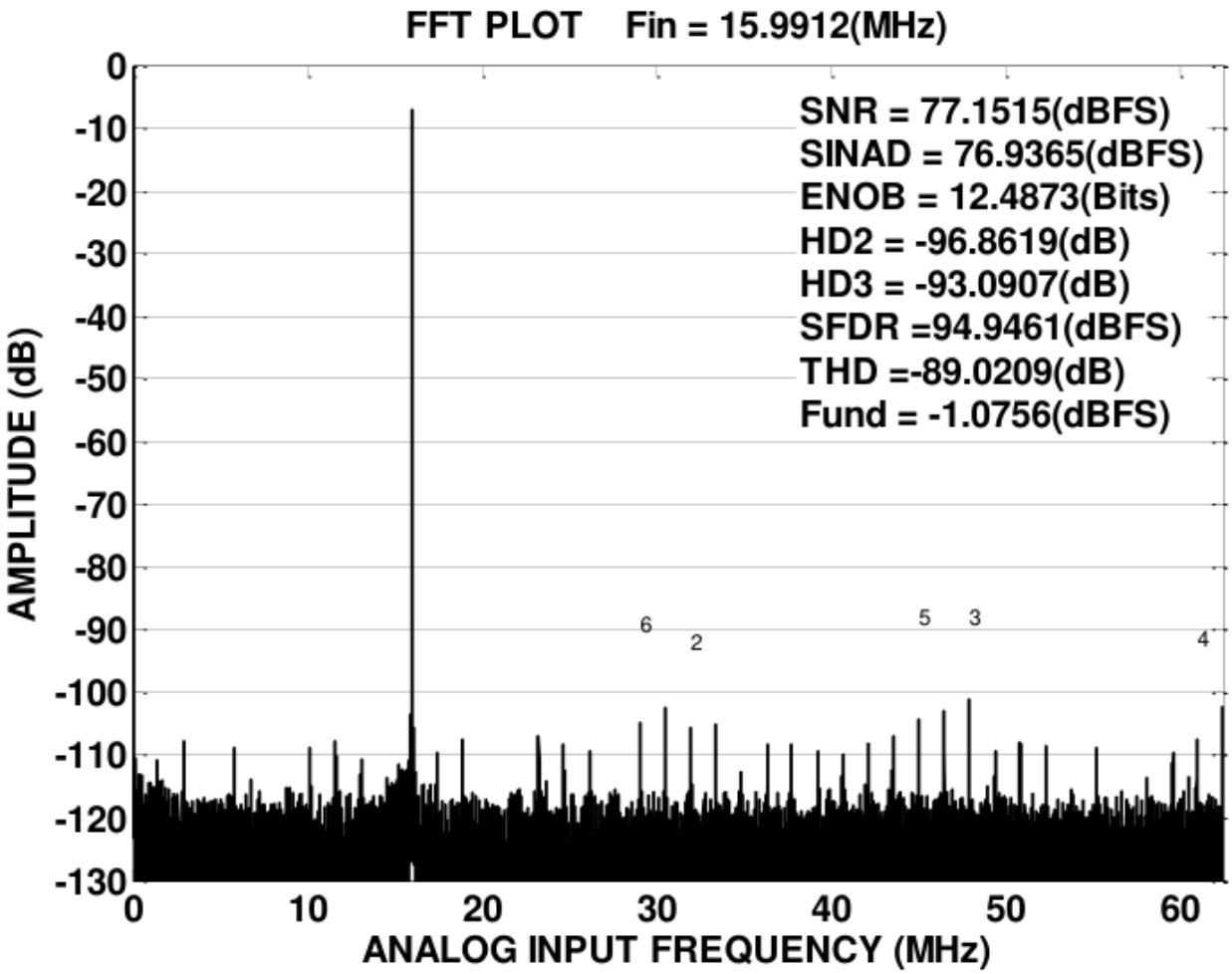


Figure 14: Single-tone 32K FFT plot (fIN=16MHz, fS=125MSPS), SNR=77.1515dBFS, SINAD=76.9365dBFS, ENOB=12.4873Bits, SFDR=94.9461dBFS

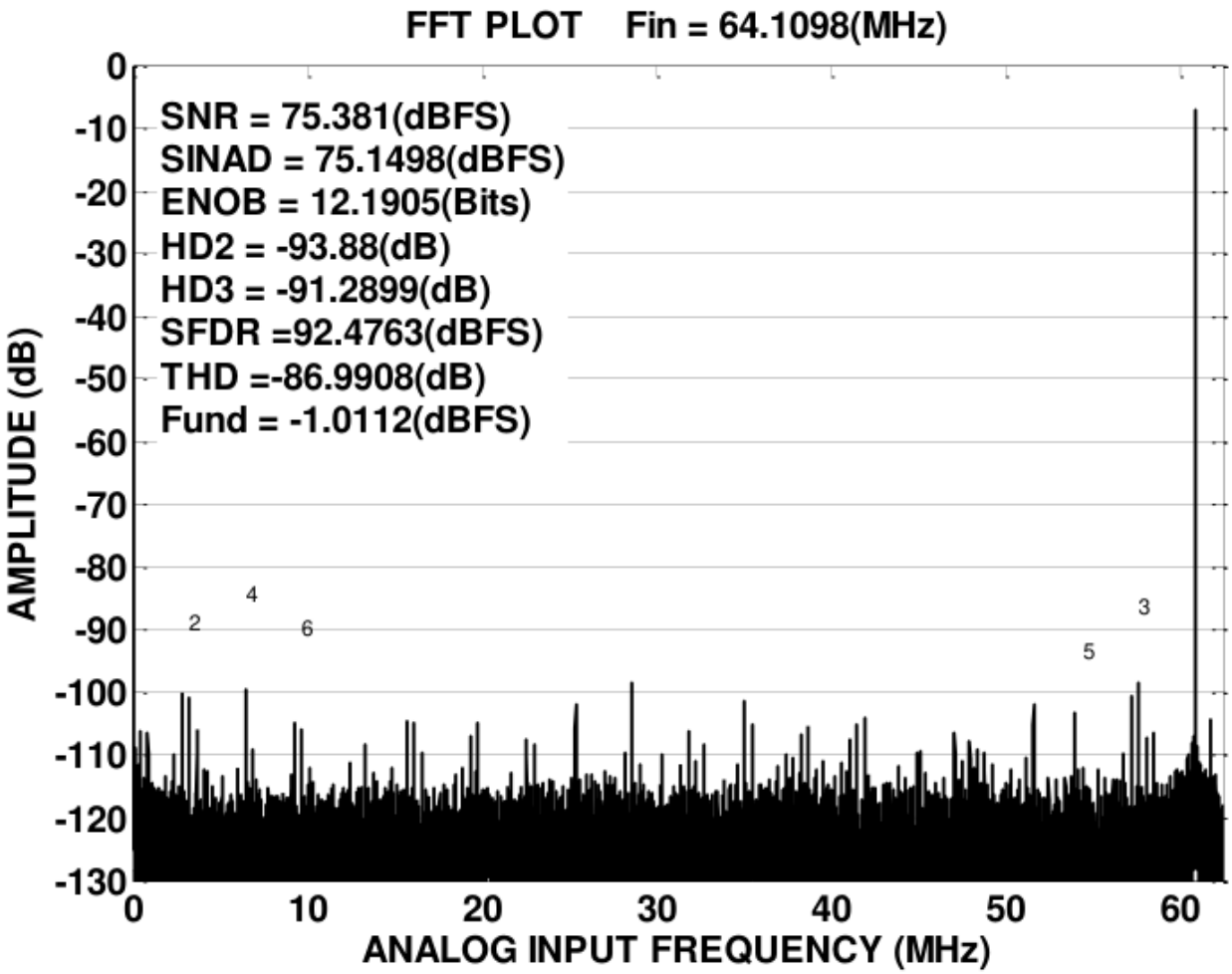


Figure 15: Single-tone 32K FFT plot (fIN=64MHz, fS=125MSPS), SNR=75.381dBFS, SINAD=75.1498dBFS, ENOB=12.1905Bits, SFDR=92.4763dBFS

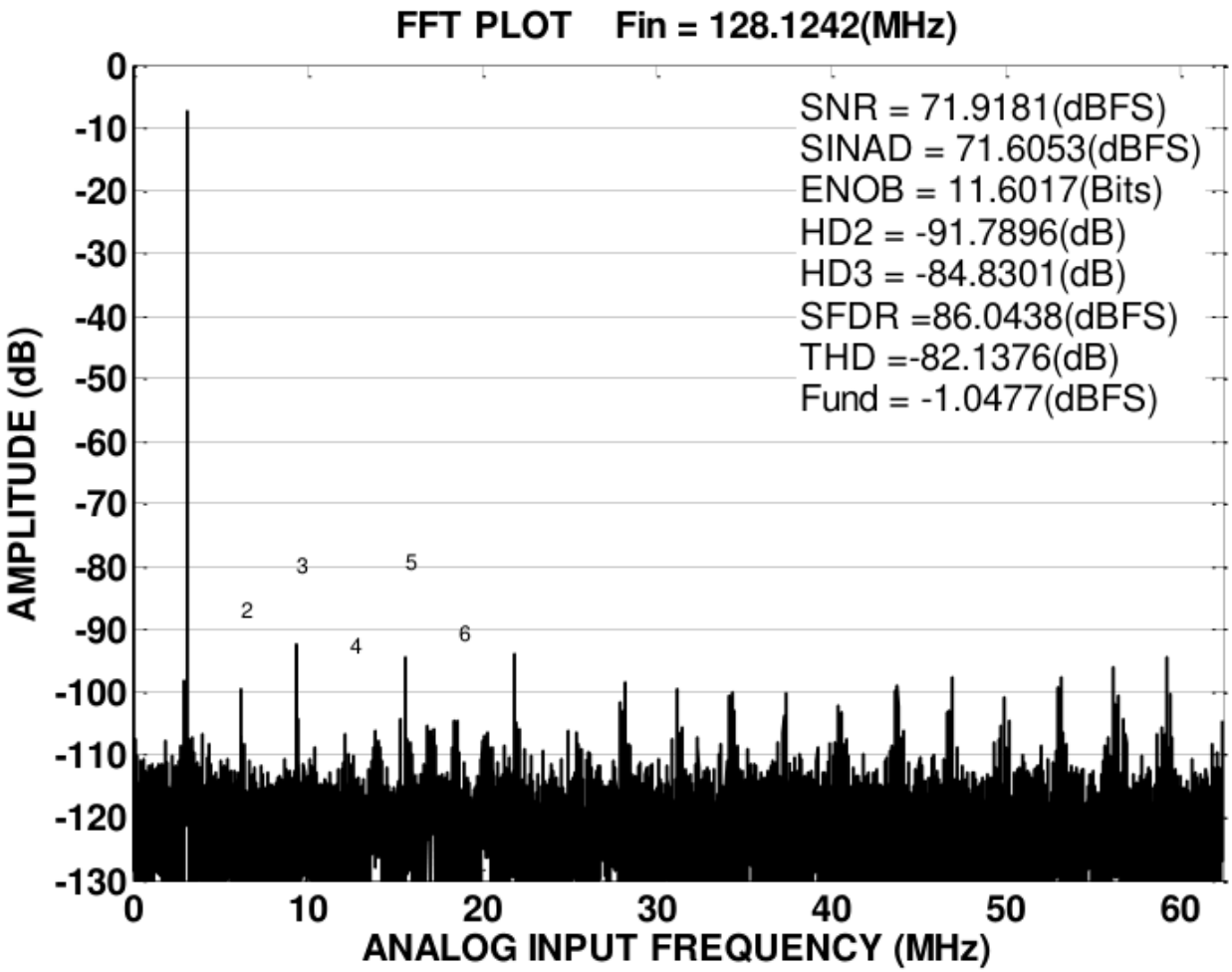


Figure 16: Single-tone 32K FFT plot (fIN=128MHz, fS=125MSPS), SNR=71.9181dBFS, SINAD=71.6053dBFS, ENOB=11.6017Bits, SFDR=86.0438dBFS

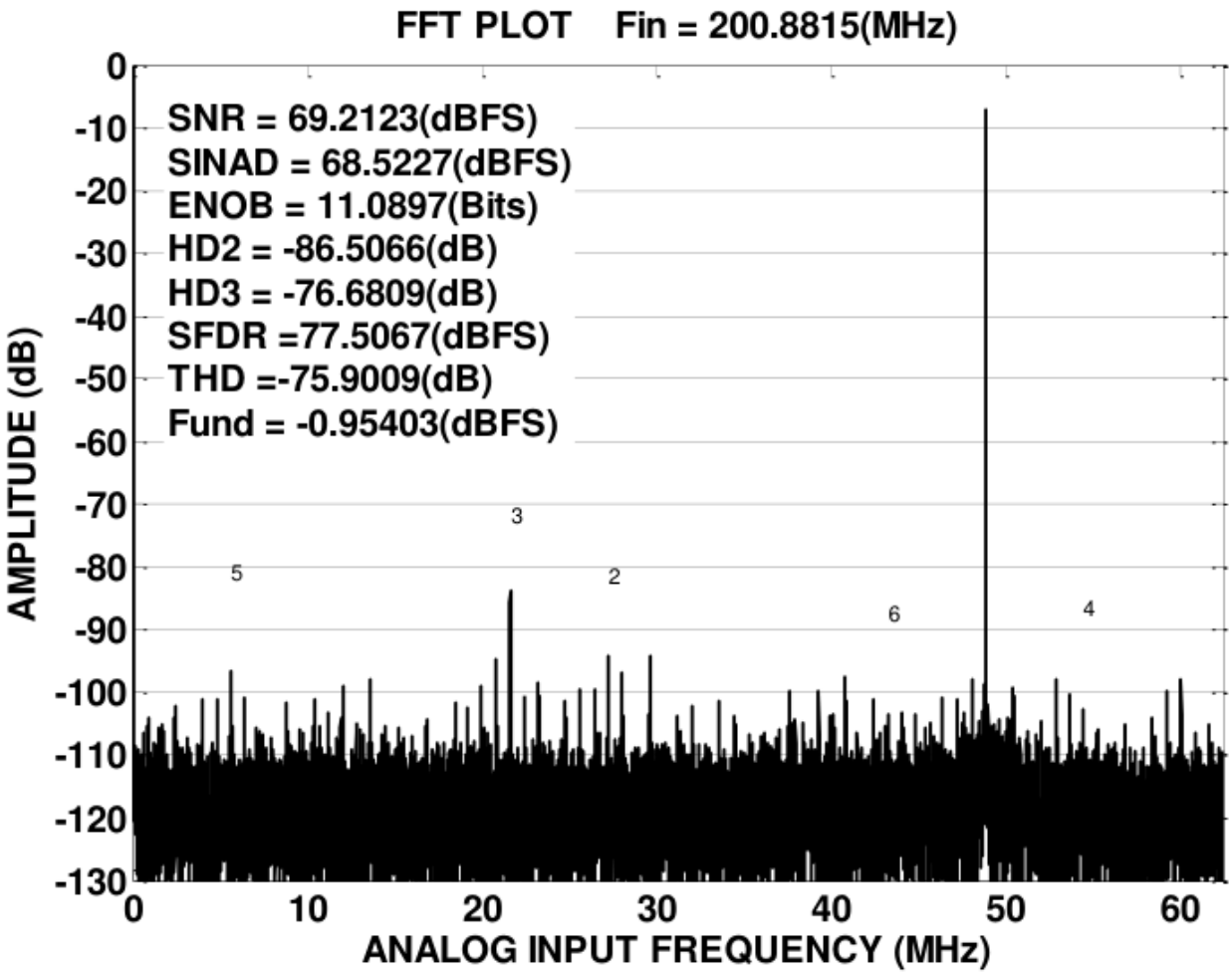


Figure 17: Single-tone 32K FFT plot (fIN=201MHz, fS=125MSPS), SNR=69.2123dBFS, SINAD=68.5227dBFS, ENOB=11.0897Bits, SFDR=77.5067dBFS

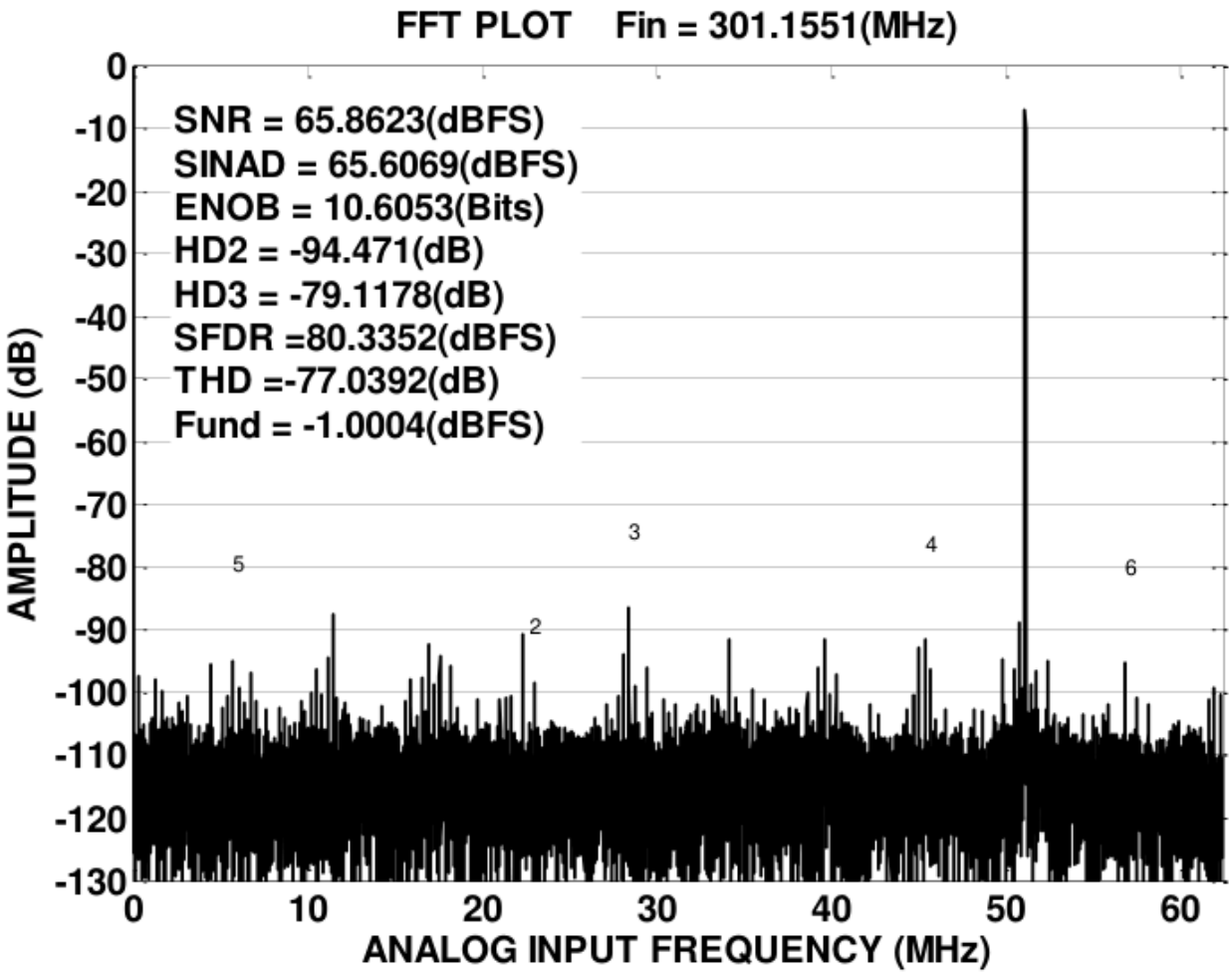


Figure 18: Single-tone 32K FFT plot (fIN=301MHz, fS=125MSPS), SNR=65.8623dBFS, SINAD=65.6069dBFS, ENOB=10.6053Bits, SFDR=80.3352dBFS

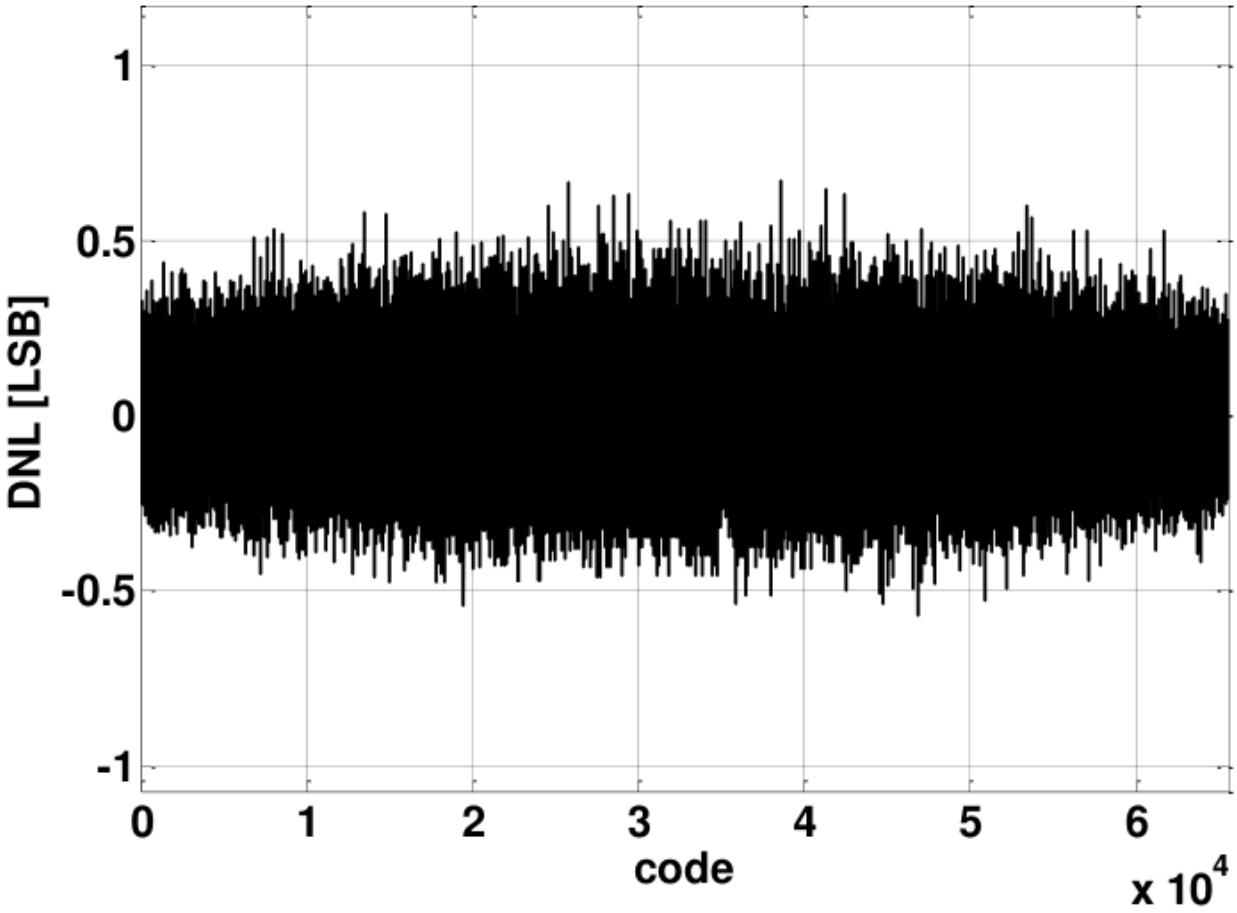


Figure 19: Differential nonlinearity DNL (fIN=10MHz, fS=125MSPS)

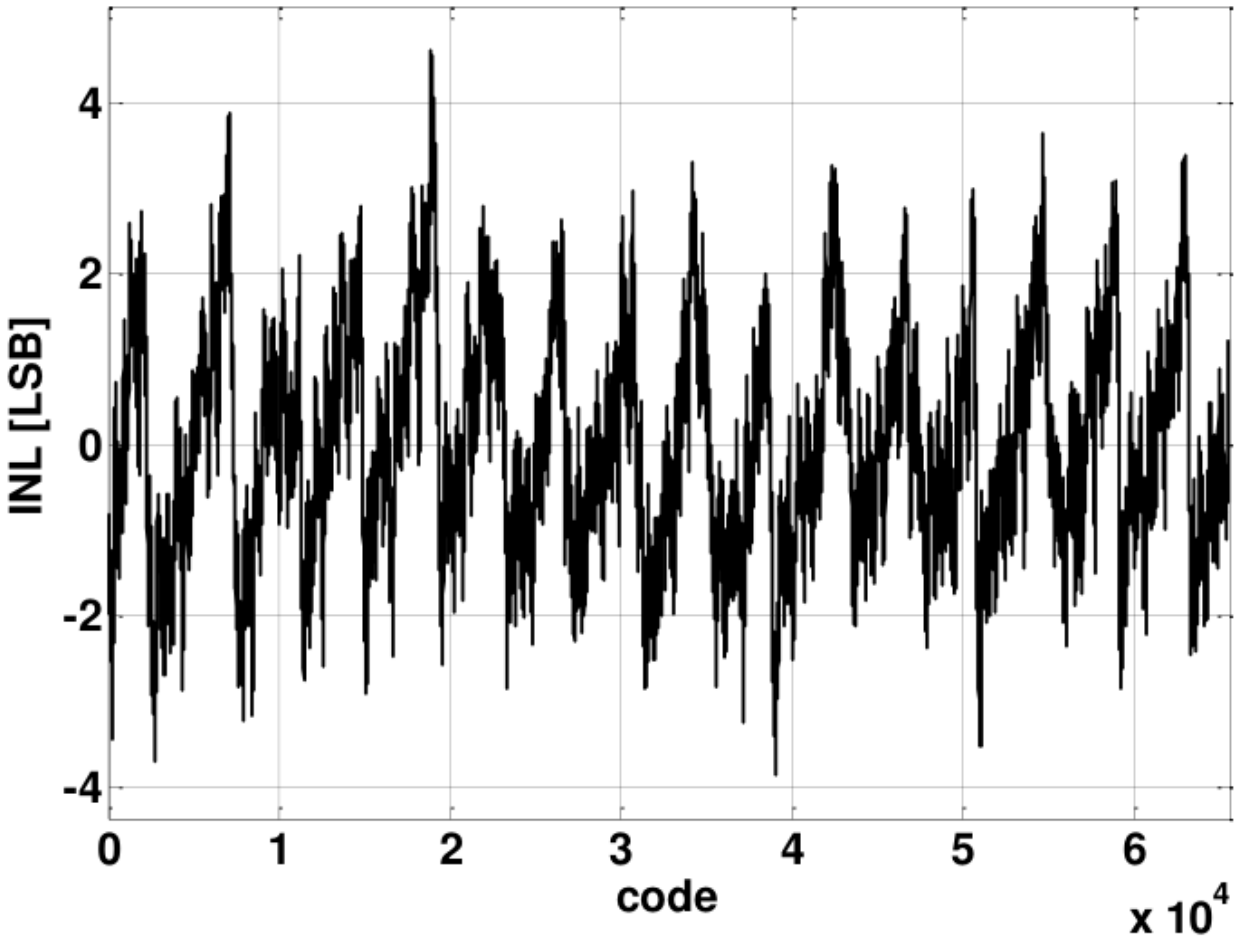


Figure 20: Integral nonlinearity INL (fIN=10MHz, fS=125MSPS)

Typical Application Circuits / 典型应用线路图

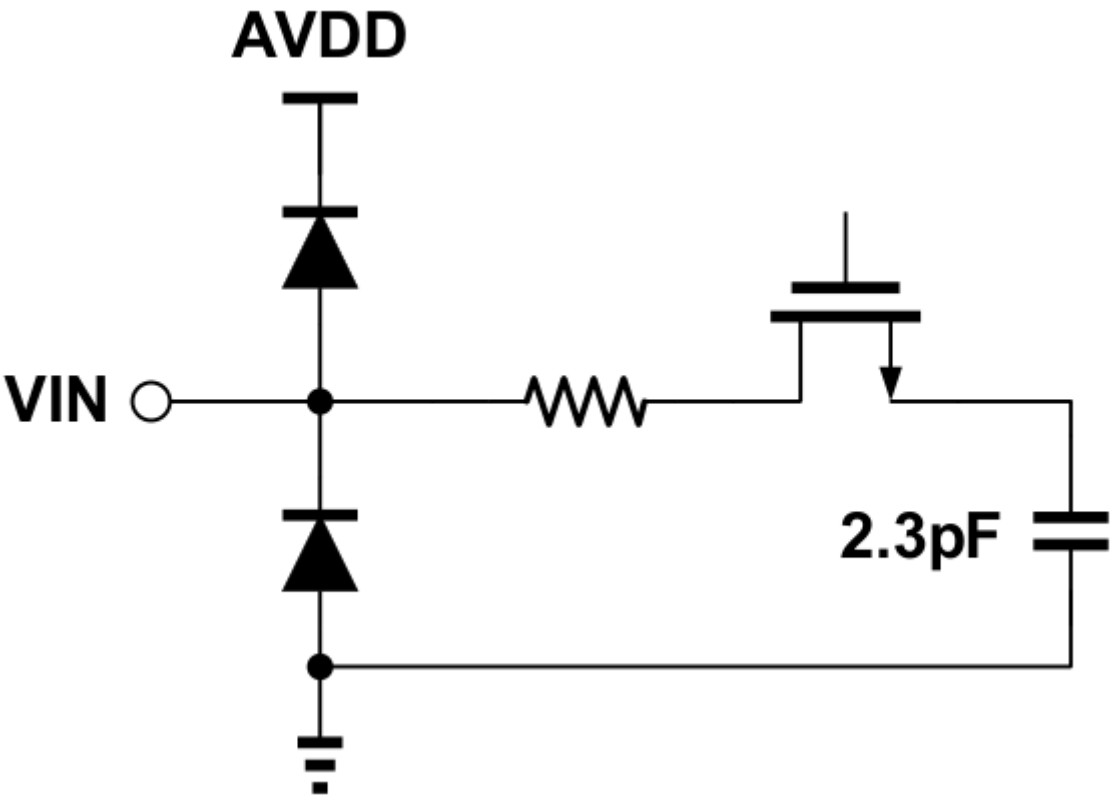


Figure 21: Equivalent analog input circuit

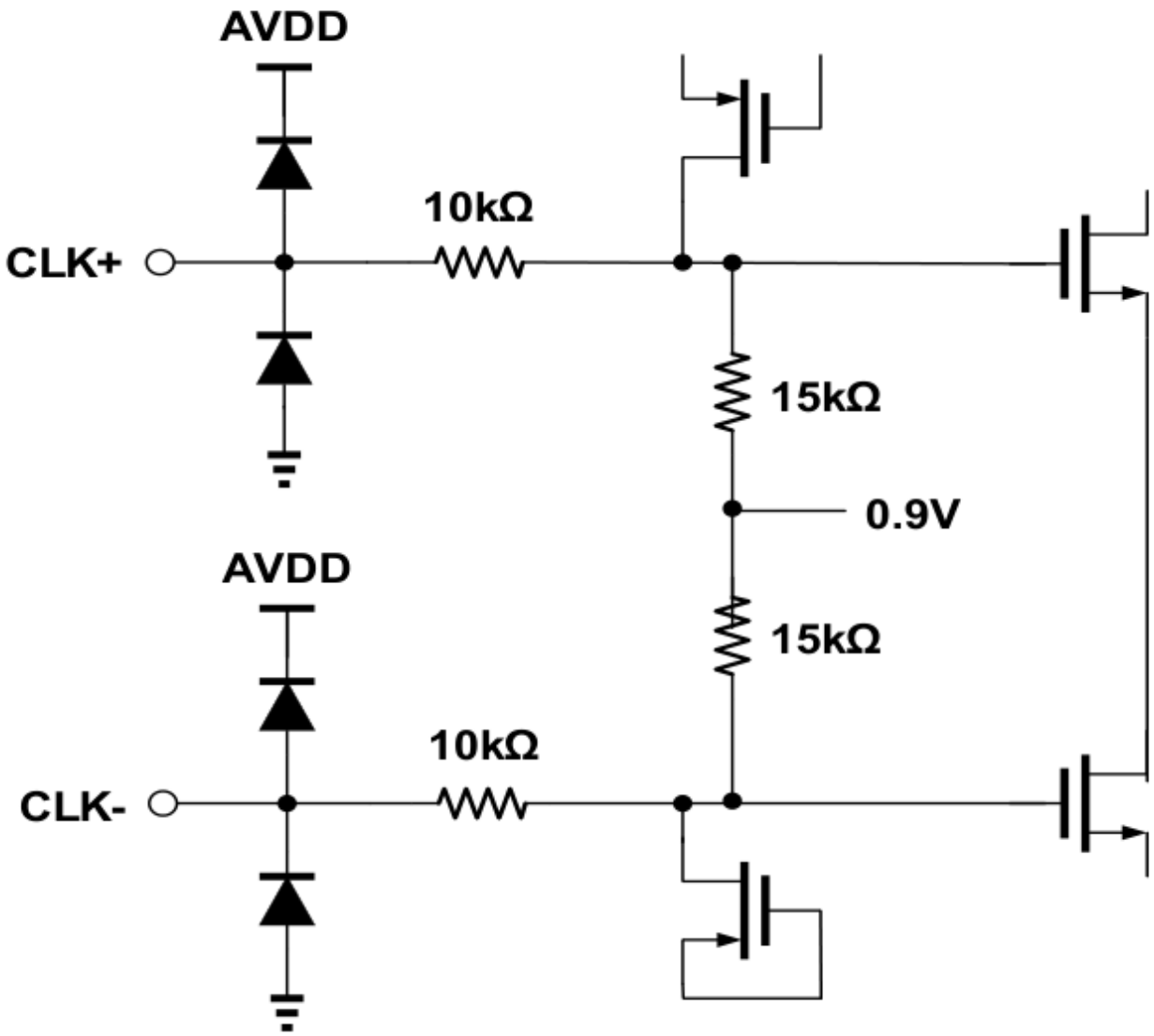


Figure 22: Equivalent clock input circuit

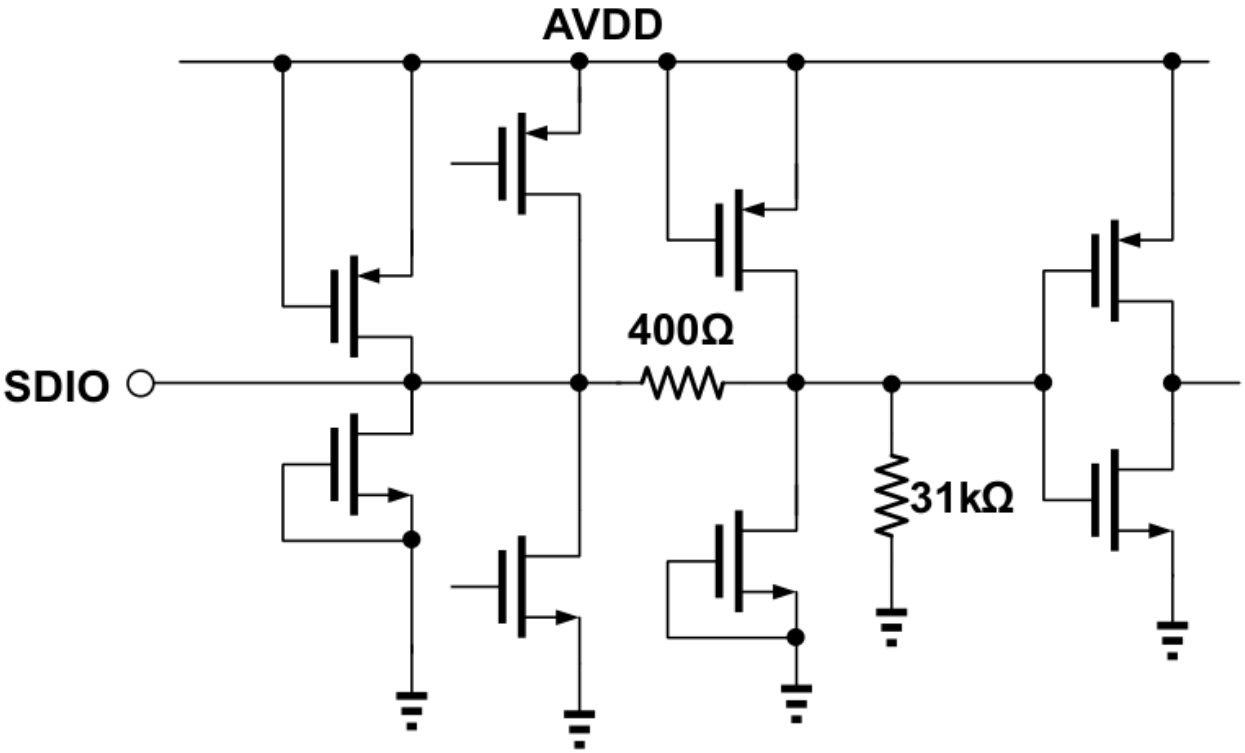


Figure 23: Equivalent SDIO input circuit

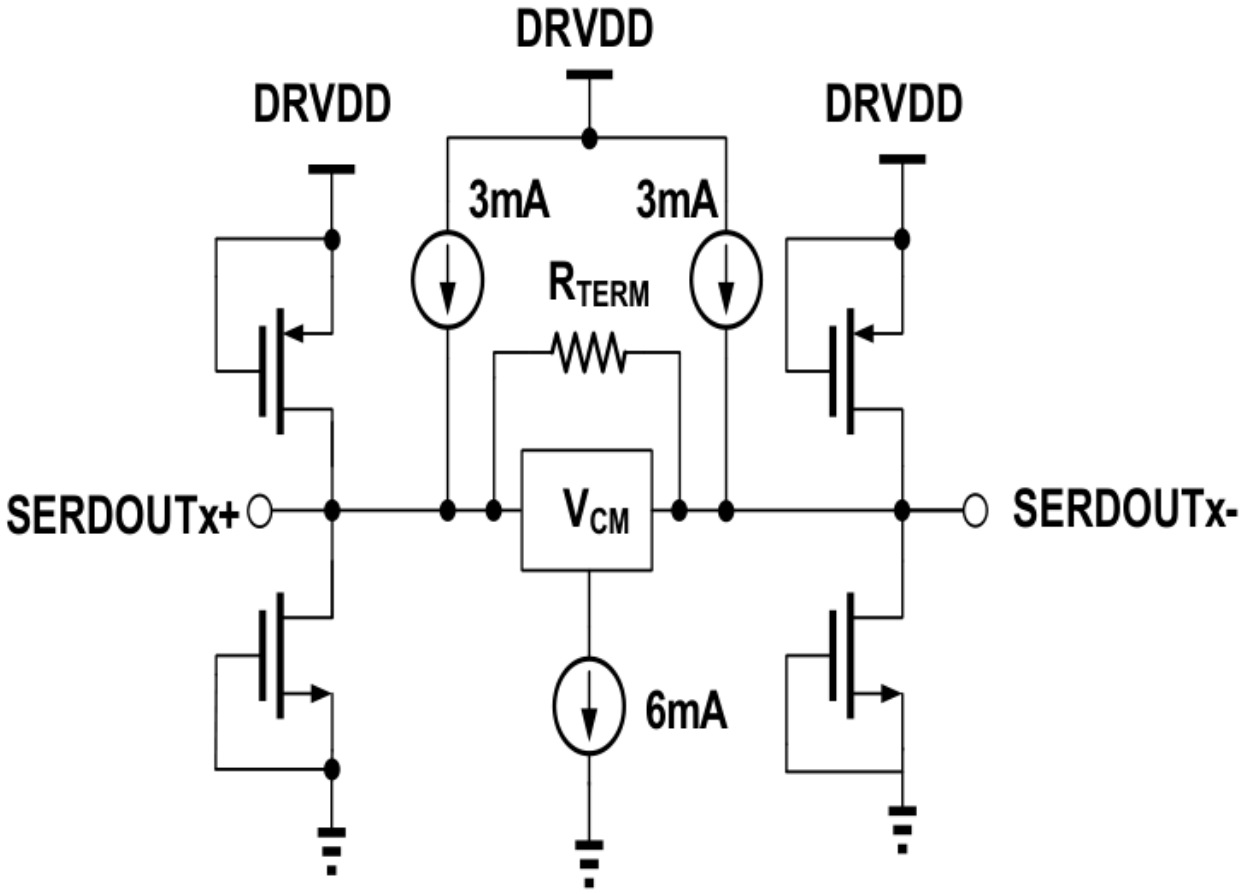


Figure 24: Equivalent SERDOUT± circuit

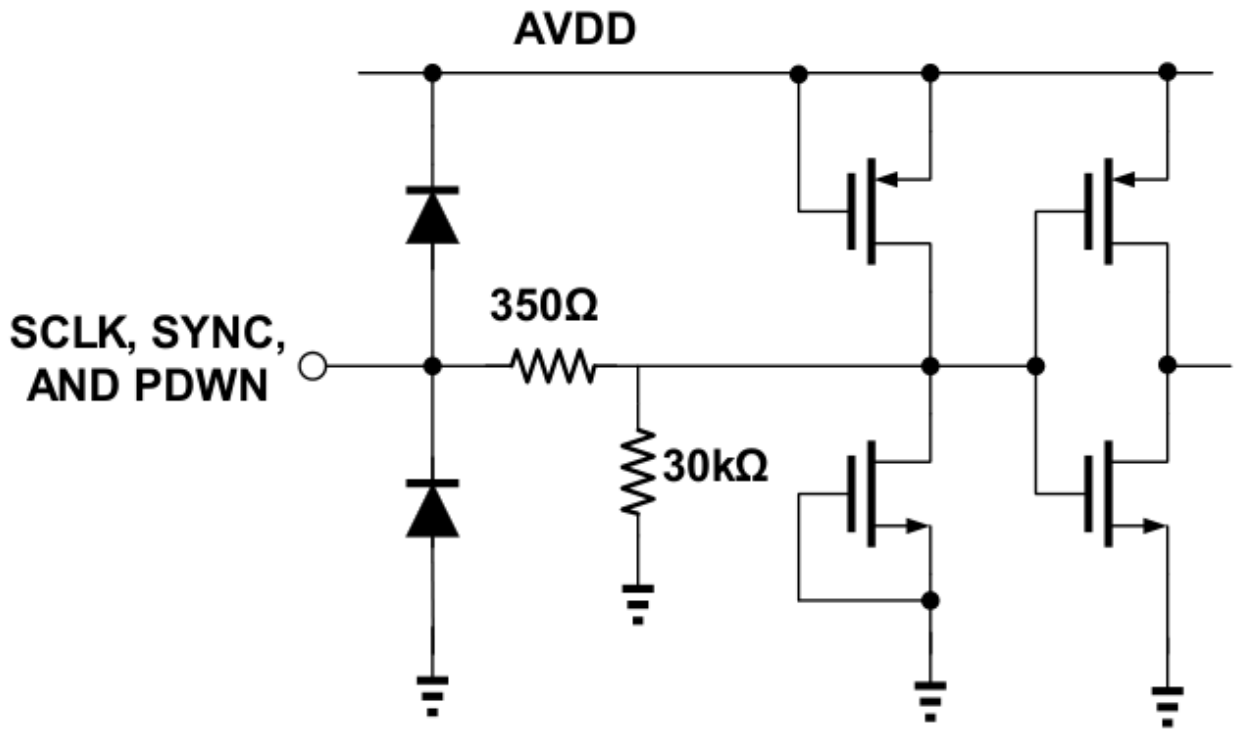


Figure 25: Equivalent SCLK, SYNC, PDWN circuit

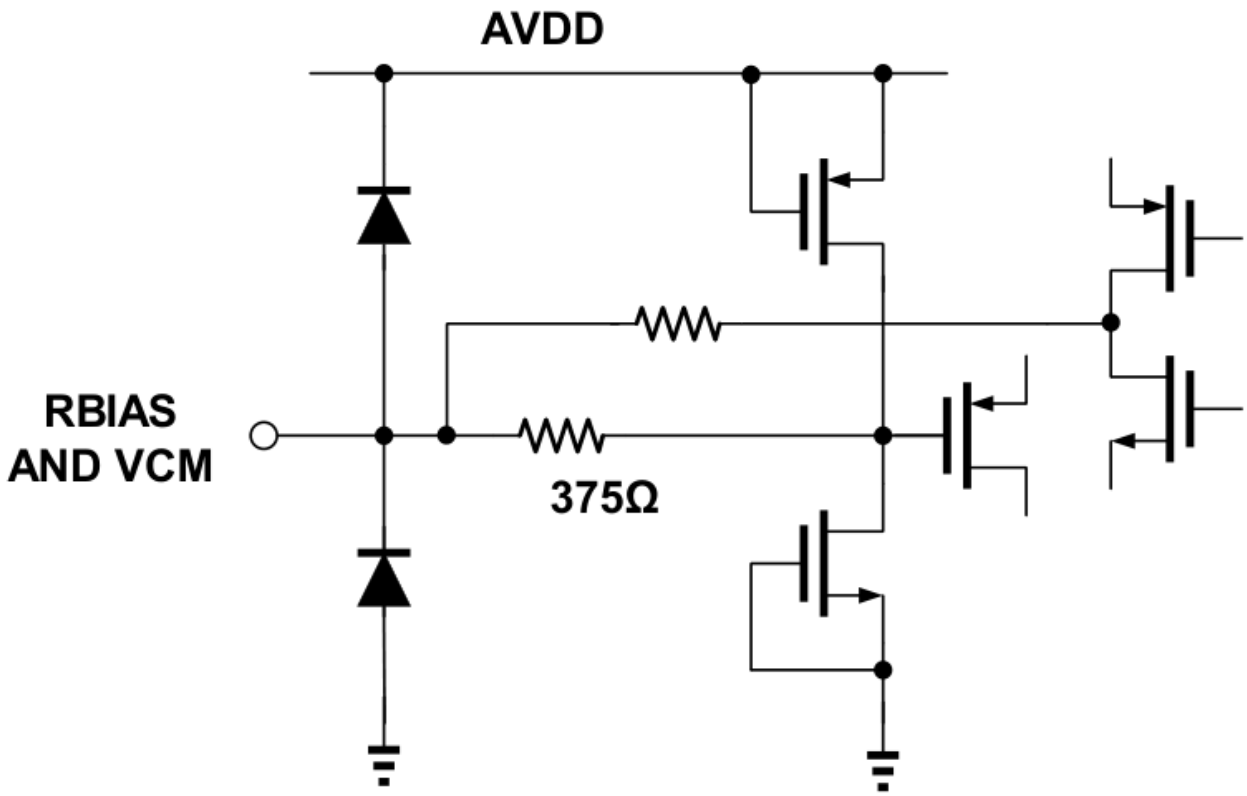


Figure 26: Equivalent RBIAS, VCM circuit

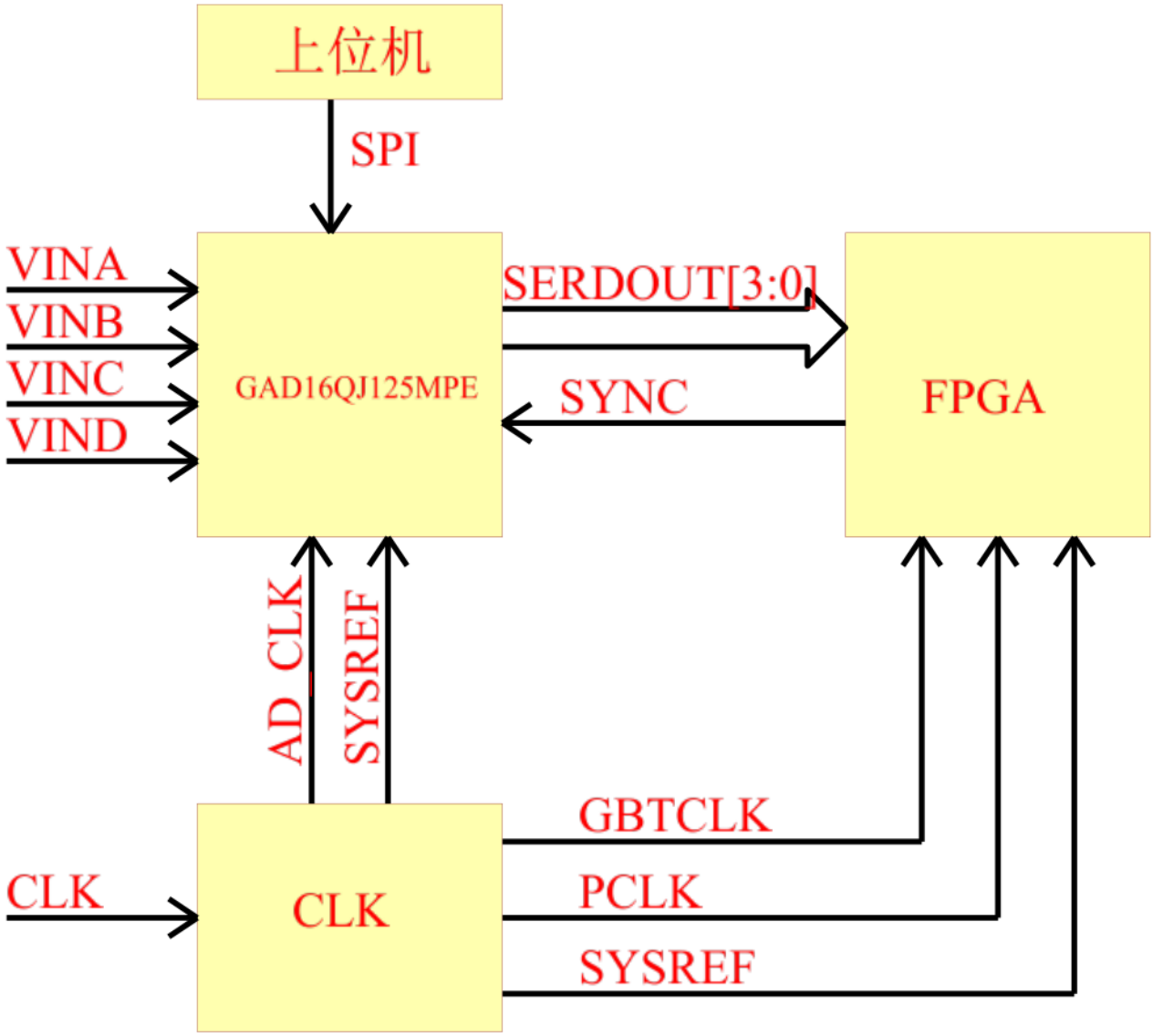


Figure 27: SXA009 typical peripheral circuit

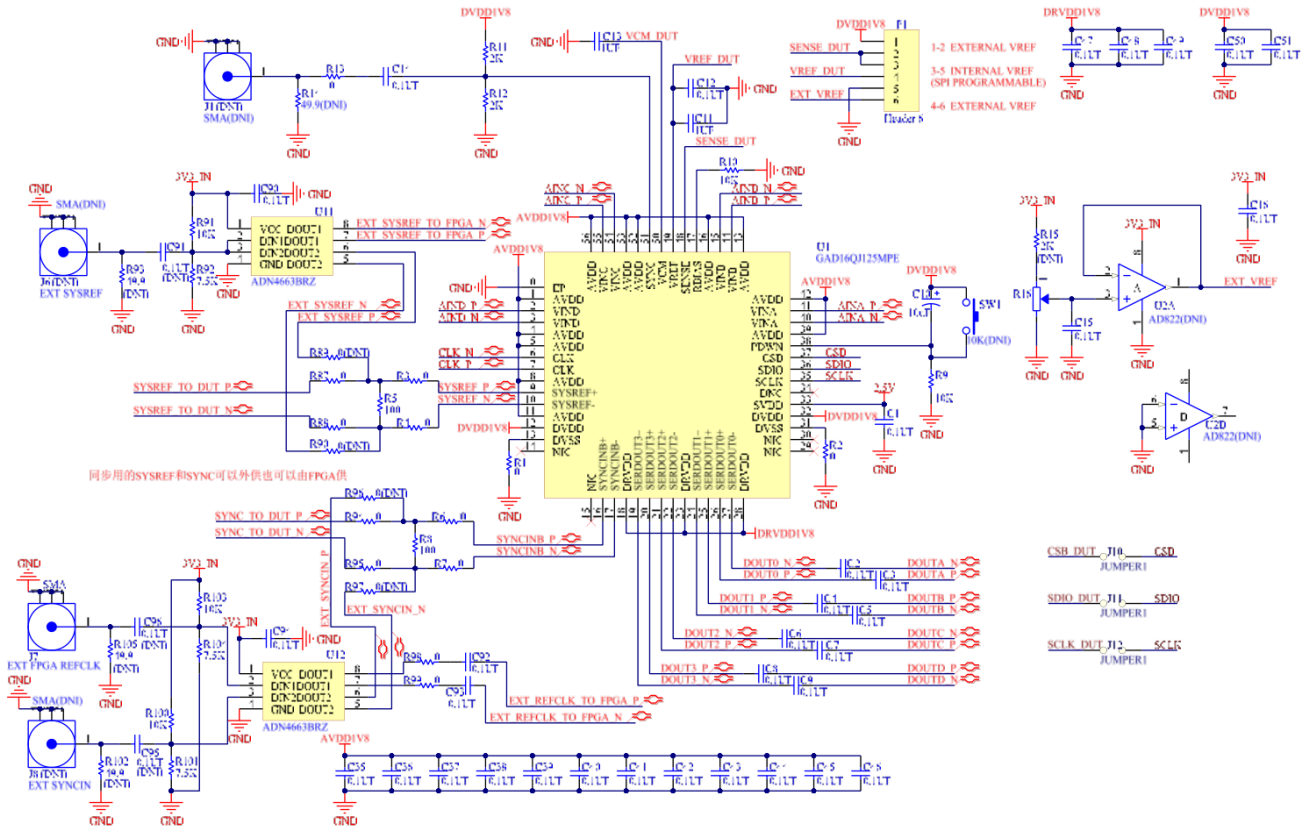


Figure 28: Main circuit diagram

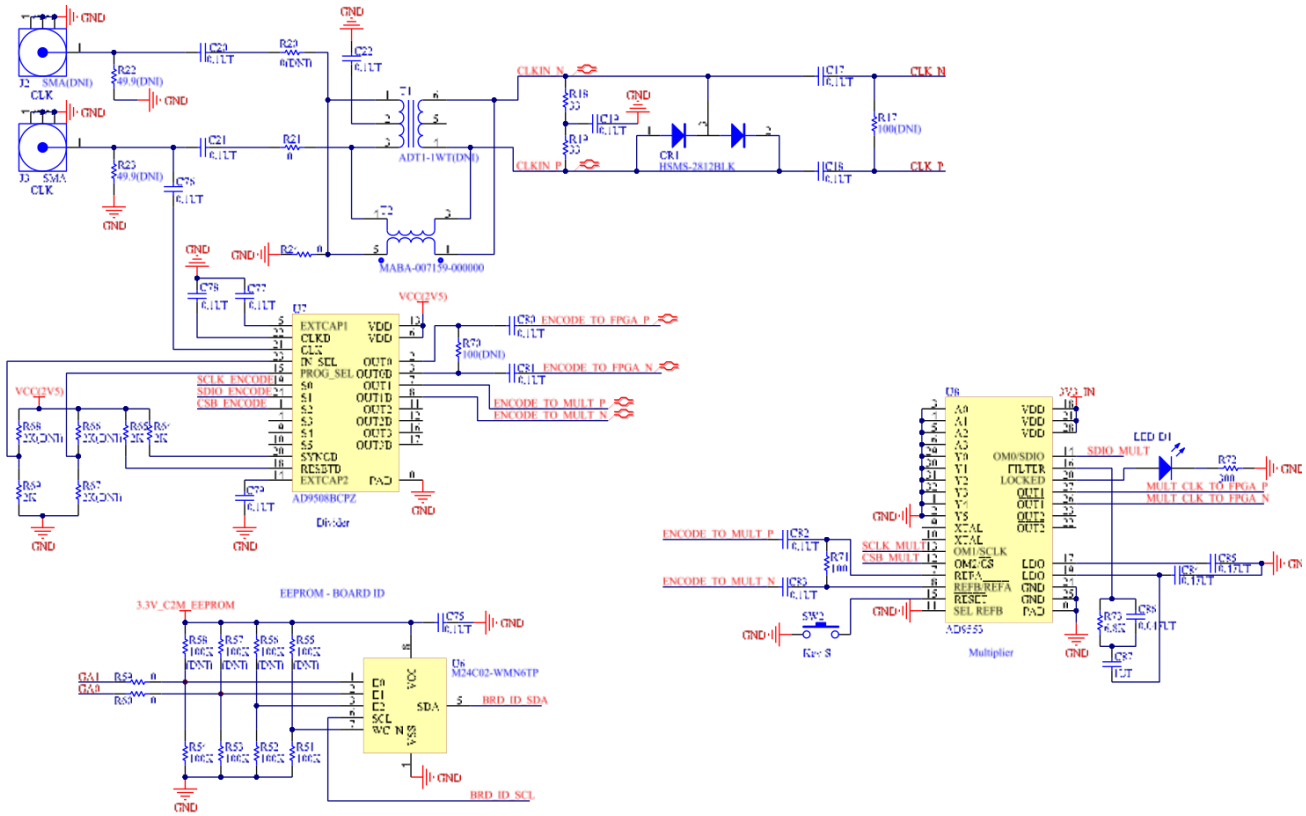


Figure 29: Clock circuit

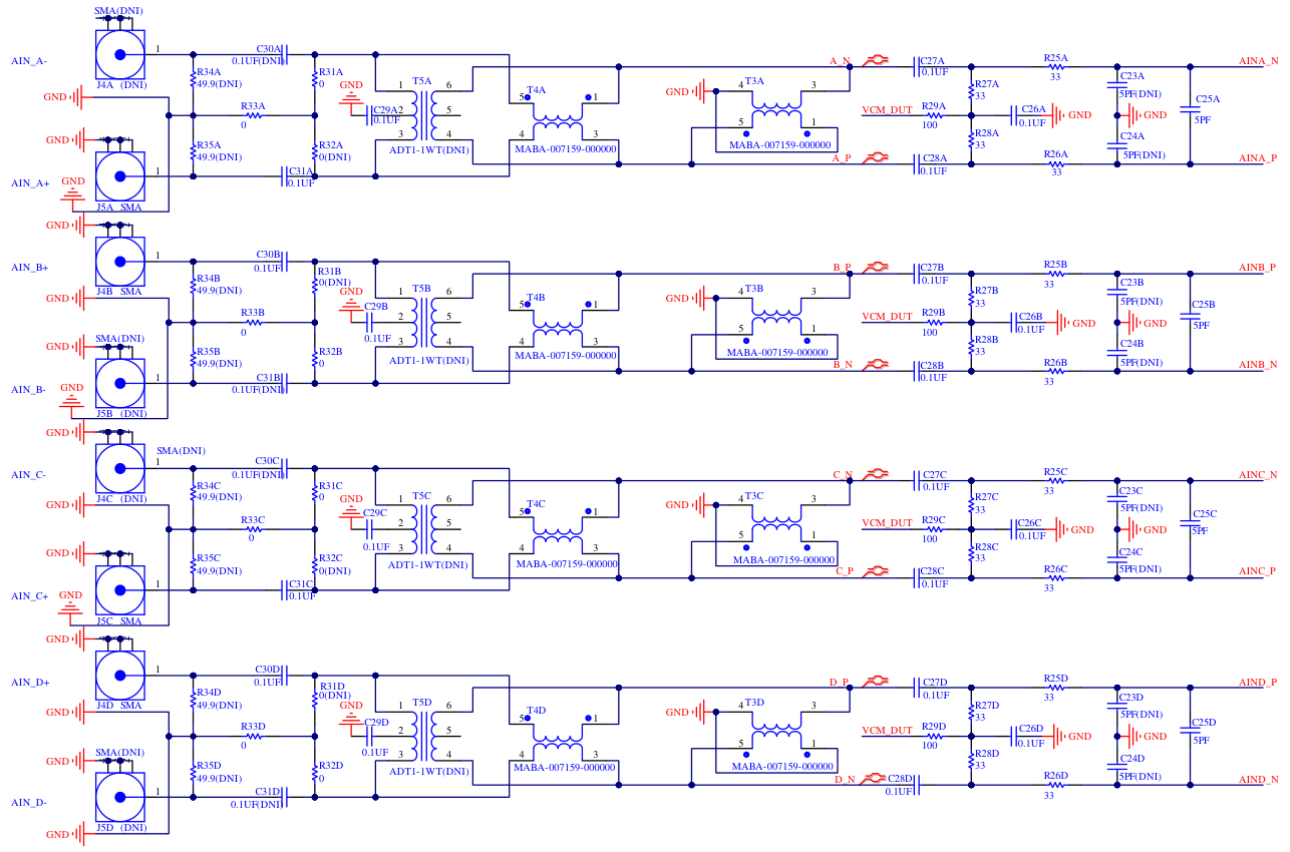


Figure 30: Analog input (schematic)

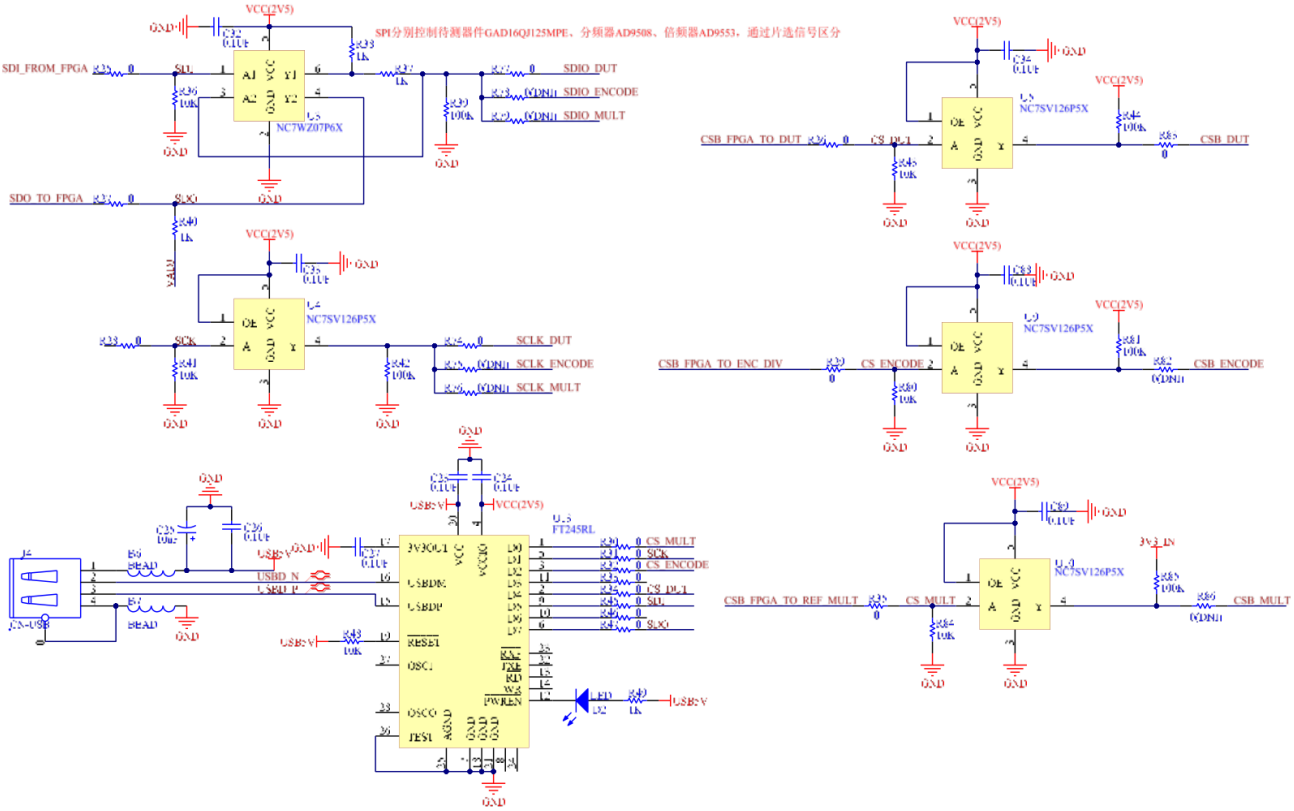


Figure 31: SPI circuit

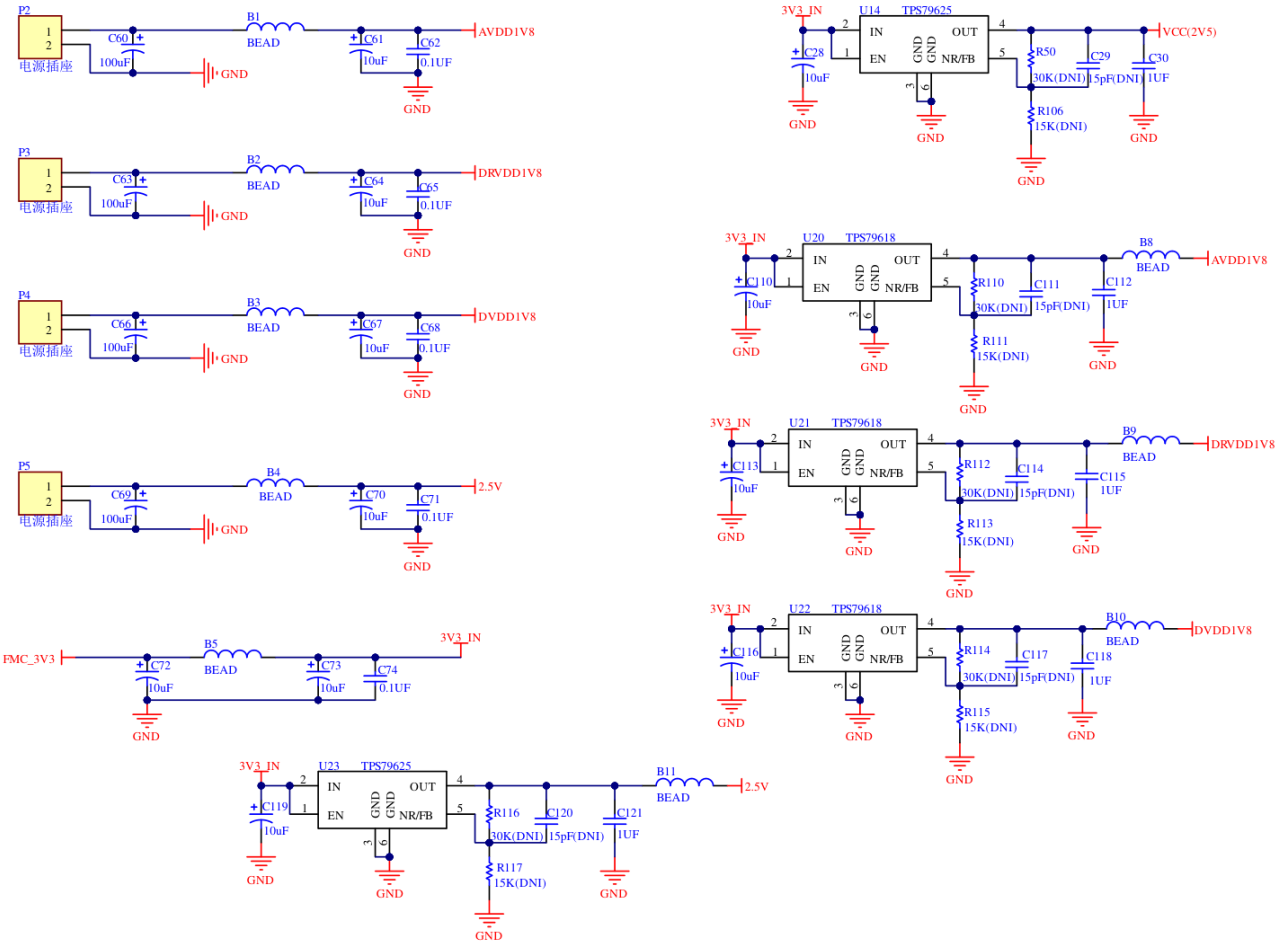


Figure 32: Power supply circuit diagram

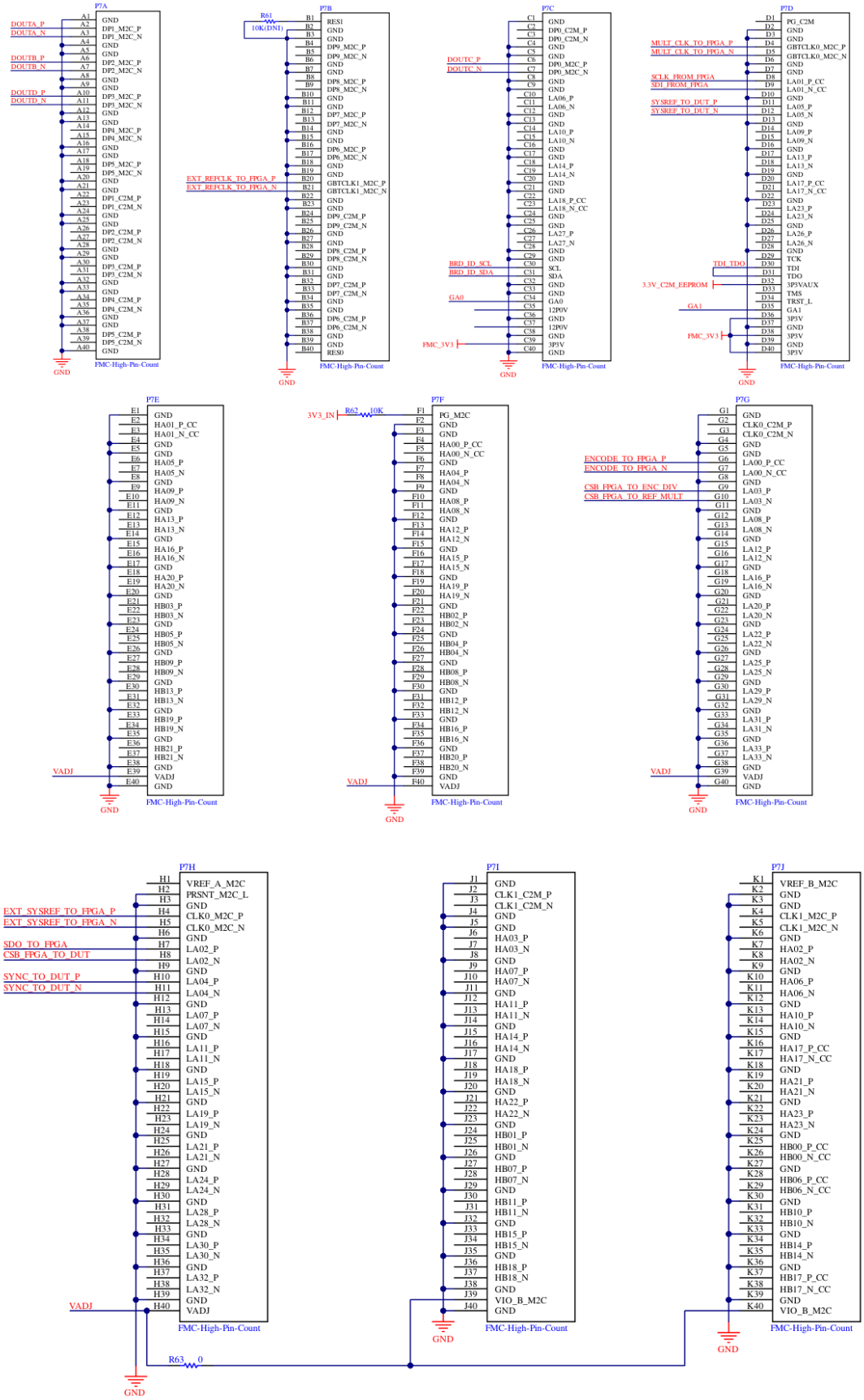


Figure 33: Interface circuit diagram

Functional Blocks and Theory of Operation / 单元模块及工作原理

1. Theory Overview / 1、原理概述

The core of this device uses a multi-stage pipelined ADC architecture, with each stage providing one redundant bit to eliminate offset errors of the coarse quantization comparators. The pipelined quantization stages are reconstructed in the digital domain by shift-adders to form the 16-bit conversion result. The serializer transmits the conversion result in 16-bit output format.

本产品内核使用多级流水线型 ADC 架构，各级提供一位冗余位消除粗量化比较器的失调误差。各级流水线量化结构在数字域由移位加法器重构形成 16 位转换结果。串化器以十六位输出格式发送该转换结果。

Except for the last stage, each pipeline stage consists of a low-resolution Flash ADC, a connected switched-capacitor DAC, and an inter-stage residue amplifier (e.g., multiplying digital-to-analog converter [MDAC]). The residue amplifier amplifies the difference between the reconstructed DAC output and the Flash input for the next pipeline stage. To assist digital correction of Flash errors, each stage is assigned one bit of redundancy. The last stage consists only of a Flash ADC.

除最后一级以外，流水线的每一级都由一个低分辨率 Flash 型 ADC、与之相连的一个开关电容 DAC 和一个级间余量放大器(例如乘法数模转换器[MDAC])组成。余量放大器放大重构 DAC 输出与 Flash 型输入之差，以便提供给流水线的下一级。为了帮助对 Flash 误差进行数字校正，每一级设定了一位的冗余量。最后一级仅由一个 Flash 型 ADC 组成。

2. Analog Input / 2、模拟输入

The analog input of this device is a differential switched-capacitor circuit designed to handle differential input signals. The circuit supports a wide common-mode range while maintaining excellent performance. When the input common-mode voltage is at mid-supply, signal-dependent errors are minimized and optimum performance is achieved.

本产品的模拟输入端为一个差分开关电容电路，设计用于处理差分输入信号。该电路支持宽共模范围，同时能保持出色的性能。当输入共模电压为中间电源电压时，信号相关误差最小，并且能实现最佳性能。

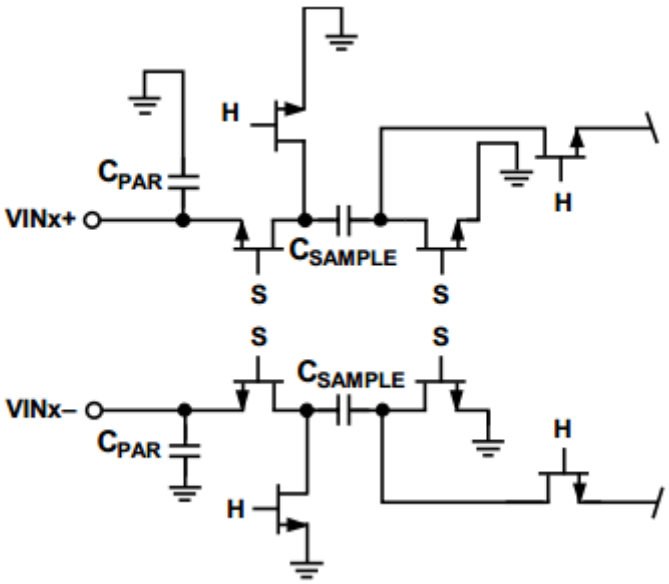


Figure 34: Analog input equivalent circuit

The input circuit switches between sample mode and hold mode according to the clock signal (see Figure 38). When the input circuit switches to sample mode, the signal source must be able to charge the sampling capacitors and settle within half a clock cycle. A small resistor is placed in series with each input to help reduce peak transient currents injected from the driver output stage. Additionally, a low-Q inductor or ferrite bead may be used on each side of the input to reduce the high differential capacitance at the analog input, thereby achieving the maximum ADC bandwidth. When driving the converter front end at high intermediate frequencies (IF), a low-Q inductor or ferrite bead must be used. A differential capacitor or two single-ended capacitors may be used at the input to provide a matched passive network. This ultimately forms a low-pass filter at the input to limit unwanted wideband noise.

输入电路根据时钟信号在采样模式和保持模式之间切换(见图 38)。当输入电路切换到采样模式时，信号源必须能够对采样电容充电，并且在半个时钟周期内完成建立。每个输入端都串联一个小电阻，帮助降低从驱动源输出级注入的峰值瞬态电流。此外，输入端的每一侧可以使用低 Q 电感或铁氧体磁珠，以减小模拟输入端的高差分电容，从而实现 ADC 的最大带宽。在高中频(IF)下驱动转换器前端时，必须使用低 Q 电感或铁氧体磁珠。输入端可以使用一个差分电容或两个单端电容，以提供匹配的无源网络。这最终会在输入端形成一个低通滤波器，用来限制无用的宽带噪声。

3. Input Common-Mode Level / 3、输入共模电平

The analog input of this device has no internal DC bias; in AC-coupled applications, the user must provide external bias. For optimum dynamic performance, the device must be configured so that the input common-mode level VCM=AVDD/2. Reasonable performance can also be obtained over a wider input common-mode range, as shown in Figures 35 and 36.

本产品的模拟输入端无内部直流偏置，在交流耦合应用中，用户必须提供外部偏置。为了获得最佳的动态性能，用户必须对器件进行配置，使输入共模电平 VCM=AVDD/2。本器件在更宽的输入共模范围内也能获得合理的性能，如图 35 和图 36 所示。

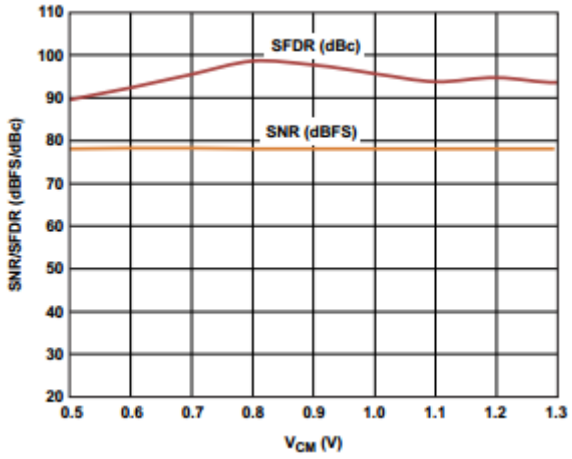


Figure 35: SNR/SFDR vs. input common-mode level (VCM) (fIN=9.7MHz, fSAMPLE=125MSPS, VREF=1.0V)

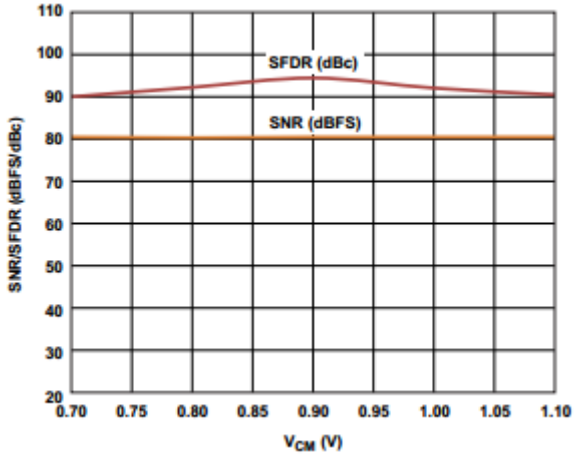


Figure 36: SNR/SFDR vs. input common-mode level (VCM) (fIN=9.7MHz, fSAMPLE=125MSPS, VREF=1.4V)

This device provides an on-chip reference voltage through the VCM pin; the VCM pin must be bypassed to ground with a 0.1F capacitor .

本产品通过引脚 VCM 提供片内基准电压，必须使用一个 0.1F 电容将 VCM 引脚旁路到地。

In differential configuration, setting the device input to maximum range achieves the highest signal-to-noise ratio (SNR) performance; for this device the input range depends on the reference voltage, and performance degrades sharply beyond the input range.

在差分配置中，将器件输入设置为最大范围可以实现最高的信噪比(SNR)性能，对于本产品输入范围取决于基准电压，超过输入范围性能将急剧恶化。

4. Differential Input Configuration / 4、差分输入配置

There are various active and passive ways to effectively drive this device; driving differentially suppresses even-order harmonics to achieve optimum performance.

有多种有源和无源方式可以有效驱动本产品，通过差分方式驱动可以抑制偶次谐波从未获得最佳性能。

In baseband applications, driving this device with a differential balun configuration provides excellent performance and flexible interfacing for the ADC (see Figure 37).

在基带应用中，利用差分巴伦配置驱动本产品能够为 ADC 提供出色的性能和灵活接口（参考图 37）。

In applications where SNR is a critical parameter, since the noise performance of most amplifiers is insufficient to meet the true performance of this device, the input configuration requires differential transformer coupling (see Figure 38).

在 SNR 为关键参数的应用中，因为绝大部分放大器的噪声性能不足以满足本产品的真实性能，所以输入配置要求采用差分变压器耦合(参考图 38)。

The C capacitor values in both applications above must be matched to the input spectrum; it is recommended to reduce the capacitor value or remove the capacitor when converting high-frequency analog input signals.

以上两种应用中的 C 电容值需要和输入频谱配合使用，建议转换高频模拟输入信号时减小该电容容值或者移除该电容。

Single-ended input drive of this device is not recommended.

不建议单端输入方式驱动本产品。

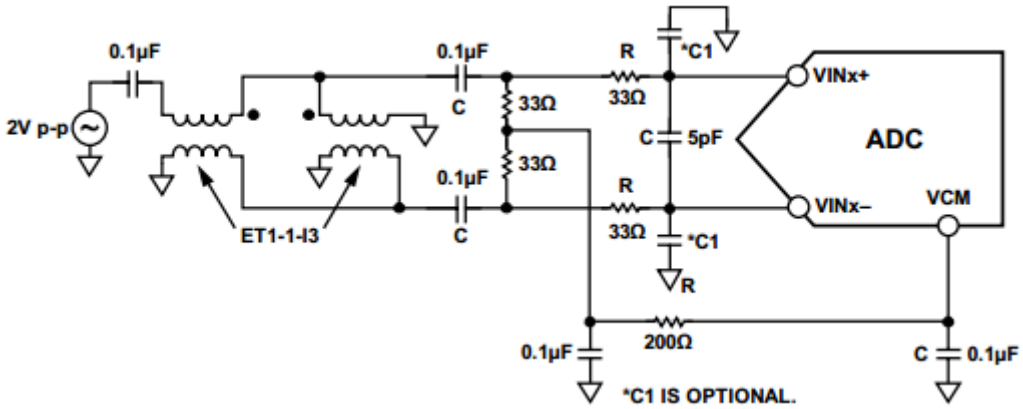


Figure 37: Differential dual-balun configuration

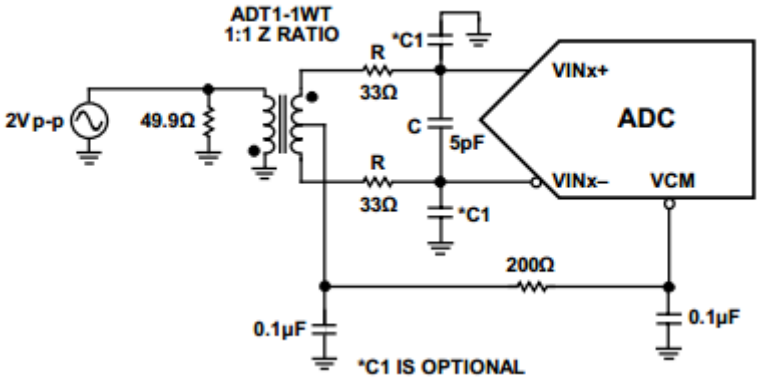


Figure 38: Differential transformer coupling

5. Reference Voltage / 5、基准电压

This device integrates a stable, precision reference voltage source. VREF can be configured using the internal 1.0 V reference, an externally applied 1.0 V to 1.4 V reference, or an external resistor divider acting on the internal reference, to produce a user-selectable reference voltage. See the "Internal Reference Connection" and "External Reference" sections for a description of reference source modes. The VREF pin should be bypassed to ground through an external parallel combination of a low-ESR 1.0µF capacitor and a low-ESR 0.1µF ceramic capacitor.

本产品内置稳定、精确的基准电压源。VREF 可以利用内部 1.0 V 基准电压、外部施加的 1.0 V 至 1.4 V 基准电压或作用于内部基准电压的外部电阻分压器来配置，产生用户可选的基准电压。基准电压源模式说明参见"内部基准电压连接"部分和"外部基准电压"部分。VREF 引脚应通过外部一个低等效串联电阻(ESR)1.0µF 电容和一个低 ESR 0.1µF 陶瓷电容的并联旁路至地。

The built-in comparator of this device can detect the voltage on the SENSE pin, thereby configuring the reference voltage into one of three possible modes. If the SENSE pin is grounded, the reference voltage amplifier switch is connected to the internal resistor divider (see Figure 39), thus setting the VREF pin

voltage V to 1.0 V. If the SENSE pin is connected to an external resistor divider (see Figure 40), VREF is defined as:

本产品的内置比较器可检测出 SENSE 引脚的电压，从而将基准电压配置成三种可能的模式之一。如果 SENSE 引脚接地，则基准电压放大器开关与内部电阻分压器相连(见图 39)，因而将 VREF 引脚电压 V 设为 1.0 V。如果 SENSE 引脚连接到外部电阻分压器(见图 40)，则 VREF 定义为：

$$Vref = 0.5 \times (1 + R2/R1)$$

where $7\ k\Omega \leqslant (R1 + R2) \leqslant 10\ k\Omega$.

其中，$7\ k\Omega \leqslant (R1 + R2) \leqslant 10\ k\Omega$

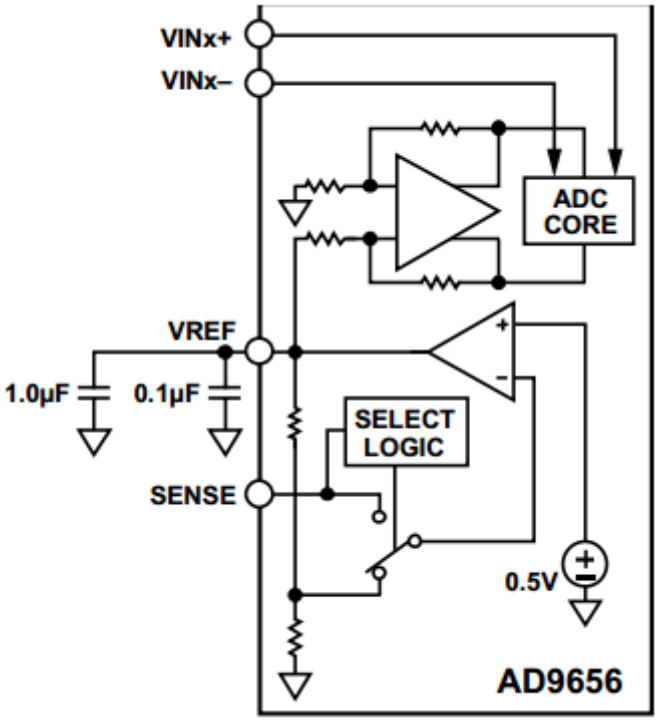


Figure 39: Reference voltage configuration 1

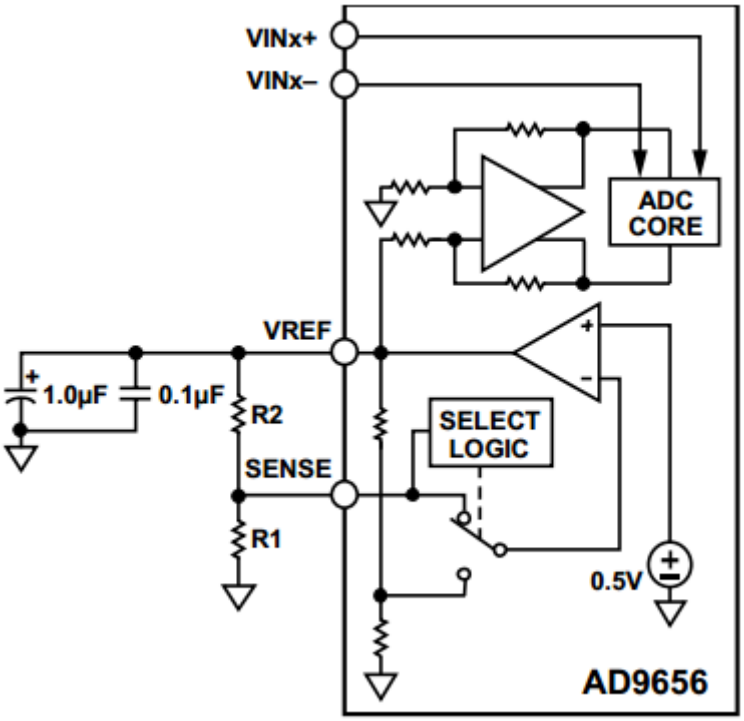


Figure 40: Reference voltage configuration 2

When using the internal reference voltage of this device to drive multiple converters to improve gain matching, the loading of the reference voltage by the other converters must be considered. Figures 41 and 42 show how loading affects the internal reference voltage.

如需利用本产品的内部基准电压来驱动多个转换器，从而提高增益的匹配度，则必须考虑到其它转换器对基准电压的负载。图 41 和图 42 显示负载如何影响内部基准电压。

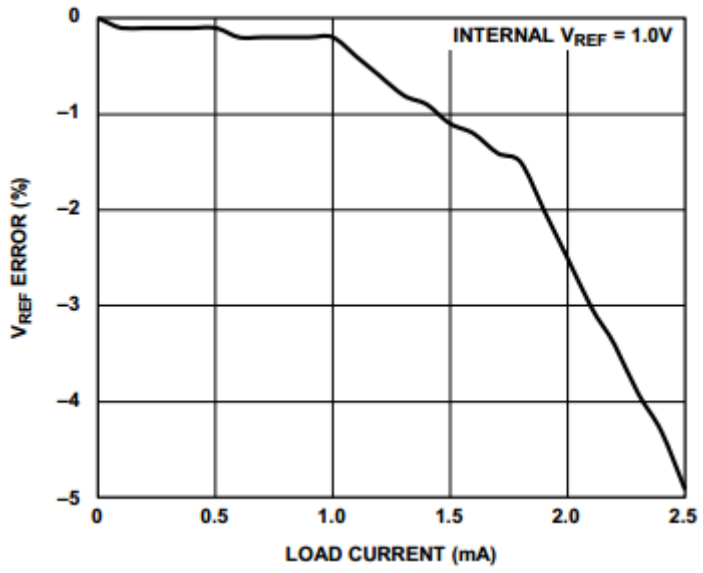


Figure 41: VREF error vs. load current (internal VREF = 1.0 V)

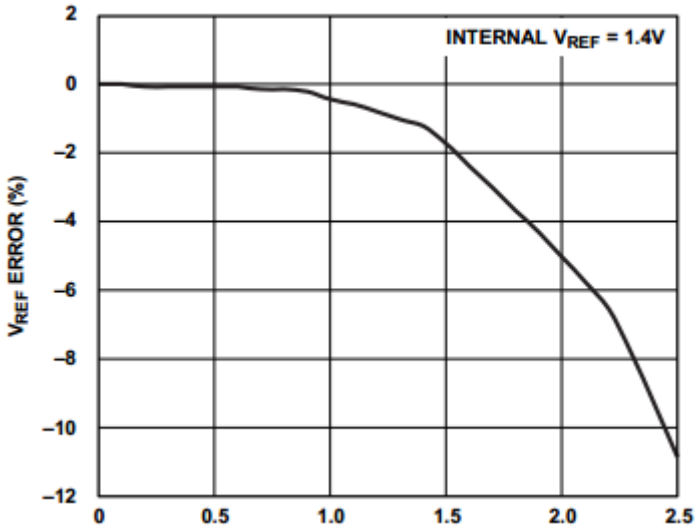


Figure 42: VREF error vs. load current (internal VREF = 1.4 V)

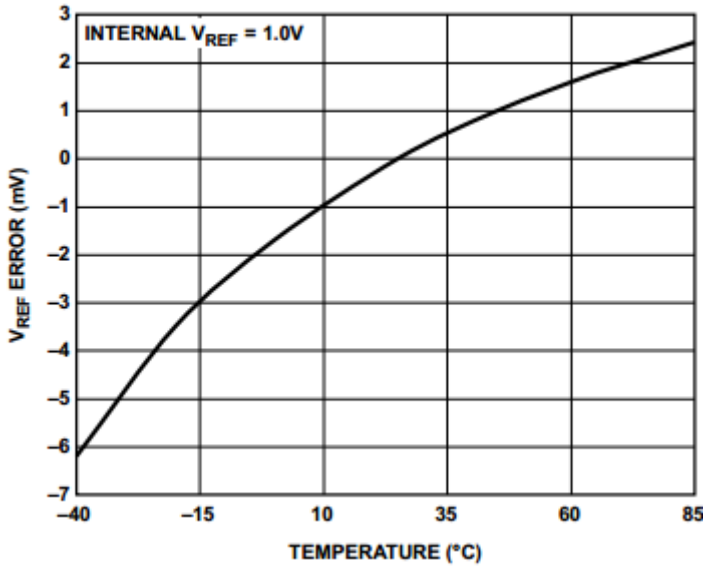


Figure 43: VREF error vs. temperature (VREF = 1.0 V typical drift)

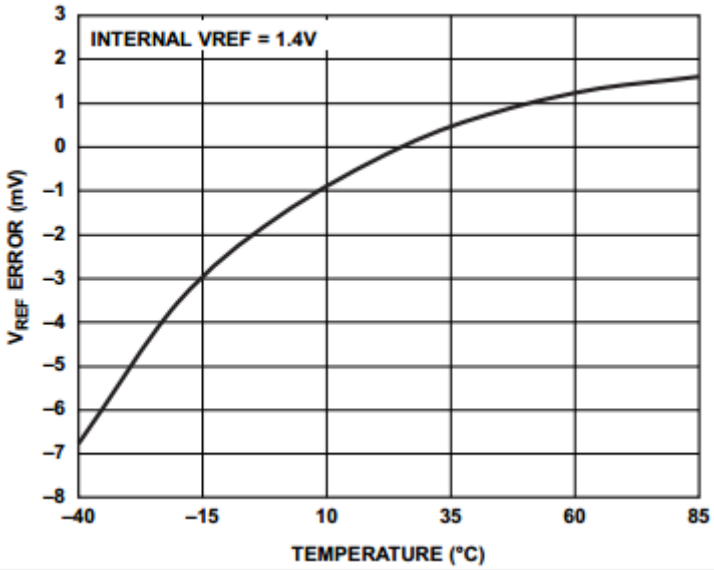


Figure 44: VREF error vs. temperature (VREF = 1.0 V typical drift)

An external reference voltage must be used to further improve ADC gain accuracy and thermal drift characteristics. Figures 43 and 44 show the typical drift characteristics of the internal reference source in 1.0 V mode and 1.4 V mode respectively. Connecting the SENSE pin to AVDD disables the internal reference source, allowing the use of an external reference source. The loading of the internal reference buffer on the external reference source is equivalent to a 7.5 kΩ load. The internal buffer generates positive and negative full-scale reference voltages for the ADC core. Floating the SENSE pin is not recommended.

必须采用外部基准电压才可能进一步提高 ADC 增益精度、改善热漂移特性。图 43 和图 44 显示内部基准电压源分别在 1.0 V 模式和 1.4 V 模式下的典型漂移特性。将 SENSE 引脚与 AVDD 相连时，可以禁用内部基准电压源，从而允许使用外部基准电压源。内部基准电压缓冲器对外部基准电压源的负载相当于 7.5 kΩ 负载。内部缓冲器为 ADC 内核生成正、负满量程基准电压。不建议悬空 SENSE 引脚。

6. Clock Input / 6、时钟输入

To fully exploit the performance of the chip, a differential signal should be used as the clock signal for the sampling clock inputs (CLK+ and CLK−) of this device. This signal is typically AC-coupled to the CLK+ and CLK− pins using a transformer or capacitors. These two pins are internally biased; no external bias is required.

为了充分发挥芯片的性能，应利用一个差分信号作为本产品采样时钟输入端(CLK+和 CLK−)的时钟信号。该信号通常使用变压器或电容器交流耦合到 CLK+和 CLK−引脚内。这两个引脚有内部偏置，无需外部偏置。

This device features a flexible clock input structure. CMOS, LVDS, LVPECL or sine-wave signals can all serve as its clock input signals. Regardless of the signal type, clock source jitter must be considered (see the jitter considerations section). Figures 45 and 46 show two preferred methods of providing clock signals to this device (clock rates up to 1 GHz before the internal clock divider). Using an RF transformer or RF balun, a single-ended signal from a low-jitter clock source can be converted to a differential signal. For clock frequencies from 125 MHz to 1 GHz, the RF balun configuration is recommended; for clock frequencies from 40 MHz to 200 MHz, the RF transformer configuration is recommended. Schottky diodes connected across the transformer/balun secondary winding can limit the clock signal into this device to approximately 0.8V peak-to-peak differential.

本产品具有灵活的时钟输入结构。CMOS、LVDS、LVPECL 或正弦波信号均可作为其时钟输入信号。无论采用哪种信号，都必须考虑到时钟源抖动(见抖动考虑部分说明)。图 45 和图 46 显示两种为本产品提供时钟信号的首选方法(内部时钟分频前的时钟速率可达 1 GHz)。利用射频变压器或射频巴伦，可将低抖动时钟源的单端信号转换成差分信号。对于 125 MHz 至 1 GHz 的时钟频率，建议采用射频巴伦配置；对于 40 MHz 至 200 MHz 的时钟频率，建议采用射频变压器配置。跨接在变压器/巴伦次级绕组上的肖特基二极管可以将输入到本产品中的时钟信号限制为约差分 0.8V 峰峰值。

This both prevents large voltage swings of the clock from feeding through to other parts of this device and preserves fast rise and fall times of the signal, which is important for achieving low-jitter performance. However, diode capacitance has an effect at frequencies above 500 MHz. Appropriate signal-limiting diodes must be carefully selected.

这样，既可以防止时钟的大电压摆幅馈通至本产品的其它部分，还可以保留信号的快速上升和下降时间，这一点对实现低抖动性能来说非常重要。但是，当频率高于 500 MHz 时，二极管电容会产生影响。必须小心选择适当的信号限幅二极管。

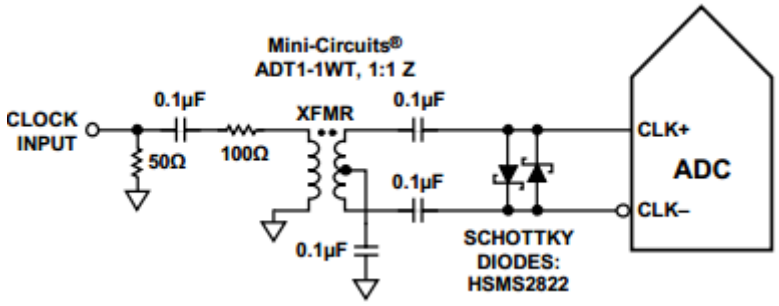


Figure 45: Transformer-coupled differential clock (frequencies up to 200 MHz)

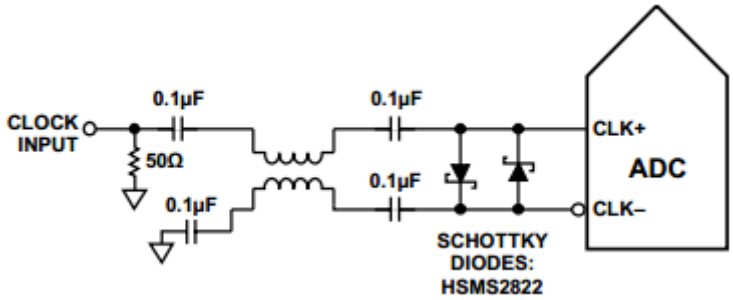


Figure 46: Balun-coupled differential clock (frequencies up to 1 GHz)

If no low-jitter clock source is available, another approach is to AC-couple a differential PECL signal to the sampling clock input pins (as shown in Figure 47). AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

如果没有低抖动的时钟源，那么，另一种方法是对差分 PECL 信号进行交流耦合，并传输至采样时钟输入引脚(如图 47 所示)。AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 时钟驱动器具有出色的抖动性能。

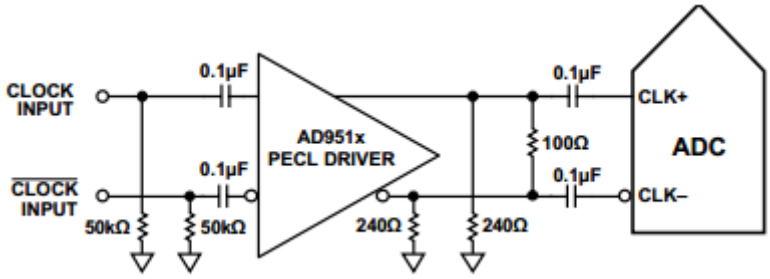


Figure 47: Differential PECL sampling clock (frequencies up to 1 GHz)

Another approach is to AC-couple a differential LVDS signal to the sampling clock input pins (as shown in Figure 48). AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

另一种方法是将差分 LVDS 信号交流耦合至采样时钟输入引脚(如图 48 所示)。AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 时钟驱动器具有出色的抖动性能。

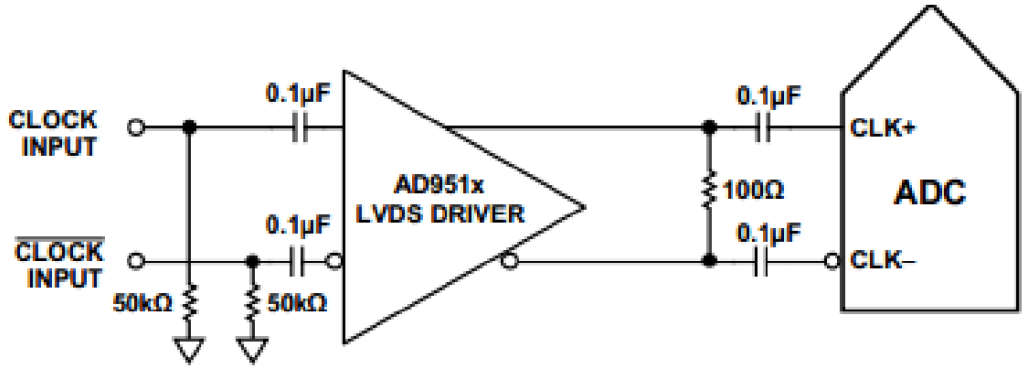


Figure 48: Single-ended 1.8 V CMOS input clock (frequencies up to 200 MHz)

7. Input Clock Divider / 7、输入时钟分频器

This device integrates an input clock divider that can divide the input clock by integer factors of 1 to 8. The clock divider of this device can be synchronized using the external SYNC input signal. By writing to bits 0 and 1 of register 0x109, the clock divider can be set to resynchronize after each SYNC signal or only after the first SYNC signal. A valid SYNC resets the divider to its initial state. This synchronization feature aligns the clock dividers of multiple devices, ensuring simultaneous input sampling.

本产品内置一个输入时钟分频器，可对输入时钟进行 1 至 8 整数倍分频。利用外部 SYNC 输入信号，可同步本产品时钟分频器。通过对寄存器 0x109 的位 0 和位 1 进行写操作，可以设置每次收到 SYNC 信号或者仅第一次收到 SYNC 信号后对时钟分频器再同步。有效 SYNC 可使分频器复位至初始状态。该同步特性可让多个器件的时钟分频器对准，从而保证同时进行输入采样。

8. Duty Cycle / 8、占空比

Typical high-speed ADCs use both clock edges to generate different internal timing signals and are therefore very sensitive to clock duty cycle. Generally, to maintain ADC dynamic performance, the clock duty cycle tolerance should be ±5%.

典型的高速 ADC 利用两个时钟边沿产生不同的内部定时信号，因此，它对时钟占空比非常敏感。通常，为保持 ADC 的动态性能，时钟占空比容差应为±5%。

This device integrates a duty cycle stabilizer (DCS) that retimes the non-sampling edge (falling edge) and provides an internal clock signal with a nominal 50% duty cycle. This feature minimizes performance degradation when the clock input duty cycle deviates from the nominal 50% by more than ±5%. Enabling the DCS function significantly improves noise and distortion performance for clock input duty cycles of 30% to 45% and 55% to 70%.

本产品内置一个占空比稳定器(DCS)，可对非采样边沿(下降沿)进行重新定时，并提供标称占空比为 50%的内部时钟信号。当时钟输入占空比偏离标称 50%占空比的幅度大于±5%额定值时，该特性可最大程度减少性能的下降。使能 DCS 功能可显著改善 30%至 45%和 55%至 70%的时钟输入占空比的噪声和失真性能。

Jitter on the input rising edge remains a concern and cannot be easily reduced by the internal stabilization circuit. In applications where the clock rate changes dynamically, the time constants associated with this loop must be considered. A wait of 1.5 µs to 5 µs is required before the DCS loop relocks to the input signal.

输入上升沿的抖动依然值得关注，且无法借助内部稳定电路来轻易减少这种抖动。在时钟速率动态改变的应用中，必须考虑与该环路相关的时间常量。在 DCS 环路重新锁定输入信号前，都需要等待 1.5 µs 至 5 µs 的时间。

9. Jitter Considerations / 9、抖动考虑

High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. Intermediate-frequency undersampling applications are especially sensitive to jitter (see Figure 49).

高速、高分辨率 ADC 对时钟输入信号的质量非常敏感。中频欠采样应用对抖动尤其敏感(见图 49)。

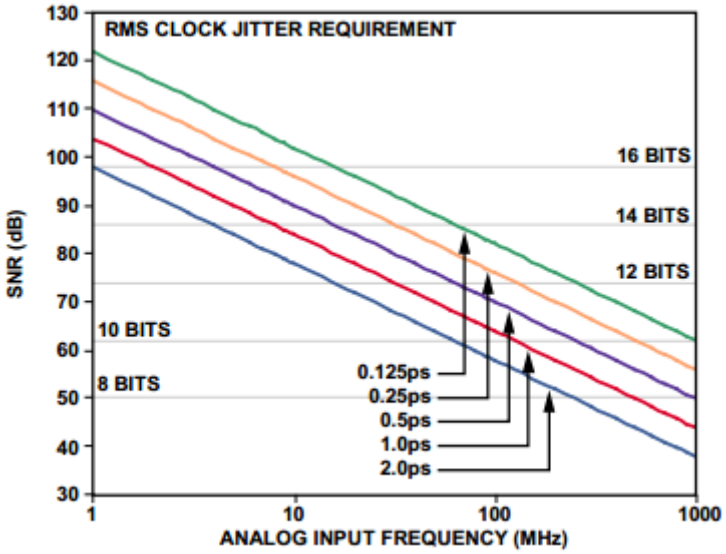


Figure 49: Ideal SNR vs. analog input frequency and jitter

When aperture jitter may affect the dynamic range of this device, the clock input signal should be treated as an analog signal. Separate the clock driver supply from the ADC output driver supply to avoid mixing digital noise into the clock signal. A low-jitter crystal-controlled oscillator provides the best clock source. If the clock signal comes from another type of clock source (via gating, frequency division, or other methods), the original clock should be used for retiming in the final step.

当孔径抖动可能影响本产品的动态范围时，应将时钟输入信号视为模拟信号。将时钟驱动器电源与 ADC 输出驱动器电源分离，以免在时钟信号内混入数字噪声。低抖动的晶体控制振荡器可提供最佳时钟源。如果时钟信号来自其它类型的时钟源(通过门控、分频或其它方法)，则需要在最后一步中利用原始时钟进行重定时。

10. Power Consumption and Power-Saving Modes / 10、功耗和省电模式

As shown in Figures 50 and 51, the power consumption of this device is proportional to its sampling rate. This device can be placed in power-saving mode via the SPI port or by setting the PDWN pin high. In power-saving mode, the typical power consumption of the ADC is 14 mW. In power-saving mode, the output drivers are in a high-impedance state. Setting the PDWN pin low returns this device to normal operating mode. Note that PDWN is referenced to the data output driver supply voltage (DRVDD) and must not exceed that supply voltage.

如图 50 和图 51 所示，本产品的功耗与其采样速率成比例关系。通过 SPI 端口或将 PDWN 引脚置位高电平，可使本产品进入省电模式。在省电模式下，ADC 的典型功耗为 14 mW。省电模式下，输出驱动器处于高阻抗状

态。将 PDWN 引脚置位低电平时，本产品返回正常工作模式。注意，PDWN 以数据输出驱动器电源电压(DRVDD)为基准，且不得高于该电源电压。

In power-saving mode, low power consumption is achieved by powering down the reference voltage source, reference voltage buffer, bias network, and clock. When entering power-saving mode, internal capacitors discharge; when returning to normal operating mode, internal capacitors must be recharged. Therefore, wake-up time depends on the time spent in power-saving mode; the shorter the time in power-saving mode, the shorter the corresponding wake-up time. Using the SPI port interface, the user can place the ADC in power-saving mode or standby mode. For shorter wake-up times, standby mode can be used, in which the internal reference voltage circuit remains powered. For more information on using these features, see the "Memory Map" section.

在省电模式下，通过关闭基准电压源、基准电压缓冲器、偏置网络以及时钟，可实现低功耗。进入省电模式时，内部电容放电；返回正常工作模式时，内部电容必须重新充电。因此，唤醒时间与处于省电模式的时间有关；处于省电模式的时间越短，则相应的唤醒时间越短。使用 SPI 端口接口时，用户可将 ADC 置于省电模式或待机模式。如需较短的唤醒时间，可以使用待机模式，该模式下内部基准电压电路处于通电状态。有关使用这些功能的更多信息，请参见"存储器映射"部分。

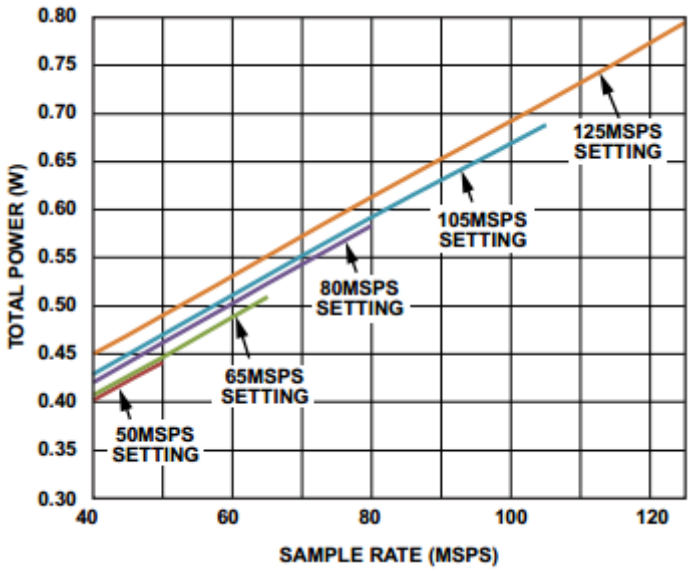


Figure 50: Total power consumption vs. fSAMPLE (fIN = 9.7 MHz, 4 channels, VREF = 1.4 V)

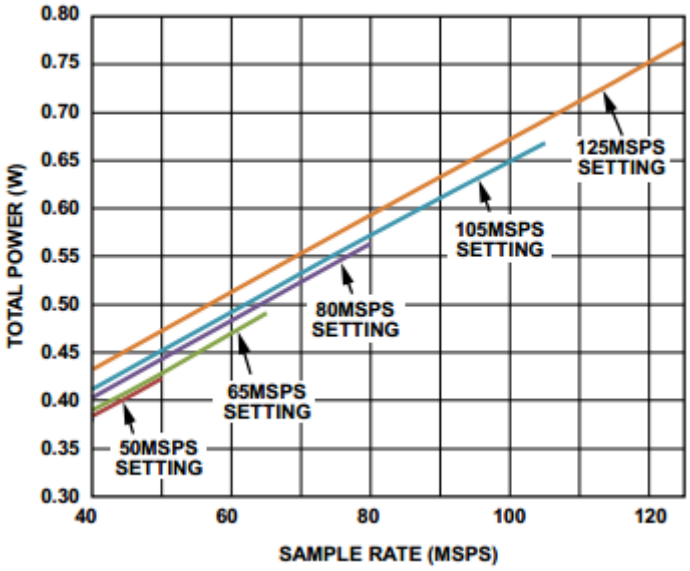


Figure 51: Total power consumption vs. fSAMPLE (fIN = 9.7 MHz, 4 channels, VREF = 1.0 V)

11. JESD204B Transmitter Top-Level Description / 11、JESD204B 发送顶层描述

12. JESD204B Overview / 12、JESD204B 概述

The digital output of this device uses the JEDEC standard (standard number: JESD204B, serial interface for data converters). JESD204B is the protocol by which this device connects to digital processing devices through a serial interface (up to 6.4 Gbps link speed). Advantages of the JESD204B interface include: less board space required for data interface routing, and smaller packages for converters and logic devices. This device supports single-lane, dual-lane and quad-lane interfaces.

本产品数字输出采用 JEDEC 标准(标准号：JESD204B，数据转换器串行接口)。JESD204B 是本产品通过串行接口(最高 6.4 Gbps 链路速度)连接数字处理设备的协议。JESD204B 接口的优势包括：数据接口路由所需电路板空间更少，以及转换器和逻辑器件的封装更小。本产品支持单通道、双通道和四通道接口。

The JESD204B data transmit module JTX combines parallel data from the ADC into data frames, and outputs serial data using 8b/10b encoding and optional data scrambling. During initial link establishment, special characters support lane synchronization; additional synchronization is achieved in the subsequent data stream. A matched external receiver is required to lock to the serial data stream and recover data and clock. For more information on the JESD204B interface, see the JESD204B standard.

JESD204B 数据发送模块 JTX 可将来自 ADC 的并行数据组合成数据帧，并使用 8b/10b 编码以及可选数据加扰技术，输出串行数据。在初始链路的建立过程中，使用特殊字符可支持通道同步；而额外的同步则在随后的数据流中实现。需要使相匹配的外部接收机锁定在串行数据流上，并恢复数据和时钟。有关 JESD204B 接口的更多信息，请参见 JESD204B 标准。

The JESD204B transmit module of this device maps the outputs of four ADCs onto the link. The link can be configured to use single, dual or quad serial differential outputs, called lanes. The JESD204B specification defines the link with multiple parameters; these parameters of the JESD204B transmitter (the outputs of this device) and the receiver must match.

本产品 JESD204B 发送模块将四个 ADC 的输出映射到链路上。链路可配置为使用单路、双路或四路串行差分输出，称为通道。JESD204B 规范用多个参数来定义链路，JESD204B 发射机(本产品的输出)和接收机的这些参数必须匹配。

A JESD204B link can be described by the following parameters:

JESD204B 链路可通过下列参数描述：

- S = samples transmitted / converter / frame period (value for this device: 1) / S = 传送的样本/单个转换器/帧周期(本产品的值为 1)
- M = number of converters (value for this device: 4) / M = 转换器数/转换器(本产品的值为 4)
- L = number of lanes / converter (value for this device: 1, 2 or 4) / L = 通道数/转换器(本产品的值为 1、2 或 4)
- N = converter resolution (value for this device: 16) / N = 转换器分辨率(本产品的值为 16)
- N' = total bits per sample (value for this device: 16) / N' = 每个样本的总位数(本产品的值为 16)
- CF = number of control words / frame clock period / converter (value for this device: 0) / CF = 控制字数/帧时钟周期/转换器(本产品的值为 0)
- CS = number of control bits / conversion sample (value for this device: 0) / CS = 控制位数/转换样本(本产品的值为 0)
- K = number of frames per multiframe (configurable on this device) / K = 每个多帧的帧数(可在本产品上配置)
- HD = high-density mode (value for this device: 0) / HD = 高密度模式(本产品的值为 0)
- F = 8-bit words / frame (value for this device: 2, 4 or 8, depending on L = 4, 2 or 1 respectively) / F = 8 位字/帧(本产品的值为 2、4 或 8，取决于相应 L 的值为 4、2 或 1)
- C = control bits (overrange, overflow, underflow; not provided in this device's default mode) / C = 控制位(超量程、上溢、下溢；本产品默认模式不提供该特性)
- T = tail bits (not provided in this device's default mode) / T = 结束位(本产品默认模式不提供该特性)
- SCR = scrambler enable/disable (configurable on this device) / SCR = 加扰器使能/禁用(可在本产品上配置)
- FCHK = checksum of JESD204B parameters (automatically calculated and stored in the register map) / FCHK = JESD204B 参数的校验和(自动计算并存储在寄存器映射中)

The default configuration of this device uses four converters and one lane. This device supports other configurations, such as combining the outputs of two or four converters into a single lane, so that data from four converters is output through two lanes. The mapping of digital output paths 0, 1, 2, 3 can be changed. These modes are set via the quick-configuration registers in the SPI register map, with additional customization options available.

本产品默认配置为使用四个转换器和一个通道。本产品支持其它配置，如将两个或四个转换器的输出组合成单通道，使得四个转换器的数据通过两个通道输出。可以改变 0、1、2、3 条数字输出路径的映射。这些模式可通过 SPI 寄存器映射中的快速配置寄存器进行设置，并且提供额外的自定义选项。

By default, the 16-bit word of each converter of this device is split into two 8-bit words (data bits are 8 bits). The first 8-bit word includes bit 0 (MSB) through bit 7, and the second 8-bit word includes bit 8 through bit 15 (LSB).

默认情况下，本产品每个转换器的 16 位字被分为两个 8 位字(数据位为 8 位)。第一个 8 位字包括位 0 (MSB)到位 7，第二个 8 位字包括位 8 到位 15 (LSB)。

The two generated 8-bit words can be scrambled. Scrambling is optional; this option avoids spectral spikes when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation 1 + x14 + x15. The descrambler in the receiver must also use a self-synchronizing version of the scrambler polynomial.

可对生成的两个 8 位字进行加扰。加扰为可选；该选项可在传输相似的数字数据模式时避免频谱尖峰。加扰器采用自同步、基于多项式的算法，由方程 1 + x14 + x15 定义。接收机中的解扰器也必须使用加扰器多项式的自同步版本。

The two 8-bit words are then encoded by the 8b/10b encoder. The 8b/10b encoder encodes 8 data bits (one 8-bit word) into a 10-bit symbol. Figure 52 shows the default data format.

之后，这两个 8 位字通过 8b/10b 编码器进行编码。8b/10b 编码器将 8 个数据位(1 个 8 位字)编码为一个 10 位的符号。图 52 显示了默认的数据格式。

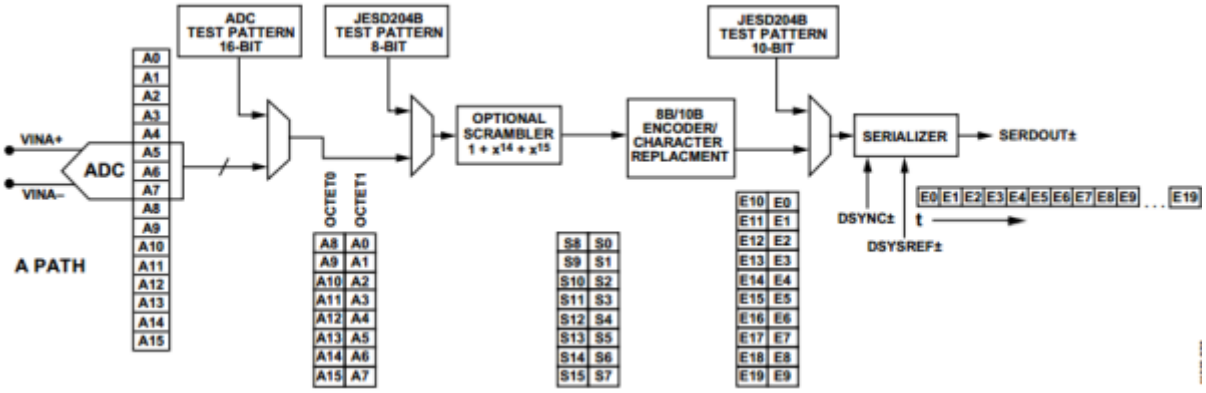


Figure 52: Digital processing of the JESD204B lanes of this device

In the data link layer, in addition to 8b/10b encoding, character replacement is used so that the receiver can monitor frame alignment. Character replacement occurs at frame and multiframe boundaries, and its implementation depends on which boundary the process occurs at and whether scrambling is enabled.

在数据链路层，除 8b/10b 编码外，还使用字符替换，以便接收机监控帧对齐。字符替换发生在帧和多帧的边界处，并且它的实现取决于该过程发生在哪个边界上，以及是否使能了加扰。

If scrambling is disabled, the following measures apply. If the last scrambled 8-bit word of the last frame in a multiframe equals the last 8-bit word of the previous frame, the transmitter replaces that last 8-bit word with the control character /A/ = /K28.3/. For other frames in the multiframe, if the last 8-bit word in the frame equals the last 8-bit word of the previous frame, the transmitter replaces that last 8-bit word with the control character /F/ = /K28.7/.

若禁用了加扰，则采用以下措施。如果多帧中最后一帧的最后一个加扰 8 位字等于上一帧的最后一个 8 位字，则发射机以控制字符/A/ = /K28.3/替换最后那个 8 位字。对于多帧中的其它帧而言，如果帧内的最后一个 8 位字等于上一帧的最后一个 8 位字，则发射机以控制字符/F/ = /K28.7/替换最后那个 8 位字。

If scrambling is enabled, the following measures apply. If the last 8-bit word of the last frame in a multiframe equals 0x7C, the transmitter replaces that last 8-bit word with the control character /A/ = /K28.3/. For other frames in the multiframe, if the last 8-bit word equals 0xFC, the transmitter replaces that last 8-bit word with the control character /F/ = /K28.7/.

若使能了加扰，则采用以下措施。如果多帧中最后一帧的最后一个 8 位字等于 0x7C，则发射机以控制字符/A/ = /K28.3/替换最后那个 8 位字。对于多帧中的其它帧而言，如果最后一个 8 位字等于 0xFC，则发射机以控制字符/F/ = /K28.7/替换最后那个 8 位字。

For more information on the JESD204B interface, see the JEDEC standard (standard number: JESD204B, July 2011).

JESD204B 接口的更多信息，请参见 JEDEC 标准(标准号：JESD204B，2011 年 7 月)。

13. JESD204B Synchronization Details / 13、JESD204B 同步详解

This device is a JESD204B Subclass 1 device, achieving link synchronization through two control signals (SYSREF and DSYNC). At the system level, multiple converter devices use a common DSYSREF and device clock (CLK) for alignment.

本产品是一款 JESD204B Subclass 1 器件，可通过两个控制信号(SYSREF 和 DSYNC)实现链路同步。在系统层面，多个转换器件利用通用 DSYSREF 和器件时钟(CLK)实现对齐。

The synchronization process is completed in three phases: code group synchronization (CGS), initial lane alignment sequence (ILAS), and data transmission. If scrambling is enabled, data bits are not actually scrambled until the data transmission phase; neither the CGS nor the ILAS phase performs scrambling.

同步过程分三阶段完成：代码组同步(CGS)、初始化通道对齐序列(ILAS)和数据传输。若使能加扰，则在数据传输阶段之前，数据位都不会真正进行加扰，CGS 和 ILAS 阶段都不执行加扰。

In the CGS phase, the JESD204B transmit module transmits /K28.5/ characters. The receiver (external logic device) must use clock and data recovery (CDR) techniques to find K28.5 characters in the input data stream.

在 CGS 阶段，JESD204B 的传送模块将传送/K28.5/字符。接收机(外部逻辑器件)必须使用时钟和数据恢复(CDR)技术，在输入数据流中找到 K28.5 字符。

Once a certain number of consecutive K28.5 characters are detected on the link lane, the receiver generates a DSYSREF edge signal so that this device's transmitted data establishes the internal local multiframe clock (LMFC) signal.

一旦在链路通道上检测到一定数量的连续 K28.5 字符，接收机便产生一个 DSYSREF 边沿信号，以便本产品的传输数据建立内部的本地多帧时钟(LMFC)信号。

The DSYSREF edge can also reset any sampling edge of the ADC to synchronize sampling instances with the LMFC. This is very important for maintaining synchronization across multiple devices.

DSYSREF 边沿还可复位 ADC 的任意采样边沿，以使采样实例与 LMFC 同步。这对于在多个器件之间保持同步而言非常重要。

The receiver or logic device deasserts the SYNC~ signal applied to DSYNC, and the transmitter module begins the ILAS phase.

接收机或逻辑器件对施加于 DSYNC 的 SYNC~信号解除置位，并且发射机模块开始执行 ILAS 阶段。

In the ILAS phase, the transmitter sends known patterns, and the receiver aligns all lane links and verifies link parameters. After SYNC~ is deasserted (goes high), the ILAS phase begins. The transmit module starts sending 4 multiframes. Pseudo-samples are inserted in the required characters to transmit complete multiframes. The 4 multiframes include:

在 ILAS 阶段中，发射机发送已知模式，接收机对齐所有通道链路并验证链路参数。SYNC~解除置位后(变为高电平)，便进入 ILAS 阶段。发送模块开始发送 4 个多帧。在所需的字符中插入伪采样，以便传送完整的多帧。4 个多帧包括：

- Multiframe 1: starts with /R/ character [K28.0], ends with /A/ character [K28.3]. / 多帧 1：以/R/字符[K28.0]开始，以/A/字符[K28.3]结束。
- Multiframe 2: starts with /R/ character, followed by /Q/ [K28.4] character, then 14 configuration 8-bit words of link configuration parameters (see Table 1), ending with /A/ character. / 多帧 2：以/R/字符开始，后接/Q/ [K28.4]字符，然后是 14 个配置 8 位字的链路配置参数(见表 1)，最后以/A/字符结束。
- Multiframe 3: same as multiframe 1. / 多帧 3：同多帧 1。
- Multiframe 4: same as multiframe 1. / 多帧 4：同多帧 1。

Table 1: 14 Configuration 8-bit Words in the ILAS Phase / 表1 ILAS 阶段的 14 个配置 8 位字

No. / 编号	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2						LID[4:0]		
3	SCR					L[4:0]		
4	F[7:0]							
5						K[4:0]		
6	M[7:0]							
7		CS[1:0]			N[4:0]			
8		SUBCLASS[2:0]				N'[4:0]		
9			JESDV[2:0]			S[4:0]		
10						CF[4:0]		
11	Reserved, don't care (RES1) / 保留，无关(RES1)							
12	Reserved, don't care (RES2) / 保留，无关(RES2)							
13	FCHK[7:0]							

In the data transmission phase, frame alignment is monitored via control characters. Character replacement is performed at the end of frames. Character replacement is performed on the transmitter when:

在数据传输阶段，通过控制字符监控帧对齐。在帧的结尾处执行字符替换。出现下列情况时，会对发送器执行字符替换：

- If scrambling is disabled, and the last 8-bit word of a frame or multiframe equals the 8-bit word of the previous frame. / 若禁用了加扰，并且帧或多帧的最后一个 8 位字等于上一帧的 8 位字。
- If scrambling is enabled, and the last 8-bit word of a multiframe equals 0x7C, or the last 8-bit word of a frame equals 0xFC. / 若使能了加扰，并且多帧的最后一个 8 位字等于 0x7C，或帧的最后一个 8 位字等于 0xFC。

14. Link Configuration Parameters / 14、链路设置参数

The following shows how to configure the JESD204B interface of this device. Steps for configuring the output include:

以下内容展示了如何配置本产品 JESD204B 接口。配置输出的步骤包括：

1. Disable the lanes before changing the configuration. / 更改配置前先禁用通道。
2. Select a quick-configuration option. / 选择一个快速配置选项。
3. Configure detailed options. / 配置详细选项。
4. Check the FCHK checksum of the JESD204B interface parameters. / 检查 JESD204B 接口参数的校验和 FCHK。
5. Set other digital output configuration options. / 设置其它数字输出配置选项。
6. Re-enable the lanes. / 再次使能通道。

Disable the lanes before changing the configuration. Before changing the JESD204B link parameters, disable the link and hold it in the reset register. This is done by writing logic 1 to register 0x5F (bit 0).

更改配置前先禁用通道。在改变 JESD204B 的链路参数前，先禁用链路并保持在复位寄存器。通过向寄存器 0x5F(位 0)写入逻辑 1，可完成此设置。

Select a quick-configuration option. Write to register 0x5E (JESD204B quick-configuration register) to select a configuration option. Configuration options and corresponding JESD204B parameter values are shown in Table 2.

选择快速配置选项。写入寄存器 0x5E(JESD204B 快速配置寄存器)以便选择配置选项。配置选项及对应的 JESD204B 参数值见表 2。

- 0x41 = 4 converters, 1 lane / 0x41 = 4 个转换器，1 个通道
- 0x42 = 4 converters, 2 lanes / 0x42 = 4 个转换器，2 个通道
- 0x44 = 4 converters, 4 lanes / 0x44 = 4 个转换器，4 个通道
- 0x21 = 2 converters, 1 lane / 0x21 = 2 个转换器，1 个通道
- 0x22 = 2 converters, 2 lanes / 0x22 = 2 个转换器，2 个通道
- 0x11 = 1 converter, 1 lane / 0x11 = 1 个转换器，1 个通道

Table 2: Quick Configuration / 表2 快速配置

JESD204B Quick Config (Reg 0x5E) / JESD204B 快速配置 (寄存器 0x5E)	M (converters, reg 0x71 [7:0]) / M(转换器数，寄存器 0x71，[7:0])	L (lanes, reg 0x6E [4:0]) / L(通道数，寄存器 0x6E，[4:0])	F (8-bit words/frame, reg 0x6F [7:0]) / F(8 位字/帧，寄存器 0x6F，[7:0])	S (samples/ADC/frame, reg 0x74 [4:0]) / S(样本/ADC/帧，寄存器 0x74，[4:0])	HD (high-density mode, reg 0x75 [7]) / HD(高密度模式，寄存器 0x75，[7])
0x41	4	1	8	1	0
0x42	4	2	4	1	0
0x44	4	4	2	1	0
0x22	2	2	2	1	0
0x21	2	1	4	1	0
0x11	1	1	2	1	0

Configure detailed options. Configure tail bits and control bits.

配置详细选项。配置结束位和控制位。

- Since N' = 16 and N = 14 (non-default configuration), each sample has 2 data bits available for transmitting additional information over the JESD204B link. Tail bits or control bits may optionally be selected. Tail bits with a value of 0b00 are used by default. / 由于 N' = 16 且 N = 14(非默认配置)，每个样本都有 2 个数据位可用于通过 JESD204B 链路传输额外信息。可选择结束位或控制位。默认使用数值为 0b00 的结束位。

- Tail bits are pseudo-data bits sent over the link to complete two 8-bit words; they carry no information about the input signal. Tail bits can be fixed zero values (default) or pseudo-random numbers (register 0x5F bit 6). / 结束位是伪数据位，通过链路发送，以使两个 8 位字完整；它不传送有关输入信号的任何信息。结束位可以是固定的零值(默认)，或伪随机数字(寄存器 0x5F 位 6)。

- One or two control bits can be selected via register 0x72 bits [7:6] to replace the tail bits. The meaning of the control bits can be set via register 0x14 bits [7:5]. / 可通过寄存器 0x72 的位[7:6]选择一个或两个控制位来代替结束位。控制位的意义可通过寄存器 0x14 的位[7:5]设置。
- Set lane identification values. / 设置通道标识值。
- JESD204B supports identifying devices and lanes with parameters. These parameters are transmitted during the ILAS phase and are accessible via internal registers. / JESD204B 支持以参数标识器件和通道。这些参数在 ILAS 阶段时传送，并且可通过内部寄存器访问。
- The three identification values are device ID (DID), module ID (BID) and lane ID (LID). DID and BID are device-specific identifications and can therefore be used to identify circuits. / 三个标识值分别是器件标识(DID)、模块标识(BID)和通道标识(LID)。DID 和 BID 属于器件专有标识，因此可用于标识电路。
- Set the number of frames K per multiframe. / 设置每个多帧的帧数目 K。
- Per the JESD204B specification, a multiframe is defined as a group of K consecutive frames, with K ranging from 1 to 32, and the number of 8-bit words is required to be between 17 and 1024. Register 0x70 (bits [4:0]) sets the K value to 32 by default. Note that the K value is the register value plus 1. / 根据 JESD204B 规范，多帧定义为一组 K 个连续帧，K 取值范围为 1 至 32，并且要求 8 位字的数量位于 17 至 1024 之间。寄存器 0x70(位[4:0])默认将 K 值设为 32。注意，K 值为寄存器值加 1。
- The K value can be changed but must satisfy certain conditions. Based on the settings in the JESD204B quick configuration, this device uses a fixed 8-bit word value for each frame [F]. K must also be a multiple of 4 and satisfy the following equation: / K 值可更改，但必须满足一定条件。基于 JESD204B 快速配置中的设定，针对每一帧[F]，本产品采用固定的 8 位字数值。K 还必须是 4 的倍数，同时满足下列方程：
- 32 ⩾ K ⩾ Ceil (17/F)
- The JESD204B specification also specifies the number of 8-bit words per multiframe, i.e., (K × F), in the range of 17 to 1024. The F value is set to a fixed value via quick configuration to ensure this relationship holds true. / JESD204B 规范还指定了每个多帧的 8 位字数，即(K x F)的范围为 17 至 1024。F 值通过快速配置设定为固定值，以确保该关系式为真。

Table 3: JESD204B Configurable Identification Values / 表3 JESD204B 可配置标识值

DID Value / DID 值	Register, Bits / 寄存器，位	Value Range / 取值范围
LID (lane 0) / LID(通道 0)	0x66, [4:0]	0…31
LID (lane 1) / LID(通道 1)	0x67, [4:0]	0…31
DID	0x64, [7:0]	0…255

DID Value / DID 值	Register, Bits / 寄存器，位	Value Range / 取值范围
BID	0x65, [3:0]	0…15

Scrambling, SCR. Scrambling can be enabled or disabled via bit 7 of register 0x6E. Scrambling is enabled by default. Per the JESD204B protocol, scrambling is only effective after the lanes complete synchronization.

加扰、SCR。可通过寄存器 0x6E 的位 7 使能或禁用加扰。默认使能加扰。根据 JESD204B 协议，加扰仅在通道完成同步后方有效。

Select lane synchronization options. Most JESD204B interface synchronization functions are enabled by default to facilitate typical applications. In some cases these features can be disabled or changed as follows:

选择通道同步选项。大部分 JESD204B 接口的同步功能均默认使能，以利于典型应用。可通过以下方式，在某些情况下禁用或更改这些特性：

- Register 0x5F (bits [3:2]) can enable ILAS, enabled by default. Additionally, to support certain specific interfaces (e.g., NMCDA-SL), the JESD204B interface can be programmed to disable the ILAS sequence or to continuously repeat the ILAS sequence. / 寄存器 0x5F(位[3:2])可使能 ILAS，默认为使能。另外，为了支持某些特定接口(如 NMCDA-SL)，JESD204B 接口可编程设置为禁用 ILAS 序列或连续重复 ILAS 序列。
- This device has some fixed JESD204B interface parameter values, as follows: / 本产品具有一些固定的 JESD204B 接口参数值，具体如下：
- [N'] = 16: 16 bits per sample (register 0x73, bits [4:0]) / [N'] = 16：每个样本的位数为 16(寄存器 0x73，位[4:0])
- [CF] = 0: 0 control words / frame clock period / number of converters (register 0x75, bits [4:0]) / [CF] = 0：控制字/帧时钟周期/转换器数为 0(寄存器 0x75，位[4:0])
- Verify read-only values: the number of lanes per link (L), the number of 8-bit words per frame (F), the number of converters (M), and the number of samples per converter per frame (S). This device calculates certain JESD204B parameter values based on other settings (particularly the quick-configuration register options). The following read-only values in the register map are used for verification. / 验证只读数值：每个链路的通道数(L)、每一帧的 8 位字数(F)、转换器数(M)和每个转换器每一帧的样本数(S)。本产品基于其它设置(特别是快速配置寄存器的选项)计算某些 JESD204B 的参数值。寄存器映射中的以下只读数值用于验证。
- [L] = number of lanes per link can be 1, 2 or 4; read this value from register 0x6E (bits [4:0]) / [L] = 每个链路的通道数可以是 1、2 或 4，从寄存器 0x6E (位[4:0])读取该值
- [F] = number of 8-bit words per frame can be 2, 4 or 8; read this value from register 0x6F (bits [7:0]) / [F] = 每一帧的 8 位字数可以是 2、4 或 8，从寄存器 0x6F(位[7:0])读取该值
- [HD] = high-density mode is 0; read from register 0x75 (bit 7) / [HD] = 高密度模式为 0，从寄存器 0x75(位 7)读取该值
- [M] = number of converters per link, default 4, but can be 1, 2 or 4; read from register 0x71 (bits [7:0]) / [M] = 每个链路的转换器数，默认为 4，但可以是 1、2 或 4；从寄存器 0x71(位[7:0])读取该值
- [S] = number of samples per converter per frame is 1; read from address 0x74 (bits [4:0]) / [S] = 每帧每个转换器的样本数为 1；从地址 0x74(位[4:0])读取该值

Check the FCHK checksum of the JESD204B interface parameters. JESD204B parameters can be verified via the FCHK checksum of the JESD204B interface parameters. Each link has its own corresponding FCHK

value. The FCHK value is transmitted during the second multiframe of ILAS and can be read via internal registers.

检查 JESD204B 接口参数的校验和 FCHK。JESD204B 参数可通过 JESD204B 接口参数的校验和[FCHK]验证。每个链路都有各自相应的 FCHK 值。FCHK 值在 ILAS 的第二个多帧时传送，并可通过内部寄存器读取。

The checksum is the modulo-256 sum of the parameters listed in the "No." column of Table 4. The checksum is calculated as follows: the parameters are summed before being packed into 8-bit words as shown in Table 4.

校验和是表 4 的"编号"列中所列参数的模 256 求和值。校验和通过如下方式计算：在参数字段如表 4 所示被封装入 8 位字之前，将其相加。

The FCHK of the lane configuration outputting data from lane 0 can be read from register 0x78. Similarly, the FCHK of the lane configuration outputting data from lane 1 can be read from register 0x79, from lane 2 from register 0x7A, and from lane 3 from register 0x7B.

从通道 0 输出数据的通道配置的 FCHK 可从寄存器 0x78 读取。类似地，从通道 1 输出数据的通道配置的 FCHK 可从寄存器 0x79 读取，从通道 2 输出数据的通道配置的 FCHK 可从寄存器 0x7A 读取，从通道 3 输出数据的通道配置的 FCHK 可从寄存器 0x7B 读取。

Table 4: JESD204B Configuration Table for ILAS and Checksum Calculation / 表4 用于 ILAS 和校验和计算的 JESD204B 配置表

No. / 编号	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2						LID[4:0]		
3	SCR					L[4:0]		
4	F[7:0]							
5						K[4:0]		
6	M[7:0]							
7		CS[1:0]			N[4:0]			
8		SUBCLASS[2:0]				N'[4:0]		
9			JESDV[2:0]			S[4:0]		
10						CF[4:0]		

Set other digital output configuration options. Other data format controls include:

设置其它数字输出配置选项。其它数据格式控制包括：

- Serial output data polarity inversion: register 0x60 bit 1 / 串行输出数据极性反转：寄存器 0x60 的位 1
- ADC data format (offset binary or two's complement): register 0x14 bits [1:0] / ADC 数据格式(偏移二进制或二进制补码)：寄存器 0x14 的位[1:0]
- Options for interpreting signals on DSYSREF and DSYNC: register 0x3A bits [4:3] / 解读 DSYSREF 和 DSYNC 上信号的选项：寄存器 0x3A 的位[4:3]
- Options for remapping converter (logical lane) and SERDOUTx± (physical lane) assignments: registers 0x82 and 0x83. Figure 53 shows a simplified functional block diagram. / 重映射转换器(逻辑通道)和 SERDOUTx±(物理通道)分配的选项：寄存器 0x82 和寄存器 0x83。图 53 给出了简化功能框图。

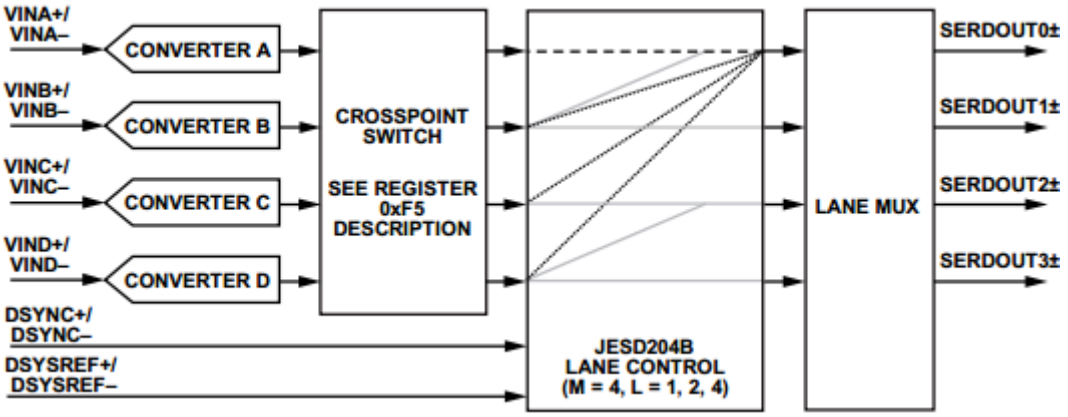


Figure 53: Simplified functional block diagram of the transmit link of this device

Re-enable the lanes after configuration. After changing JESD204B link parameters, the link lanes should be enabled to begin synchronization. This is done by writing logic 0 to register 0x5F (bit 0).

配置后再使能通道。更改 JESD204B 链路参数后，应使能链路通道以便开始同步。通过向寄存器 0x5F(位 0)写入逻辑 0，可完成此设置。

15. Frame and Lane Alignment Monitoring and Correction / 15、帧和通道的排列监控与校正

Frame alignment monitoring and correction are part of the JESD204B specification. A 16-bit word requires two 8-bit words to complete transmission of all data. Two 8-bit words (MSB and LSB, F = 2) form one frame. Under normal operating conditions, frame alignment monitoring is achieved through alignment characters; frame tails can be inserted when certain conditions are met. Table 5 summarizes the conditions under which character insertion can occur, and the expected characters in various operating modes. If lane synchronization is enabled, the replacement character value depends on whether the 8-bit word is at the tail of a single frame or at the tail of a multiframe.

帧排列监控和校正都属于 JESD204B 规范的部分内容。16 位字需要占用两个 8 位字才能完成所有数据的传送。两个 8 位字(MSB 和 LSB，F = 2)组成一帧。正常工作条件下，通过排列字符实现帧排列监控；满足一定条件时可插入帧的尾部。表 5 总结了可进行字符插入的条件，以及各种工作模式下的期望字符。若使能通道同步，则替换字符值取决于 8 位字是位于单帧的尾部，还是位于多帧的尾部。

By correctly receiving the replacement characters, the receiver can remain synchronized to frame boundaries in different operating modes.

通过正确接收替换字符，接收机可保证在不同工作模式下依然与帧边界同步。

Table 5: Conditions for Character Insertion / 表5 字符插入的条件

Scrambling / 加扰	Lane Sync / 通道同步	Character Requiring Replacement / 需要替换的字符	Is Last 8-bit Word of Multiframe / 是否为多帧中的最后 8 位字	Replacement Character / 替换字符
Off / 关	On / 开	Last 8-bit word repeats previous frame content / 最后 8 位字重复前一帧内容	No / 否	K28.7
Off / 关	On / 开		Yes / 是	K28.3

Scrambling / 加扰	Lane Sync / 通道同步	Character Requiring Replacement / 需要替换的字符	Is Last 8-bit Word of Multiframe / 是否为多帧中的最后 8 位字	Replacement Character / 替换字符
		Last 8-bit word repeats previous frame content / 最后 8 位字重复前一帧内容		
Off / 关	Off / 关	Last 8-bit word repeats previous frame content / 最后 8 位字重复前一帧内容	N/A / 不适用	K28.7
On / 开	On / 开	Last 8-bit word equals D28.7 / 最后 8 位字等于 D28.7	No / 否	K28.3
On / 开	On / 开	Last 8-bit word equals D28.3 / 最后 8 位字等于 D28.3	Yes / 是	K28.7
On / 开	Off / 关	Last 8-bit word equals D28.7 / 最后 8 位字等于 D28.7	N/A / 不适用	

Note: Table 5 as extracted from the original PDF is partially garbled (replacement-character column misaligned in the source text extraction); kept as close to the original as possible. / 注：表5 从原 PDF 提取时部分错位（替换字符列在源文本中错位），已尽量按原文还原。

16. Digital Outputs and Timing / 16、数字输出和时序

At power-up, this device defaults to differential digital outputs. The driver current comes from the chip, setting the output current of each output to a nominal 4 mA. Each output has a 100K dynamic internal termination resistor to reduce reflection interference.

本产品上电时，默认具有差分数字输出。驱动器电流来自芯片，并将各输出端的输出电流设置为标称值 4 mA。每个输出都具有 100K 的动态内部端接电阻，可降低反射干扰。

Placing a 100 K differential termination resistor at the input of each receiver achieves a nominal 600 mV p-p receiver differential swing (see Figure 54). Single-ended 50 K termination resistors may also be used. When using single-ended termination resistors, the termination voltage must be DRVDD/2; additionally, AC-coupling capacitors terminated to any single-ended voltage may be used.

在每个接收机的输入端放置一个 100 K 差分端接电阻，可实现标称 600 mV p-p 的接收机差分摆幅(见图 54)。也可使用单端 50 K 端接电阻。使用单端端接电阻时，终端电压必须为 DRVDD/2；此外，还可使用端接至任意单端电压的交流耦合电容。

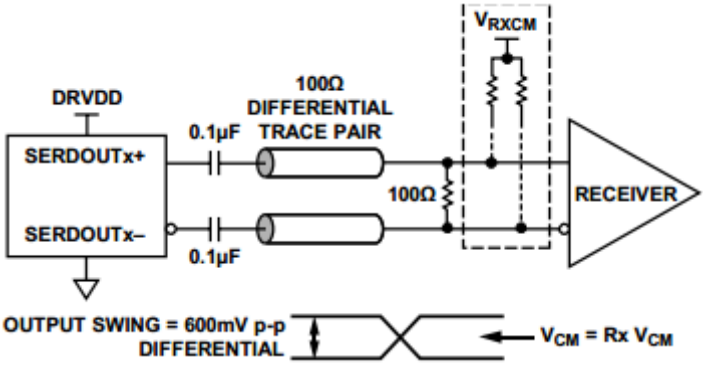


Figure 54: AC-coupled digital output termination example

The digital outputs of this device can interface with custom ASICs and FPGA receivers to achieve excellent switching performance in high-noise environments. A single point-to-point network topology is recommended, with a single 100 K differential termination resistor placed as close to the receiver as possible. For DC-coupled connections (as shown in Figure 55), the common-mode digital output automatically biases itself to the middle of the receiver's supply (i.e., when the receiver supply is 1.8 V, the common-mode voltage is 0.9 V). For receivers whose logic levels are outside the DRVDD supply boundaries, AC-coupled connections are used. Place a 0.1 µF capacitor on each output pin and use a 100 K differential termination resistor near the receiver.

本产品数字输出可与定制的 ASIC 和 FPGA 接收器接口，从而在高噪声环境中实现出色的开关性能。推荐使用单一点到点网络拓扑结构，并将单个 100 K 差分端接电阻尽可能靠近接收器放置。若使用了直流耦合连接(如图 55)，则共模数字输出可自动使自身偏置到接收机的电源中间位置(即接收机电源为 1.8 V 时，共模电压为 0.9 V)。对于逻辑电平不在 DRVDD 电源边界范围内的接收机，则使用交流耦合连接。在每个输出引脚上放置一个 0.1 µF 电容，并在靠近接收机处使用 100 K 差分端接电阻。

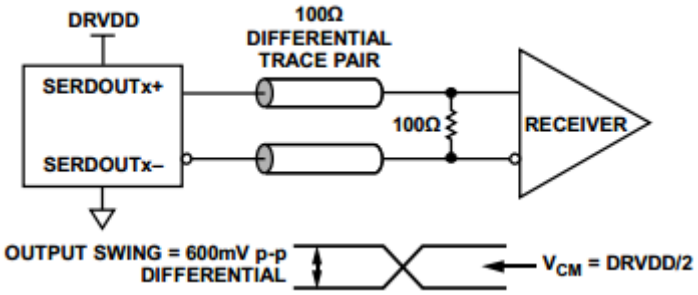


Figure 55: DC-coupled digital output termination example

If there is no far-end receiver termination resistor, or if differential trace routing is poor, timing errors may result. To avoid timing errors, it is recommended that trace lengths not exceed 6 inches, and differential output traces should be routed as close to each other as possible and of equal length.

如果没有远端接收机端接电阻，或者差分走线布线不佳，可能会导致时序错误。为避免产生时序错误，建议走线长度不要超过 6 英寸，差分输出走线应尽可能彼此靠近且长度相等。

Figure 56 shows an example of the digital output data eye diagram, time interval error (TIE) jitter histogram, and bathtub curve when the lanes of this device operate at 6.4 Gbps. Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs to drive longer traces. Using this option provides DRVDD supply power consumption.

图 56 显示本产品通道工作在 6.4 Gbps 时的数字输出数据眼图、时间间隔误差(TIE)抖动直方图，以及浴盆曲线的示例。附加 SPI 选项允许用户进一步提高所有四路输出的输出驱动器电压摆幅，从而驱动更长的走线。使用此选项会提供 DRVDD 电源的功耗。

The output data format defaults to two's complement. To change the output data format to offset binary, see the memory map section and register 0x14.

输出数据格式默认为二进制补码。若要将输出数据格式变为偏移二进制，请参阅存储器映射部分和寄存器 0x14。

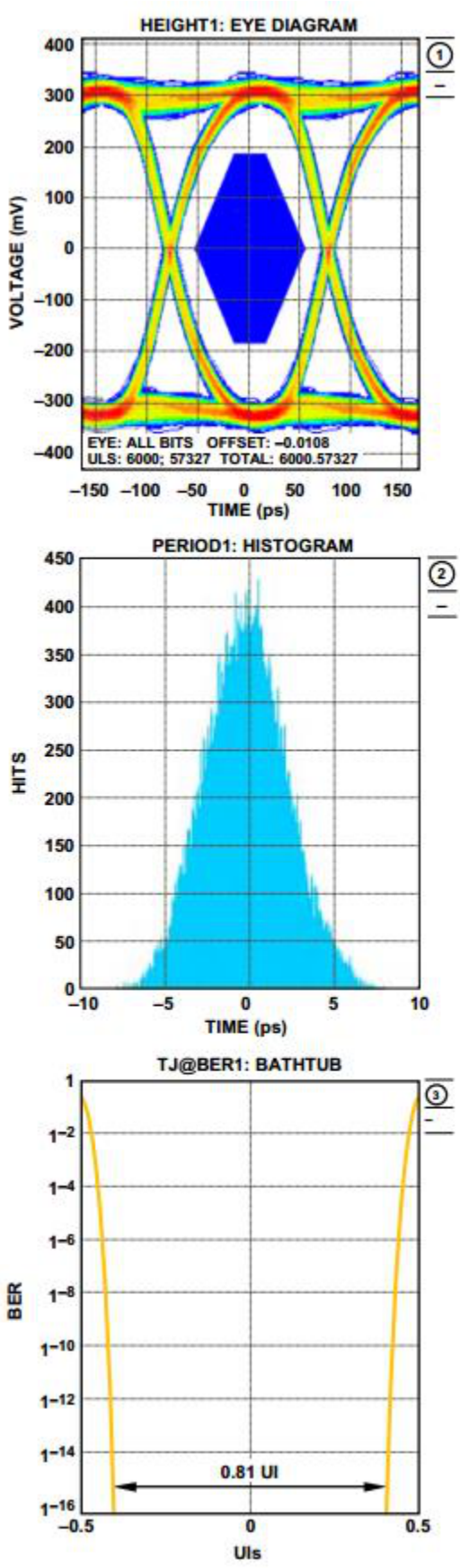


Figure 56: Digital output data eye diagram, histogram and bathtub plot of this device (100 K external termination resistor at 6.4 Gbps)

Registers / 寄存器

1. Reading the Memory Map Register Table / 1、读取存储器映射寄存器表

Each row of the memory map register table has 8 bits. The memory map is roughly divided into three sections: chip configuration registers (addresses 0x00 to 0x02), channel index and transfer registers (addresses 0x05 and 0xFF), and ADC function registers including settings, control and test (addresses 0x08 to 0x10A).

存储器映射寄存器表的每一行有 8 位。存储器映射大致分为三个部分：芯片配置寄存器(地址 0x00 至地址 0x02)、通道索引和传送寄存器(地址 0x05 和地址 0xFF)，以及 ADC 功能寄存器，包括设置、控制和测试(地址 0x08 至地址 0x10A)。

The memory map register table (see Table 6) records each hexadecimal address and its hexadecimal default value. The bit 7 (MSB) column is the starting bit for a given hexadecimal default value. For example, the output mode register (address 0x14) has a hexadecimal default value of 0x01. This indicates bit 0 = 1, while all other bits are 0. This setting is the default output format value (two's complement).

存储器映射寄存器表(见表 6)记录了每个十六进制地址及其十六进制默认值。位 7 (MSB)栏为给定十六进制默认值的起始位。例如，输出模式寄存器(地址 0x14)的十六进制默认值为 0x01。这表明，位 0=1，而其余位均为 0。此设置是默认输出格式值(二进制补码)。

2. Disabled and Reserved Locations / 2、禁用位置和保留位置

This device does not support all addresses and bits not included in Table 6. Unused bits at valid address locations should be written with 0. Write operations to these locations are only permitted when only some bits at the address (e.g., address 0x18) are disabled. If an entire address (e.g., address 0x13) is disabled, no write operation should be performed to that address.

此器件不支持表 6 中未包括的所有地址和位。应向有效地址位置的未使用位写入 0。在该地址(例如：地址 0x18)仅有部分位处于禁用状态时，才可以对这些位置进行写操作。如果整个地址(例如地址 0x13)禁用，则不应对该地址进行写操作。

3. Default Values / 3、默认值

After reset of this device, key registers are loaded with default values. The memory map register table (see Table 6) lists the default values of each register.

本产品复位后，关键寄存器将载入默认值。存储器映像寄存器表(见表 6)列出了各寄存器的默认值。

4. Logic Levels / 4、逻辑电平

The terminology for logic levels is explained below:

以下是逻辑电平的术语说明：

- "Set" means "set a bit to logic 1" or "write logic 1 to a bit". / "置位"指"将某位设置为逻辑 1"或"向某位写入逻辑 1"。

- "Clear bit" means "set a bit to logic 0" or "write logic 0 to a bit". / "清除位"指"将某位设置为逻辑 0"或"向某位写入逻辑 0"。

5. Channel-Specific Registers / 5、特定通道寄存器

Different values can be programmed for certain functions of each channel. In these cases, channel address locations are replicated internally for each channel. These registers and corresponding bits are referred to as local registers in Table 6. By setting channel 0, channel 1, channel 2 or channel 3 bits of register 0x05, these local registers and corresponding bits can be accessed. If all four bits are set, subsequent write operations affect the registers of all four channels. In a read cycle, only one channel is set, and a read operation is performed on 1 of the 4 registers. If all bits are set in an SPI read cycle, the device returns the value of channel 0. The global registers and corresponding bits given in Table 6 affect the characteristics of the entire device and channels, and each channel cannot be set separately. Settings in register 0x05 do not affect the values of global registers and corresponding bits.

可通过编程为每个通道的某些功能设置不同的值。在这些情况下，可在内部为每个通道复制通道地址位置。这些寄存器及相应的位在表 6 中被称为局部寄存器。通过设置寄存器 0x05 的通道 0、通道 1、通道 2 或通道 3 位，可访问这些局部寄存器及相应位。如果这四个位均置位，后续写操作将影响所有四个通道的寄存器。在一个读周期内，仅设置一个通道，对 4 个寄存器中的 1 个执行读操作。如果在一个 SPI 读周期内置位所有位，则器件返回通道 0 的值。表 6 给出的全局寄存器及相应位会影响整个器件和通道的特性，不允许分别设置每个通道。寄存器 0x05 中的设置不影响全局寄存器及相应位的值。

6. Channel-Specific Registers (duplicate heading kept verbatim from original) / 6、特定通道寄存器

Different values can be programmed for certain functions of each channel. In these cases, channel address locations are replicated internally for each channel. These registers and corresponding bits are referred to as local registers in Table 6. By setting channel 0, channel 1, channel 2 or channel 3 bits of register 0x05, these local registers and corresponding bits can be accessed. If all four bits are set, subsequent write operations affect the registers of all four channels. In a read cycle, only one channel is set, and a read operation is performed on 1 of the 4 registers. If all bits are set in an SPI read cycle, the device returns the value of channel 0. The global registers and corresponding bits given in Table 6 affect the characteristics of the entire device and channels, and each channel cannot be set separately. Settings in register 0x05 do not affect the values of global registers and corresponding bits.

可通过编程为每个通道的某些功能设置不同的值。在这些情况下，可在内部为每个通道复制通道地址位置。这些寄存器及相应的位在表 6 中被称为局部寄存器。通过设置寄存器 0x05 的通道 0、通道 1、通道 2 或通道 3 位，可访问这些局部寄存器及相应位。如果这四个位均置位，后续写操作将影响所有四个通道的寄存器。在一个读周期内，仅设置一个通道，对 4 个寄存器中的 1 个执行读操作。如果在一个 SPI 读周期内置位所有位，则器件返回通道 0 的值。表 6 给出的全局寄存器及相应位会影响整个器件和通道的特性，不允许分别设置每个通道。寄存器 0x05 中的设置不影响全局寄存器及相应位的值。

7. Register Addresses / 7、寄存器地址

This device uses a 3-wire interface with 16-bit addressing. Bits 0 and 7 of register 0x00 are set to 0, bits 3 and 4 are set to 1. When bit 5 of register 0x00 is set to 1, the SPI enters soft reset, all user registers return to

default values, and bit 2 is automatically cleared to 0. After power-up, complete the register reset operation first.

本产品采用 3 线接口和 16 位寻址方式。寄存器 0x00 的位 0 和位 7 置 0，位 3 和位 4 置 1。当寄存器 0x00 的位 5 置 1 时，SPI 进入软复位，所有用户寄存器恢复默认值，位 2 自动清 0。上电后，请先完成寄存器复位操作。

Table 6: Memory Map Registers (SPI registers/bits not marked "local" are "global" registers/bits) / 表 6 存储器映射寄存器(未标记为"局部"的 SPI 寄存器/位为"全局"寄存器/位)

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
0x00	SPI port configuration / SPI端口配置	0	LSB first / LSB优先	Soft reset / 软复位	1	1	Soft reset / 软复位	LSB first / LSB优先	0	0x18	
0x01	Chip ID / 芯片ID	8-bit chip ID [7:0]; this device = 0xC0 (4 channels, 16-bit, 125 MSPS, JESD204B) / 8位芯片ID[7:0]；本产品 = 0xC0(四通道、16位、125 MSPS、JESD204B)	0xC0	Read only / 只读							
0x02	Chip grade / 芯片等级	Disabled / 禁用	Speed grade ID [6:4]; 110 = 125 MSPS / 速度等级ID[6:4]；110 = 125 MSPS	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	0x60	Read only / 只读		
0x05	Device index / 器件索引	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Data channel 3 / 数据通道3	Data channel 2 / 数据通道2	Data channel 1 / 数据通道1	Data channel 0 / 数据通道0	0x0F	
0xFF	Transfer / 传输	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Transfer register 0x100 override (self-clearing) / 启动寄存器 0x100 覆盖(自清零)	0x00	

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
0x08	Power mode / 功耗模式	Disabled / 禁用	Disabled / 禁用	PDWN pin function: 0 = full power-down, 1 = standby / PDWN 引脚功能：0 = 完全掉电，1 = 待机	JTX standby mode: 0 = ignore standby, 1 = do not ignore standby / JTX 待机模式：0 = 忽略待机，1 = 不忽略待机	Reserved / 保留	Power mode: 00 = normal operation, 01 = full power-down, 10 = standby, 11 = digital reset / 功耗模式：00 = 正常工作，01 = 完全掉电，10 = 待机，11 = 数字复位	0x00			
0x09	Clock / 时钟	Disabled / 禁用	0	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Duty cycle stabilizer: 0 = off, 1 = on / 占空比稳定器：0 = 关，1 = 开	0x00		
0x0A	PLL_STATUS	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	PLL lock status bit: 0 = PLL unlocked, 1 = PLL locked; JTX link status: 0 = not ready, 1 = ready / PLL 锁定状态位：0 = PLL 未锁定，1 = PLL 锁定；JTX 链路状态：0 = 未	Read only / 只读		

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
								就绪，1 = 就绪			
0x0B	Clock divider / 时钟分频器	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Clock divide ratio [2:0]: 000 = divide by 1, 001 = divide by 2, 010 = divide by 3, 011 = divide by 4, 100 = divide by 5, 101 = divide by 6, 110 = divide by 7, 111 = divide by 8 / 时钟分频比[2:0]：000 = 1分频，001 = 2分频，010 = 3分频，011 = 4分频，100 = 5分频，101 = 6分频，110 = 7分频，111 = 8分频	0x00			
0x0C	Enhancement control / 增强控制	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Chopping mode: 0 = off, 1 = on / 斩波模式：0 = 关，1 = 开	Disabled / 禁用	Disabled / 禁用	0x00	
0x0D	Test mode (local, except PN sequence reset) / 测试模式(局部，PN 序列复位除外)	User input test mode: 00 = single pseudo-random, 01 = alternating pseudo-random, 10 = single one-time, 11 = alternating one-time (only affects user input test mode bits [3:0] = 1000) / 用户输入测试模式：00 = 单一伪随机，01 = 交替伪随机，10 = 单一一次，11 = 交替一次(仅影响用户输入测试模式位[3:0] = 1000)	Reset PN long sequence generator / 复位 PN 长序列发生器	Reset PN long sequence generator / 复位PN长序列发生器	Output test mode [3:0] (local): 0000 = off (default), 0001 = midscale short, 0010 = positive full-scale (FS), 0011 = negative FS, 0100 = alternating checkerboard, 0101 = PN23 sequence, 0110 = PN9 sequence, 0111 = 1/0 word toggle, 1000 = user input, 1001 = 1/0 bit toggle, 1010 = 1× sync, 1011 = 1-bit high, 1100 = mixed bit frequency / 输出测试模式3:0：0000 = 关(默认)，0001 = 中间电平短，0010 = 正满量程(FS)，0011 = 负FS，0100 = 交替棋盘形式，0101 = PN23序列，0110 = PN9序列，	0x00	When set, test data replaces normal data at output pins / 置1时，测试数据将取代正常数据被置于输出引脚上				

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
					0111 = 1/0字反转，1000 = 用户输入，1001 = 1/0位反转，1010 = 1×同步，1011 = 1位高电平，1100 = 混合位频率						
0x10	Offset adjust (local) / 失调调整(局部)	8-bit device offset adjust [7:0] (local); offset adjust in LSB units, from +127 to −128 (two's complement format) / 8位器件失调调整7:0；失调调整以LSB为单位，从+127到−128(二进制补码格式)	0x00	Device offset adjust / 器件失调调整							
0x14	Output mode / 输出模式	JTX CS mode: 000 = {overrange||underrange, valid flag}, 001 = {overrange, underrange}, 010 = {overrange|| underrange, empty}, 011 = {empty, valid flag}, 100 = {empty, empty}, others = {overrange|| underrange, valid flag} / JTX CS模式：000 = {超量程||欠量程，有效标志}，001 = {超量程，欠量程}，010 = {超量程||欠量程，空}，011 = {空，有效标志}，100 = {空，空}，其他 = {超量程||欠量程，有效标志}	ADC output valid flag: 0 = output valid, 1 = output invalid (local) / ADC 输出有效标志：0 = 输出有效，1 = 输出无效(局部)	Disabled / 禁用	Disabled / 禁用	Output format: 0 = offset binary, 1 = two's complement / 输出格式：0 = 偏移二进制，1 = 二进制补码	0x01				
0x15	Output adjust / 输出调整	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Typical CML differential output drive level: 000 = 473 mV p-p, 001 = 524 mV p-p, 010 =	0x03			

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
							574 mV p-p, 011 = 621 mV p-p (default), 100 = 667 mV p-p, 101 = 716 mV p-p, 110 = 763 mV p-p, 111 = 811 mV p-p / 典型CML差分输出驱动电平：000 = 473 mV p-p，001 = 524 mV p-p，010 = 574 mV p-p，011 = 621 mV p-p(默认)，100 = 667 mV p-p，101 = 716 mV p-p，110 = 763 mV p-p，111 = 811 mV p-p				
0x16	Clock phase control / 时钟相位控制	Disabled / 禁用	Input clock phase adjust [2:0] (value is the number of input clock cycles of phase delay) / 输入时钟相位调整2:0	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	0x00			
0x18	Input range select / 输入范围选择	Internal VREF adjust [1:0]: 00 = 1.0 V, 01 = 1.2 V, 10 = 1.3 V, 11 = 1.4 V / 内部VREF调整[1:0]：00 = 1.0 V，01 = 1.2 V，10 = 1.3 V，11 = 1.4 V	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Differential range adjust: 000 = 50% of nominal, 001 = 57% of nominal, 010 = 67% of	0x04				

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
						nominal, 011 = 80% of nominal, 100 = nominal value / 差分范围调整：000 = 正常值 50%，001 = 正常值57%，010 = 正常值 67%，011 = 正常值80%，100 = 正常值					
0x19	User test code 1 LSB / 用户测试码1 LSB	User test code 1 [7:0] / 用户测试码1[7:0]	0x00								
0x1A	User test code 1 MSB / 用户测试码1 MSB	User test code 1 [15:8] / 用户测试码1[15:8]	0x00								
0x1B	User test code 2 LSB / 用户测试码2 LSB	User test code 2 [7:0] / 用户测试码2[7:0]	0x00								
0x1C	User test code 2 MSB / 用户测试码2 MSB	User test code 2 [15:8] / 用户测试码2[15:8]	0x00								
0x21		Disabled / 禁用			Disabled / 禁用		Disabled / 禁用			0x00	

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
	FLEX_SERIAL_CONTROL		Disabled / 禁用	Disabled / 禁用		PLL low-rate mode: 0 = lane rate ⩾ 2 Gbps, 1 = lane rate < 2 Gbps / PLL低速率模式：0 = 通道速率 ⩾ 2 Gbps，1 = 通道速率 < 2 Gbps		Disabled / 禁用	Disabled / 禁用		
0x22	FLEX_SERIAL_CH_STAT	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Lane power-down (local) / 通道掉电 (局部)	0x00	
0x3A	SYSREF_CTRL	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Normal mode / 普通模式，1 = realign lanes on each DSYNC± activation / 每次激活 DSYNC± 时重新对齐通道	0 = realign lanes only when DSYSREF± causes counter resync, 1 = realign lanes on each DSYNC± / 0 = 仅当 DSYSREF± 引起计数器重新同步时重新对齐通道，1 = 每个 DSYNC± 上重新对齐通道	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	0x00
0x3B	REALIGN_PATTERN_CTRL	When aligning a lane, write this pattern code to FIFO: 00 = lane output all 0; 55 = lane output alternating pattern code / 对齐一个通道时，将此模式码写入FIFO：00	0x55								

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
		= 通道输出全0；55 = 通道输出交替模式码									
0x5E	JESD204B quick configuration / JESD204B 快速配置	0x41 = 4 converters, 1 lane; 0x42 = 4 converters, 2 lanes; 0x44 = 4 converters, 4 lanes; 0x22 = 2 converters, 2 lanes; 0x21 = 2 converters, 1 lane; 0x11 = 1 converter, 1 lane / 0x41 = 4个转换器、1个通道；0x42 = 4个转换器、2个通道；0x44 = 4个转换器、4个通道；0x22 = 2个转换器、2个通道；0x21 = 2个转换器、1个通道；0x11 = 1个转换器、1个通道	0x00	Self-clearing, always reads back 0x00 / 自清零，始终读出 0x00							
0x5F	JESD204B link control 1 / JESD204B 链路控制1	Disabled / 禁用	Tail bit mode: 0 = fill 0, 1 = fill PN sequence bits / 结束位模式：0 = 填充 0，1 = 填充 9 位PN序列	JTX transport layer test: 0 = not enabled, 1 = transport layer test enabled / JTX传输层测试：0 = 未使能，1 = 传输层测试使能	Multiframe alignment character insertion: 0 = disabled, 1 = enabled / 多帧对齐字符插入：0 = 禁用，1 = 使能	ILAS mode: 00 = ILAS disabled, 01 = ILAS enabled (normal mode), 11 = ILAS always on (test mode) / ILAS 模式：00 = ILAS禁用，01 = ILAS使能(正常模式)，11 = ILAS始终开启(测试模式)	Frame alignment character insertion: 0 = enabled, 1 = disabled / 帧对齐字符插入：0 = 使能，1 = 禁用	0 = JTX link enabled, 1 = JTX link disabled / 0 = JTX 链路使能，1 = JTX 链路禁用	0x14		
0x60	JESD204B link control 2 /	Reserved / 保留	DSYNC± pin invert: 0 = not	DSYNC± pin input offset: 0 =	Disabled / 禁用	Disabled / 禁用	JTX output invert: 0 = normal, 1 = inverted / JTX输出反	Reserved / 保留	0x10		

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
	JESD204B 链路控制2		inverted, 1 = inverted / DSYNC± 引脚反转：0 = 不反转，1 = 反转	disabled, 1 = enabled / DSYNC± 引脚输入偏置：0 = 禁用，1 = 使能			转：0 = 正常，1 = 反转				
0x61	JESD204B link control 3 / JESD204B 链路控制3	Reserved / 保留	Reserved / 保留	Test data injection point: 01 = inject 10-bit data at 8b/10b encoder output, 10 = 8-bit data at scrambler input / 测试数据注入点：01 = 8b/10b编码器输出时注入10位数据，10 = 加扰输入时的8位数据	JTX test mode codes: 0000 = normal operation (test mode disabled), 0001 = alternating checkerboard, 0010 = 1/0 word toggle, 0011 = PN23 PN sequence, 0100 = PN9 PN sequence, 0101 = continuous/repeated user test mode, 0110 = single user test mode, 0111 = reserved, 1000 = modified RPAT test sequence (8-bit data only), 1100 = PN7 PN sequence, 1101 = PN15 PN sequence, other settings unused / JTX 测试模式码：0000 = 正常工作(测试模式禁用)，0001 = 交替棋盘形式，0010 = 1/0字交替，0011 = PN 序列为PN23，0100 = PN序列为 PN9，0101 = 连续/重复用户测试模式，0110 = 单用户测试模式，0111 = 保留，1000 = 更改的 RPAT 测试序列(仅 8 位数据)，1100 = PN序列为PN7，1101 = PN序列为PN15，其他设置未使用	0x00					
0x62	JESD204B link control 4 / JESD204B 链路控制4	Reserved / 保留	0x00								
0x64	JESD204B DID configurati	Device ID (DID) = C0 / 器件标识(DID) = C0	0xC0	Read only / 只读							

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
	on / JESD204B DID 配置										
0x65	JESD204B BID configuration / JESD204B BID 配置	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	JTX module ID (BID) number / JTX 模块标识(BID)号	0x00				
0x66	JESD204B LID configuration 0 / JESD204B LID 配置0	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	JTX lane ID (LID) number for lane 0 / 通道0的JTX通道标识(LID)号	0x00					
0x67	JESD204B LID configuration 1 / JESD204B LID 配置1	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	JTX lane ID (LID) number for lane 1 / 通道1的JTX通道标识(LID)号	0x01					
0x68	JESD204B LID configuration 2 / JESD204B LID 配置2	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	JTX lane ID (LID) number for lane 2 / 通道2的JTX通道标识(LID)号	0x02					
0x69	JESD204B LID configuration 3 / JESD204B LID 配置3	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	JTX lane ID (LID) number for lane 3 / 通道3的JTX通道标识(LID)号	0x03					

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
0x6E	JESD204B parameter SCR/L / JESD204B 参数 SCR/L	JESD204B scrambling (SCR): 0 = disabled, 1 = enabled / JESD204B加扰 (SCR)：0 = 禁用，1 = 使能	Disabled / 禁用	Disabled / 禁用	JESD204B serial lane control: 0 = 1 lane per link (L = 1), 1 = 2 lanes per link (L = 2), 2 = unused, 3 = 4 lanes per link (L = 4), 4 to 31 = unused / JESD204B串行通道控制：0 = 每链路1个通道(L = 1)，1 = 每链路 2个通道(L = 2)，2 = 未使用，3 = 每链路4个通道(L = 4)，4至31 = 未使用	0x80					
0x6F	JESD204B parameter F / JESD204B 参数F	Number of 8-bit words per JESD204B frame (F); calculated value, F = (2 × M)/L / JESD204B每帧的8位字个数(F)；计算值，F = (2 × M)/L	0x00	Read only / 只读							
0x70	JESD204B parameter K / JESD204B 参数K	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Number of frames per JESD204B multiframe (K); K = register content + 1, and K must be a multiple of 4 eight-bit words / JESD204B每个多帧的帧数 (K)；K = 寄存器内容 + 1，同时K必须是4个8位字的倍数	0x1F					
0x71	JESD204B parameter M / JESD204B 参数M	Number of JESD204B converters (M): 0 = 1 converter (M = 1), 1 = 2 converters (M = 2), 3 = 4 converters (M = 4, default) / JESD204B转换器数(M)：0 = 1个转换器(M = 1)，1 = 2个转换器(M = 2)，3 = 4个转换器(M = 4，默认值)	0x03								
0x72	JESD204B parameter CS/N /	00 = 0 control bits per sample (CS = 0) / 00 = 每个样本发送0 个控制位数 (CS = 0)	Disabled / 禁用	JTX converter resolution (N): 0x0F =	0x0F						

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
	JESD204B 参数CS/N			16-bit, 0x0D = 14-bit, 0x0B = 12-bit, 0x09 = 10-bit / JTX转换器分辨率 (N)：0x0F = 16位，0x0D = 14位，0x0B = 12位，0x09 = 10位							
0x73	JESD204B parameter subclass/ N' / JESD204B 参数 subclass/N'	JESD204B subclass: 0x0 = subclass 0, 0x1 = subclass 1 (default) / JESD204B子类：0x0 = 子类0，0x1 = 子类1(默认)	Number of bits per JESD204B sample (N'); N' = register content + 1 / JESD204B 每个样本的位数(N')；N' = 寄存器内容 + 1	0x2F							
0x74	JESD204B parameter S / JESD204B 参数S	Reserved / 保留	Number of converter samples per JESD204B frame (S); S = register content + 1 / JESD204B	0x20	Read only / 只读						

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
			每帧的转换器样本数 (S)；S = 寄存器内容 + 1								
0x75	JESD204B parameter HD and CF / JESD204B 参数HD 和 CF	JESD204B HD value = 0 / JESD204B HD 值 =0	Disabled / 禁用	Disabled / 禁用	JESD204B control words per frame clock period per link (CF = 0, fixed value) / 每链路上每个帧时钟周期的 JESD204B控制字(CF = 0，固定值)	0x00	Read only / 只读				
0x76	JESD204B RESV1	JESD204B serial reserved field 1 in link configuration, see Table 12 (RES1) / 链路配置中的 JESD204B串行保留域1，参见表12 (RES1)	0x00								
0x77	JESD204B RESV2	JESD204B serial reserved field 2 in link configuration, see Table 12 (RES2) / 链路配置中的 JESD204B串行保留域2，参见表12 (RES2)	0x00								
0x78	JESD204B CHKSUM0	JESD204B serial checksum value in link configuration, lane 0 of Table 12 (FCHK) / 链路配置中的JESD204B串行校验和值，参见表12的通道0 (FCHK)	Read only / 只读								
0x79	JESD204B CHKSUM1	JESD204B serial checksum value in link configuration, lane 1 of	Read only / 只读								

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
		Table 12 (FCHK) / 链路配置中的JESD204B串行校验和值，参见表12的通道1 (FCHK)									
0x7A	JESD204B CHKSUM2	JESD204B serial checksum value in link configuration, lane 2 of Table 12 (FCHK) / 链路配置中的JESD204B串行校验和值，参见表12的通道2 (FCHK)	Read only / 只读								
0x7B	JESD204B CHKSUM3	JESD204B serial checksum value in link configuration, lane 3 of Table 12 (FCHK) / 链路配置中的JESD204B串行校验和值，参见表12的通道3 (FCHK)	Read only / 只读								
0x80	JTX physical lane disable / JTX物理通道禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Lane 3: 0 = enabled, 1 = disabled / 通道3：0 = 使能，1 = 禁用	Lane 2: 0 = enabled, 1 = disabled / 通道2：0 = 使能，1 = 禁用	Lane 1: 0 = enabled, 1 = disabled / 通道1：0 = 使能，1 = 禁用	Lane 0: 0 = enabled, 1 = disabled / 通道0：0 = 使能，1 = 禁用	0x00	Lane serialization, output driver off / 通道串行化，输出驱动器关断
0x82	JESD204B lane alignment 1 / JESD204B 通道对齐1	Disabled / 禁用	Physical lane 1 alignment: 000 = logical lane 0, 001 = logical lane	Disabled / 禁用	Physical lane 0 alignment: 000 = logical lane 0, 001 = logical lane 1, 010 = logical lane 2, 011 = logical lane 3 / 物理通道0对齐：000 = 逻辑通道0，001 = 逻辑通道1，010 = 逻辑通道2，011 = 逻辑通道3	0x10					

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
			1, 010 = logical lane 2, 011 = logical lane 3 / 物理通道1对齐：000 = 逻辑通道0，001 = 逻辑通道1，010 = 逻辑通道2，011 = 逻辑通道3								
0x83	JESD204B lane alignment 2 / JESD204B 通道对齐2	Disabled / 禁用	Physical lane 3 alignment: 000 = logical lane 0, 001 = logical lane 1, 010 = logical lane 2, 011 = logical lane 3 / 物理通道3对齐：000 = 逻辑通道0，001 = 逻辑通道1，010 = 逻辑通道2，011 = 逻辑通道3	Disabled / 禁用	Physical lane 2 alignment: 000 = logical lane 0, 001 = logical lane 1, 010 = logical lane 2, 011 = logical lane 3 / 物理通道2对齐：000 = 逻辑通道0，001 = 逻辑通道1，010 = 逻辑通道2，011 = 逻辑通道3	0x32					
0x86	JESD204B lane inversion /	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Lane 3: 0 = not inverted, 1 = inverted / 通道3：0 = 不	Lane 2: 0 = not inverted, 1 = inverted / 通道2：0 = 不反转，1 = 反转	Lane 1: 0 = not inverted, 1 = inverted /	Lane 0: 0 = not inverted, 1 = inverted /	0x00	

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
	JESD204B 通道反转					反转，1 = 反转		通道1：0 = 不反转，1 = 反转	通道0：0 = 不反转，1 = 反转		
0x8B	JESD204B LMFC offset / JESD204B LMFC 偏移	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Local multiframe clock (LMFC) phase offset value; reset value of LMFC phase counter when DSYSREF± is set; used for deterministic latency applications / 本地多帧时钟(LMFC)相位偏移值；DSYSREF±置位时 LMFC相位计数器的复位值；用于确定性延迟应用	0x00					
0xA0	JTX user pattern word 0, LSB / JTX用户模式码8位字0，LSB	User test code least significant byte, 8-bit word 0 / 用户测试码最低有效字节，8位字0	0x00								
0xA1	JTX user pattern word 0, MSB / JTX用户模式码8位字0，MSB	User test code most significant byte, 8-bit word 0 / 用户测试码最高有效字节，8位字0	0x00								
0xA2	JTX user pattern word 1, LSB / JTX用户模式码8位字1，LSB	User test code least significant byte, 8-bit word 1 / 用户测试码最低有效字节，8位字1	0x00								
0xA3	JTX user pattern word 1, MSB / JTX	User test code most significant byte, 8-bit word 1 / 用户测试码最高有效字节，8位字1	0x00								

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
	用户模式码 8位字1，MSB										
0xA4	JTX user pattern word 2, LSB / JTX用户模式码8位字2，LSB	User test code least significant byte, 8-bit word 2 / 用户测试码最低有效字节，8位字2	0x00								
0xA5	JTX user pattern word 2, MSB / JTX用户模式码8位字2，MSB	User test code most significant byte, 8-bit word 2 / 用户测试码最高有效字节，8位字2	0x00								
0xA6	JTX user pattern word 3, LSB / JTX用户模式码8位字3，LSB	User test code least significant byte, 8-bit word 3 / 用户测试码最低有效字节，8位字3	0x00								
0xA7	JTX user pattern word 3, MSB / JTX用户模式码8位字3，MSB	User test code most significant byte, 8-bit word 3 / 用户测试码最高有效字节，8位字3	0x00								
0xF5	JTX converter mapping / JTX转换器映射	JTX converter 3: 0 = ADCA, 1 = ADCB, 2 = ADCC, 3 = ADCD / JTX转换器3：0 = ADCA，1 =	JTX converter 2: 0 = ADCA, 1 = ADCB, 2 =	JTX converter 1: 0 = ADCA, 1 = ADCB, 2 =	JTX converter 0: 0 = ADCA, 1 = ADCB, 2 = ADCC, 3 = ADCD / JTX转换器0：0 = ADCA，1 = ADCB，2 = ADCC，3 = ADCD	0xE4					

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
		ADCB，2 = ADCC，3 = ADCD	ADCC, 3 = ADCD / JTX 转换器2：0 = ADCA，1 = ADCB，2 = ADCC，3 = ADCD	ADCC, 3 = ADCD / JTX 转换器1：0 = ADCA，1 = ADCB，2 = ADCC，3 = ADCD							
0x100	Resolution/ sample-rate override / 分辨率/采样速率覆盖	Disabled / 禁用	Override enable / 覆盖使能	Resolution: 0 = 16-bit, 1 = 14-bit, 2 = 12-bit, 3 = 10-bit / 分辨率：0 = 16位，1 = 14位，2 = 12位，3 = 10位	Disabled / 禁用	Sample rate: 001 = 40 MSPS, 010 = 50 MSPS, 011 = 65 MSPS, 100 = 80 MSPS, 101 = 105 MSPS, 110 = 125 MSPS / 采样速率：001 = 40 MSPS，010 = 50 MSPS，011 = 65 MSPS，100 = 80 MSPS，101 = 105 MSPS，110 = 125 MSPS	0x00	Sample-rate override (requires transfer register 0xFF) / 采样速率覆盖 (需要传输寄存器 0xFF)			
0x101	User I/O control 2 / 用户I/O控制 2	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	SDIO pull-down / SDIO 下拉	0x00	Disable SDIO pull-down resistor / 禁用 SDIO 下拉电阻
0x102		Disabled / 禁用			Disabled / 禁用		Disabled / 禁用			0x00	

Address (Hex) / 地址(十六进制)	Register Name / 寄存器名称	Bit 7 (MSB) / 位 7 (MSB)	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位1	Bit 0 (LSB) / 位 0 (LSB)	Default (Hex) / 默认值 (十六进制)	Notes / 注释/备注
	User I/O control 3 / 用户I/O控制 3		Disabled / 禁用	Disabled / 禁用		VCM power-down / VCM 掉电		Disabled / 禁用	Disabled / 禁用		VCM control / VCM控制
0x109	Clock divider sync control / 时钟分频器同步控制	Clock divider sync mode: 0 = use SYNC pin, 1 = use DSYSREF± pins / 时钟分频器同步模式：0 = 使用 SYNC 引脚，1 = 使用 DSYSREF± 引脚	Reserved / 保留					Sync clock divider on SYNC: 0 = disabled, 1 = enabled / 收到复位时钟分频器同步使能：0 = 禁用，1 = 使能	Sync clock divider / 同步时钟分频器	0x00	
0x10A	Clock divider sync received / 收到时钟分频器同步	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Disabled / 禁用	Clock divider sync received / 收到时钟分频器同步	0x00	Read only / 只读

8. Register Address Descriptions / 8、寄存器地址说明

Memory map register descriptions. For more general information on the functions controlled by registers 0x00 to 0xFF, see application note AN-877: "Interfacing to High-Speed ADCs via SPI."

存储器映射寄存器描述。如需了解有关寄存器 0x00 至寄存器 0xFF 所控制功能的更多一般信息，请参见应用笔记 AN-877："通过 SPI 与高速 ADC 接口。"

Device index (register 0x05). For certain features designated as local in the map, each channel can be set independently, while other features are globally applicable (depending on context) regardless of which channel is selected. Bits [3:0] of register 0x05 can be used to select which data channels are affected.

器件索引(寄存器 0x05)。对于映射中指定为局部的某些特性，各通道可以独立设置，而其它特性则是全局适用(取决于上下文)，不论选择哪一通道。寄存器 0x05 的位[3:0]可以用来选择哪些数据通道受影响。

Transfer (register 0xFF). Except for register 0x100, all other registers are updated immediately upon writing. When bit 0 of the transfer register is set to 1, the settings of the resolution/sample-rate override register (address 0x100) are initialized.

传送(寄存器 0xFF)。除寄存器 0x100 外，所有其它寄存器都在写入时立刻更新。传送寄存器的位 0 置 1 时，分辨率/采样速率覆盖寄存器(地址 0x100)的设置初始化。

Power mode (register 0x08).

功耗模式(寄存器 0x08)

- Bit 5 — PDWN pin function. When set to 1, the PDWN pin initiates standby mode. When set to 0 (cleared to 0), the PDWN pin initiates full power-down mode. / 位 5—PDWN 引脚功能。置 1 时，PDWN 引脚启动待机模式。置 0(清 0)时，PDWN 引脚启动完全掉电模式。
- Bit 4 — JTX standby mode. When set to 1, if the chip standby function is enabled, the JTX module enters standby mode. In standby mode, only the PLL keeps running. When cleared to 0, if the chip standby function is enabled, the JTX module keeps running. / 位 4—JTX 待机模式。置 1 时，若芯片待机功能启用，则 JTX 模块进入待机模式。待机模式下，仅 PLL 仍然运行。清 0 时，若芯片待机功能启用，则 JTX 模块仍然运行。
- Bits [1:0] — Power mode. In normal operation (bits [1:0] = 00), all ADC channels and the JTX module are enabled. / 位[1:0]—功耗模式。正常工作(位[1:0] = 00)时，所有 ADC 通道和 JTX 模块均启用。
- In full power-down mode (bits [1:0] = 01), all ADC channels and the JTX module are powered down, the digital datapath clock is disabled, and the digital datapath is reset. Outputs are disabled. / 在完全掉电模式(位[1:0] = 01)下，所有 ADC 通道和 JTX 模块均掉电，数字数据路径时钟禁用，数字数据路径复位。输出禁用。
- In standby mode (bits [1:0] = 10), all ADC channels are partially powered down and the digital datapath clock is disabled. If JTX standby mode is set, outputs are also disabled. / 在待机模式(位[1:0] = 10)下，所有 ADC 通道部分掉电，数字数据路径时钟禁用。若设置了 JTX 待机模式，则输出也禁用。
- During digital reset (bits [1:0] = 11), all other digital datapath clocks and outputs (where applicable) of the chip are reset except the SPI port. Note that the SPI is always under user control and is never automatically disabled or reset (except power-on reset). When digital reset is deasserted, the foreground calibration sequence starts. / 数字复位(位[1:0] = 11)期间，除 SPI 端口外，芯片的所有其它数字数据路径时钟和输出(适用时)均复位。注意，SPI 始终受用户的控制，从不会自动禁用或复位(除非上电复位)。数字复位无效时，启动前台校准序列。

Enhancement control (register 0x0C). Bit 2 — Chopping mode.

增强控制(寄存器 0x0C)。位 2—斩波模式

Certain applications are sensitive to offset voltage and other low-frequency noise, such as zero-IF or direct-conversion receivers; for these applications, bit 2 can be set to enable the chopping feature of the first stage of this device. In the frequency domain, chopping converts offset and other low-frequency noise to fCLK/2, which can be filtered out by filters.

某些应用对失调电压和其它低频噪声敏感，如零差或直接变频接收机等；针对这些应用，可以设置位 2 来使能本产品第一级的斩波特性。在频域中，斩波将失调和其它低频噪声转换为 fCLK/2，可以通过滤波器予以滤除。

Output mode (register 0x14).

输出模式(寄存器 0x14)

- Bits [7:5] — JTX CS mode. Specifies the meaning of JTX control bits. / 位[7:5]—JTX CS 模式。指定 JTX 控制位的意义。
- Bits [1:0] — Output format. By default this field is set to 1, and data is output in two's complement format. When this field is cleared to 0, the output mode becomes offset binary. / 位[1:0]—输出格式。默认情况下，此域置 1，数据以二进制补码格式输出。此域清 0 时，输出模式变为偏移二进制。

Clock phase control (register 0x16). Bits [6:4] — Input clock phase adjust.

时钟相位控制(寄存器 0x16)。位[6:4]—输入时钟相位调整

When using the clock driver (register 0x0B), the applied clock frequency is higher than the internal sampling clock. Bits [6:4] determine at which phase of the external clock sampling is performed. This only applies when the clock divider is used. Bits [6:4] cannot be set greater than the value of bits [2:0] of register 0x0B.

使用时钟驱动器(寄存器 0x0B)时，施加的时钟频率高于内部采样时钟。位[6:4]决定在外部时钟的哪个相位执行采样。这只在使用时钟分频器时适用。位[6:4]不可设置大于寄存器 0x0B 位[2:0]的值。

JTX user pattern codes (registers 0xA0 to 0xA7).

JTX 用户模式码(寄存器 0xA0 至寄存器 0xA7)

When bits [3:0] of register 0x61 are set to 5 or 6, the pattern codes in these registers are output on all valid lanes. When bits [5:4] of register 0x61 are set to 2, a 32-bit pattern code formed by concatenating registers 0xA0, 0xA2, 0xA4 and 0xA6 is inserted before the scrambler. When bits [5:4] of register 0x61 are set to 1 (40-bit pattern code), the pattern code inserted before the 8b/10b encoder is formed by concatenating: bits [1:0] of register 0xA1 and bits [7:0] of register 0xA0; bits [1:0] of register 0xA3 and bits [7:0] of register 0xA2; bits [1:0] of register 0xA5 and bits [7:0] of register 0xA4; bits [1:0] of register 0xA7 and bits [7:0] of register 0xA6.

当寄存器 0x61 的位[3:0]设置为 5 或 6 时，这些寄存器中的模式码在所有有效通道上输出。当寄存器 0x61 的位[5:4]设置为 2 时，加扰器之前插入一个由寄存器 0xA0、寄存器 0xA2、寄存器 0xA4 和寄存器 0xA6 连接而成的 32 位模式码。当寄存器 0x61 的位[5:4]设置为 1 时(40 位模式码)，8b10b 编码器之前插入由以下内容连接而成的模式码：寄存器 0xA1 的位[1:0]和寄存器 0xA0 的位[7:0]；寄存器 0xA3 的位[1:0]和寄存器 0xA2 的位[7:0]；寄存器 0xA5 的位[1:0]和寄存器 0xA4 的位[7:0]；寄存器 0xA7 的位[1:0]和寄存器 0xA6 的位[7:0]。

Resolution/sample-rate override (register 0x100).

分辨率/采样速率覆盖(寄存器 0x100)

In applications not requiring the highest resolution and/or sample rate, the user can use this register to reduce resolution and/or maximum sample rate (to reduce power consumption). The settings of this register are initialized after bit 0 of the transfer register (register 0xFF) is written high.

在不需要最高分辨率和/或采样速率的应用中，用户可利用此寄存器降低分辨率和/或最大采样速率(以便降低功耗)。此寄存器的设置在传送寄存器(寄存器 0xFF)的位 0 写入高电平后初始化。

Bits [2:0] do not affect the sample rate, but rather affect the maximum sample rate of the ADC.

位[2:0]不影响采样速率，而是影响 ADC 的最大采样速率。

User I/O control 2 (register 0x101). Bit 0 — SDIO pull-down.

用户 I/O 控制 2(寄存器 0x101)。位 0—SDIO 下拉

Bit 0 can be set to disable the built-in 30 kK pull-down resistor of the SDIO pin. When many devices are connected to the SPI bus, this setting can be used to limit loading.

可以设置位 0 以禁用 SDIO 引脚内置的 30 kK 下拉电阻。当许多器件连接到 SPI 总线时，此设置可用来限制负载。

User I/O control 3 (register 0x102). Bit 3 — VCM power-down.

用户 I/O 控制 3(寄存器 0x102)。位 3—VCM 掉电

By setting bit 3 to high level, the internal VCM generator can be turned off. Use this feature when using an external reference voltage source.

通过将位 3 设置为高电平，可关断内部 VCM 发生器。使用外部基准电压源时使用此功能。

Power Supply Protection / 电源地间保护

To improve the device's ESD immunity, the following ESD protection loops exist between the various supply pins inside the device. The forward conduction voltage drop of each ESD protection diode is approximately 0.35V; avoid keeping these ESD protection diodes forward-conducting for extended periods during power-up and normal use.

为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.35V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。

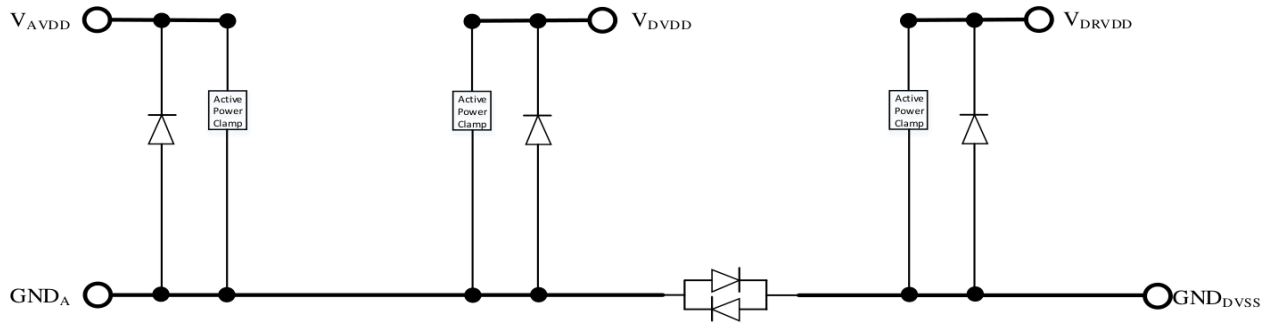


Figure 57: Internal ESD protection circuit between power supplies (VAVDD / VDVDD / VDRVDD, GNDA / GNDDVSS)

Precautions / 注意事项

1. Product Installation Precautions / 1、产品安装注意事项

1. Pay attention to device orientation during soldering to avoid misalignment. / 焊接时请注意器件方向，以免焊错。
2. Instruments and meters used for circuit debugging must have good common grounding. PCB design must maintain good grounding and power supply decoupling. / 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。
3. Take care not to reverse the power supply or short input/output terminals to the power supply, as this can easily damage the circuit. / 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2. Product Usage Precautions / 2、产品使用注意事项

1. Differential inputs should be routed as close together and as parallel as possible. / 差分输入应尽量靠近且相互平行。
2. Input traces should be kept as short as possible to minimize parasitic capacitance and noise pickup. / 输入连线应尽量短以最小化寄生电容和噪声引入。
3. For better heat dissipation and electrical performance, the die paddle of the chip should be soldered to a large ground area on the PCB board, maximizing the thermal performance of the package. / 为了更好的散热并获得更好的电性能，芯片的底板应焊接到 PCB 板的一个大的地端，从而最大限度发挥封装的热性能。
4. It is important that the chip ground be connected to the PCB ground plane through as many channels and as much area as possible. / 很重要的是，芯片的地应该通过尽量多的渠道和足够多的面积与 PCB 板的地层相连。
5. After power-up, it is recommended to reset the circuit first before use. / 推荐上电后首先对电路进行复位，再进行使用。

3. Product Protection Precautions / 3、产品防护注意事项

1. All terminals of this circuit are designed with ESD protection structures, but large-energy electrical pulses may still damage the circuit; therefore, pay attention to ESD protection during testing, handling and storage. / 该电路所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。
2. Exceeding the absolute maximum ratings may cause permanent damage to the device. These are only rated maximum values and do not indicate that the device can operate normally under these conditions or under any other conditions exceeding those shown in this product manual. / 超出绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。
3. Under conditions avoiding direct exposure to rain and snow, packing cases containing the product can be transported by safe means of transport. However, they must not be stacked together with acidic, alkaline or other corrosive objects. Packaging should be secure, and existing means of transport may be used. / 在避免雨、雪直接影响的条件下，装有产品的包装箱可以用安全的运输工具运输。但不能和带有酸性、碱性和其它腐蚀性物体堆放在一起。包装应是安全的，可以采用现有的运输工具。

4. The storage environment for packaged products shall meet the Class I warehouse conditions specified in Q/W 657A Section 8.1 (temperature: 15°C~25°C, humidity: 25%~65%), with no acids, alkalis or other corrosive gases nearby, good ventilation, and appropriate ESD protection measures. / 包装好的产品贮存环境应满足 Q/W 657A 第 8.1 规定的 I 类库房条件要求（温度：15°C~25°C，湿度：25%~65%），周围没有酸、碱或其它腐蚀性气体，通风良好，且具备相应防静电措施。

4. Assembly Instructions / 4、电装说明

1. The moisture sensitivity level of this device is MSL3. After removing the device from the moisture-proof bag, performing dry storage or baking, the allowable time of exposure to the ambient environment before reflow soldering is: ≤30°C/60RH%, 168h. / 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h；
2. If device storage conditions cannot be controlled or traced, strictly perform baking at 125°C for 8h before assembly. / 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤；
3. If the temperature and humidity of the assembly environment cannot be guaranteed at ≤30°C/60RH%, complete soldering within 12h after baking. / 若电装环境温湿度无法保证≤30°C/60RH%，请在烘烤后 12h 内完成焊接；
4. After baking, the device is highly susceptible to static electricity; pay attention to ESD protection during all operations. / 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护；
5. For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C~235°C, the maximum peak temperature should preferably not exceed 235°C, dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60~90s, ramp-up rate 2~4°C/s, ramp-down rate 2~6°C/s. / 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s；
6. For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C~245°C, the maximum peak temperature should preferably not exceed 260°C, dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60~90s, ramp-up rate 2~4°C/s, ramp-down rate 2~6°C/s. / 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~6°C/s；

   Note: The original text for item 6 lists the ramp-down rate as "2~6°C" (missing "/s"); kept verbatim. / 注：原文第 6 条降温速率为"2~6°C"（漏"/s"），按原文保留。

1. If a mixed assembly process requires higher temperatures, ensure the device body temperature does not exceed 260°C (the device body temperature measurement point is located on the top surface of the device during reflow). / 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）；
2. The solder terminal plating of this device is nickel-palladium-gold, but the gold content is less than 3%; gold embrittlement will not occur and tinning is not required. / 本产品焊接端镀层为镍钯金，但含量小于 3%，不会出现金脆现象，不需要搪锡；
3. If forced tinning is required, perform tinning per the national aerospace industry standard QJ3267 "Tinning Process Technical Requirements for Electronic Components". Note that the device must be dried before tinning, the tinning set temperature must not exceed 300°C, each side of the four-sided

pins shall be heated for less than 5s, the heat-sink surface for less than 30s, and tinning shall not exceed 1 time. / 若有强制搪锡需求，按《国家航天行业标准 QJ3267 电子元器件搪锡工艺技术要求》标准进行搪锡。应注意搪锡前器件需烘干，搪锡设置温度不超过 300°C，四边引脚每边受热时间小于 5s，热沉表面受热时间小于 30s，搪锡次数不超过 1 次。

5. Thermal Resistance / 5、热阻

Table 7: Package Thermal Resistance / 表7 封装热阻

Item / 项目	Measured Value / 实测值	Basis, Standard and Method / 依据标准及方法
Rthja (junction-to-ambient thermal resistance) / Rthja（结到环境的热阻）	24.72 K/W	JESD51-2, natural convection thermal test for integrated circuits, environmental requirements and test methods / JESD51-2 集成电路自然对流热测试环境要求及测试方法
Rthjt (junction-to-top thermal resistance) / Rthjt(结到器件顶面的热阻)	1.971 K/W	JESD51-14, one-dimensional heat transfer path, dual-interface separation method / JESD51-14 一维传热路径双界面分离法
Rthj-bottom (junction-to-bottom thermal resistance) / Rthj-bottom（结到器件底面的热阻）	1.118 K/W	JESD51-14, inflection-point theory, device internal structure delamination / JESD51-14 拐点理论器件内部结构分层得到

Troubleshooting / 常见故障及处理办法

1. No signal output: check whether the power supply voltage, input signal and clock are correctly applied. / 无信号输出：检查电源电压、输入信号、时钟是否正确加载。
2. Device malfunction: clarify the device operating mode and confirm the configuration is correct. / 器件功能不正常：明确器件工作模式，确认配置是否正确。
3. Device operates unstably: check the power supply to ensure stable supply voltage. / 器件工作不稳定：检查电源，保证电源电压稳定。

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Additional Notes / 附加说明

1. First release date of this manual: July 2026. / 本说明书首次发布日期：2026 年 7 月。
2. Product status: ☑ Production (this product model is currently in production; formal products can be supplied) / 本产品状态：☑生产（该产品型号目前已在生产，可以提供正式产品） ☐ Pre-release (this product model has not yet entered formal production; samples can be supplied) / ☐预发布（该产品型号尚未投入正式生产，可以提供样品）
3. Import-device replacement notes: / 替代进口器件情况说明：

1) Absolute maximum ratings comparison / 绝对最大额定值对比

Appendix Table 1: Absolute Maximum Ratings Comparison / 附表1 绝对最大额定值对比

Parameter / 参数	SXA009 Specification Requirement / SXA009 规范要求	Imported Device Manual / 进口器件手册	Comparison Result / 比对结果
Analog supply voltage (VAVDD) / 模拟电源电压（VAVDD）	2V	2V	Consistent / 一致
Digital supply voltage (VDVDD) / 数字电源电压（VDVDD）	2V	2V	Consistent / 一致
Storage temperature (Tstg) / 贮存温度（Tstg）	−55°C~125°C	−65°C~150°C	Inconsistent / 不一致
Junction temperature (TJ) / 结温（TJ）	150°C	150°C	Consistent / 一致

2) Recommended operating conditions comparison / 推荐工作条件对比

Appendix Table 2: Recommended Operating Conditions Comparison / 附表2 推荐工作条件对比

Parameter / 参数	SXA009 Specification Requirement / SXA009 规范要求	Imported Device Manual / 进口器件手册	Comparison Result / 比对结果
Operating frequency (fCLK) / 工作频率（fCLK）	≤125MHz	≤125MHz	Consistent / 一致
Analog supply voltage (VAVDD) / 模拟电源电压（VAVDD）	1.75V~1.9V	1.7V~1.9V	Consistent / 一致
Digital supply voltage (VDVDD) / 数字电源电压（VDVDD）	1.75V~1.9V	1.7V~1.9V	Consistent / 一致
Input signal amplitude range (peak-to-peak) (VIN(P-P)) / 输入信号幅度范围（峰峰值）（VIN(P-P)）	≤2V	≤2V	Consistent / 一致
Analog input common-mode voltage (VCM) / 模拟输入共模电压（VCM）	0.5V~1.3V	0.7V~1.1V	Inconsistent / 不一致
Operating ambient temperature (TA) / 工作环境温度（TA）	−55°C~100°C	−40°C~85°C	Inconsistent / 不一致

3) Electrical characteristics comparison / 电特性对比

Test conditions (unless otherwise specified): VPP=2.0V, VAVDD=VDVDD=VSVDD=VDRVDD=1.8V, GNDA=GNDDVSS=0V, fS=125MSPS, −55°C≤TA≤100°C.

条件（除另有规定外，VPP=2.0V，VAVDD=VDVDD=VSVDD=VDRVDD=1.8V，GNDA=GNDDVSS=0V，fS=125MSPS，-55°C≤TA≤100°C）

Appendix Table 3: Electrical Characteristics Comparison / 附表3 电特性对比

Parameter / 参数	Symbol / 符号	Conditions / 条件	SXA009 Detailed Spec Requirement / SXA009 详细规范要求		Imported Device Manual / 器件手册		Unit / 单位	Comparison Result / 对比结果
			Min / 最小值	Max / 最大值	Min / 最小值	Max / 最大值		
Resolution / 分辨率	RES		16		16		bits	Consistent / 一致
Number of channels / 通道数	—		4		4		—	Consistent / 一致
Differential nonlinearity error / 微分线性误差	EDL	fIN=10MHz	−0.99	+0.99	±0.6 (typical only) / ±0.6（仅典型值）		LSB	Imported device typical value only / 国外仅典型值
Integral nonlinearity error / 积分非线性误差	EIL	fIN=10MHz	−11	+11	±6 (typical only) / ±6（仅典型值）		LSB	Imported device typical value only / 国外仅典型值
Power consumption / 功耗	PW	Four channels / 四通道	—	839	771 (typical only) / 771（仅典型值）		mW	Imported device typical value only / 国外仅典型值
Conversion rate / 转换率	SR		40	125	40	125	MSPS	Consistent / 一致
Signal-to-noise ratio / 信噪比	SNR	−1dBFS, fIN=10MHz	74	—	78 (typical only) / 78（仅典型值）		dBFS	Imported device typical value only / 国外仅典型值
		−1dBFS, fIN=128MHz	69	—	74.3 (typical only) / 74.3（仅典型值）		dBFS	Imported device typical value only / 国外仅典型值
Signal-to-noise and distortion ratio / 信噪失真比	SINAD	−1dBFS, fIN=10MHz	73	—	78 (typical only) / 78（仅典型值）		dBFS	Imported device typical value only / 国外仅典型值
		−1dBFS, fIN=128MHz	68	—	74 (typical only) / 74（仅典型值）		dBFS	Imported device typical value only / 国外仅典型值
Effective number of bits / 有效位	ENOB	−1dBFS, fIN=10MHz	12	—	12.7 (typical only) / 12.7（仅典型值）		bits	Imported device typical value only / 国外仅典型值
		−1dBFS, fIN=128MHz	11	—	12 (typical only) / 12（仅典型值）		bits	Imported device typical value only / 国外仅典型值
Spurious-free dynamic range / 无杂散动态范围	SFDR	−1dBFS, fIN=10MHz	80	—	99 (typical only) / 99（仅典型值）		dBFS	Imported device typical value only / 国外仅典型值
		−1dBFS, fIN=128MHz	74	—	87 (typical only) / 87（仅典型值）		dBFS	Imported device typical value only / 国外仅典型值

4) Other parameters comparison / 其它指标对比

Appendix Table 4: Other Parameters Comparison / 附表4 其它指标对比

Parameter / 参数	SXA009	Imported Device / 进口器件	Comparison Result / 比对结果
Package / 封装形式	QFN56	QFN56	Consistent / 一致
Quality grade / 质量等级	Enterprise standard / 企标	Industrial grade / 工业级	Different / 有差异
Dimensions / 尺寸	8mm×8mm×0.75mm	8mm×8mm×0.75mm	Consistent / 一致
Replacement recommendation / 替代建议	☐ Direct replacement / ☐直接替代 ☐ Effective replacement / ☐有效替代 ☑ Functional replacement / ☑功能替代		

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