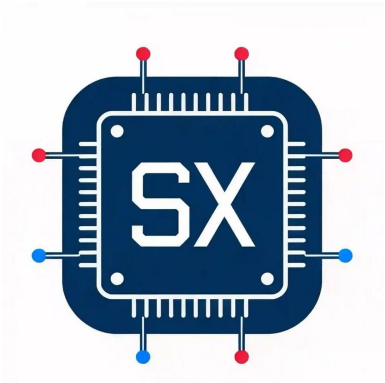


SXA023

Quad 16-Bit, 250 MSPS A/D Converter

四通道 16 位 250MSPS A/D 转换器

16-bit | 4 channels | 250 MSPS | QFN56 | JESD204B

16位 | 四通道 | 250MSPS | QFN56 | JESD204B

对标 / Cross Reference: AD9653 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXA023 Quad-Channel 16-Bit 250MSPS A/D Converter — Product Manual (Bilingual)

SXA023 型四通道 16 位 250MSPS A/D 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深信科技 **V1.20260727**

对标 / Cross Reference: AD9653 — pin-to-pin compatible alternative

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19. 附加说明 / Additional Notes

版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20260727	20260727	——	首次发布 / Initial release	

产品用途及应用范围 / Applications and Scope

English: Medical imaging; high-speed imaging; radio receivers; portable measurement equipment.

中文： 医疗成像；高速成像；无线电接受机；便携式测量设备。

标准 / Standards

English: Detailed specification and approval number: Q/GC 0221-2026 — Detailed Specification for Semiconductor Integrated Circuit SXA023 Quad-Channel 16-Bit 250MSPS A/D Converter. Quality grade: enterprise standard.

中文： 详细规范及确认号：Q/GC 0221-2026 《半导体集成电路 SXA023 型四通道 16 位 250MSPS A/D 转换器详细规范》；质量等级：企标。

产品特点 / Features

English: - Supply voltage: 1.8V - Resolution: 16bit - Number of channels: 4 channels - Conversion rate: 250MSPS - SNR: 73.5dBFS @9.7M (typical) - SFDR: 86dBc @9.7M (typical) - DNL: ±0.6LSB (typical) - INL: ±6LSB (typical) - Power consumption: ≤1.2W (typical 1.07W) - Input data interface: JESD204B - ESD rating: Class 1C, HBM model: 1000V - Product weight: 1.07g±0.1g

中文： - 电源电压：1.8V - 分辨率：16bit - 通道数：4 通道 - 转换速率：250MSPS - SNR：73.5dBFS@9.7M（典型值） - SFDR：86dBc@9.7M（典型值） - DNL：±0.6LSB（典型值） - INL：±6LSB（典型值） - 功耗：≤1.2W（典型值1.07W） - 输入数据接口：JESD204B - ESD 等级：1C 级，HBM 模型：1000V - 产品重量：1.07g±0.1g

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产品描述 / Product Description

English: The SXA023 is a 4-channel, 16-bit analog-to-digital converter (ADC) with a 250 MSPS sampling rate, developed specifically for low power consumption, small size, and application flexibility. The device supports conversion rates up to 250 MSPS, with excellent dynamic performance and ultra-low power characteristics, suitable for a wide range of applications.

The ADC operates from a single 1.8 V supply with an LVPECL/CMOS/LVDS-compatible sampling clock signal. No external reference source or drivers are required.

Each internal channel can be independently powered down; with all channels disabled, typical power consumption is less than 50 mW. The ADC integrates multiple functions, including programmable clock output, data alignment, and generation of digital test patterns. Available digital test patterns include built-in fixed test patterns and pseudo-random test patterns, and user-defined test patterns via the serial port interface (SPI) are also supported.

This product is packaged in a 64-lead ceramic package (CQFN64D).

The functional block diagram of this product is shown in Figure 1.

中文： SXA023 是一款 4 通道，16 位，250 MSPS 采样率的模数转换器（Analog-to-Digital Converter，ADC），专门针对低功耗、小尺寸和使用灵活性进行开发设计。该产品转换速率最高可达到 250 MSPS，具有优异的动态性能和超低功耗特性，适用多种应用场景。

该 ADC 采用 1.8 V 单电源供电和 LVPECL/CMOS/LVDS 兼容型采样时钟信号。无需外部基准电压源和驱动器即可满足需求。

支持独立关闭内部各通道功能；禁用全部通道后，典型功耗小于 50mW。该 ADC 内置多种功能，包括可编程时钟输出、数据对齐、生成数字测试码等。可获得的数字测试码包括：内置固定测试码和伪随机测试码，也支持用户通过串行端口接口（SPI）自定义测试码的方式。

该产品采用 64 无引线陶瓷封装（CQFN64D）。

该产品功能框图如图 1 所示。

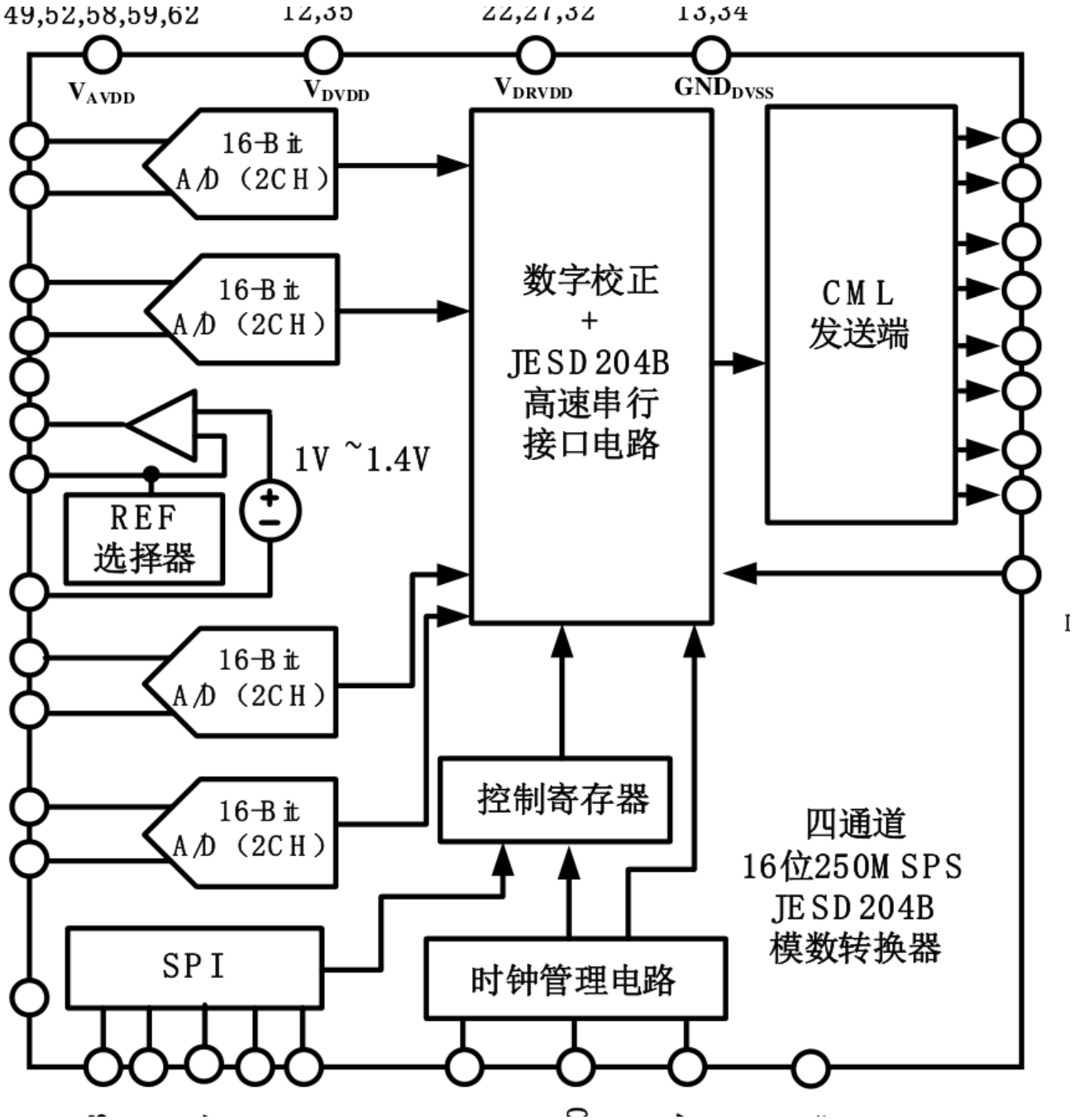
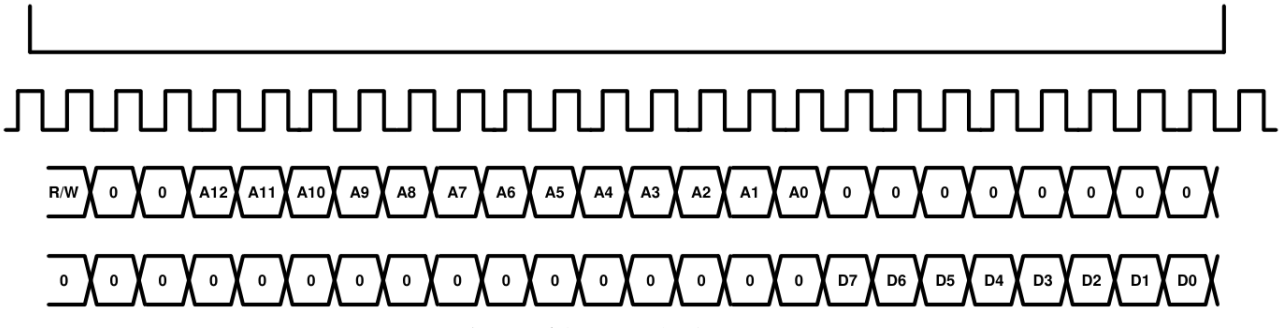


Figure 1: Functional block diagram


R/W
0
0
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
0
0

引出端排列（俯视图）/ Pin Arrangement (Top View)

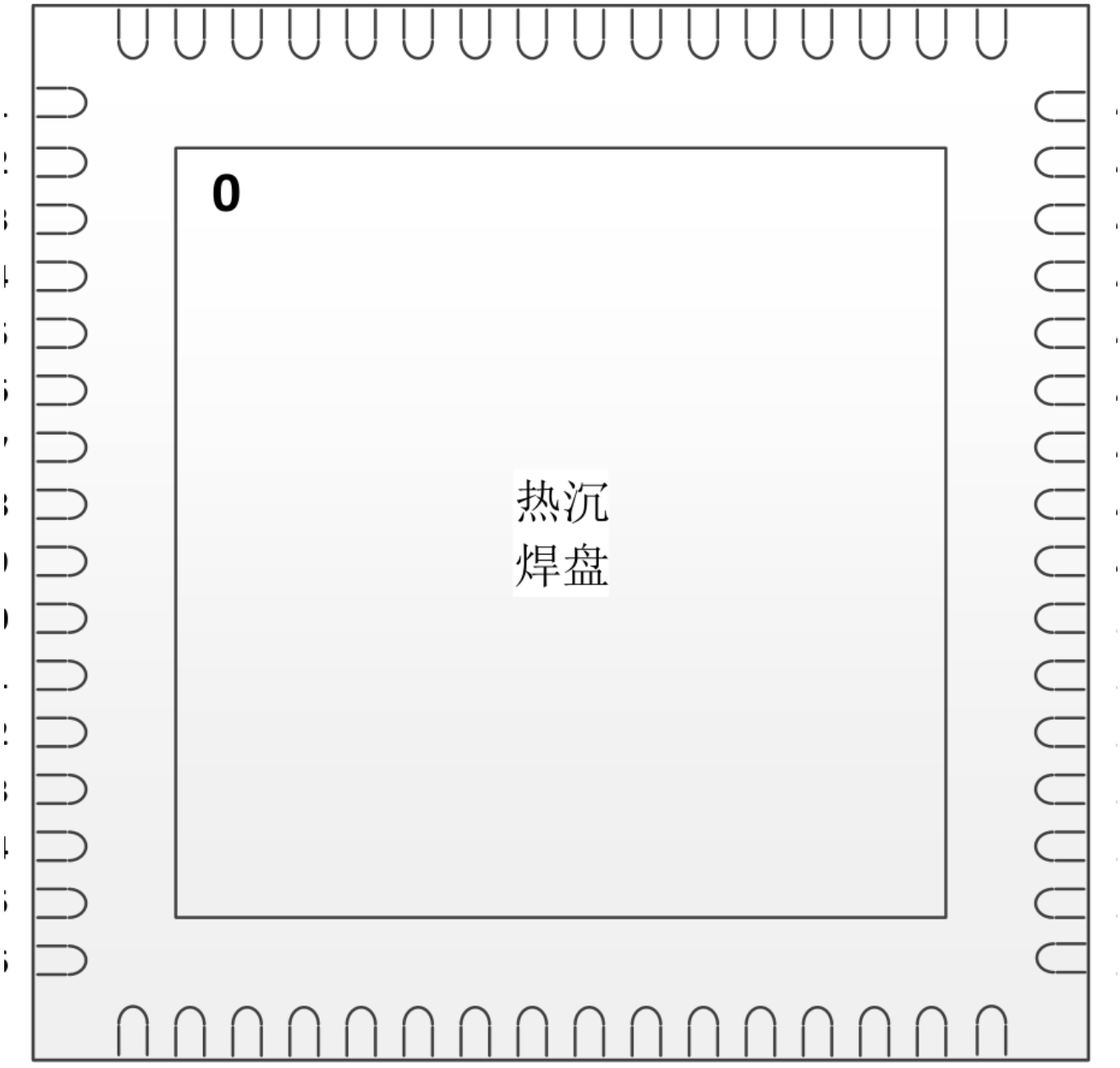


Figure 4: Pin arrangement (top view)

引出端功能符号表 / Pin Function Table

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
0	GNDA	模拟地 / Analog ground	/	33	NIC	空 / Not connected internally	/
1	VAVDD		/	34	GNDDVSS	数字地引脚 / Digital ground pin	/

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
		1.8V 模拟电源引脚 / 1.8V analog supply pin					
2	VIND+	ADC D 通道模拟输入(+) / ADC channel D analog input (+)	I	35	VDVDD	数字电源引脚 / Digital supply pin	/
3	VIND-	ADC D 通道模拟输入(-) / ADC channel D analog input (-)	I	36	SDO	SPI 数据输出 / SPI data output	O
4	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/	37	SDI	SPI 数据输入 / SPI data input	I
5	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/	38	DNC	不连接 / Do not connect	/
6	CLK-	差分时钟(-) / Differential clock (-)	I	39	VSVDD	SPI 电源引脚 / SPI supply pin	/
7	CLK+	差分时钟(+) / Differential clock (+)	I	40	DNC	不连接 / Do not connect	/
8	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/	41	SCLK	SPI 时钟输入 / SPI clock input	I
9	DSYSREF+	DSYSREF 输入 (+) / DSYSREF input (+)	I	42	DNC	不连接 / Do not connect	/
10	DSYSREF-	DSYSREF 输入 (-) / DSYSREF input (-)	I	43	CSB	SPI 片选信号 / SPI chip-select signal	I
11	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/	44	PDWN	数字输入（高电平=关断；低电平=工作）/ Digital input (high = power-down; low = operation)	I
12	VDVDD	数字电源引脚 / Digital supply pin	/	45	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
13	GNDDVSS	数字地引脚 / Digital ground pin	/	46	VINA-	ADC A 通道模拟输入(-) / ADC channel A analog input (-)	I
14	NIC	空 / Not connected internally	/	47	VINA+	ADC A 通道模拟输入(+) / ADC channel A analog input (+)	I
15	NIC	空 / Not connected internally	/	48	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
16	NIC	空 / Not connected internally	/	49	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
17	NIC	空 / Not connected internally	/	50	VINB+	ADC B 通道模拟输入(+) / ADC channel B analog input (+)	I
18	NIC	空 / Not connected internally	/	51	VINB-	ADC B 通道模拟输入(-) / ADC channel B analog input (-)	I
19	NIC	空 / Not connected internally	/	52	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
20	DSYNC+	DSYNC 输入(+) / DSYNC input (+)	I	53	RBIAS	模拟电路偏置 / Analog circuit bias	I

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
21	DSYNC-	DSYNC 输入(-) / DSYNC input (-)	I	54	SENSE	基准电压模式选择 / Reference voltage mode select	I
22	VDRVDD	数字输出驱动电源引脚 / Digital output driver supply pin	/	55	VREF	基准电压输入和输出引脚 / Reference voltage input/output pin	O
23	SEROUT3-	Lane3 数字输出(-) / Lane 3 digital output (-)	O	56	VCM	模拟输入共模电压 / Analog input common-mode voltage	O
24	SEROUT3+	Lane3 数字输出(+) / Lane 3 digital output (+)	O	57	SYNC	数字输入，时钟分频器的同步输入 / Digital input, SYNC input of the clock divider	I
25	SEROUT2+	Lane2 数字输出(+) / Lane 2 digital output (+)	O	58	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
26	SEROUT2-	Lane2 数字输出(-) / Lane 2 digital output (-)	O	59	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
27	VDRVDD	数字输出驱动电源引脚 / Digital output driver supply pin	/	60	VINC-	ADC C 通道模拟输入(-) / ADC channel C analog input (-)	I
28	SEROUT1-	Lane1 数字输出(-) / Lane 1 digital output (-)	O	61	VINC+	ADC C 通道模拟输入(+) / ADC channel C analog input (+)	I
29	SEROUT1+	Lane1 数字输出(+) / Lane 1 digital output (+)	O	62	VAVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
30	SEROUT0+	Lane0 数字输出(+) / Lane 0 digital output (+)	O	63	NIC	空 / Not connected internally	/
31	SEROUT0-	Lane0 数字输出(-) / Lane 0 digital output (-)	O	64	NIC	空 / Not connected internally	/
32	VDRVDD	数字输出驱动电源引脚 / Digital output driver supply pin	/				

注：封装底部的热沉焊盘为模拟地端 GNDA。/ Note: the heat-sink pad at the bottom of the package is the analog ground terminal GNDA.

绝对最大额定值 / Absolute Maximum Ratings

English: - Analog supply voltage (VAVDD): -0.3V~2V - Digital supply voltage (VDVDD): -0.3V~2V - Digital output driver voltage (VDRVDD): -0.3V~2V - Storage temperature (Tstg):

中文： - 模拟电源电压（VAVDD）： -0.3V~2V - 数字电源电压（VDVDD）： -0.3V~2V - 数字输出驱动电压（VDRVDD）： -0.3V~2V - 贮存温度（Tstg）：

推荐工作条件 / Recommended Operating Conditions

English: - Operating frequency (fCLK): 80MHz~250MHz - Analog supply voltage (VAVDD): 1.7V~1.9V - Digital supply voltage (VDVDD): 1.7V~1.9V - Digital output driver voltage (VDRVDD): 1.7V~1.9V - Input signal amplitude range (peak-to-peak): ≤2V - Operating ambient temperature (TA): -40°C~85°C

中文： - 工作频率（fCLK）：80MHz~250MHz - 模拟电源电压（VAVDD）：1.7V~1.9V - 数字电源电压（VDVDD）：1.7V~1.9V - 数字输出驱动电压（VDRVDD）：1.7V~1.9V - 输入信号幅度范围（峰峰值）：≤2V - 工作环境温度（TA）：-40°C~85°C

性能指标 / Performance Specifications

Conditions / 条件（除另有规定外 / unless otherwise specified）: 1.0V 基准模式 / 1.0V reference mode, VAVDD=VDVDD=VSVDD=VDRVDD=1.8V, GNDA=GNDDVSS=0V, FS=250 MSPS, -55°C≤TC≤125°C.

特性 / Parameter	符号 / Symbol	条件 / Conditions	最小 / Min	典型值 / Typical	最大 / Max	单位 / Unit
通道数 / Number of channels	N	—		4		—
分辨率 / Resolution	RES	—		16		Bits
微分误差 / Differential nonlinearity	DNL	—	-0.99	0.6/+0.6	1.75	LSB
线性误差 / Integral nonlinearity	INL	—	-9	-6/+6	9	LSB
失调误差 / Offset error	EO	—	-0.6	0.3	0.6	%FSR
增益误差 / Gain error	EG	—	-9	1.1	9	%FSR
输出基准电压 / Output reference voltage	VREF	—	0.8	1	1.2	V
模拟电源电流 / Analog supply current	IAVDD	—	—	287	310	mA
数字电源电流 / Digital supply current	IDVDD	—	—	169	185	mA
输出接口电源电流 / Output interface supply current	IDRVDD	—	—	132	165	mA
功耗 / Power consumption	PW	—	—	1.06	1.2	W
掉电功耗 / Power-down power	PD	—	—	25	50	mW
信噪比 / SNR	SNR	fIN=10MHz, -1.0dBFS, FS=250MSPS	70	73.5	—	dBFS
信噪比 / SNR	SNR	fIN=40MHz, -1.0dBFS, FS=250MSPS	70	72	—	dBFS
信噪比 / SNR	SNR	fIN=70MHz, -5.0dBFS, FS=250MSPS	70	72	—	dBFS
信噪失真比 / SINAD	SINAD	fIN=10MHz, -1.0dBFS, FS=250MSPS	69	73.3	—	dBFS
信噪失真比 / SINAD	SINAD	fIN=40MHz, -1.0dBFS, FS=250MSPS	69	71.9	—	dBFS
信噪失真比 / SINAD	SINAD	fIN=70MHz, -5.0dBFS, FS=250MSPS	69	71.9	—	dBFS

特性 / Parameter	符号 / Symbol	条件 / Conditions	最小 / Min	典型值 / Typical	最大 / Max	单位 / Unit
无杂散动态范围 / SFDR	SFDR	fIN=10MHz, -1.0dBFS, FS=250MSPS	78	86	—	dBFS
无杂散动态范围 / SFDR	SFDR	fIN=40MHz, -1.0dBFS, FS=250MSPS	78	84	—	dBFS
无杂散动态范围 / SFDR	SFDR	fIN=70MHz, -5.0dBFS, FS=250MSPS	78	85	—	dBFS
二阶谐波 / Second harmonic	HD2	fIN=10MHz, -1.0dBFS, FS=250MSPS	—	-93	-75	dBFS
二阶谐波 / Second harmonic	HD2	fIN=40MHz, -1.0dBFS, FS=250MSPS	—	-92	-75	dBFS
二阶谐波 / Second harmonic	HD2	fIN=70MHz, -5.0dBFS, FS=250MSPS	—	-98	-75	dBFS
三阶谐波 / Third harmonic	HD3	fIN=10MHz, -1.0dBFS, FS=250MSPS	—	-86	-75	dBFS
三阶谐波 / Third harmonic	HD3	fIN=40MHz, -1.0dBFS, FS=250MSPS	—	-100	-75	dBFS
三阶谐波 / Third harmonic	HD3	fIN=70MHz, -5.0dBFS, FS=250MSPS	—	-100	-75	dBFS
总谐波失真 / Total harmonic distortion	THD	fIN=10MHz, -1.0dBFS, FS=250MSPS	—	-83	-71	dBFS
总谐波失真 / Total harmonic distortion	THD	fIN=40MHz, -1.0dBFS, FS=250MSPS	—	-89	-71	dBFS
总谐波失真 / Total harmonic distortion	THD	fIN=70MHz, -5.0dBFS, FS=250MSPS	—	-90	-71	dBFS
有效位数 / ENOB	ENOB	fIN=10MHz, -1.0dBFS, FS=250MSPS	11	11.7	—	Bits
通道隔离度 [a] / Channel isolation [a]	CT	fIN=10MHz, -1.0dBFS, FS=250MSPS	—	-100	-70	dBFS
JESD204B Lane 速率 / Lane rate	fSDATA	—	—	—	5	Gbps
JESD204B Lane 通道数 / Number of lanes	L	—	—	—	4	Lane
高电平输入电压 / Logic input high	VIH,CSB	—	1.5	1.8	1.8	V
低电平输入电压 / Logic input low	VIL,CSB	—	0	0	0.3	V
高电平输入电压 / Logic input high	VIH,SCLK	—	1.5	1.8	1.8	V
低电平输入电压 / Logic input low	VIL,SCLK	—	0	0	0.3	V
高电平输入电压 / Logic input high	VIH,SDI	—	1.5	1.8	1.8	V
低电平输入电压 / Logic input low	VIL,SDI	—	0	0	0.3	V
时钟输入频率 / Clock input frequency	fclk	—	80	250	250	MHz
采样频率 / Sampling frequency	FS	—	—	250	250	MSPS

[a] 未纳入考核，仅供用户参考使用。/ Not subject to acceptance testing; provided for user reference only.

注：典型值为常温测试数据。/ Note: typical values are room-temperature test data.

主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

VREF = 1.0 V:

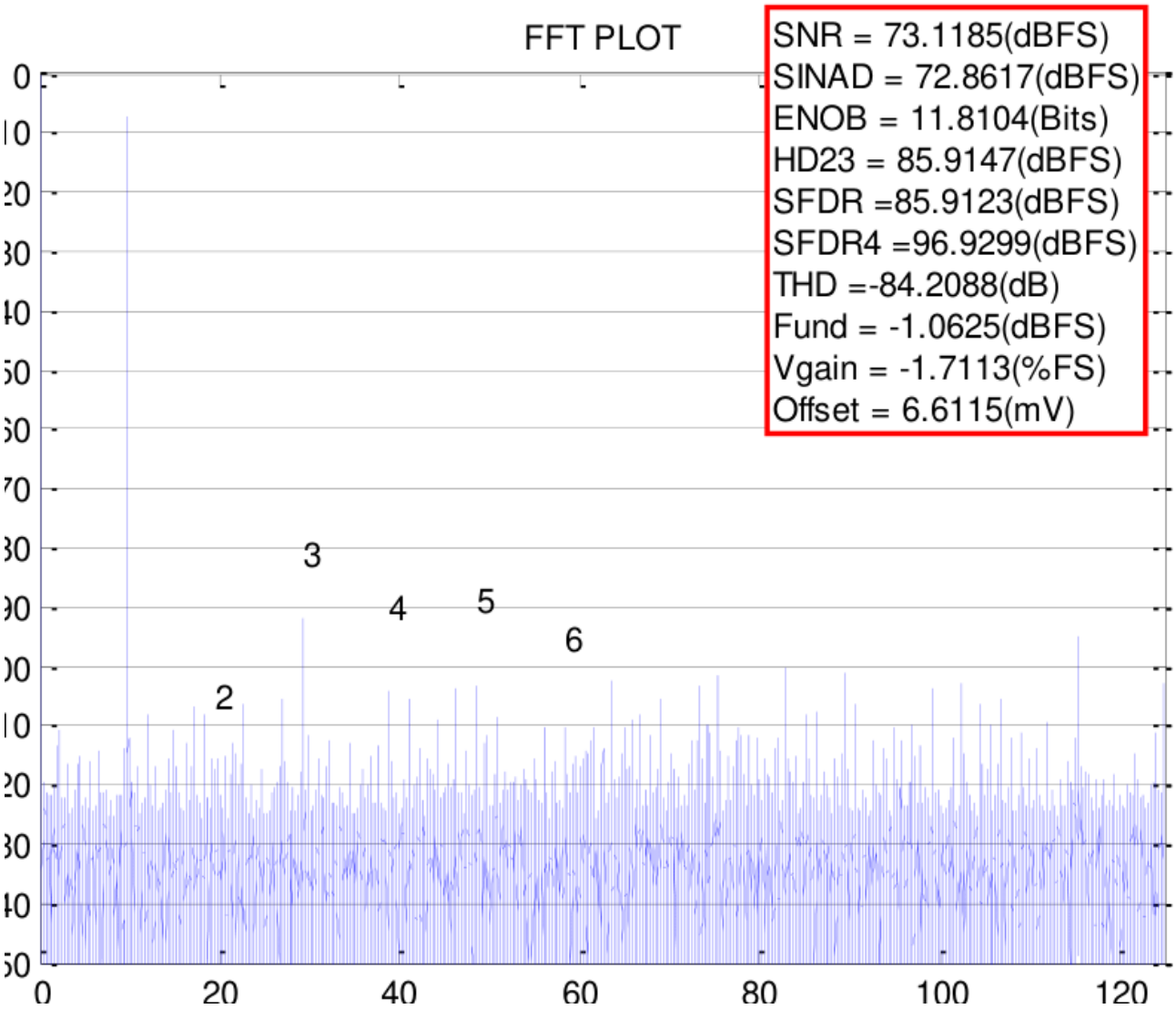


Figure 5: Single-tone 32K FFT (fIN=10MHz, fS=250MSPS)

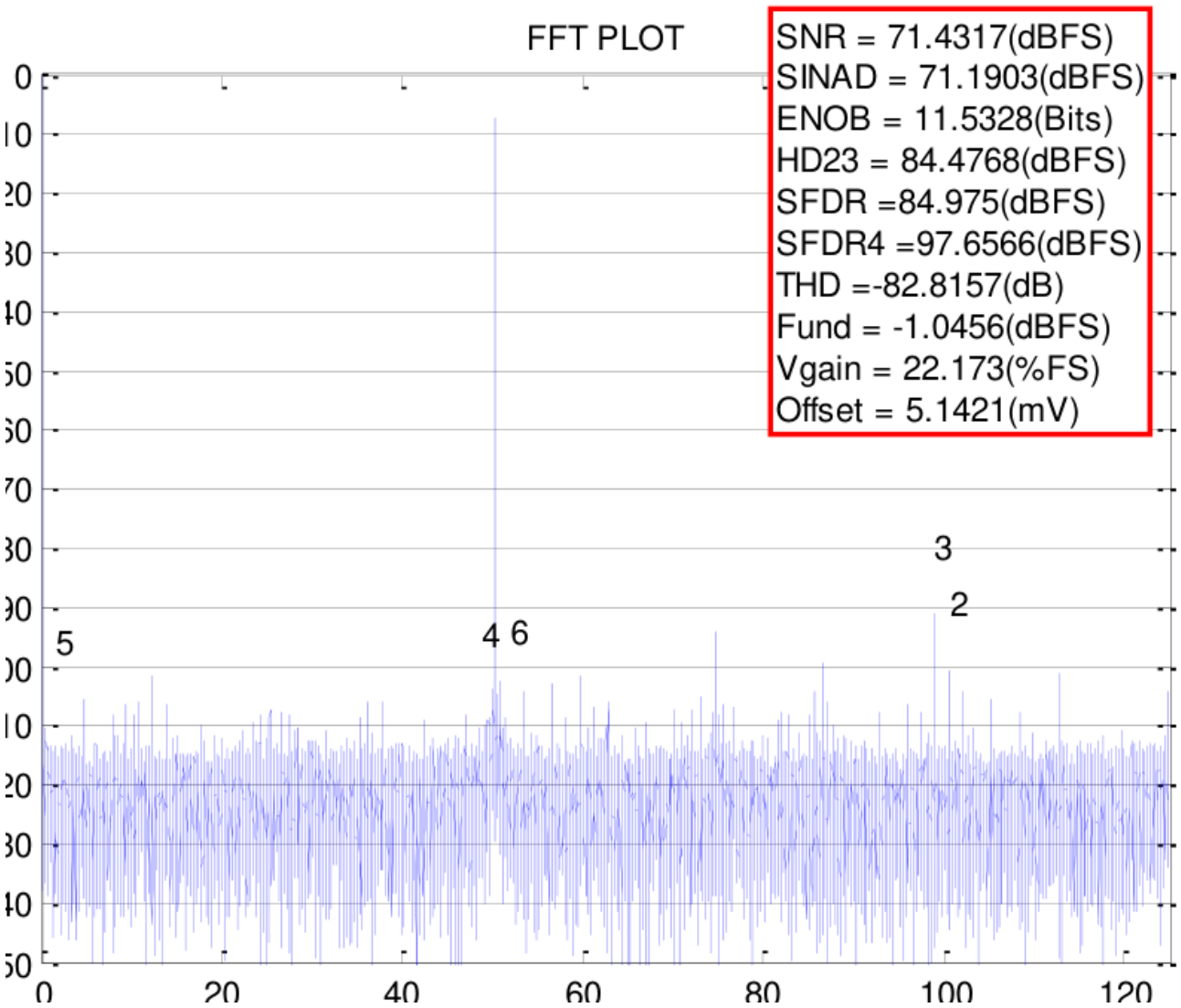


Figure 6: Single-tone 32K FFT (fIN=50MHz, fS=250MSPS)

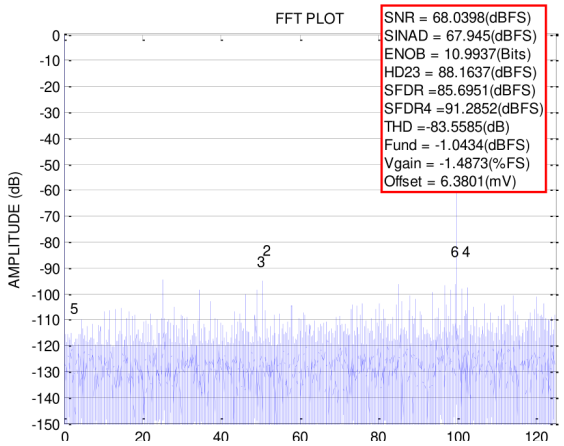


Figure 7: Single-tone 32K FFT (fIN=100MHz, fS=250MSPS)

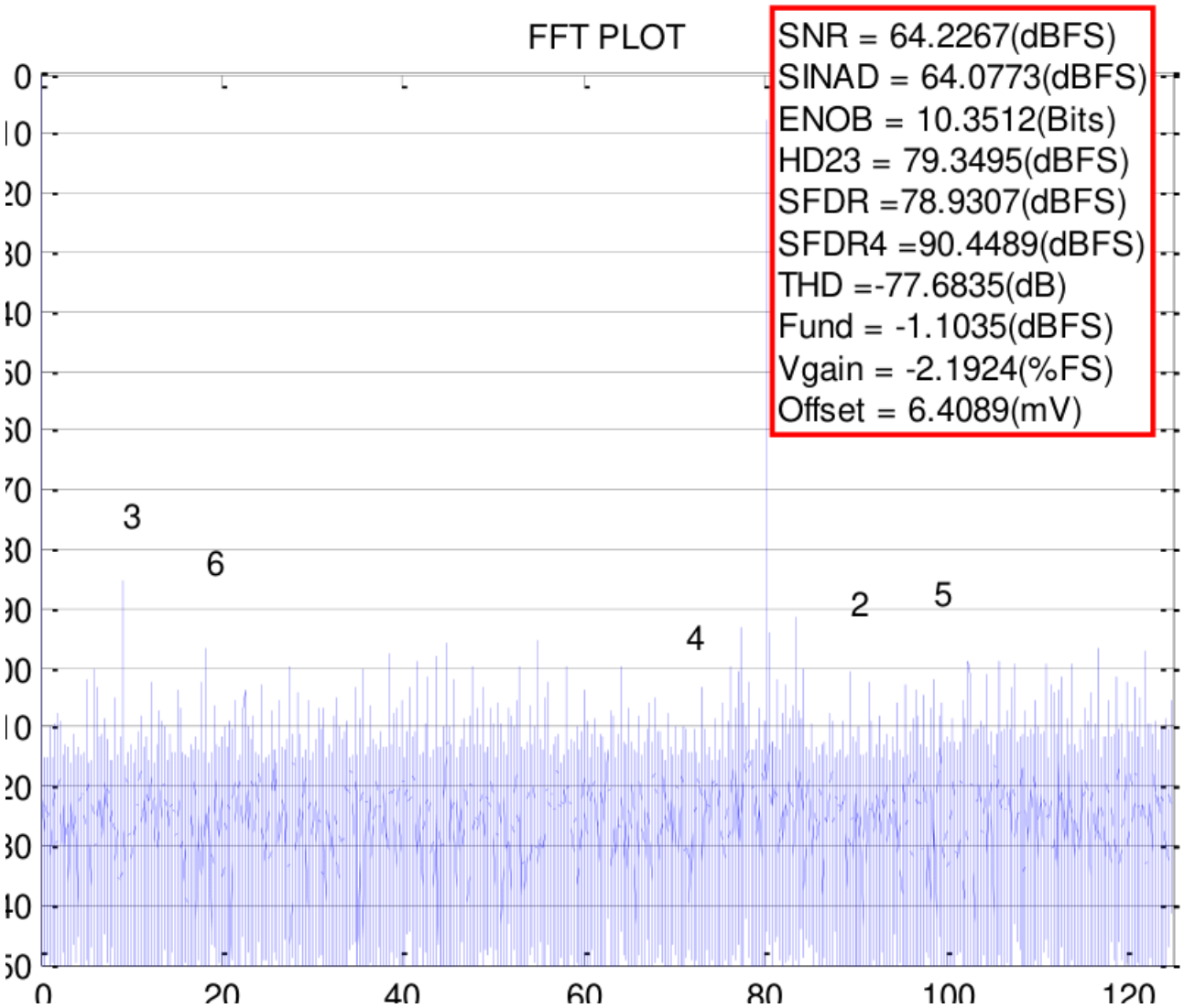


Figure 8: Single-tone 32K FFT (fIN=170MHz, fS=250MSPS)

Figure 9: Static DNL/INL test (fIN=1MHz, fS=250MSPS)

[原图待插入。需要详细原图请联系FAE。 / figure to be inserted. Contact FAE for detailed original figures.]

VREF = 1.4 V:

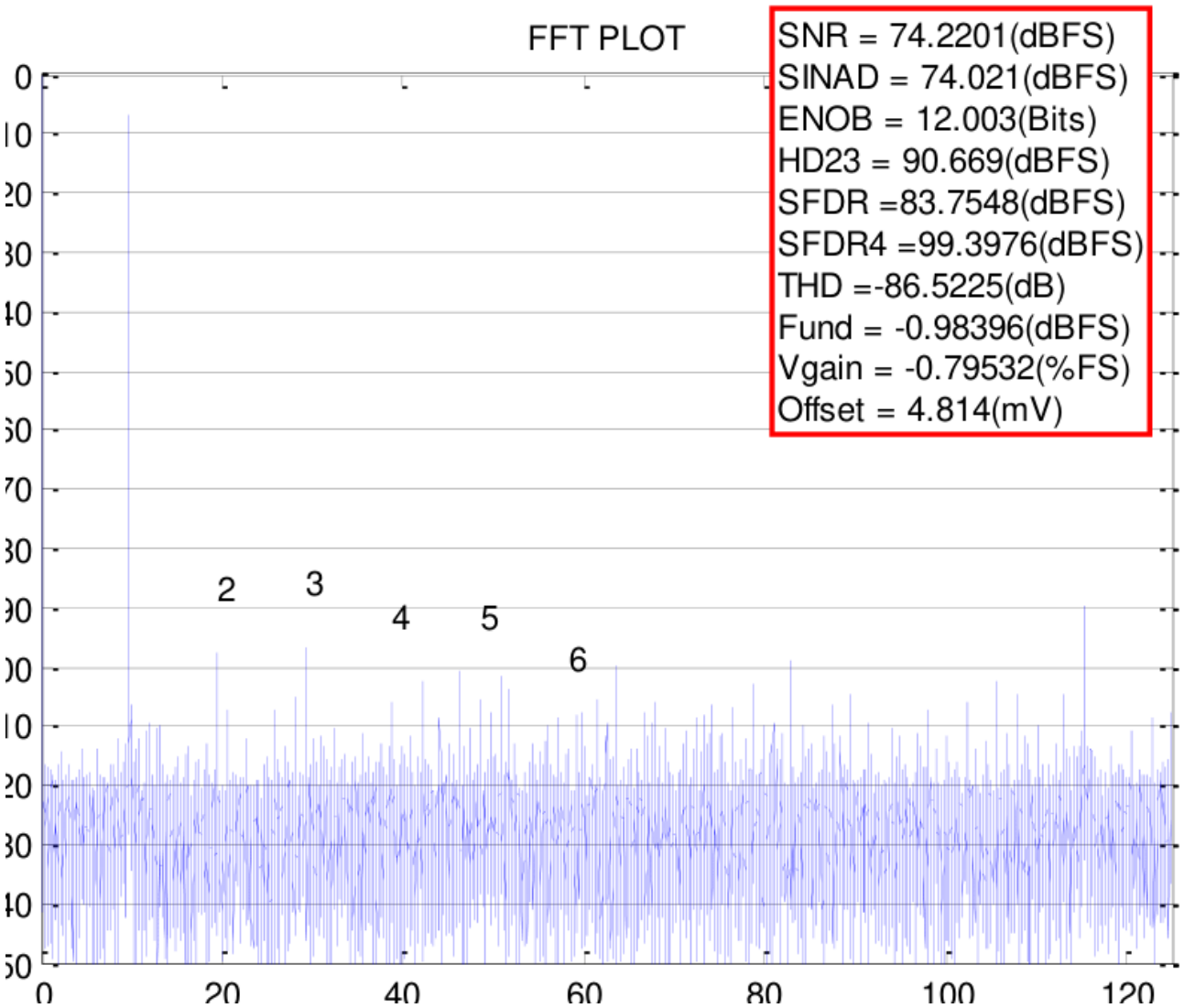


Figure 10: Single-tone 32K FFT (fIN=10MHz, fS=250MSPS)

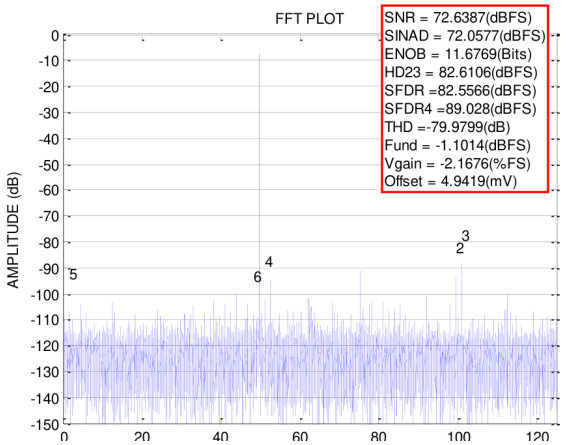


Figure 11: Single-tone 32K FFT (fIN=50MHz, fS=250MSPS)

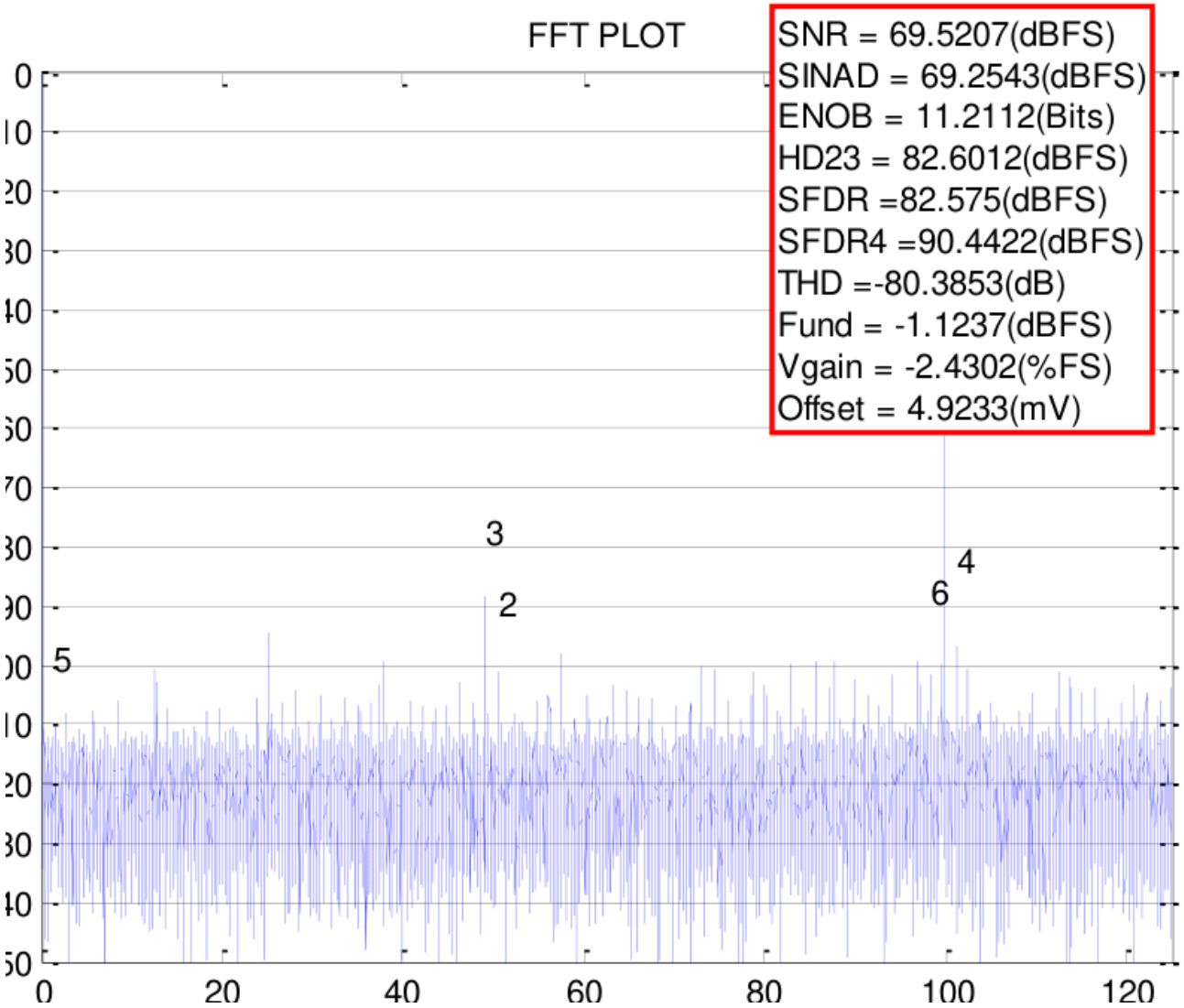


Figure 12: Single-tone 32K FFT (fIN=100Hz, fS=250MSPS)

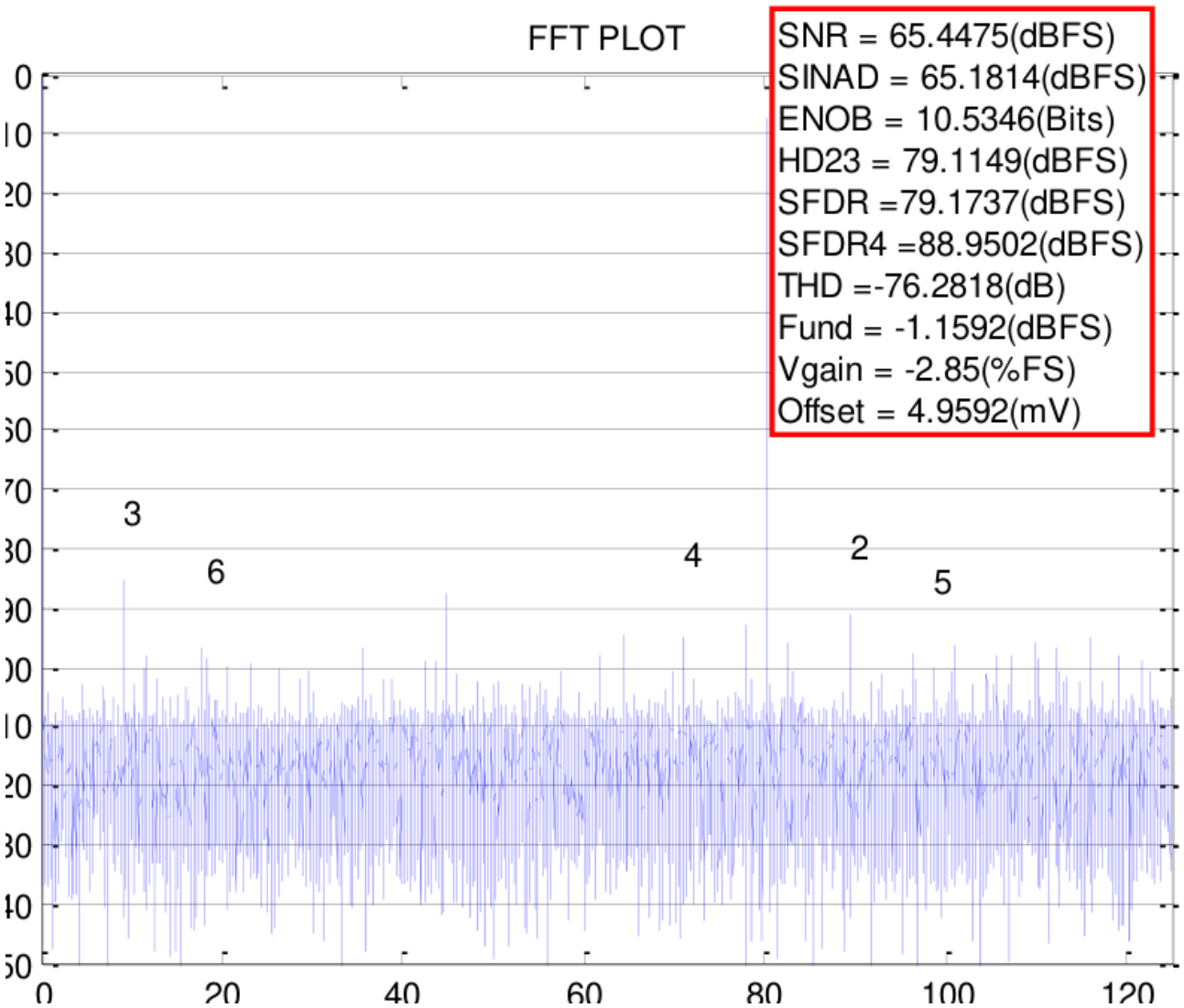


Figure 13: Single-tone 32K FFT (fIN=170MHz, fS=250MSPS)

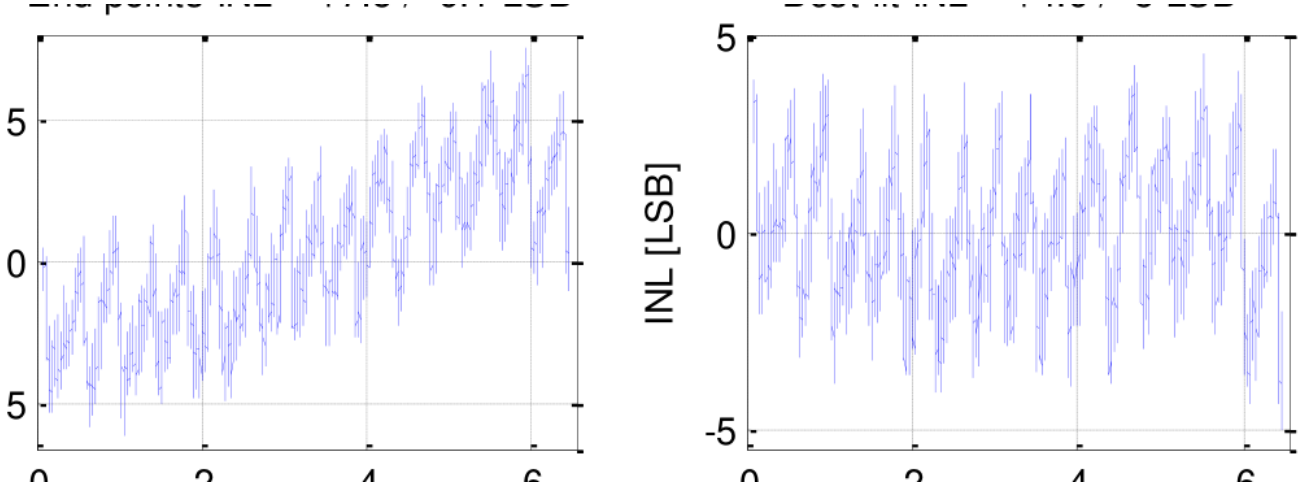


Figure 14: Static DNL/INL test (fIN=1MHz, fS=250MSPS)

典型应用线路图 / Typical Application Circuit

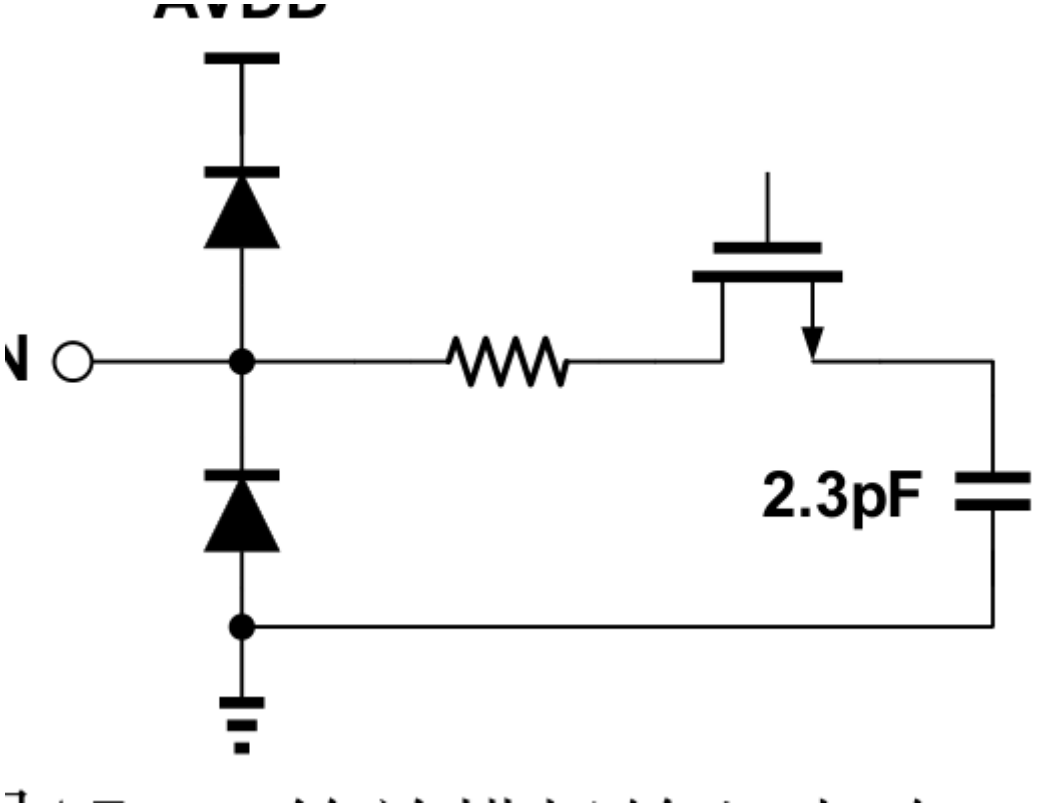


Figure 15: Equivalent analog input circuit

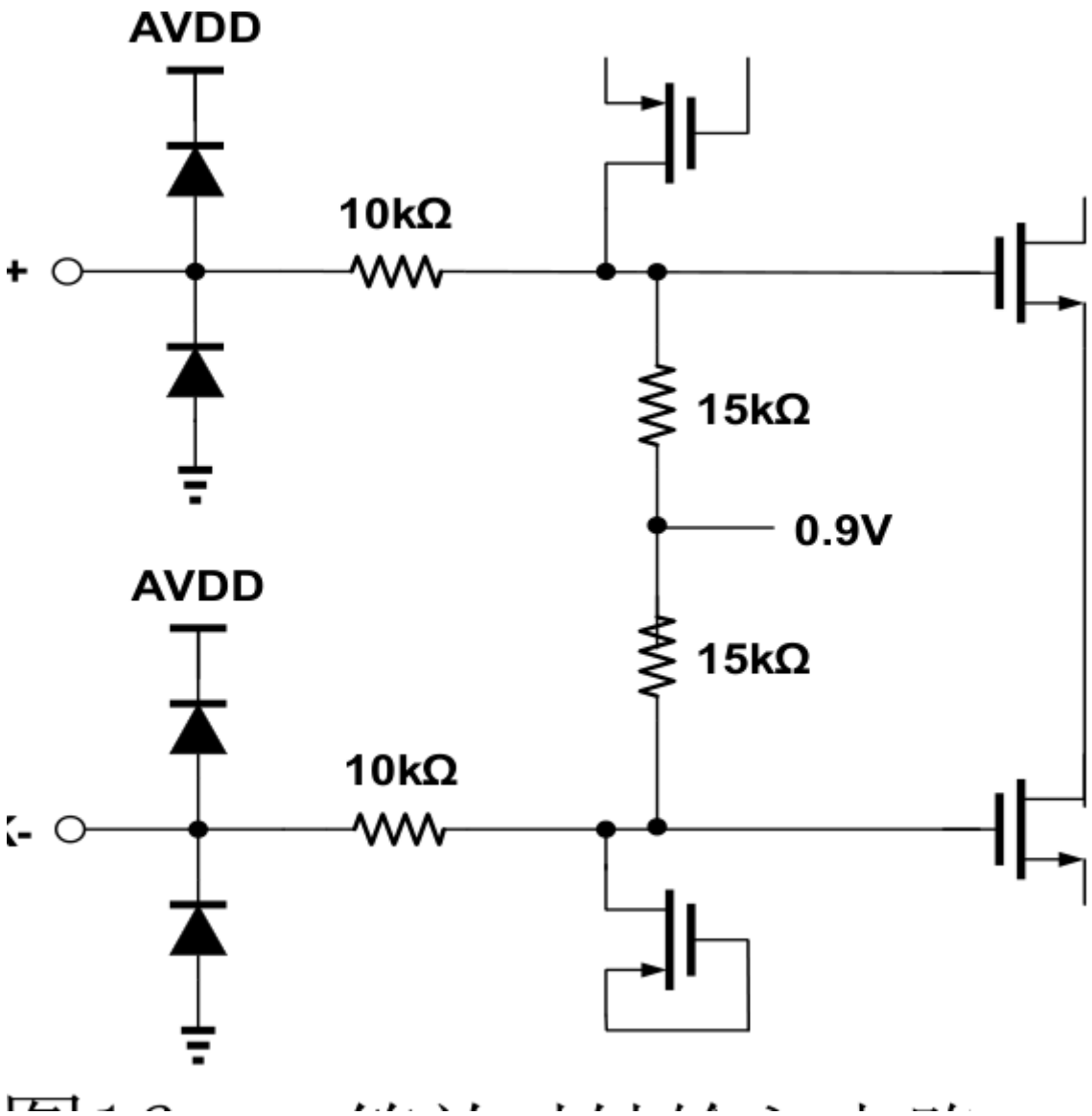


Figure 16: Equivalent clock input circuit

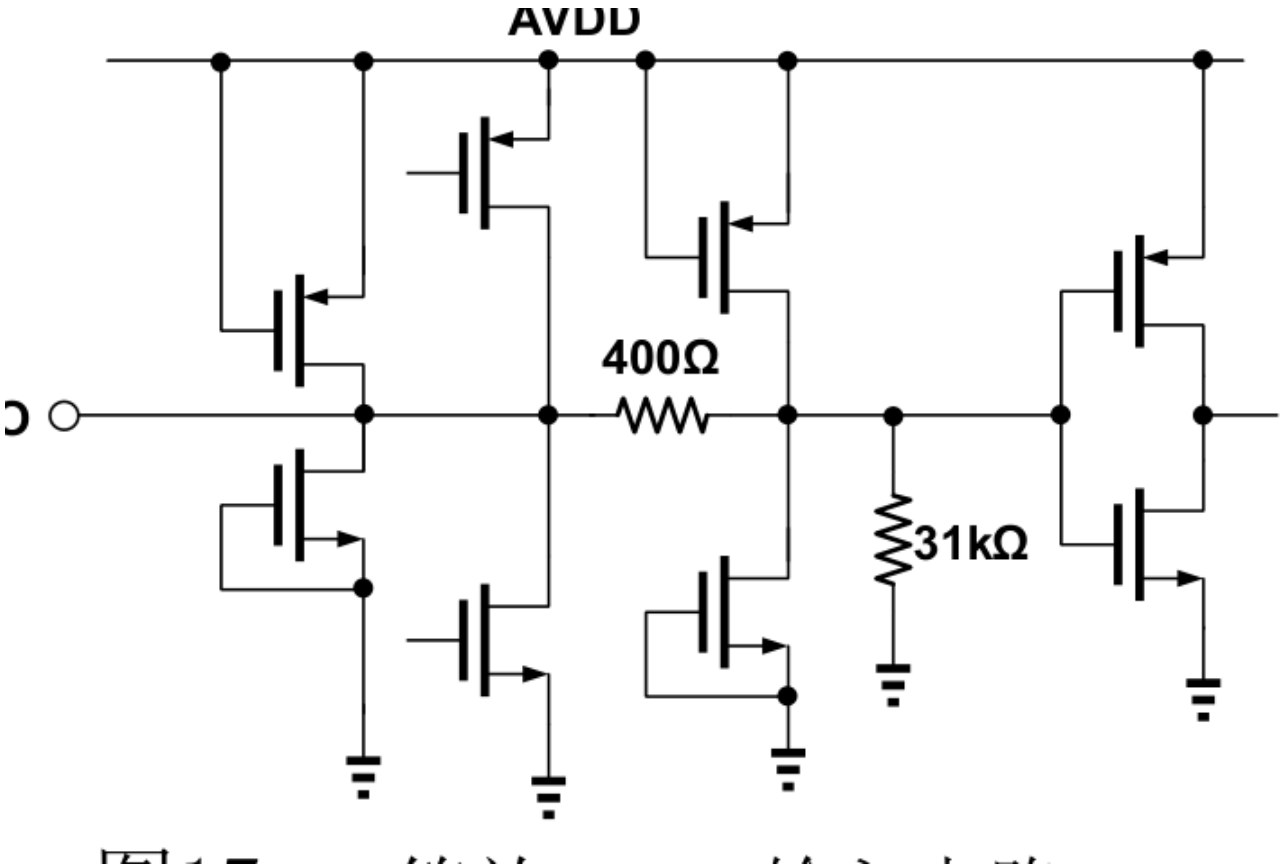


Figure 17: Equivalent SDIO input circuit

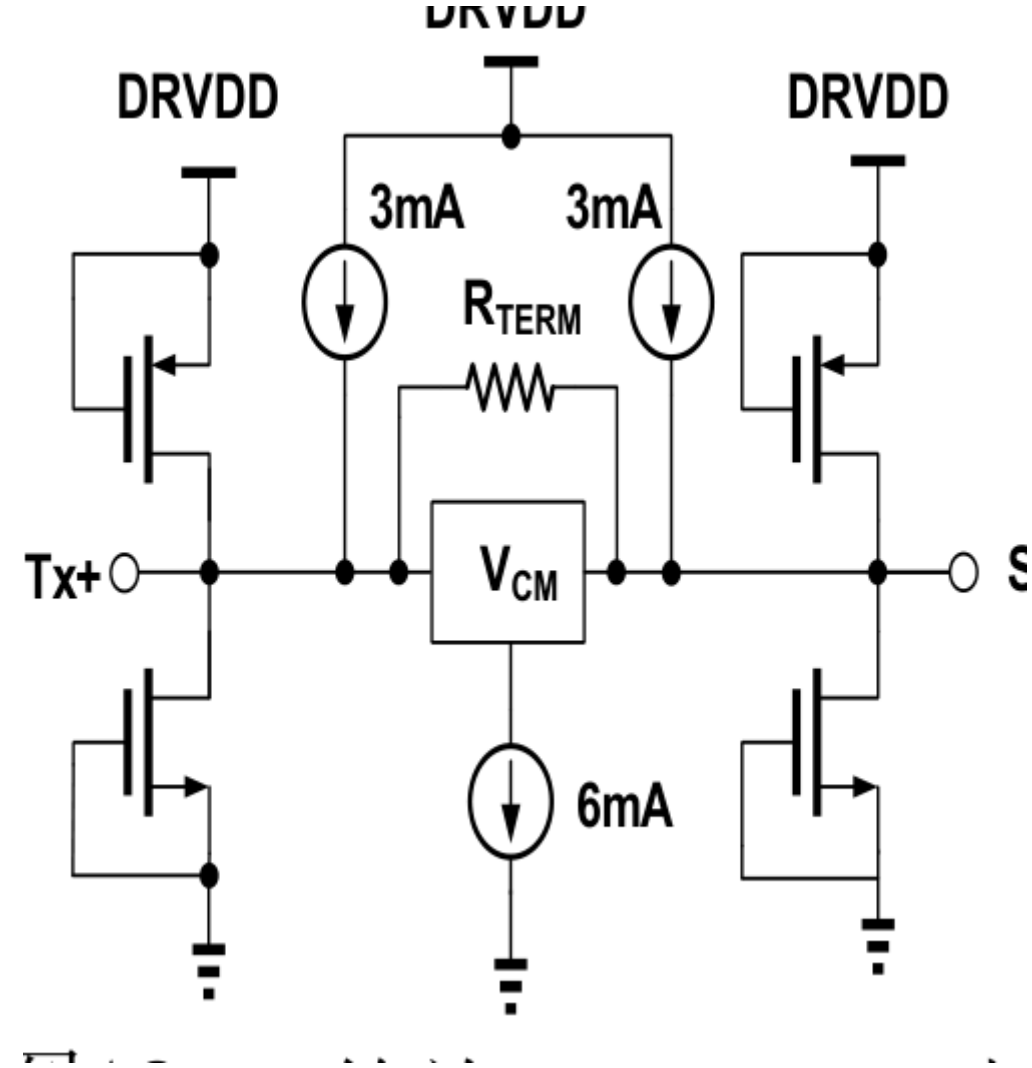


Figure 18: Equivalent SERDOUT± circuit

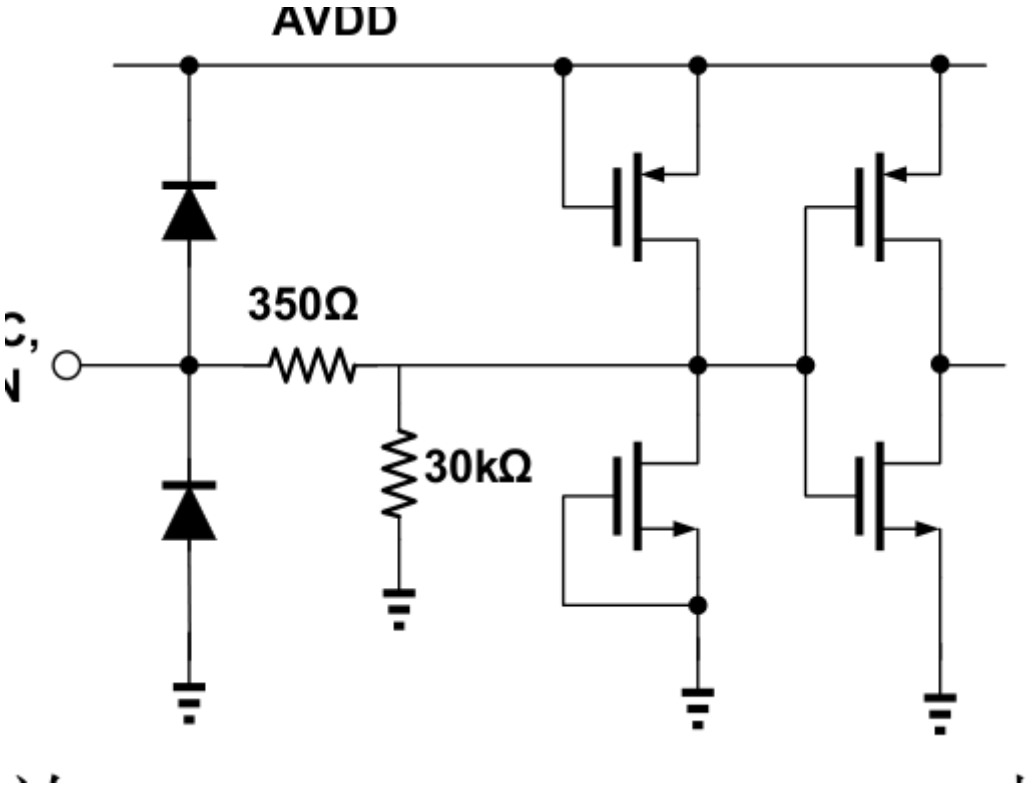


Figure 19: Equivalent SCLK, SYNC and PDWN circuit

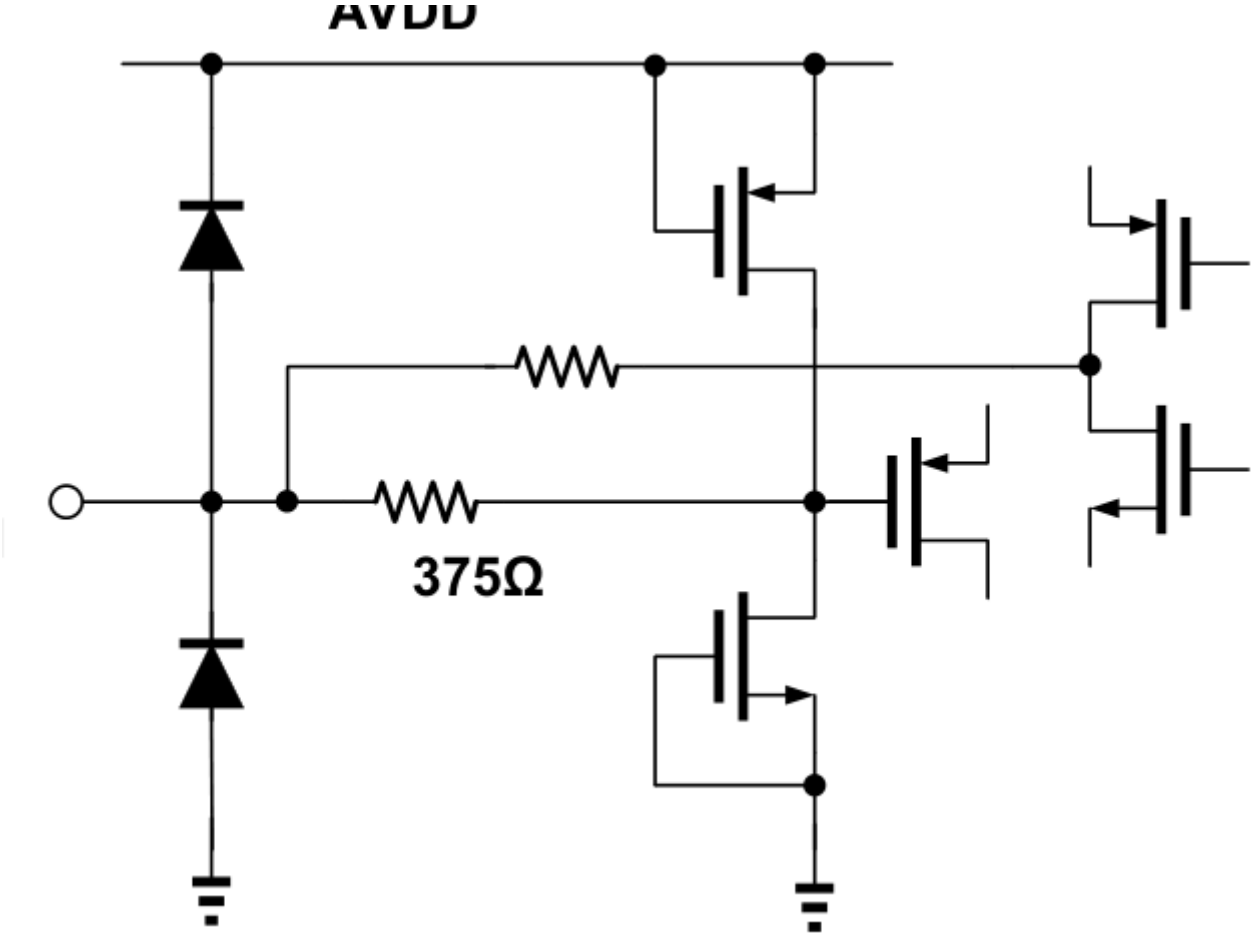


Figure 20: Equivalent RBIAS and VCM circuit

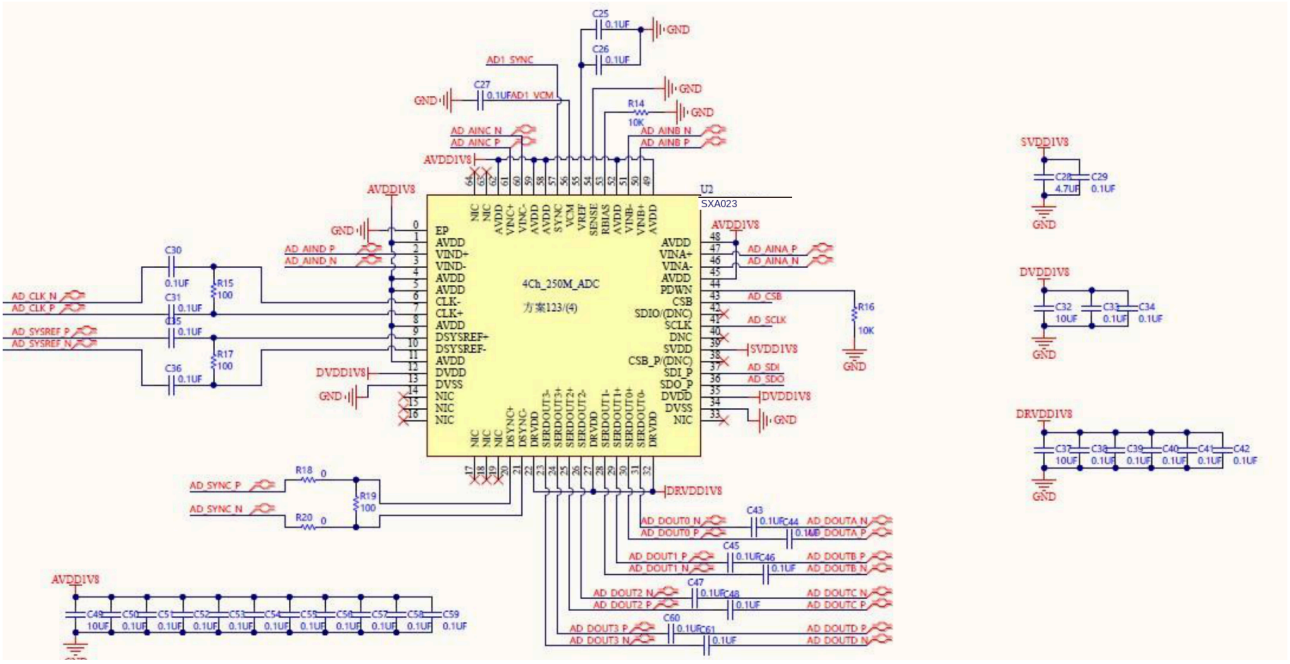


图21: SXA023 典型外围电路图

Figure 21: SXA023 typical peripheral circuit

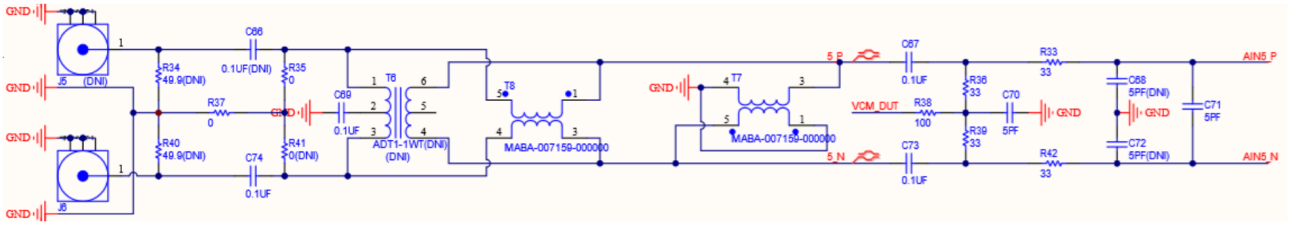


Figure 22: Analog front end

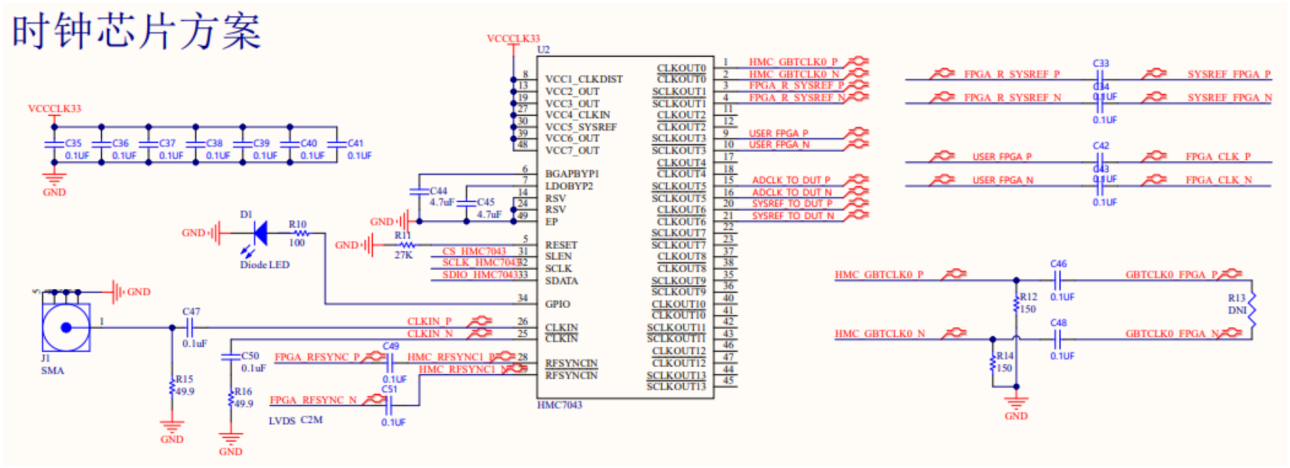


Figure 23: Clock circuit

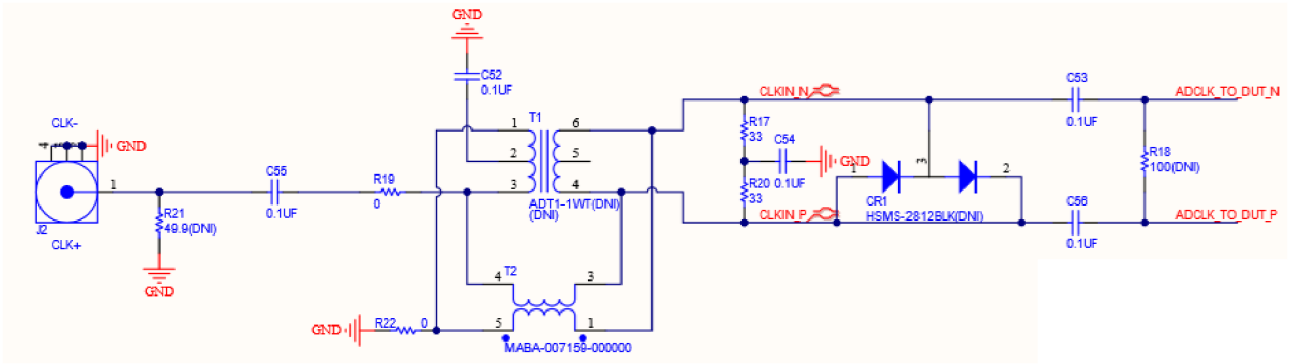


Figure 24: External clock supply circuit

单元模块及工作原理 / Functional Blocks and Operating Principles

1、原理概述 / Overview

English: The core of this product uses a multistage pipelined ADC architecture, in which each stage provides one redundant bit to eliminate the offset error of the coarse quantization comparators. The pipelined quantization structures of all stages are reconstructed in the digital domain by a shift-and-add unit to form the 16-bit conversion result. A serializer transmits this conversion result in a 16-bit output format.

Except for the last stage, each pipeline stage consists of a low-resolution flash ADC, a switched-capacitor DAC connected to it, and an interstage residue amplifier (for example, a multiplying DAC [MDAC]). The

residue amplifier amplifies the difference between the reconstructed DAC output and the flash input and provides it to the next pipeline stage. To assist digital correction of flash errors, each stage is assigned one bit of redundancy. The last stage consists of a flash ADC only.

中文： 本产品内核使用多级流水线型 ADC 架构，各级提供一位冗余位消除粗量化比较器的失调误差。各级流水线量化结构在数字域由移位加法器重构形成 16 位转换结果。串化器以十六位输出格式发送该转换结果。

除最后一级以外，流水线的每一级都由一个低分辨率 Flash 型 ADC、与之相连的一个开关电容 DAC 和一个级间余量放大器（例如乘法数模转换器 [MDAC]）组成。余量放大器放大重构 DAC 输出与 Flash 型输入之差，以便提供给流水线的下一级。为了帮助对 Flash 误差进行数字校正，每一级设定了一位的冗余量。最后一级仅由一个 Flash 型 ADC 组成。

2、模拟输入 / Analog Input

English: The analog input of this product is a differential switched-capacitor circuit designed to process differential input signals. The circuit supports a wide common-mode range while maintaining excellent performance. Signal-related errors are smallest, and the best performance is achieved, when the input common-mode voltage is at mid-supply.

The input circuit switches between sample mode and hold mode according to the clock signal (see Figure 25). When the input circuit switches to sample mode, the signal source must be able to charge the sampling capacitor and settle within half a clock cycle. A small resistor in series with each input helps reduce the peak transient current injected from the driver output stage. In addition, a low-Q inductor or ferrite bead can be used on each side of the input to reduce the high differential capacitance at the analog input, thereby achieving the maximum ADC bandwidth. When driving the converter front end at high IF, a low-Q inductor or ferrite bead must be used. A differential capacitor or two single-ended capacitors can be used at the input to provide a matched passive network. This ultimately forms a low-pass filter at the input, limiting unwanted wideband noise.

中文： 本产品的模拟输入端为一个差分开关电容电路，设计用于处理差分输入信号。该电路支持宽共模范围，同时能保持出色的性能。当输入共模电压为中间电源电压时，信号相关误差最小，并且能实现最佳性能。

输入电路根据时钟信号在采样模式和保持模式之间切换（见图 25）。当输入电路切换到采样模式时，信号源必须能够对采样电容充电，并且在半个时钟周期内完成建立。每个输入端都串联一个小电阻，帮助降低从驱动源输出级注入的峰值瞬态电流。此外，输入端的每一侧可以使用低 Q 电感或铁氧体磁珠，以减小模拟输入端的高差分电容，从而实现 ADC 的最大带宽。在高中频（IF）下驱动转换器前端时，必须使用低 Q 电感或铁氧体磁珠。输入端可以使用一个差分电容或两个单端电容，以提供匹配的无源网络。这最终会在输入端形成一个低通滤波器，用来限制无用的宽带噪声。

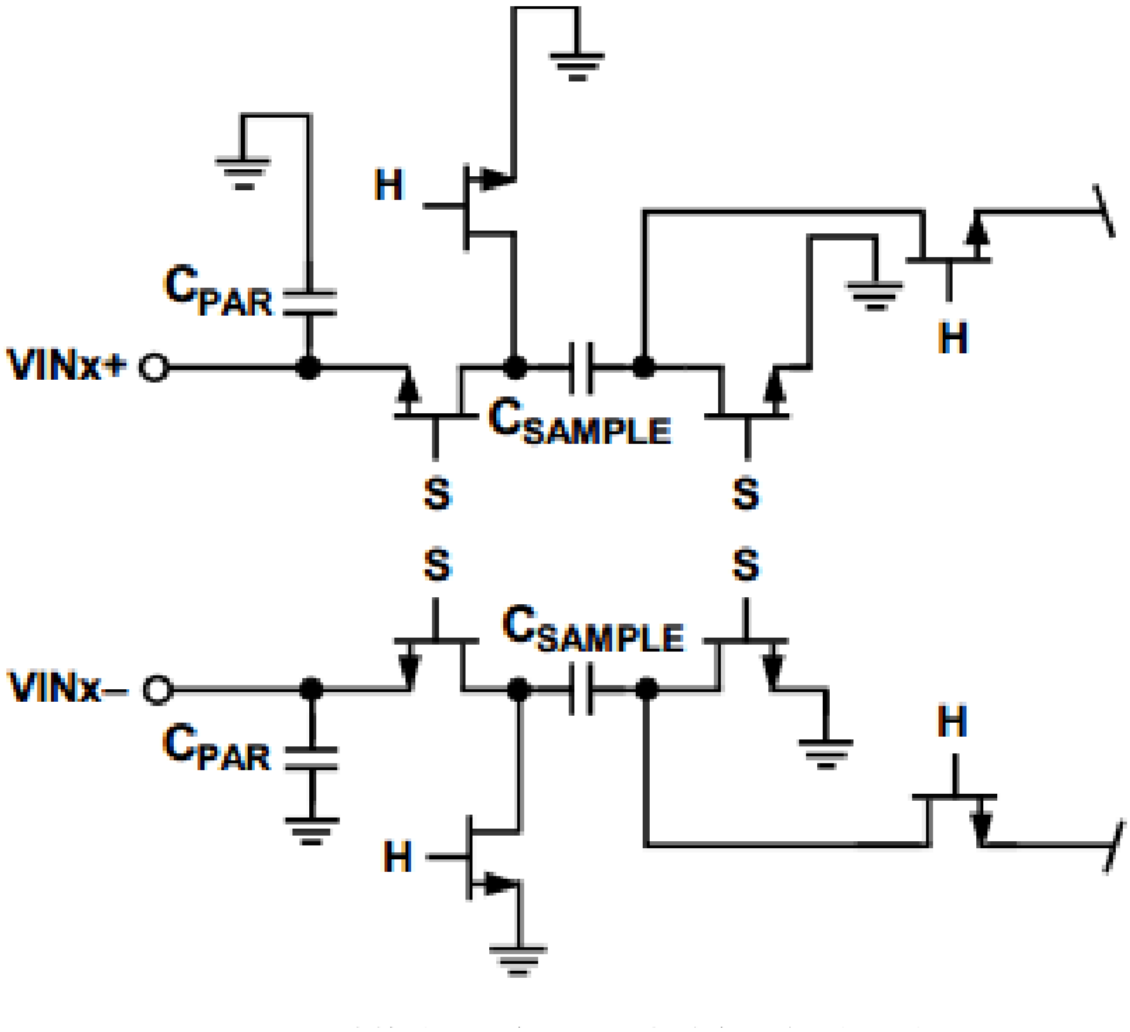


Figure 25: Analog input equivalent circuit

3、输入共模电平 / Input Common-Mode Level

English: The analog input of this product has no internal DC bias; in AC-coupled applications, the user must provide an external bias. For the best dynamic performance, the user must configure the device so that the input common-mode level VCM = AVDD/2. This device can also achieve reasonable performance over a wider input common-mode range, as shown in Figure 26 and Figure 27.

This product provides an on-chip reference voltage through the VCM pin; the VCM pin must be bypassed to ground with a 0.1 µF capacitor.

In a differential configuration, setting the device input to the maximum range achieves the highest signal-to-noise ratio (SNR) performance. For this product the input range depends on the reference voltage; performance degrades sharply beyond the input range.

中文： 本产品的模拟输入端无内部直流偏置，在交流耦合应用中，用户必须提供外部偏置。为了获得最佳的动态性能，用户必须对器件进行配置，使输入共模电平 VCM=AVDD/2。本器件在更宽的输入共模范围内也能获得合理的性能，如图 26 和图 27 所示。

本产品通过引脚 VCM 提供片内基准电压，必须使用一个 0.1F 电容将 VCM 引脚旁路到地。

在差分配置中，将器件输入设置为最大范围可以实现最高的信噪比（SNR）性能，对于本产品输入范围取决于基准电压，超过输入范围性能将急剧恶化。

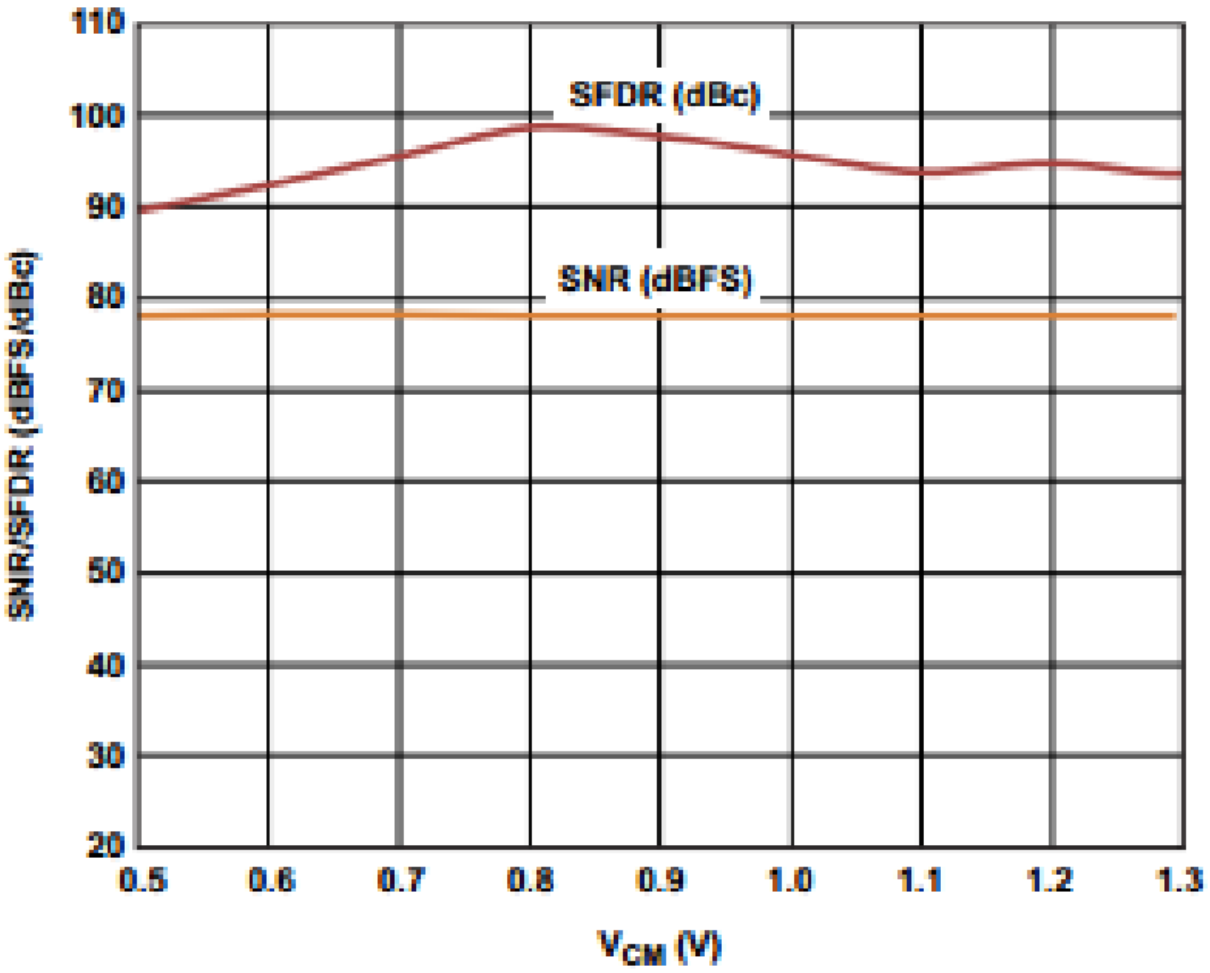


Figure 26: SNR/SFDR vs. input common-mode level (VCM) (fIN=9.7MHz, fSAMPLE=250MSPS, VREF=1.0V)

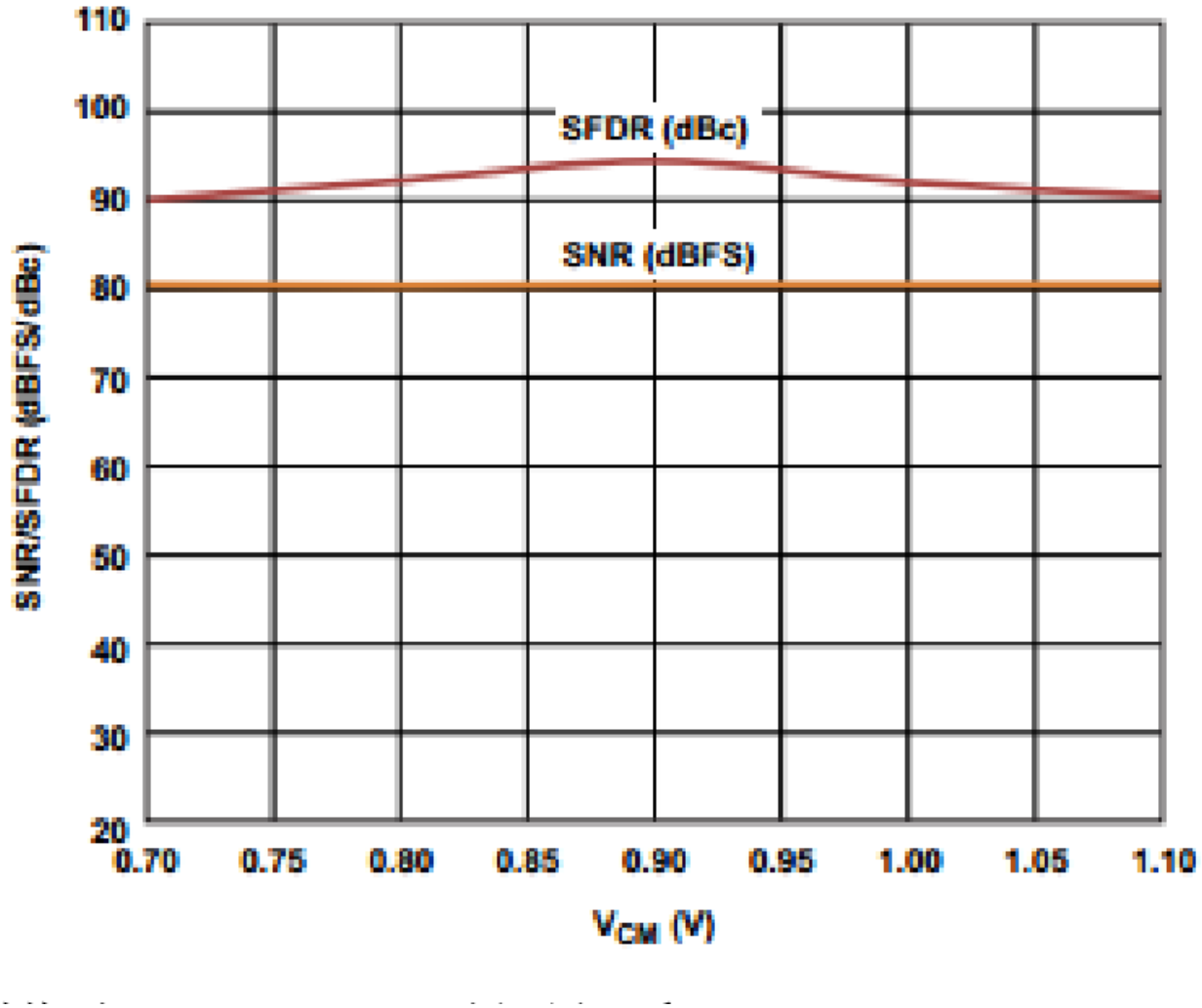


Figure 27: SNR/SFDR vs. input common-mode level (VCM) (fIN=9.7MHz, fSAMPLE=250MSPS, VREF=1.4V)

4、差分输入配置 / Differential Input Configuration

English: There are multiple active and passive methods to drive this product effectively; differential driving suppresses even-order harmonics and yields the best performance.

In baseband applications, driving this product with a differential balun configuration provides excellent performance and a flexible interface for the ADC (see Figure 28).

In applications where SNR is the key parameter, because the noise performance of most amplifiers is insufficient for the true performance of this product, the input configuration requires differential transformer coupling (see Figure 29).

The C capacitor values in both applications above must be used in conjunction with the input spectrum; when converting high-frequency analog input signals, it is recommended to reduce this capacitance or remove the capacitor.

Single-ended input driving of this product is not recommended.

中文： 有多种有源和无源方式可以有效驱动本产品，通过差分方式驱动可以抑制偶次谐波从而获得最佳性能。

在基带应用中，利用差分巴伦配置驱动本产品能够为 ADC 提供出色的性能和灵活接口（参考图 28）。

在 SNR 为关键参数的应用中，因为绝大部分放大器的噪声性能不足以满足本产品的真实性能，所以输入配置要求采用差分变压器耦合（参考图 29）。

以上两种应用中的 C 电容值需要和输入频谱配合使用，建议转换高频模拟输入信号时减小该电容容值或者移除该电容。

不建议单端输入方式驱动本产品。

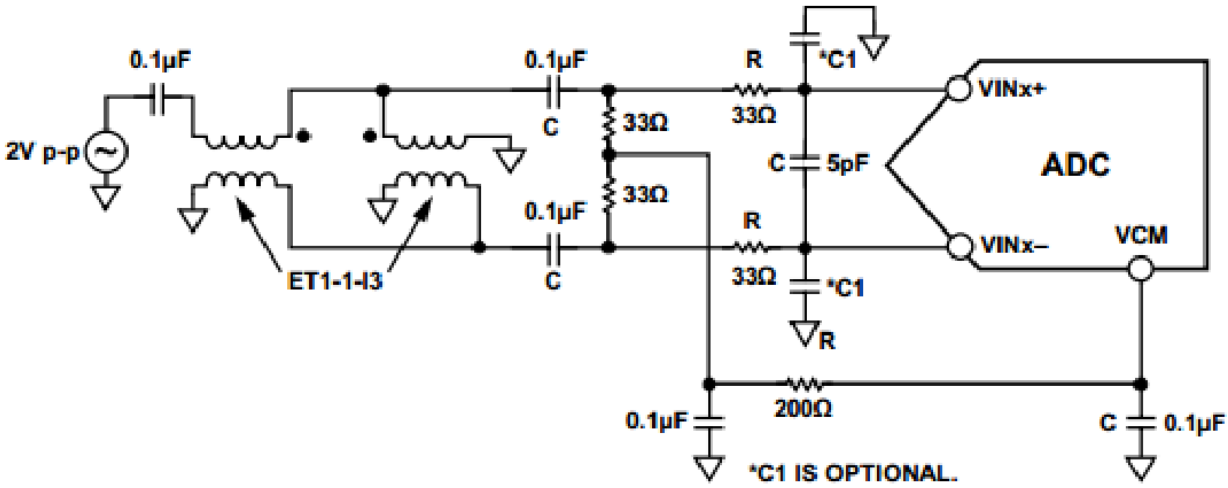


Figure 28: Differential dual-balun configuration

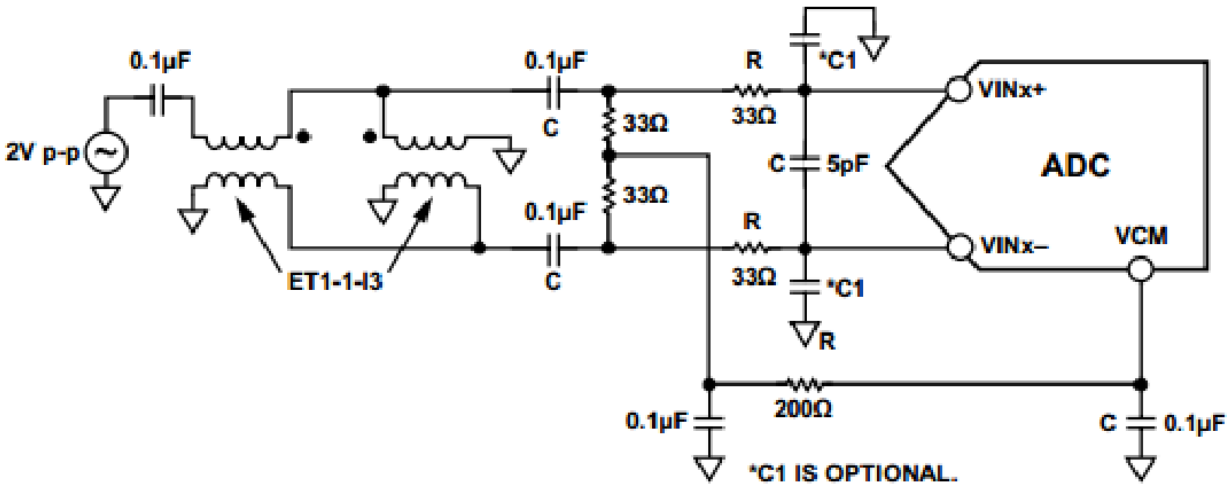


图28　差分双巴伦配置

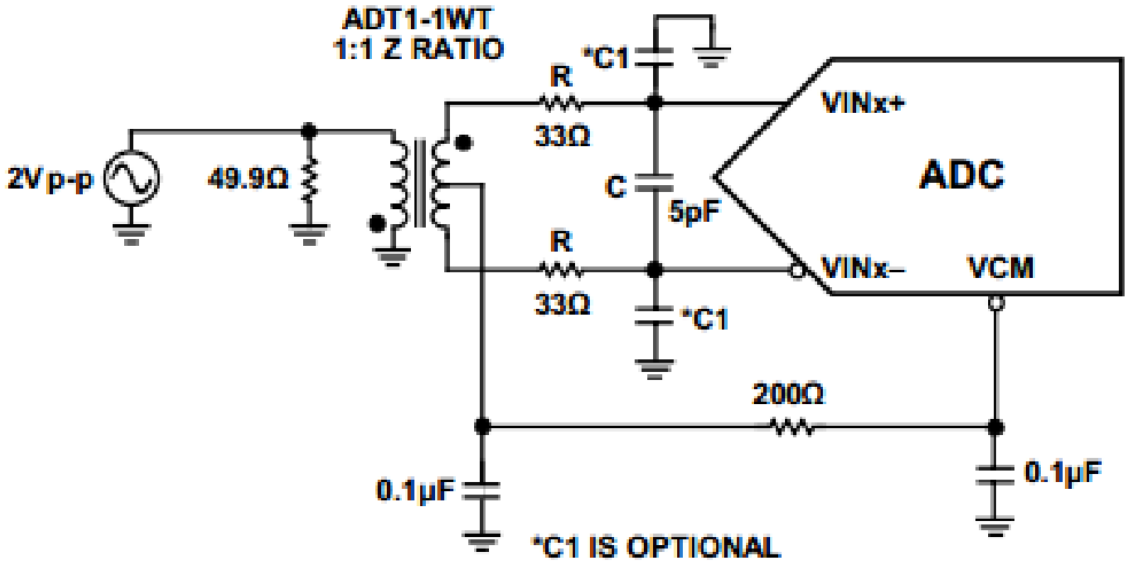


Figure 29: Differential transformer coupling

5、基准电压 / Reference Voltage

English: This product integrates a stable, accurate reference voltage source. VREF can be configured using the internal 1.0 V reference, an externally applied reference of 1.0 V to 1.4 V, or an external resistor divider acting on the internal reference, producing a user-selectable reference voltage. For a description of the reference source modes, see the "Internal Reference Connection" and "External Reference" sections. The VREF pin should be bypassed to ground with a parallel combination of an external low-ESR 1.0 μF capacitor and a low-ESR 0.1 μF ceramic capacitor.

The built-in comparator of this product can detect the voltage on the SENSE pin, thereby configuring the reference into one of three possible modes. If the SENSE pin is grounded, the reference amplifier switch

connects to the internal resistor divider (see Figure 30), setting the VREF pin voltage to 1.0 V. If the SENSE pin is connected to an external resistor divider (see Figure 31), then VREF is defined as:

Vref = 0.5 × (1 + R2/R1), where 7 kΩ ⩽ (R1 + R2) ⩽ 10 kΩ.

If the internal reference of this product is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 32 and Figure 33 show how loading affects the internal reference.

An external reference may be required to further improve ADC gain accuracy and thermal drift characteristics. Figure 34 and Figure 35 show the typical drift characteristics of the internal reference source in 1.0 V mode and 1.4 V mode, respectively. Connecting the SENSE pin to AVDD disables the internal reference source, allowing an external reference source to be used. The internal reference buffer presents a load equivalent to 7.5 kΩ to the external reference source. The internal buffer generates the positive and negative full-scale references for the ADC core. Leaving the SENSE pin floating is not recommended.

中文： 本产品内置稳定、精确的基准电压源。VREF 可以利用内部 1.0 V 基准电压、外部施加的 1.0 V 至 1.4 V 基准电压或作用于内部基准电压的外部电阻分压器来配置，产生用户可选的基准电压。基准电压源模式说明参见"内部基准电压连接"部分和"外部基准电压"部分。VREF 引脚应通过外部一个低等效串联电阻（ESR）1.0μF 电容和一个低 ESR 0.1μF 陶瓷电容的并联旁路至地。

本产品的内置比较器可检测出 SENSE 引脚的电压，从而将基准电压配置成三种可能的模式之一。如果 SENSE 引脚接地，则基准电压放大器开关与内部电阻分压器相连（见图 30），因而将 VREF 引脚电压设为 1.0 V。如果 SENSE 引脚连接到外部电阻分压器（见图 31），则 VREF 定义为：

Vref=0.5 x (1 + R2/R1)，其中，7 kΩ ⩽ (R1 + R2) ⩽ 10 kΩ。

如需利用本产品的内部基准电压来驱动多个转换器，从而提高增益的匹配度，则必须考虑到其它转换器对基准电压的负载。图 32 和图 33 显示负载如何影响内部基准电压。

必须采用外部基准电压才可能进一步提高 ADC 增益精度、改善热漂移特性。图 34 和图 35 显示内部基准电压源分别在 1.0 V 模式和 1.4 V 模式下的典型漂移特性。将 SENSE 引脚与 AVDD 相连时，可以禁用内部基准电压源，从而允许使用外部基准电压源。内部基准电压缓冲器对外部基准电压源的负载相当于 7.5 kΩ 负载。内部缓冲器为 ADC 内核生成正、负满量程基准电压。不建议悬空 SENSE 引脚。

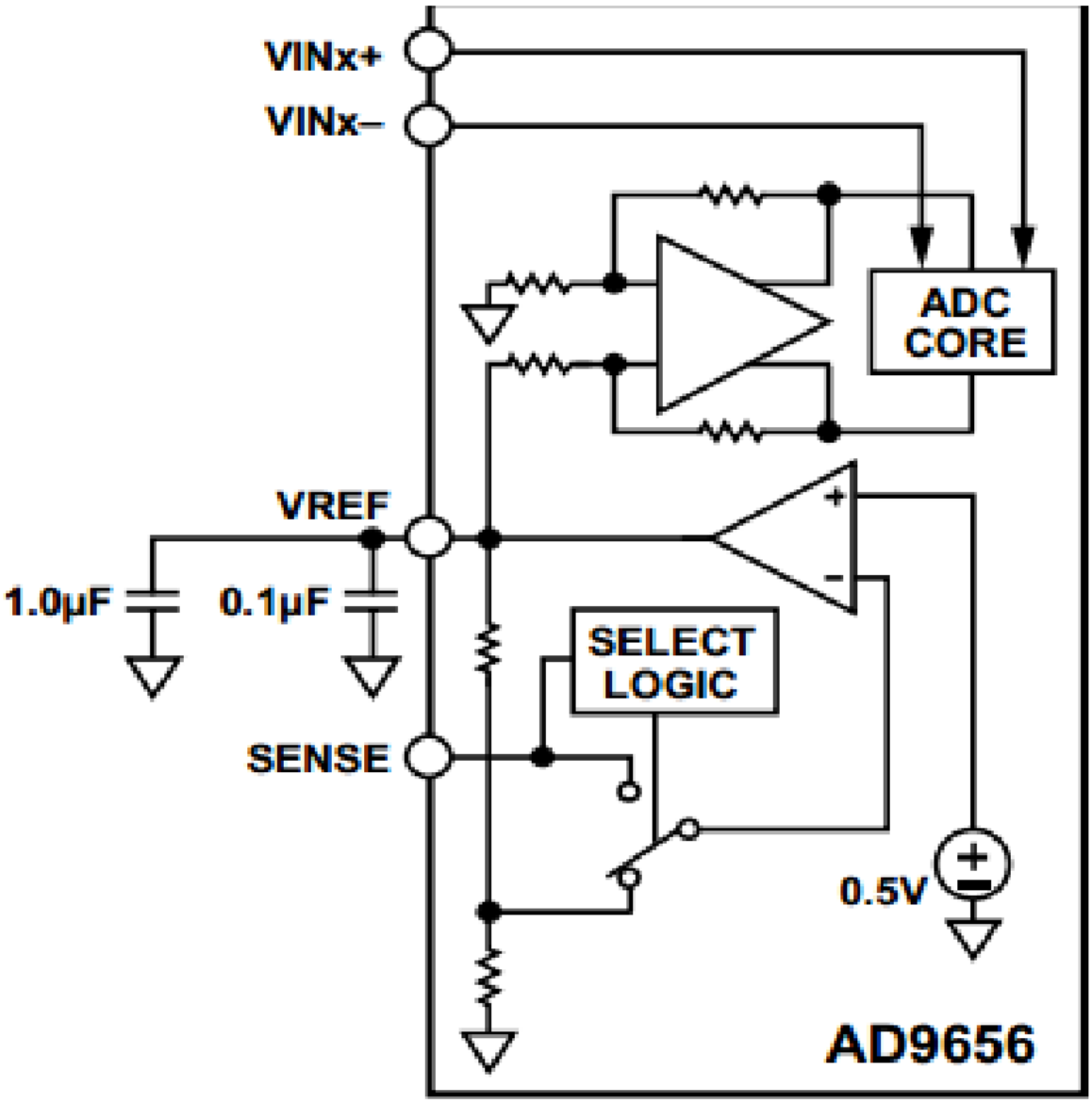


Figure 30: Reference voltage configuration 1

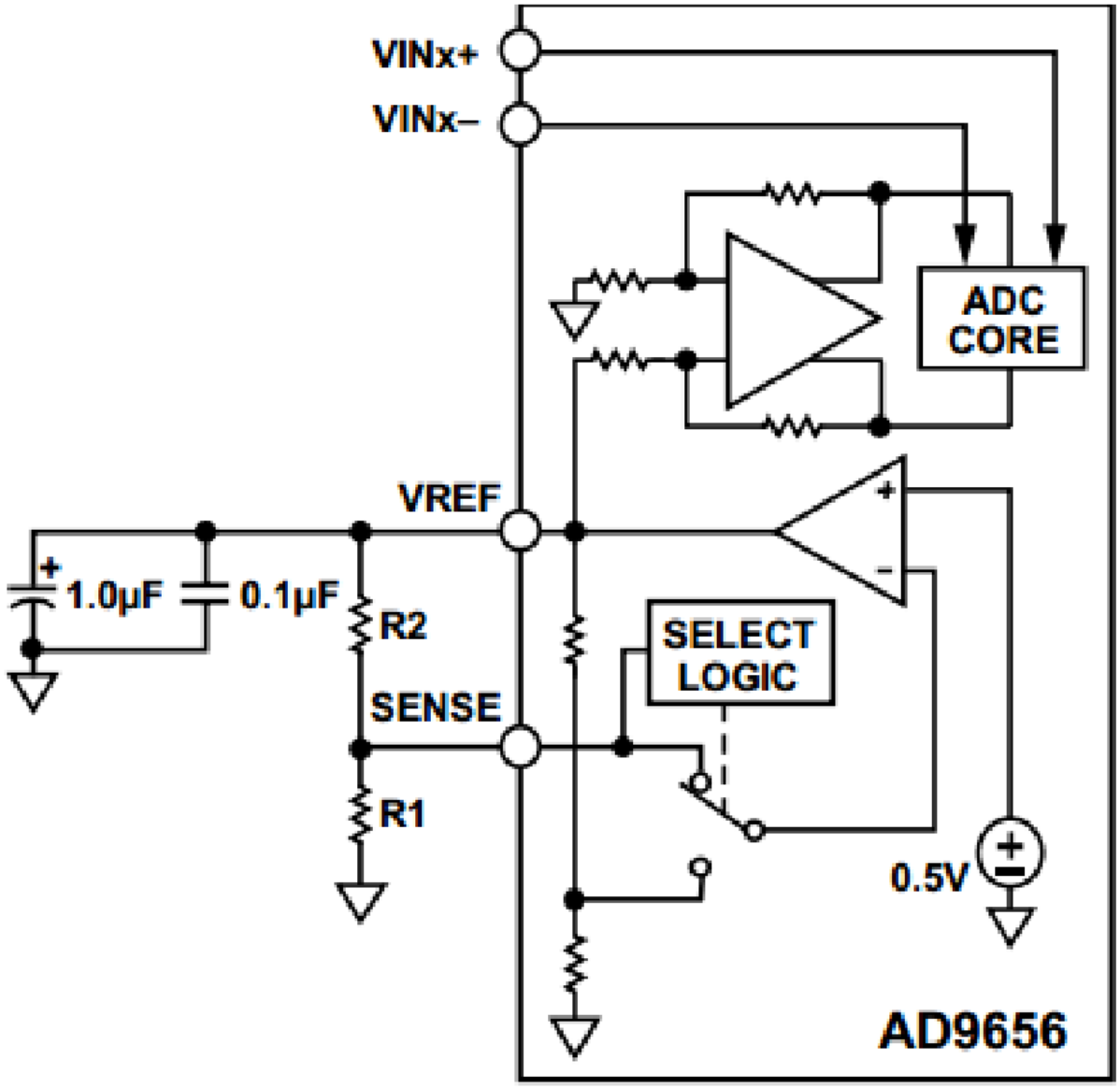


Figure 31: Reference voltage configuration 2

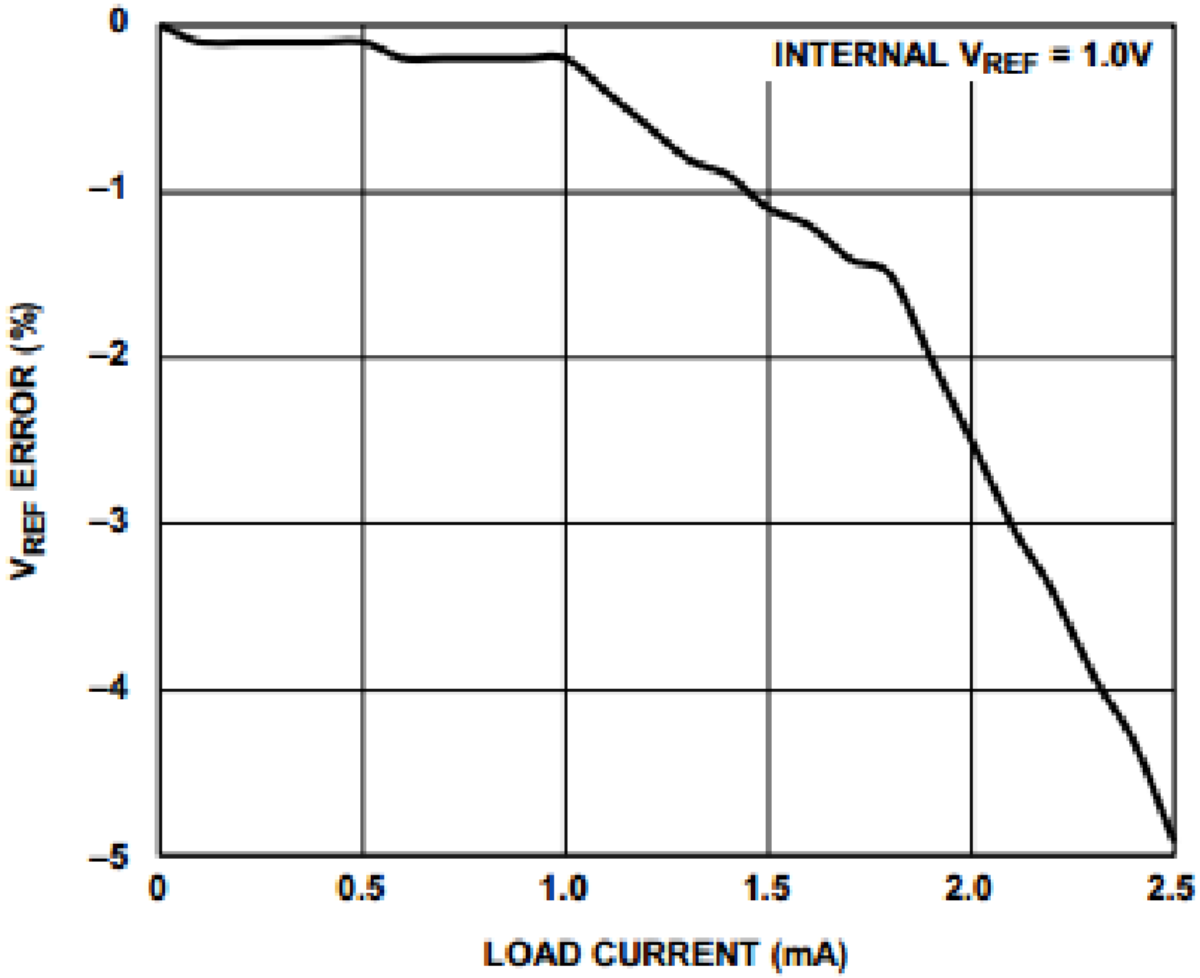


Figure 32: VREF error (internal VREF = 1.0 V) vs. load current

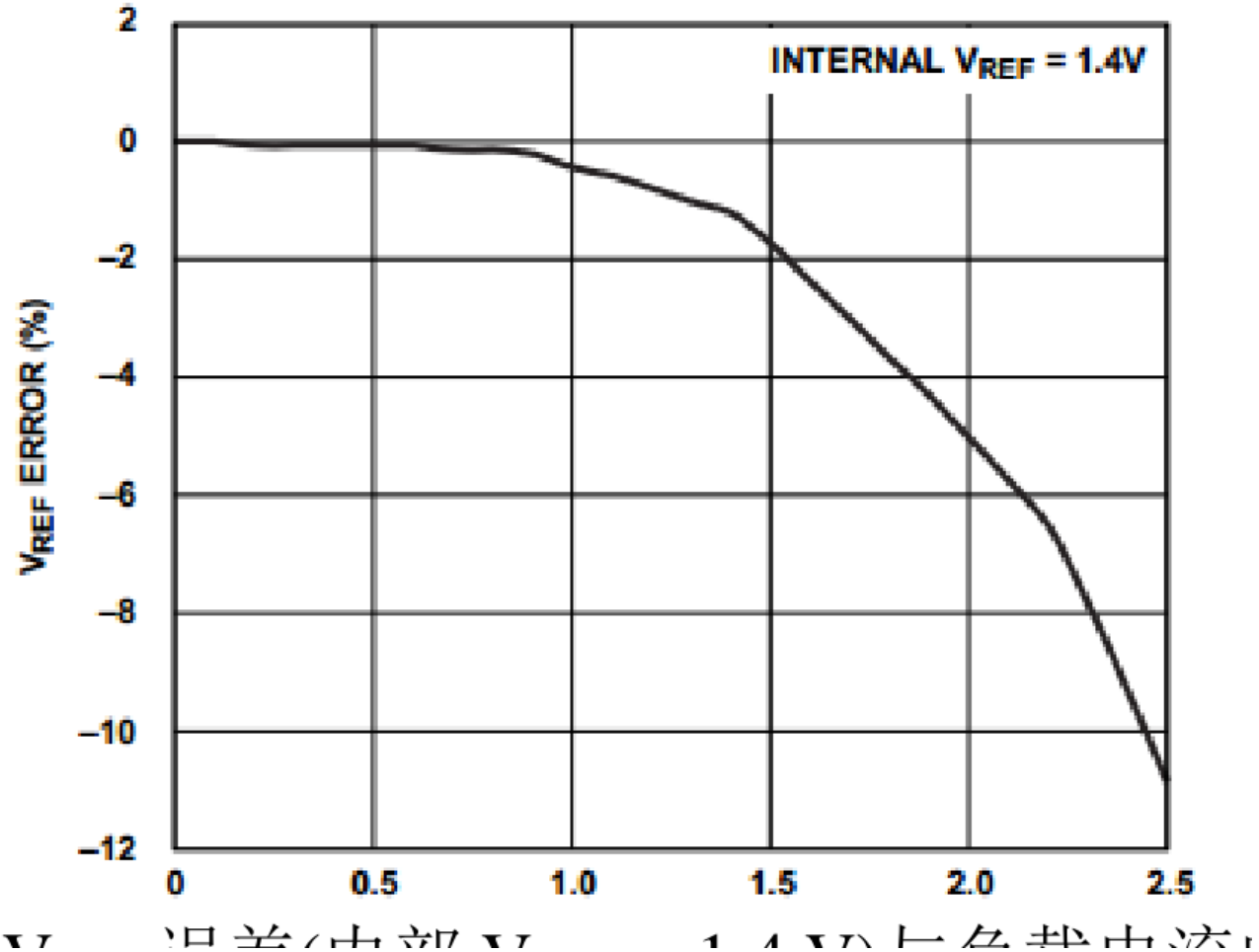


Figure 33: VREF error (internal VREF = 1.4 V) vs. load current

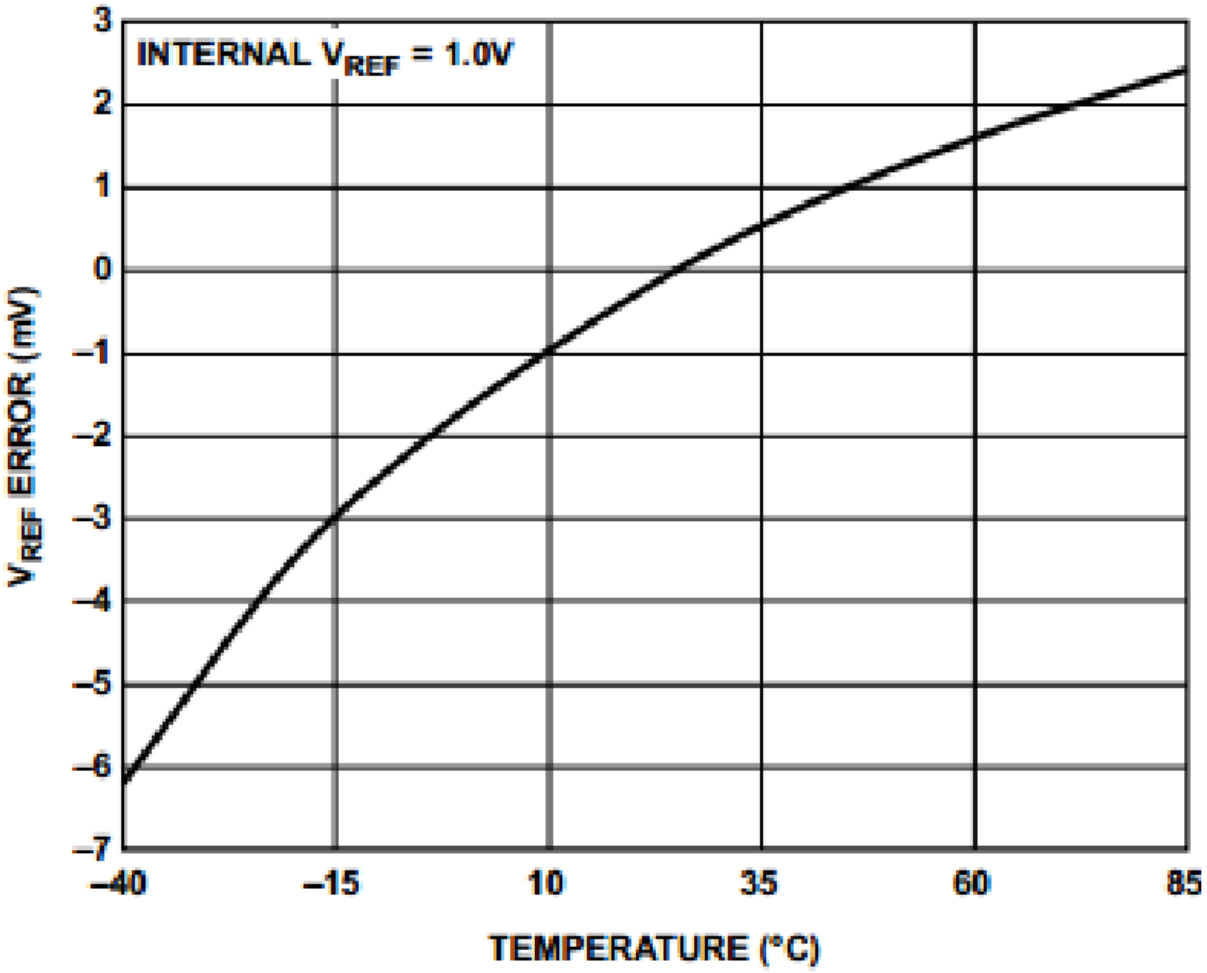


Figure 34: VREF error vs. temperature (VREF = 1.0 V typical drift)

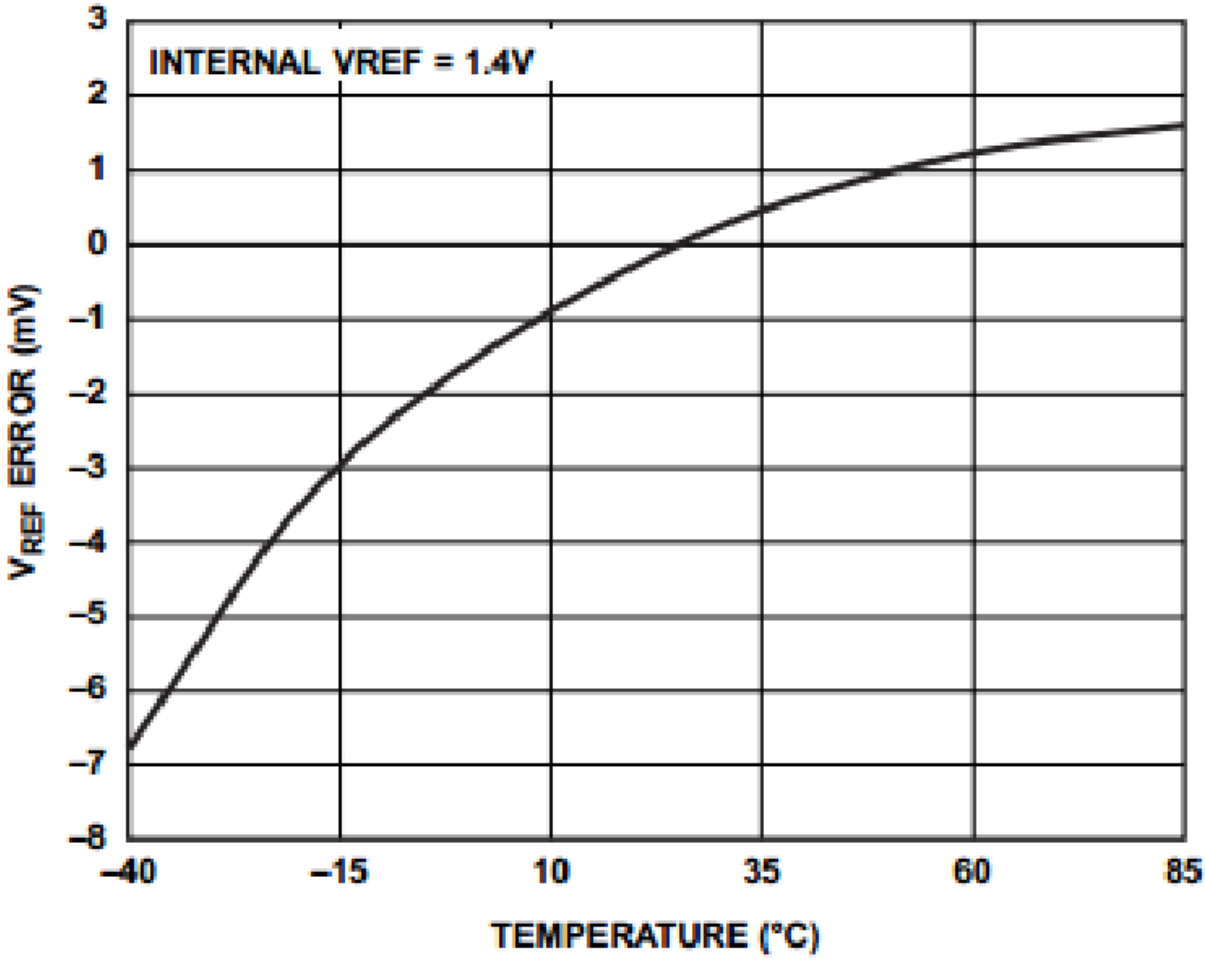


Figure 35: VREF error vs. temperature (VREF = 1.0 V typical drift)

6、时钟输入 / Clock Input

English: To fully exploit the performance of the chip, a differential signal should be used as the clock signal at the sampling clock inputs (CLK+ and CLK−) of this product. This signal is normally AC-coupled to the CLK+ and CLK− pins through a transformer or capacitors. These two pins are internally biased and require no external bias.

This product has a flexible clock input structure. CMOS, LVDS, LVPECL, or sine-wave signals can all serve as its clock input. Whichever signal is used, clock source jitter must be considered (see the jitter considerations section). Figure 36 and Figure 37 show two preferred methods of providing the clock signal to this product (clock rates up to 1 GHz before the internal clock divider). Using an RF transformer or RF balun, a single-ended low-jitter clock source can be converted into a differential signal. For clock frequencies of 125 MHz to 1 GHz, the RF balun configuration is recommended; for clock frequencies of 40 MHz to 200 MHz, the RF transformer configuration is recommended. Schottky diodes placed across the secondary winding of the transformer/balun can limit the clock signal into this product to approximately 0.8 V peak-to-peak differential.

This both prevents the large voltage swing of the clock from feeding through to other parts of this product and preserves the fast rise and fall times of the signal, which is very important for achieving low-jitter

performance. However, above 500 MHz, diode capacitance has an effect. The appropriate signal-clamping diodes must be selected carefully.

If no low-jitter clock source is available, another method is to AC-couple a differential PECL signal to the sampling clock input pins (as shown in Figure 38).

Another method is to AC-couple a differential LVDS signal to the sampling clock input pins (as shown in Figure 39).

中文： 为了充分发挥芯片的性能，应利用一个差分信号作为本产品采样时钟输入端（CLK+ 和 CLK−）的时钟信号。该信号通常使用变压器或电容器交流耦合到 CLK+ 和 CLK− 引脚内。这两个引脚有内部偏置，无需外部偏置。

本产品具有灵活的时钟输入结构。CMOS、LVDS、LVPECL 或正弦波信号均可作为其时钟输入信号。无论采用哪种信号，都必须考虑到时钟源抖动（见抖动考虑部分说明）。图 36 和图 37 显示两种为本产品提供时钟信号的首选方法（内部时钟分频前的时钟速率可达 1 GHz）。利用射频变压器或射频巴伦，可将低抖动时钟源的单端信号转换成差分信号。对于 125 MHz 至 1 GHz 的时钟频率，建议采用射频巴伦配置；对于 40 MHz 至 200 MHz 的时钟频率，建议采用射频变压器配置。跨接在变压器/巴伦次级绕组上的肖特基二极管可以将输入到本产品中的时钟信号限制为约差分 0.8V 峰峰值。

这样，既可以防止时钟的大电压摆幅馈通至本产品的其它部分，还可以保留信号的快速上升和下降时间，这一点对实现低抖动性能来说非常重要。但是，当频率高于 500 MHz 时，二极管电容会产生影响。必须小心选择适当的信号限幅二极管。

如果没有低抖动的时钟源，那么，另一种方法是对差分 PECL 信号进行交流耦合，并传输至采样时钟输入引脚（如图 38 所示）。

另一种方法是将差分 LVDS 信号交流耦合至采样时钟输入引脚（如图 39 所示）。

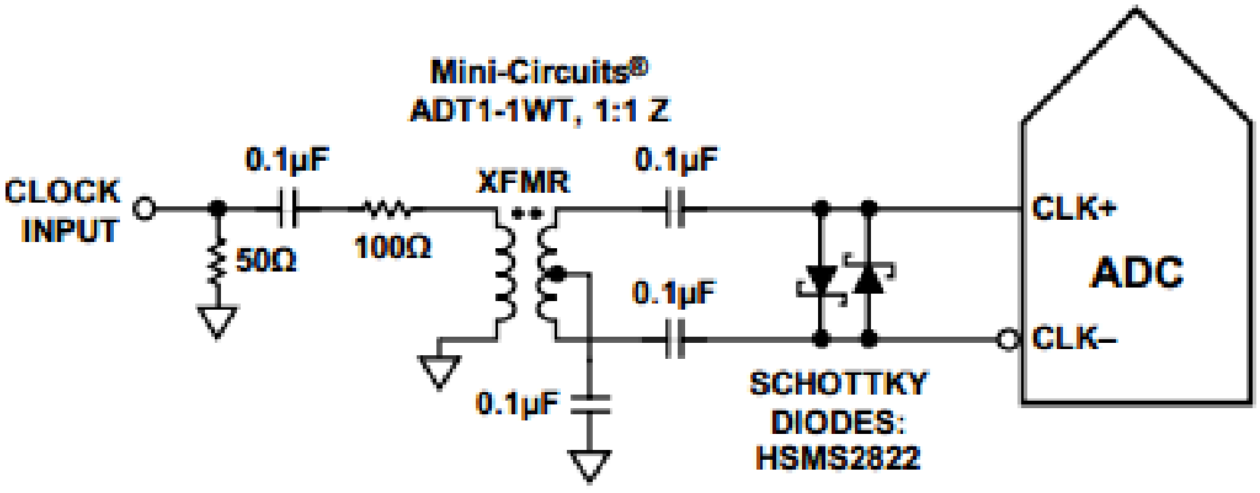


Figure 36: Transformer-coupled differential clock (frequencies up to 200 MHz)

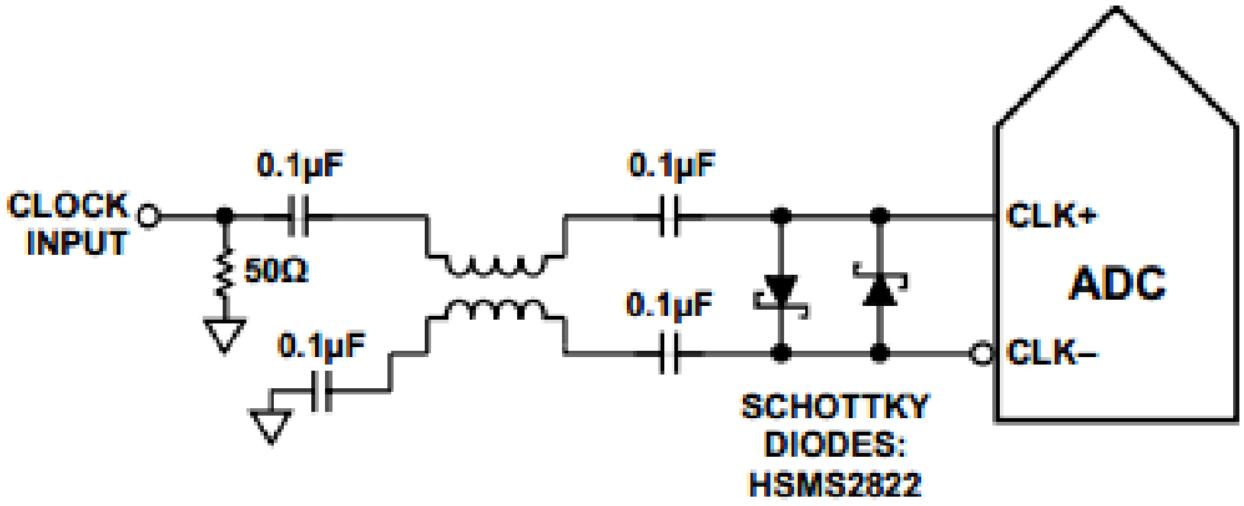


Figure 37: Balun-coupled differential clock (frequencies up to 1 GHz)

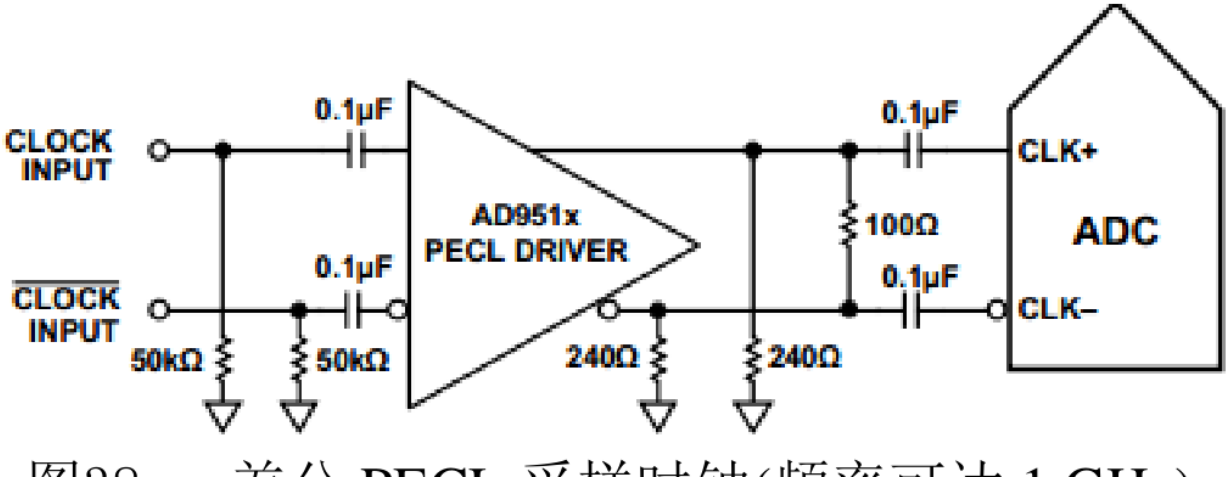


Figure 38: Differential PECL sampling clock (frequencies up to 1 GHz)

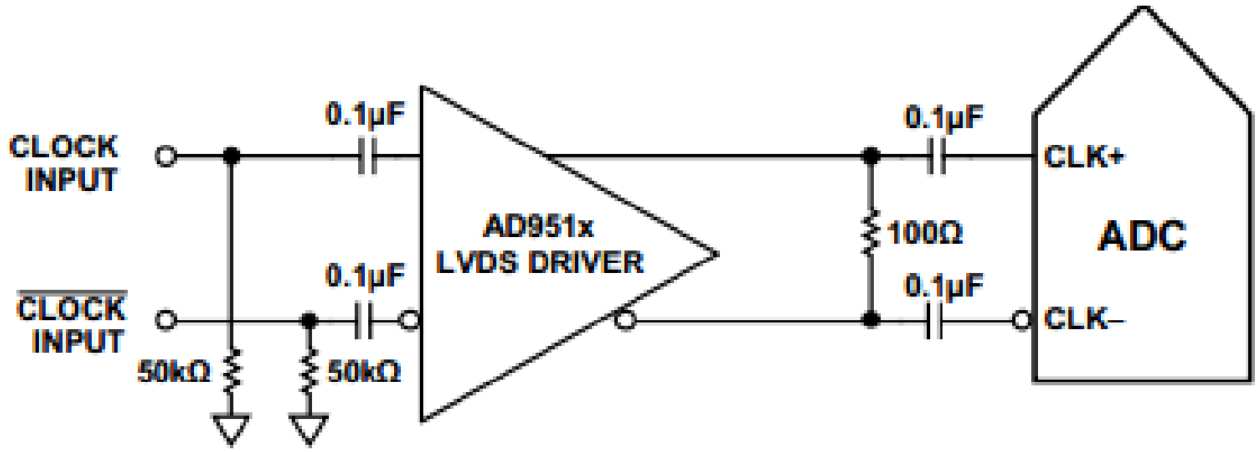


Figure 39: Single-ended 1.8 V CMOS input clock (frequencies up to 200 MHz)

7、占空比 / Duty Cycle

English: Typical high-speed ADCs use both clock edges to generate different internal timing signals and are therefore very sensitive to clock duty cycle. Generally, to maintain the dynamic performance of the ADC, the clock duty-cycle tolerance should be ±5%.

This product integrates a duty-cycle stabilizer (DCS), which re-times the non-sampling edge (falling edge) and provides an internal clock signal with a nominal duty cycle of 50%. When the clock input duty cycle deviates from the nominal 50% by more than ±5%, this feature minimizes the resulting performance degradation. Enabling the DCS function significantly improves noise and distortion performance for clock input duty cycles of 30% to 45% and 55% to 70%.

Jitter on the input rising edge remains a concern and cannot be easily reduced by internal stabilization circuitry. In applications where the clock rate changes dynamically, the time constant associated with this loop must be considered. A wait of 1.5 µs to 5 µs is required before the DCS loop relocks to the input signal.

中文： 典型的高速 ADC 利用两个时钟边沿产生不同的内部定时信号，因此，它对时钟占空比非常敏感。通常，为保持 ADC 的动态性能，时钟占空比容差应为 ±5%。

本产品内置一个占空比稳定器（DCS），可对非采样边沿（下降沿）进行重新定时，并提供标称占空比为 50% 的内部时钟信号。当时钟输入占空比偏离标称 50% 占空比的幅度大于 ±5% 额定值时，该特性可最大程度减少性能的下降。使能 DCS 功能可显著改善 30% 至 45% 和 55% 至 70% 的时钟输入占空比的噪声和失真性能。

输入上升沿的抖动依然值得关注，且无法借助内部稳定电路来轻易减少这种抖动。在时钟速率动态改变的应用中，必须考虑与该环路相关的时间常量。在 DCS 环路重新锁定输入信号前，都需要等待 1.5 µs 至 5 µs 的时间。

8、抖动考虑 / Jitter Considerations

English: High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. IF undersampling applications are especially sensitive to jitter (see Figure 40).

When aperture jitter may affect the dynamic range of this product, the clock input signal should be treated as an analog signal. Separate the clock driver supply from the ADC output driver supply to avoid mixing digital noise into the clock signal. A low-jitter crystal-controlled oscillator provides the best clock source. If the clock signal comes from another type of clock source (through gating, division, or other methods), it needs to be re-timed with the original clock in the final step.

中文： 高速、高分辨率 ADC 对时钟输入信号的质量非常敏感。中频欠采样应用对抖动尤其敏感（见图 40）。

当孔径抖动可能影响本产品的动态范围时，应将时钟输入信号视为模拟信号。将时钟驱动器电源与 ADC 输出驱动器电源分离，以免在时钟信号内混入数字噪声。低抖动的晶体控制振荡器可提供最佳时钟源。如果时钟信号来自其它类型的时钟源（通过门控、分频或其它方法），则需要在最后一步中利用原始时钟进行重定时。

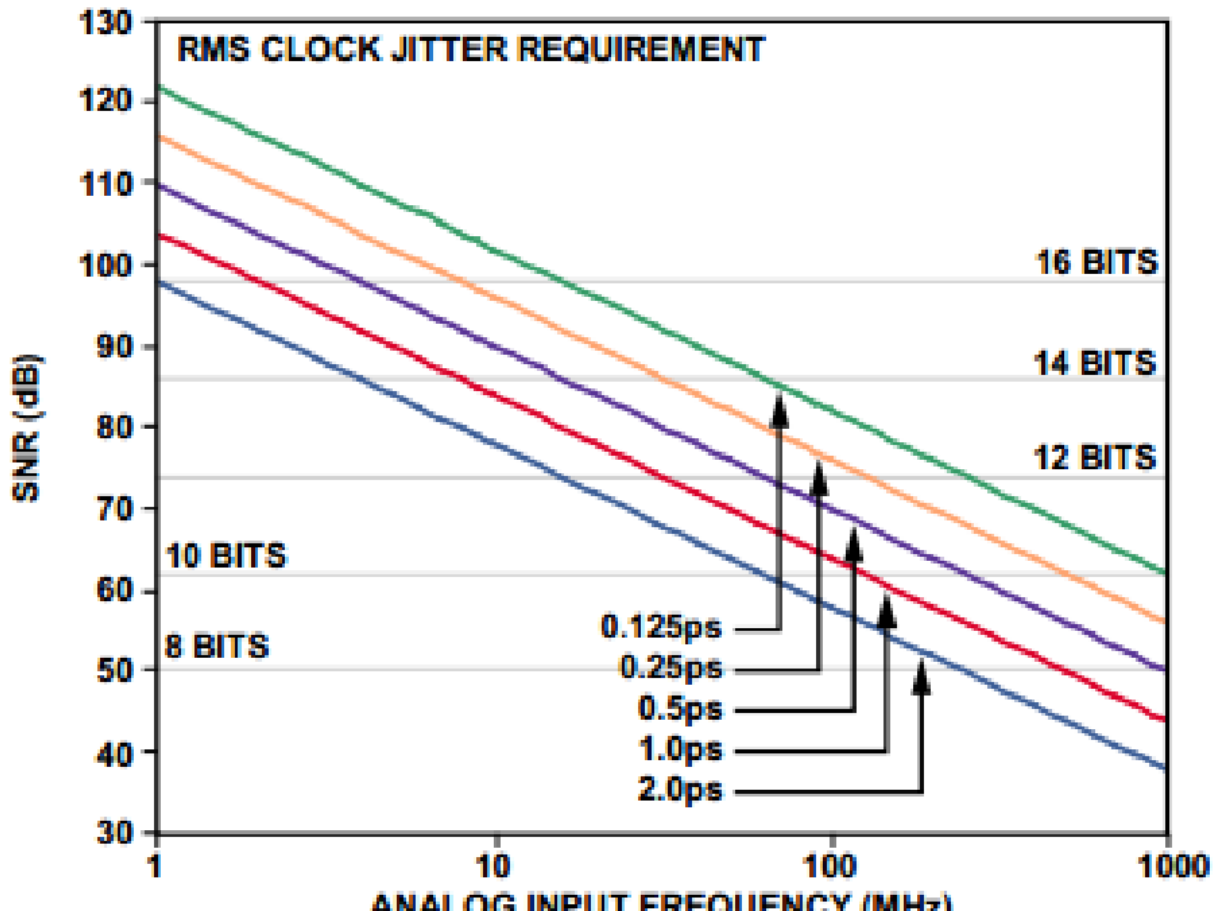


Figure 40: Ideal SNR vs. analog input frequency and jitter

9、功耗和省电模式 / Power Consumption and Power-Saving Modes

English: As shown in Figure 41 and Figure 42, the power consumption of this product is proportional to its sampling rate. Through the SPI port, or by setting the PDWN pin high, this product can be placed in power-saving mode. In power-saving mode, the typical power consumption of the ADC is 50 mW. In power-saving mode, the output drivers are in a high-impedance state. When the PDWN pin is set low, this product returns to normal operating mode. Note that PDWN is referenced to the data output driver supply voltage (DRVDD) and must not exceed that supply voltage.

In power-saving mode, low power consumption is achieved by shutting down the reference source, reference buffer, bias network, and clock. When entering power-saving mode, the internal capacitors discharge; when returning to normal operating mode, the internal capacitors must be recharged. Therefore, the wake-up time is related to the time spent in power-saving mode; the shorter the time in power-saving mode, the shorter the corresponding wake-up time. Using the SPI port interface, the user can place the ADC in power-saving mode or standby mode. If a shorter wake-up time is needed, standby mode can be used, in which the internal reference circuitry remains powered. For more information on using these functions, see the "Memory Map" section.

中文： 如图 41 和图 42 所示，本产品的功耗与其采样速率成比例关系。通过 SPI 端口或将 PDWN 引脚置位高电平，可使本产品进入省电模式。在省电模式下，ADC 的典型功耗为 50mW。省电模式下，输出驱动器处于高阻抗状态。将 PDWN 引脚置位低电平时，本产品返回正常工作模式。注意，PDWN 以数据输出驱动器电源电压（DRVDD）为基准，且不得高于该电源电压。

在省电模式下，通过关闭基准电压源、基准电压缓冲器、偏置网络以及时钟，可实现低功耗。进入省电模式时，内部电容放电；返回正常工作模式时，内部电容必须重新充电。因此，唤醒时间与处于省电模式的时间有关；处于省电模式的时间越短，则相应的唤醒时间越短。使用 SPI 端口接口时，用户可将 ADC 置于省电模式或待机模式。如需较短的唤醒时间，可以使用待机模式，该模式下内部基准电压电路处于通电状态。有关使用这些功能的更多信息，请参见"存储器映射"部分。

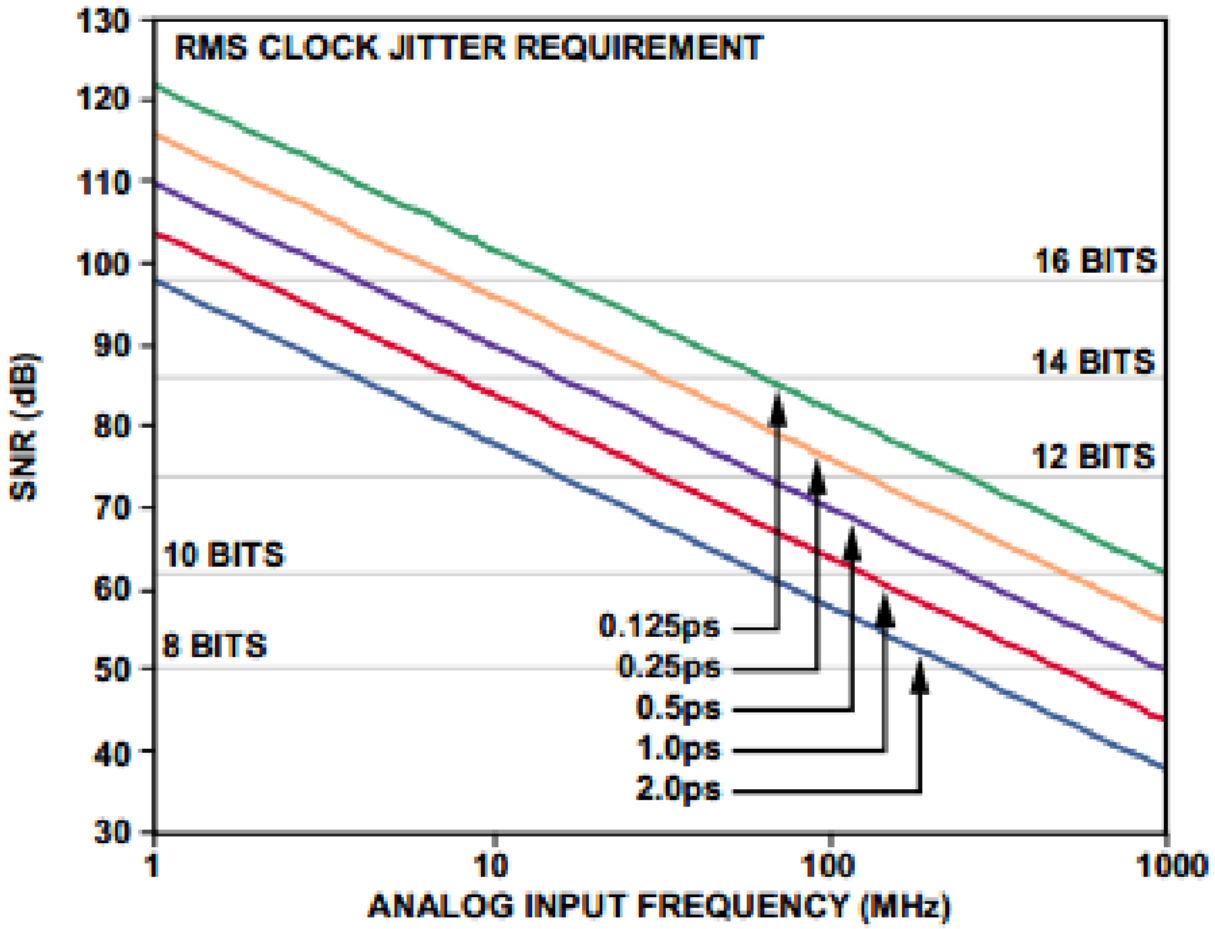


Figure 41: Total power consumption vs. fSAMPLE (fIN = 9.7 MHz, 4 channels, VREF = 1.4 V)

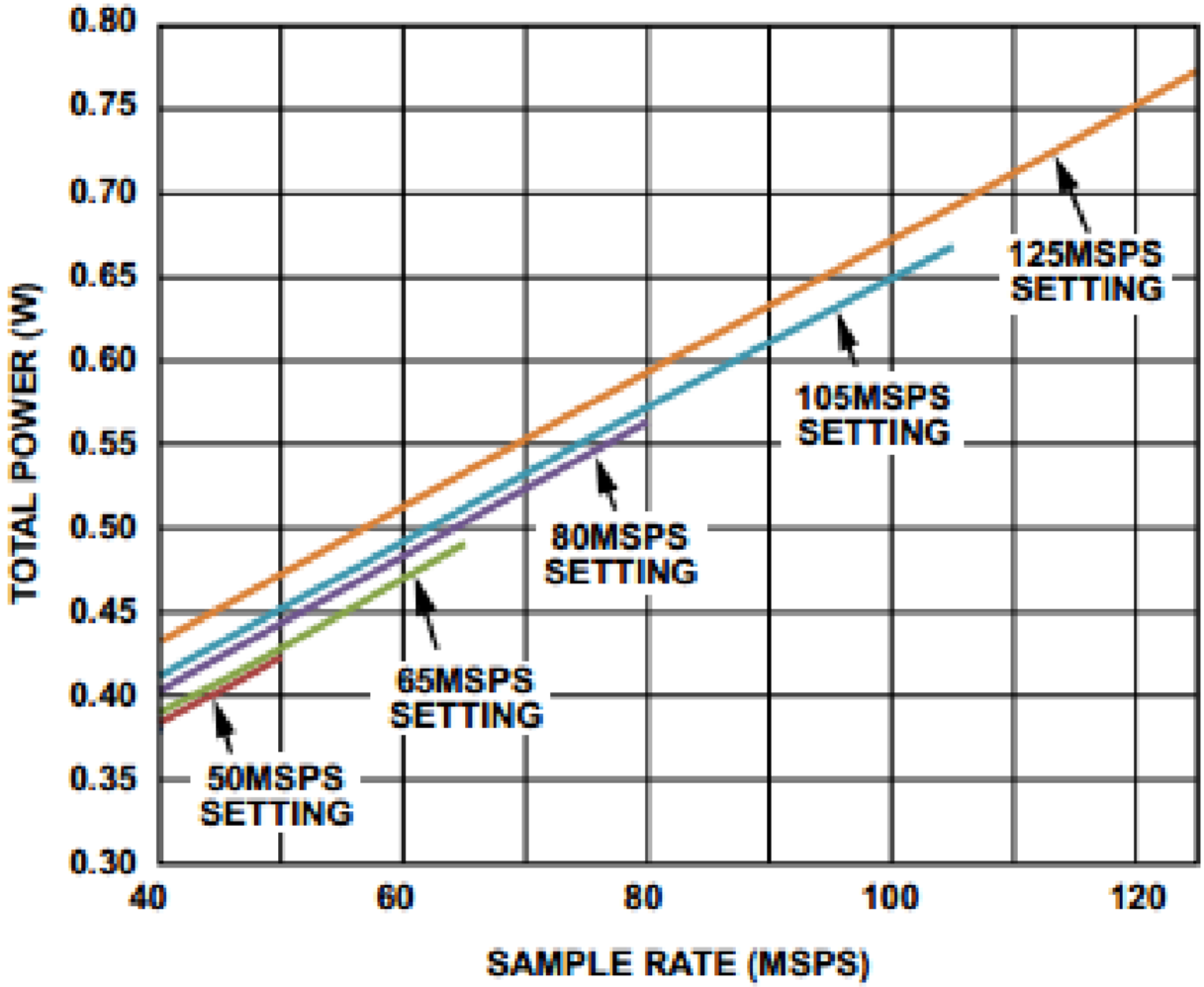


Figure 42: Total power consumption vs. fSAMPLE (fIN = 9.7 MHz, 4 channels, VREF = 1.0 V)

10、JESD204B 输出 / JESD204B Output

English: The digital output of this product adopts the JEDEC standard (standard number: JESD204B, serial interface for data converters). JESD204B is the protocol by which this product connects to digital processing equipment through a serial interface (link speed up to 6.4 Gbps). The advantages of the JESD204B interface include less board space required for data interface routing, and smaller packages for the converter and logic devices.

Table 1 gives the typical configurations of the 204B output of this product.

中文： 本产品数字输出采用 JEDEC 标准（标准号：JESD204B，数据转换器串行接口）。JESD204B 是本产品通过串行接口（最高 6.4 Gbps 链路速度）连接数字处理设备的协议。JESD204B 接口的优势包括：数据接口路由所需电路板空间更少，以及转换器和逻辑器件的封装更小。

表 1 给出了本产品 204B 输出的典型配置情况。

表 1 / Table 1: JESD204B 快速配置 / Quick configuration

配置值 / Configuration value	M	L	F	S	HD
0x44	4	4	2	1	0
0x22	2	2	2	1	0
0x11	1	1	2	1	0

11、多芯片同步 / Multi-Chip Synchronization

English: This circuit does not currently have a multi-chip synchronization function.

中文： 本电路暂不具备多芯片同步功能。

寄存器 / Registers

1、读取存储器映射寄存器表 / Reading the Memory-Mapped Register Table

English: The SPI of this product is four-wire controlled; the SPI timing control diagram is shown in Figure 2.

中文： 本产品 SPI 为四线控制，SPI 的时序控制图如图 2 所示。

2、寄存器地址 / Register Addresses

English: Table 2 gives the register address list of this product. After power-up, please first complete the register reset operation.

中文： 表 2 给出了本产品的寄存器地址列表。上电后，请先完成寄存器复位操作。

表 2 / Table 2: 存储器映射表 / Memory map

地址（十六进制）/ Address (hex)	寄存器名称 / Register Name	位定义（位7 MSB → 位0 LSB）/ Bit Definitions (bit 7 MSB → bit 0 LSB)	默认值（十六进制）/ Default (hex)	注释 / Notes
0x00	软复位 / Soft reset	位7：软复位；位6~位2：禁用/保留；位0：软复位 / Bit 7: soft reset; bits 6–1: disabled/reserved as in original; bit 0: soft reset	18	
0x08	功耗模式 / Power mode	位7、位6：禁用；位5：PDWN 引脚功能：0 = 完全掉电，1 = 待机；位4、位3：保留；位2~位0（原文功耗模式字段）：00 = 正常工作，01 = 完全掉电，10 = 待机，11 = 数字复位 / Bits 7,6: disabled; bit 5: PDWN pin function: 0 = full power-down, 1 = standby; bits 4,3: reserved; power mode field: 00 = normal operation, 01 = full power-down, 10 = standby, 11 = digital reset	0x00	
0x0B	时钟分频器 / Clock divider	位7~位3：禁用；位2~位0：时钟分频比 [2:0]：000 = 1 分频，001 = 2 分频，010 = 3 分频，011 = 4 分频，100 = 5 分频，101 = 6 分频，110 = 7 分频，111 = 8 分频 / Bits 7–3: disabled; bits 2–0: clock divide ratio [2:0]: 000 = ÷1, 001 = ÷2, 010 = ÷3, 011 = ÷4, 100 = ÷5, 101 = ÷6, 110 = ÷7, 111 = ÷8	0x00	
0x0D				

地址（十六进制）/ Address (hex)	寄存器名称 / Register Name	位定义（位7 MSB → 位0 LSB）/ Bit Definitions (bit 7 MSB → bit 0 LSB)	默认值（十六进制）/ Default (hex)	注释 / Notes
	测试模式 / Test mode	位7~位6：00 = 单一，01 = 交替；位5：复位 PN 长序列发生器；位4：复位 PN 短序列发生器；位3~位0：0000 = 关，0001 = 中间电平短，0010 = 正满量程，0011 = 负满量程，0100 = 交替棋盘，0101 = PN23，0110 = PN9，0111 = 1/0 字反转，1000 = 用户输入，1001 = 1/0 位反转，1010 = 1X 电平，1011 = 1 高电平，1100 = 混合位频率 / Bits 7–6: 00 = single, 01 = alternating; bit 5: reset PN long-sequence generator; bit 4: reset PN short-sequence generator; bits 3–0: test pattern select as listed in the original		
0x28	参考电压 / Reference voltage	位7~位6：参考电压 VREF：00 = 1.0 V，01 = 1.2 V，10 = 1.3 V，11 = 1.4 V；位5~位3：禁用；位2~位0：差分幅值：000 = 50%，001 = 57%，010 = 67%，011 = 80%，100 = 100%（默认）/ Bits 7–6: VREF select: 00 = 1.0 V, 01 = 1.2 V, 10 = 1.3 V, 11 = 1.4 V; bits 5–3: disabled; bits 2–0: differential amplitude: 000 = 50%, 001 = 57%, 010 = 67%, 011 = 80%, 100 = 100% (default)	0x04	
0x55	JESD204B 快速配置 / JESD204B quick configuration	0x44 = 4 个 ADC，4 条 lane；0x22 = 2 个 ADC，2 条 lane；0x11 = 1 个 ADC，1 条 lane / 0x44 = 4 ADCs, 4 lanes; 0x22 = 2 ADCs, 2 lanes; 0x11 = 1 ADC, 1 lane	0x44	
0x5E	JESD204B 物理层测试 / JESD204B physical-layer test	位7：PRSB 使能；位6~位5：PRBS 模式：00 = PRBS7，01 = PRBS15，10 = PRBS31；位4~位3（原文 PRBS 输出 lane 字段）：00 = lane0 输出，01 = lane1 输出，10 = lane2 输出，11 = lane3 输出 / Bit 7: PRBS enable; bits 6–5: PRBS mode: 00 = PRBS7, 01 = PRBS15, 10 = PRBS31; PRBS output lane field: 00 = lane 0 output, 01 = lane 1 output, 10 = lane 2 output, 11 = lane 3 output	0x00	
0x60	JESD204B 物理层交叉输出 / JESD204B physical-layer cross output	物理层 lane3：00 = 协议层 lane0，01 = 协议层 lane1，10 = 协议层 lane2，11 = 协议层 lane3；物理层 lane2：同上映射；物理层 lane1：同上映射；物理层 lane0：同上映射 / Physical lane 3/2/1/0 source select: 00 = protocol lane 0, 01 = protocol lane 1, 10 = protocol lane 2, 11 = protocol lane 3	0xE4	
0x80	JESD204B 物理层使能 / JESD204B physical-layer enable	物理层 lane3：0 = 使能，1 = 不使能；物理层 lane2：0 = 使能，1 = 不使能；物理层 lane1：0 = 使能，1 = 不使能；物理层 lane0：0 = 使能，1 = 不使能 / Physical lane 3/2/1/0: 0 = enabled, 1 = disabled	0x00	
0x106	比较器阈值算法 / Comparator threshold algorithm	保留；00 = 关闭，01 = 打开第 1 级，11 = 打开第 1/2 级 / Reserved; 00 = off, 01 = stage 1 on, 11 = stages 1/2 on	0x00	上电后 SPI 配置为 0x03 / Configure SPI to 0x03 after power-up
0x125	算法配置 / Algorithm configuration	保留；0 = 奇数区域，1 = 偶数区域；保留 / Reserved; 0 = odd region, 1 = even region; reserved	0xE4	

3、寄存器地址说明 / Register Address Notes

English: Affected by process or ambient temperature variations, the comparator thresholds may fluctuate; it is recommended to enable the comparator threshold correction function when in use.

The SPI pseudo-code sequence is as follows:

```
SPI_Write (0x106, 0x03);
```

中文： 受工艺或环境温度变化等影响，比较器阈值会出现波动，建议使用时打开比较器阈值矫正功能。

SPI 伪代码序列如下所示：

```
SPI_Write (0x106, 0x03);
```

电源地间保护 / Power-to-Ground Protection

English: To improve the antistatic capability of the device, the following ESD protection circuits exist between the power pins inside the device. The forward conduction voltage drop of each ESD protection device is approximately 0.35 V. During power-up and normal use, avoid these ESD protection devices conducting in the forward direction for extended periods.

中文： 为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.35V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。

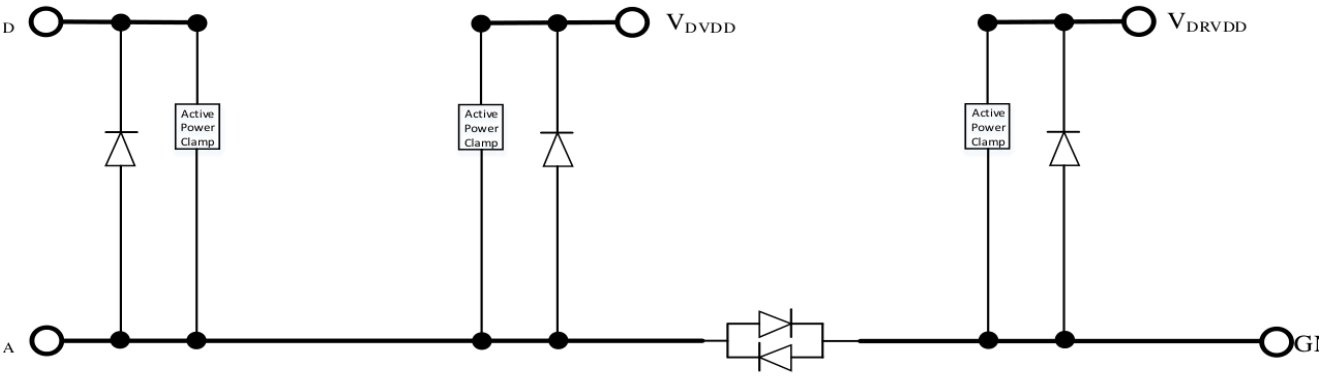


Figure 43: ESD protection circuits between internal power supplies

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注意事项 / Precautions

1、产品安装注意事项 / Product Installation Notes

English: 1) Pay attention to the device orientation when soldering to avoid soldering it incorrectly. 2) Instruments and meters used for circuit debugging must have good common grounding. PCB design must maintain good grounding and power-supply decoupling. 3) Take care not to reverse the power supply or short the input/output terminals to the power supply, which can easily cause circuit damage.

中文： 1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2、产品使用注意事项 / Product Usage Notes

English: 1) Differential inputs should be as close together and as parallel as possible. 2) Input traces should be as short as possible to minimize parasitic capacitance and noise introduction. 3) For better heat dissipation and better electrical performance, the bottom plate of the chip should be soldered to a large ground terminal on the PCB, thereby maximizing the thermal performance of the package. 4) Importantly, the chip ground should be connected to the PCB ground plane through as many paths and as much area as possible. 5) It is recommended to first reset the circuit after power-up before use.

中文： 1) 差分输入应尽量靠近且相互平行。 2) 输入连线应尽量短以最小化寄生电容和噪声引入。 3) 为了更好的散热并获得更好的电性能，芯片的底板应焊接到 PCB 板的一个大的地端，从而最大限度发挥封装的热性能。 4) 很重要的是，芯片的地应该通过尽量多的渠道和足够多的面积与 PCB 板的地层相连。 5) 推荐上电后首先对电路进行复位，再进行使用。

3、产品防护注意事项 / Product Protection Notes

English: 1) All pins of this circuit are designed with ESD protection structures; however, large-energy electrical pulses may still damage the circuit, so ESD protection should be observed during testing, handling, and storage. 2) Exceeding the absolute maximum ratings may cause permanent damage to the device. These are rating maxima only and do not indicate that the device can operate normally under these conditions or under any other conditions beyond those shown in this product manual. 3) Provided rain and snow do not directly affect them, cartons containing the product can be transported by safe means of transport. However, they must not be stacked together with acidic, alkaline, or other corrosive objects. The packaging should be secure, and existing means of transport can be used. 4) The storage environment for packaged products shall meet the Class I warehouse conditions specified in Q/W 657A, Section 8.1 (temperature: 15°C~25°C, humidity: 25%~65%), with no acidic, alkaline, or other corrosive gases around, good ventilation, and appropriate ESD protection measures.

中文： 1) 该电路所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 2) 超出绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。 3) 在避免雨、雪直接影响的条件下，装有产品的包装箱可以用安全的运输工具运输。但不能和带有酸性、碱性和其它腐蚀性物体堆放在一起。包装应是安全的，可以采用现有的运输工具。 4) 包装好的产品贮存环境应满足 Q/W 657A 第 8.1 规定的 I 类库房条件要求（温度：15°C~25°C，湿度：25%~65%），周围没有酸、碱或其它腐蚀性气体，通风良好，且具备相应防静电措施。

4、电装说明 / Assembly Instructions

English: 1) This product is in a ceramic hermetic package; no baking is required before assembly. 2) When leaded reflow soldering (Sn63Pb37) is used for assembly, the recommended peak temperature range is 210°C~220°C; the maximum peak temperature is recommended not to exceed 235°C; dwell time within ±5°C of the peak temperature ≤20 s; time above the liquidus line 60~90 s; ramp-up rate 2~4°C/s; ramp-down rate 2~6°C/s. 3) If a mixed assembly process requires a higher temperature, ensure that the device body temperature does not exceed 260°C at most; the device body temperature measurement point is located on the top surface of the device during soldering. 4) The soldering termination plating material of this product is Ni/Au, with a gold layer thickness greater than 1.3 μm; before soldering, gold removal treatment shall be performed in accordance with the national aerospace industry standard QJ3267-2006,

Process Technical Requirements for Tin Dipping of Electronic Components. 5) This product has castellated pads on its sides; it is recommended that the solder climb height after soldering be greater than 1/2 of the castellation height. 6) This package structure has a relatively weak stress-relief effect; to ensure the long-term reliability of the device, users are not recommended to use this device in thermally stressful environments with frequent temperature cycling. Users are advised to carry out board-level reliability verification in light of their specific application scenarios before use.

中文： 1) 本产品为陶瓷气密性封装，电装前无烘烤要求； 2) 电装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~220°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 3) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C，器件本体温度测量点位于焊接时器件上表面； 4) 本产品焊接端镀层材料为 Ni/Au，其中镀金层厚度大于 1.3μm，焊接前应按照《国家航天行业标准 QJ3267-2006 电子元器件搪锡工艺技术要求》进行去金处理； 5) 该产品侧面有城堡形焊盘，建议焊接后爬锡高度大于 1/2 城堡高度； 6) 该封装结构应力释放效果较弱，为保证器件的长期可靠性，不推荐用户在高频次温度循环的热应力敏感环境中使用该器件。建议用户使用前结合具体应用场景，开展板级可靠性验证。

5、热阻 / Thermal Resistance

表 3 / Table 3: 封装热阻 / Package thermal resistance

项目 / Item	实测值 / Measured Value	依据标准及方法 / Basis Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)	16.95 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2 natural-convection thermal test environment requirements and methods for integrated circuits
Rthjt（结到器件顶面的热阻）/ Rthjt (junction-to-top thermal resistance)	2.834 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14 dual-interface separation method for one-dimensional heat-transfer paths
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-bottom thermal resistance)	2.545 K/W	JESD51-14 拐点理论器件内部结构分层得到 / JESD51-14, obtained by layering the internal structure of the device per inflection-point theory

常见故障及处理办法 / Common Faults and Troubleshooting

English: 1. No signal output: check whether the supply voltage, input signal, and clock are correctly applied. 2. Device functions abnormally: clarify the device operating mode and confirm that the configuration is correct. 3. Device operates unstably: check the power supply and ensure that the supply voltage is stable.

中文： 1、 无信号输出：检查电源电压、输入信号、时钟是否正确加载。 2、 器件功能不正常：明确器件工作模式，确认配置是否正确。 3、 器件工作不稳定：检查电源，保证电源电压稳定。

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附加说明 / Additional Notes

English: 1. First release date of this manual: July 2026. 2. Product status: ☒ In production (this product model is currently in production; formal products can be provided) / ☐ Pre-release (this product model has not yet entered formal production; samples can be provided). 3. Model suffix difference description (for series products, model suffixes are described as in the following example; add this part when needed). 4. Replacement of imported devices: no cross-reference imported device.

中文： 1. 本说明书首次发布日期：2026 年 7 月。 2. 本产品状态：☒生产（该产品型号目前已在生产，可以提供正式产品）☐预发布（该产品型号尚未投入正式生产，可以提供样品） 3. 型号后缀差异性说明（系列化产品需对型号后缀说明如下示例，需要时增加此部分） 4. 替代进口器件情况说明：无对标进口器件。

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