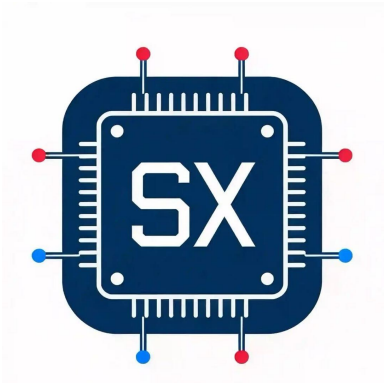


SXA026

16-Bit, Dual-Channel, 310 MSPS A/D Converter

16 位双通道 310MSPS A/D 转换器

16-bit | 2 channels | 310 MSPS | BGA144 | DDR LVDS

16位 | 双通道 | 310MSPS | BGA144 | DDR LVDS

对标 / Cross Reference: AD9652 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXA026 — 16-Bit, Dual-Channel, 310 MSPS A/D Converter

SXA026 | 16-Bit, Dual-Channel, 310 MSPS A/D Converter | 16 位双通道 310MSPS A/D 转换器

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Version / 版本：V1.20261117

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Revision History / 版本修订记录

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20261117	2026.11.17	——	首次发布 / First release	

Product Applications and Scope / 产品用途及应用范围

English: Communications; telecommunications; 3G/4G multimode digital receivers; test equipment; smart antennas.

中文： 通信；通讯；3G/4G 多模数字接收器；测试设备；智能天线。

Standard / 标准

English: Quality grade: Industrial.

中文： 质量等级：工业级。

Features / 产品特点

特性 / Feature	规格 / Specification
分辨率 / Resolution	16 位 / 16-bit
动态性能 / Dynamic Performance	SNR = 74 dBFS @ fIN = 70 MHz (AIN = -1dBFS); SFDR = 85 dBc @ fIN = 70 MHz (AIN = -1dBFS)
IF 采样性能 / IF Sampling Performance	SNR = 72.0 dBFS @ fIN = 170 MHz (AIN = -1dBFS); SFDR = 85 dBFS @ fIN = 170 MHz (AIN = -1dBFS)
全功率带宽 / Full Power Bandwidth	465 MHz
片上缓冲器 / On-Chip Buffer	3.3 V 缓冲器 / 3.3 V buffer
模拟输入 / Analog Input	2 VP-P 到 2.5 VP-P 可编程 / Programmable from 2 VP-P to 2.5 VP-P
输入时钟分频 / Input Clock Division	1、2、4、8 / 1, 2, 4, 8
总功耗 / Total Power Consumption	2.16 W
电源供电 / Power Supplies	3.3 V 和 1.8 V / 3.3 V and 1.8 V
数据输出 / Data Output	DDR LVDS 输出 / DDR LVDS output
控制接口 / Control Interface	SPI 串口控制 / SPI serial control

Product Description / 产品描述

English: The SXA026 is a dual-channel, 16-bit, 310 MSPS ADC that supports high-speed signal processing requirements and provides good dynamic range over a wide input frequency range. The ADC core uses a multistage pipeline architecture and integrates output error calibration logic. A high-performance on-chip buffer and an internal reference voltage source simplify the design. The clock input frequency is up to 1.24 GHz; integer division by 1/2/4/8 generates the sampling clock required by the ADC, and a duty-cycle stabilization function compensates for variations in the ADC clock duty cycle. The 16-bit ADC output uses double data rate (DDR) mode. A 3-wire SPI-compatible serial interface provides programmable configuration and control. The device is housed in a BGA144 ball grid array package and operates over -40°C to +85°C.

中文： 该产品是双通道 16 位 310MSPS ADC，支持高速信号处理需求，该产品在宽输入频率范围内均具有很好的动态范围。该产品的 ADC 核采用多级流水线结构，并集成了输出误差校准逻辑。高性能的片上缓冲器和内部基准电压源简化了设计。该产品时钟输入频率高达 1.24GHz，采用 1/2/4/8 整数分频产生 ADC 所需的采样时钟，具备占空比稳定功能，用来补偿 ADC 时钟占空比的变化。ADC 的 16 位输出采用双倍数据速率（DDR）模式。使用 3 线 SPI 兼容串行接口完成可编程设置和控制。采用 BGA144-球状栅格阵列封装，工作温度范围 -40°C~85°C。

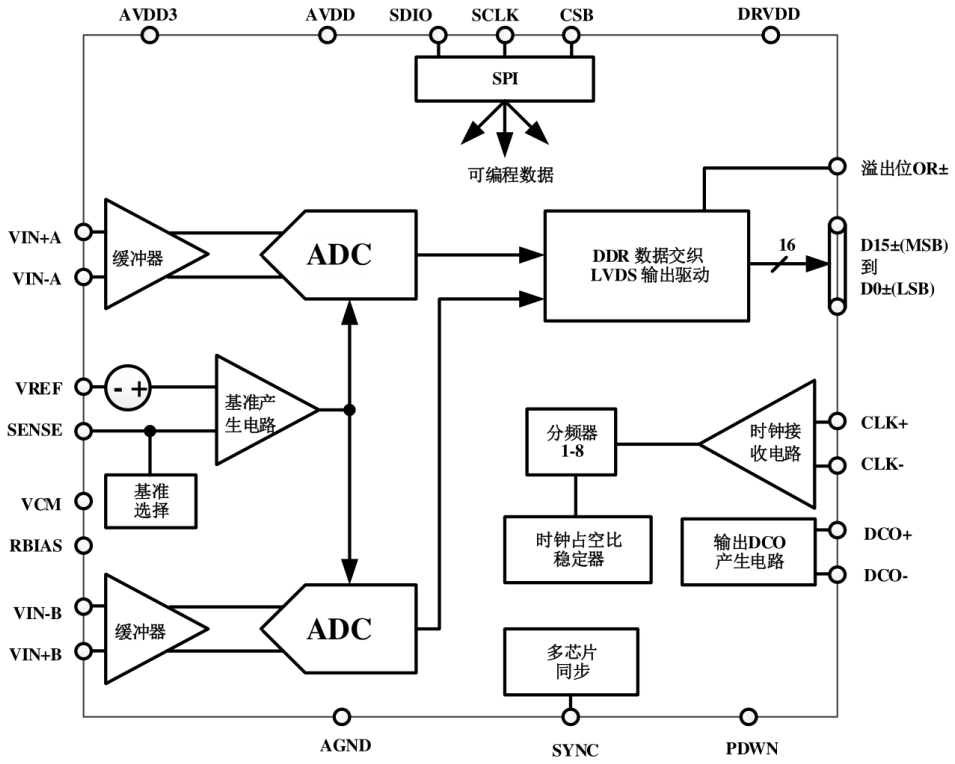


Figure 1: Functional Block Diagram / 图1 功能框图

English: The operating timing of the device is as follows:

中文： 该产品工作时序如下：

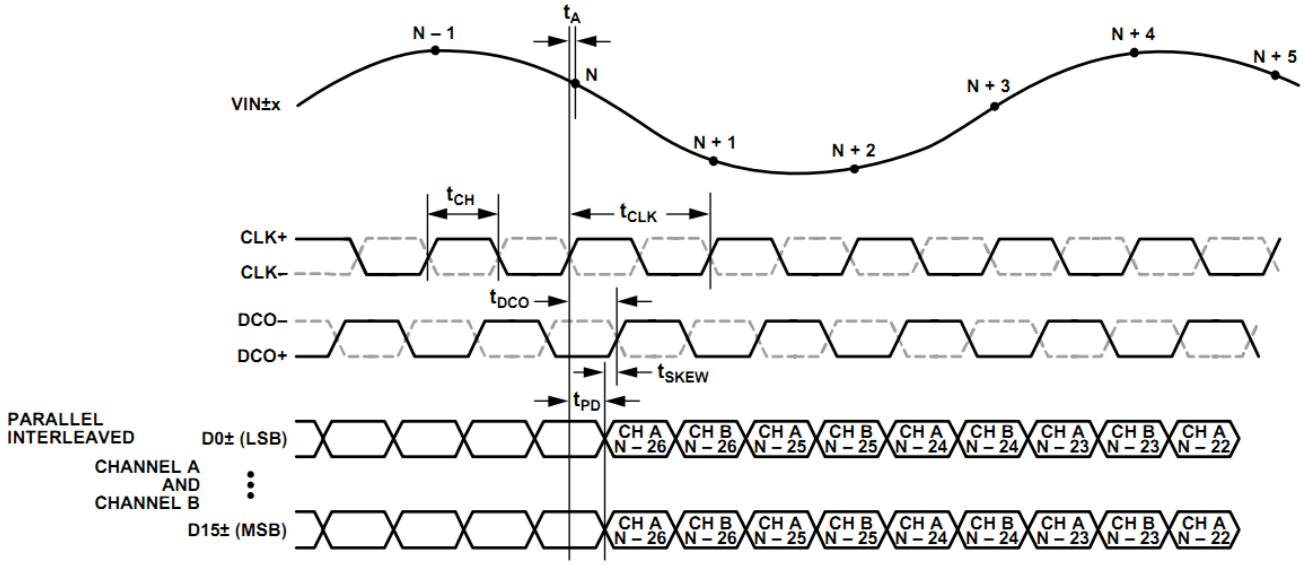


Figure 2: Operating Timing Diagram / 图2 工作时序图

Table 1. Basic Timing / 表1 基本时序参数表

电参数 / Parameter	符号 / Symbol	条件 / Conditions	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
转换速率 / Conversion Rate	SR		80	310	310	MSPS
时钟高电平时间 / Clock High Time	tCH			1.61		ns
孔径延迟 / Aperture Delay	tA			1.0		ns
传输延迟 / Propagation Delay	tPD			290		ps
数据时钟传输延迟 / DCO Propagation Delay	tDCO			290		ps
输出数据偏移 / Output Data Skew	tSKEW		-80	-280	-480	ps
流水线延迟 / Pipeline Latency		设计保证 / Guaranteed by design		26		Cycles

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Package Outline and Dimensions / 产品外形图和尺寸

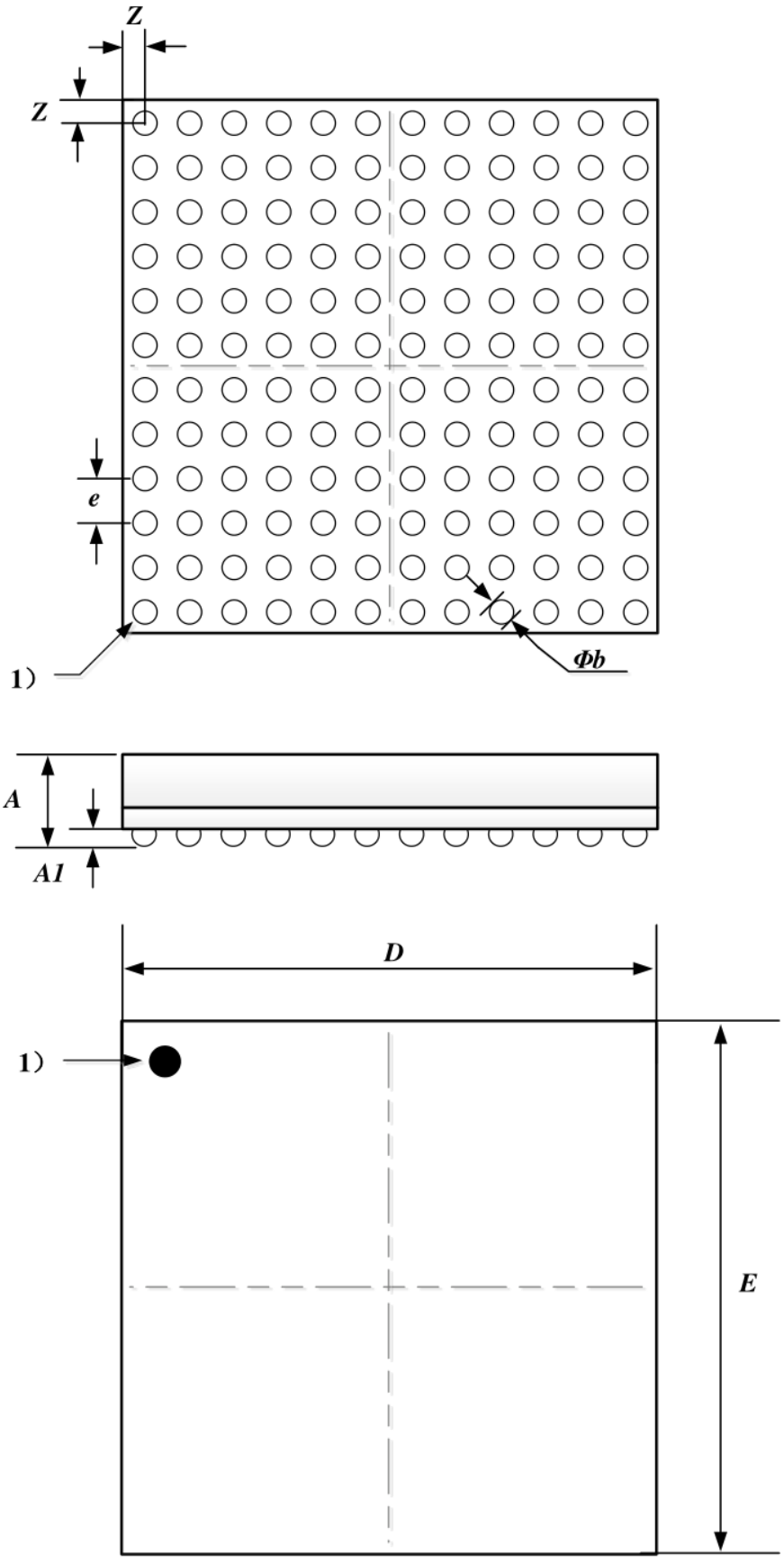


Figure 3: Package Outline / 图3 外形图

English: Unit: millimetres.

中文： 单位为毫米。

尺寸符号 / Symbol	最小 / Min	公称 / Nominal	最大 / Max
A	1.19	1.32	1.40
A1	0.20	0.34	0.45
D		10.0	10.10
E		10.0	10.10
Φb	0.40	0.45	0.50
e		0.80	
Z		0.60	0.65

Pin Configuration / 引出端排列

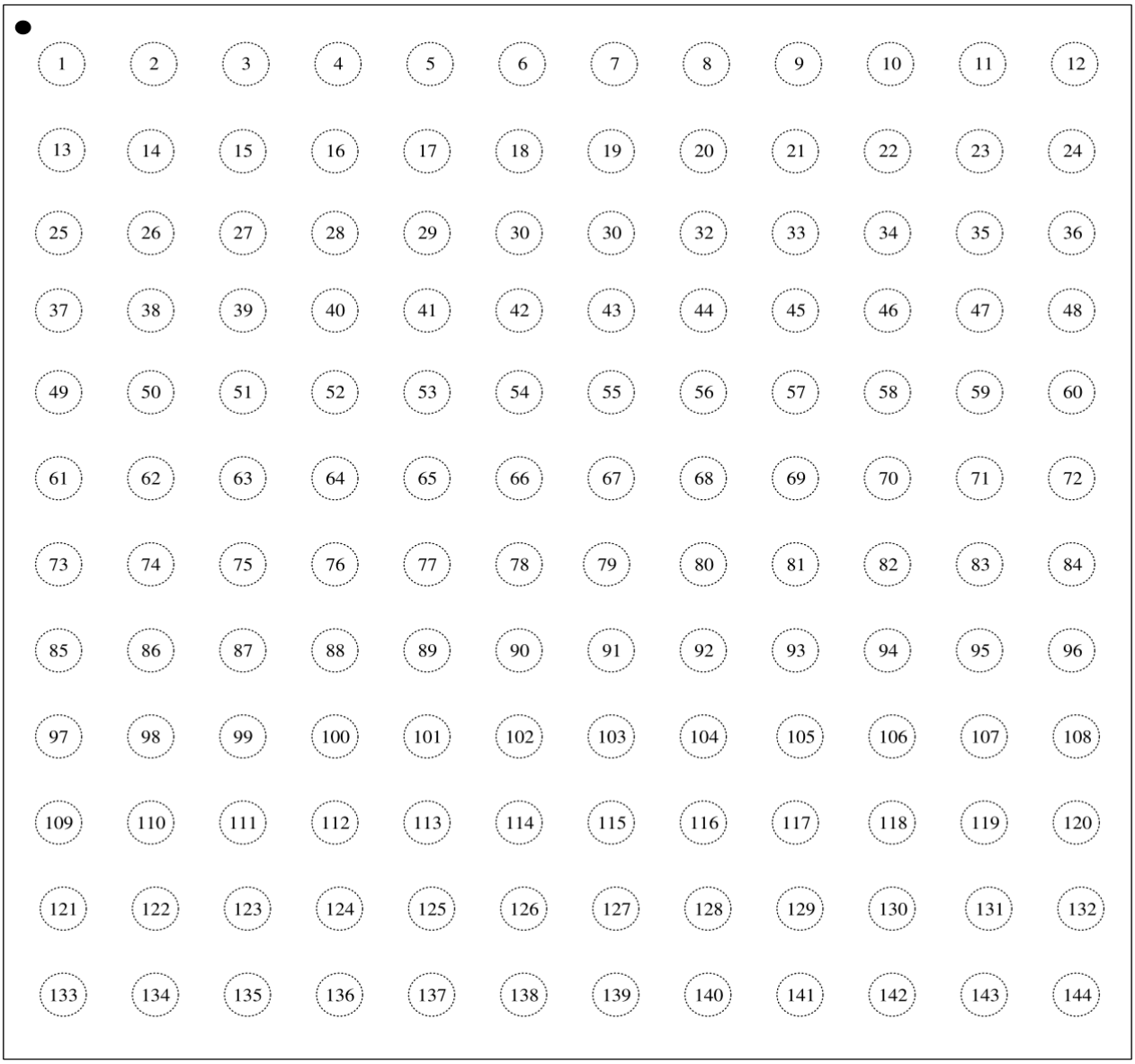


Figure 4: Pin Configuration / 图4 引出端排列

Pin Function Descriptions / 引出端功能符号表

引出端号 / Pin	符号 / Symbol	名称 / Name	Name (EN)
1	RBIAS	外部偏置端	External Bias
2	VCM	模拟输入共模电压	Analog Input Common-Mode Voltage
3	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
4	VIN+B	通道B差分输入正端	Channel B Differential Input Positive
5	VIN-B	通道B差分输入负端	Channel B Differential Input Negative
6	VDDA3	3.3V模拟电源	3.3V Analog Power Supply

引出端号 / Pin	符号 / Symbol	名称 / Name	Name (EN)
7	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
8	VIN-A	通道A差分输入负端	Channel A Differential Input Negative
9	VIN+A	通道A差分输入正端	Channel A Differential Input Positive
10	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
11	SENSE	参考模式选择	Reference Mode Select
12	VREF	参考电压输入/输出	Reference Voltage Input/Output
13	GNDA	模拟地	Analog Ground
14	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
15	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
16	GNDA	模拟地	Analog Ground
17	GNDA	模拟地	Analog Ground
18	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
19	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
20	GNDA	模拟地	Analog Ground
21	GNDA	模拟地	Analog Ground
22	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
23	VDDA3	3.3V模拟电源	3.3V Analog Power Supply
24	GNDA	模拟地	Analog Ground
25	GNDA	模拟地	Analog Ground
26	GNDA	模拟地	Analog Ground
27	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
28	GNDA	模拟地	Analog Ground
29	GNDA	模拟地	Analog Ground
30	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply
31	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply
32	GNDA	模拟地	Analog Ground
33	GNDA	模拟地	Analog Ground
34	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
35	GNDA	模拟地	Analog Ground
36	GNDA	模拟地	Analog Ground
37	CLK-	ADC时钟输入负端	ADC Clock Input Negative
38	GNDA	模拟地	Analog Ground
39	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
40	GNDA	模拟地	Analog Ground
41	GNDA	模拟地	Analog Ground
42	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply

引出端号 / Pin	符号 / Symbol	名称 / Name	Name (EN)
43	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply
44	GNDA	模拟地	Analog Ground
45	GNDA	模拟地	Analog Ground
46	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
47	GNDA	模拟地	Analog Ground
48	CSB	片选信号	Chip Select
49	CLK+	ADC时钟输入正端	ADC Clock Input Positive
50	GNDA	模拟地	Analog Ground
51	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
52	GNDA	模拟地	Analog Ground
53	GNDA	模拟地	Analog Ground
54	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply
55	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply
56	GNDA	模拟地	Analog Ground
57	GNDA	模拟地	Analog Ground
58	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
59	GNDA	模拟地	Analog Ground
60	SDIO	串行数据输入输出	Serial Data Input/Output
61	TEST	接地端（未使用端口）	Ground (Unused Port)
62	GNDA	模拟地	Analog Ground
63	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
64	GNDA	模拟地	Analog Ground
65	GNDA	模拟地	Analog Ground
66	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply
67	VDD_CLK	1.8V时钟电路电源	1.8V Clock Circuit Power Supply
68	GNDA	模拟地	Analog Ground
69	GNDA	模拟地	Analog Ground
70	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
71	GNDA	模拟地	Analog Ground
72	SCLK	串行时钟	Serial Clock
73	SYNC	同步输入端	Sync Input
74	GNDA	模拟地	Analog Ground
75	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
76	GNDA	模拟地	Analog Ground
77	GNDA	模拟地	Analog Ground
78	VDDA1	1.8V模拟电源	1.8V Analog Power Supply

引出端号 / Pin	符号 / Symbol	名称 / Name	Name (EN)
79	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
80	GNDA	模拟地	Analog Ground
81	GNDA	模拟地	Analog Ground
82	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
83	GNDA	模拟地	Analog Ground
84	OR+	通道A/B 溢出位正端	Channel A/B Overflow Bit Positive
85	PDWN	掉电模式	Power-Down Mode
86	GNDA	模拟地	Analog Ground
87	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
88	GNDA	模拟地	Analog Ground
89	GNDA	模拟地	Analog Ground
90	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
91	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
92	GNDA	模拟地	Analog Ground
93	GNDA	模拟地	Analog Ground
94	VDDA1	1.8V模拟电源	1.8V Analog Power Supply
95	GNDA	模拟地	Analog Ground
96	OR-	通道A/B 溢出位负端	Channel A/B Overflow Bit Negative
97	D0-	通道A/B输出数据D0-	Channel A/B Output Data D0-
98	D0+	通道A/B输出数据D0+	Channel A/B Output Data D0+
99	GNDD	数字地	Digital Ground
100	GNDD	数字地	Digital Ground
101	GNDD	数字地	Digital Ground
102	GNDD	数字地	Digital Ground
103	GNDD	数字地	Digital Ground
104	DCO+	通道A/B时钟输出正端	Channel A/B Clock Output Positive
105	GNDD	数字地	Digital Ground
106	GNDD	数字地	Digital Ground
107	D15+	通道A/B输出数据D15+	Channel A/B Output Data D15+
108	D15-	通道A/B输出数据D15-	Channel A/B Output Data D15-
109	D1-	通道A/B输出数据D1-	Channel A/B Output Data D1-
110	D1+	通道A/B输出数据D1+	Channel A/B Output Data D1+
111	VDDD	数字输出驱动电源	Digital Output Driver Power Supply
112	VDDD	数字输出驱动电源	Digital Output Driver Power Supply
113	VDD_SPI	SPI电源	SPI Power Supply
114	VDDD	数字输出驱动电源	Digital Output Driver Power Supply

引出端号 / Pin	符号 / Symbol	名称 / Name	Name (EN)
115	VDDD	数字输出驱动电源	Digital Output Driver Power Supply
116	DCO-	通道A/B时钟输出负端	Channel A/B Clock Output Negative
117	VDDD	数字输出驱动电源	Digital Output Driver Power Supply
118	VDDD	数字输出驱动电源	Digital Output Driver Power Supply
119	D14+	通道A/B输出数据D14+	Channel A/B Output Data D14+
120	D14-	通道A/B输出数据D14-	Channel A/B Output Data D14-
121	D2+	通道A/B输出数据D2+	Channel A/B Output Data D2+
122	D3+	通道A/B输出数据D3+	Channel A/B Output Data D3+
123	D4+	通道A/B输出数据D4+	Channel A/B Output Data D4+
124	D5+	通道A/B输出数据D5+	Channel A/B Output Data D5+
125	D6+	通道A/B输出数据D6+	Channel A/B Output Data D6+
126	D7+	通道A/B输出数据D7+	Channel A/B Output Data D7+
127	D8+	通道A/B输出数据D8+	Channel A/B Output Data D8+
128	D9+	通道A/B输出数据D9+	Channel A/B Output Data D9+
129	D10+	通道A/B输出数据D10+	Channel A/B Output Data D10+
130	D11+	通道A/B输出数据D11+	Channel A/B Output Data D11+
131	D12+	通道A/B输出数据D12+	Channel A/B Output Data D12+
132	D13+	通道A/B输出数据D13+	Channel A/B Output Data D13+
133	D2-	通道A/B输出数据D2-	Channel A/B Output Data D2-
134	D3-	通道A/B输出数据D3-	Channel A/B Output Data D3-
135	D4-	通道A/B输出数据D4-	Channel A/B Output Data D4-
136	D5-	通道A/B输出数据D5-	Channel A/B Output Data D5-
137	D6-	通道A/B输出数据D6-	Channel A/B Output Data D6-
138	D7-	通道A/B输出数据D7-	Channel A/B Output Data D7-
139	D8-	通道A/B输出数据D8-	Channel A/B Output Data D8-
140	D9-	通道A/B输出数据D9-	Channel A/B Output Data D9-
141	D10-	通道A/B输出数据D10-	Channel A/B Output Data D10-
142	D11-	通道A/B输出数据D11-	Channel A/B Output Data D11-
143	D12-	通道A/B输出数据D12-	Channel A/B Output Data D12-
144	D13-	通道A/B输出数据D13-	Channel A/B Output Data D13-

Product Marking / 产品标识

English: The product marking is as follows: SXA026-M1, date code, △C; SXA026-M2, date code, △C; SXA026-M3, date code, △C.

中文： 产品标识如下：SXA026-M1、日期代码、△C；SXA026-M2、日期代码、△C；SXA026-M3、日期代码、△C。



Figure 5: Product Marking Diagram / 图5 产品标识图

Recommended Operating Conditions / 推荐工作条件

参数 / Parameter	符号 / Symbol	范围 / Range
模拟电源 / Analog Supply	VDDA3	3.15 V ～ 3.45 V
模拟电源 / Analog Supply	VDDA1	1.70 V ～ 1.90 V
时钟电源 / Clock Supply	VDD_CLK	1.70 V ～ 1.90 V
数字电源 / Digital Supply	VDDD	1.70 V ～ 1.90 V
SPI 电源 / SPI Supply	VDD_SPI	1.70 V ～ 3.45 V
工作温度 / Operating Temperature	TA	-40°C ～ +85°C

Absolute Maximum Ratings / 绝对最大额定值

参数 / Parameter	符号 / Symbol	最大值 / Maximum
模拟电源 / Analog Supply	VDDA3	3.6 V
模拟电源 / Analog Supply	VDDA1	2.0 V
时钟电源 / Clock Supply	VDD_CLK	2.0 V
数字电源 / Digital Supply	VDDD	2.0 V
SPI 电源 / SPI Supply	VDD_SPI	3.6 V
贮存温度 / Storage Temperature	Tstg	-55°C ～ 125°C
结温 / Junction Temperature	TJ	125°C

Electrical Specifications / 性能指标

English: Unless otherwise specified, VDDA3 = 3.3 V, VDDA1 = VDD_CLK = 1.8 V, VDD_SPI = VDDD = 1.8 V, GNDA = GNDD = 0, SR = 310 MSPS, -40°C ≤ TA ≤ 85°C.

中文： 除另有规定外，VDDA3 = 3.3V，VDDA1 = VDD_CLK = 1.8V，VDD_SPI = VDDD = 1.8V，GNDA = GNDD = 0，SR = 310MSPS，-40°C ≤ TA ≤ 85°C。

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
分辨率 / Resolution	RES	—		16		Bits
失调误差 / Offset Error	Eo	—	-11	—	11	mV
增益误差 / Gain Error	EG	内基准 / Internal reference	-9.0	—	9.0	%FSR
微分线性误差 / Differential Nonlinearity	EDL	—	-1.0	—	1.5	LSB
积分线性误差 / Integral Nonlinearity	EL	—	-16	—	+16	LSB
模拟电源电流 3.3V / Analog Supply Current, 3.3 V	IVDDA3	时钟分频 = 1 / Clock divider = 1	—	—	200	mA
1.8V 模拟电源电流 / Analog Supply Current, 1.8 V	IVDDA1	时钟分频 = 1 / Clock divider = 1	—	—	900	mA
1.8V 时钟电源电流 / Clock Supply Current, 1.8 V	IVDD_CLK	时钟分频 = 1 / Clock divider = 1	—	—	70	mA
SPI 电源电流 / SPI Supply Current	IVDD_SPI	时钟分频 = 1 / Clock divider = 1	—	—	8	mA
数字输出驱动电源电流 / Digital Output Driver Supply Current	IVDDD	时钟分频 = 1 / Clock divider = 1	—	—	300	mA
功耗 / Power Consumption	PW	—	—	2.2	2.50	W
关断功耗 / Power-Down Power	PD	寄存器 0x08 = 0x81 / Register 0x08 = 0x81	—	—	20	mW
数据输出差分电压 / Data Output Differential Voltage	VOD	DDR LVDS 输出模式，100Ω 差分负载 / DDR LVDS output mode, 100Ω differential load	300	—	500	mV
数据输出共模电压 / Data Output Common-Mode Voltage	VOC	DDR LVDS 输出模式，100Ω 差分负载 / DDR LVDS output mode, 100Ω differential load	1.1	—	1.4	V
通道数 / Number of Channels	CH	—		2		CH
信噪比 / SNR	SNR	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	68.0	73	—	dBFS
信噪比 / SNR	SNR	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	68.0	74	—	dBFS
信噪比 / SNR	SNR	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	66.0	72	—	dBFS
信噪比 / SNR	SNR	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	66.0	73.5	—	dBFS
信噪失真比 / SINAD	SINAD	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	67.5	72	—	dBFS
信噪失真比 / SINAD	SINAD	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	67.5	73	—	dBFS
信噪失真比 / SINAD	SINAD	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	65.5	71	—	dBFS
信噪失真比 / SINAD	SINAD	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	65.5	71.5	—	dBFS
有效位数 / ENOB	ENOB	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	10.9	11.6	—	Bits

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
有效位数 / ENOB	ENOB	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	10.9	11.8	—	Bits
有效位数 / ENOB	ENOB	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	10.6	11.5	—	Bits
有效位数 / ENOB	ENOB	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	10.6	11.6	—	Bits
无杂散动态范围 / SFDR	SFDR	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	77	85	—	dBFS
无杂散动态范围 / SFDR	SFDR	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	77	83	—	dBFS
无杂散动态范围 / SFDR	SFDR	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	75	82	—	dBFS
无杂散动态范围 / SFDR	SFDR	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	75	80	—	dBFS
逻辑输入高电平 / Logic Input High Level	VIH	—	1.5	1.8	—	V
逻辑输入低电平 / Logic Input Low Level	VIL	—	—	0	0.3	V
逻辑输入电流 / Logic Input Current	IIN	高电平输入电流 / High-level input current	-190	—	190	μA
逻辑输入电流 / Logic Input Current	IIN	低电平输入电流 / Low-level input current	-145	—	145	μA
时钟输入电流 / Clock Input Current	ICLK	高电平输入电流 / High-level input current	4	—	155	μA
时钟输入电流 / Clock Input Current	ICLK	低电平输入电流 / Low-level input current	-155	—	-4	μA
通道隔离度 / Channel Isolation	ISO		80	90	—	dB
输入时钟范围 / Input Clock Range	fclk		80	310	1240	MHz
转换速率 / Conversion Rate	SR	—	—	310	310	MHz

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Typical Performance Characteristics / 主要特性曲线图

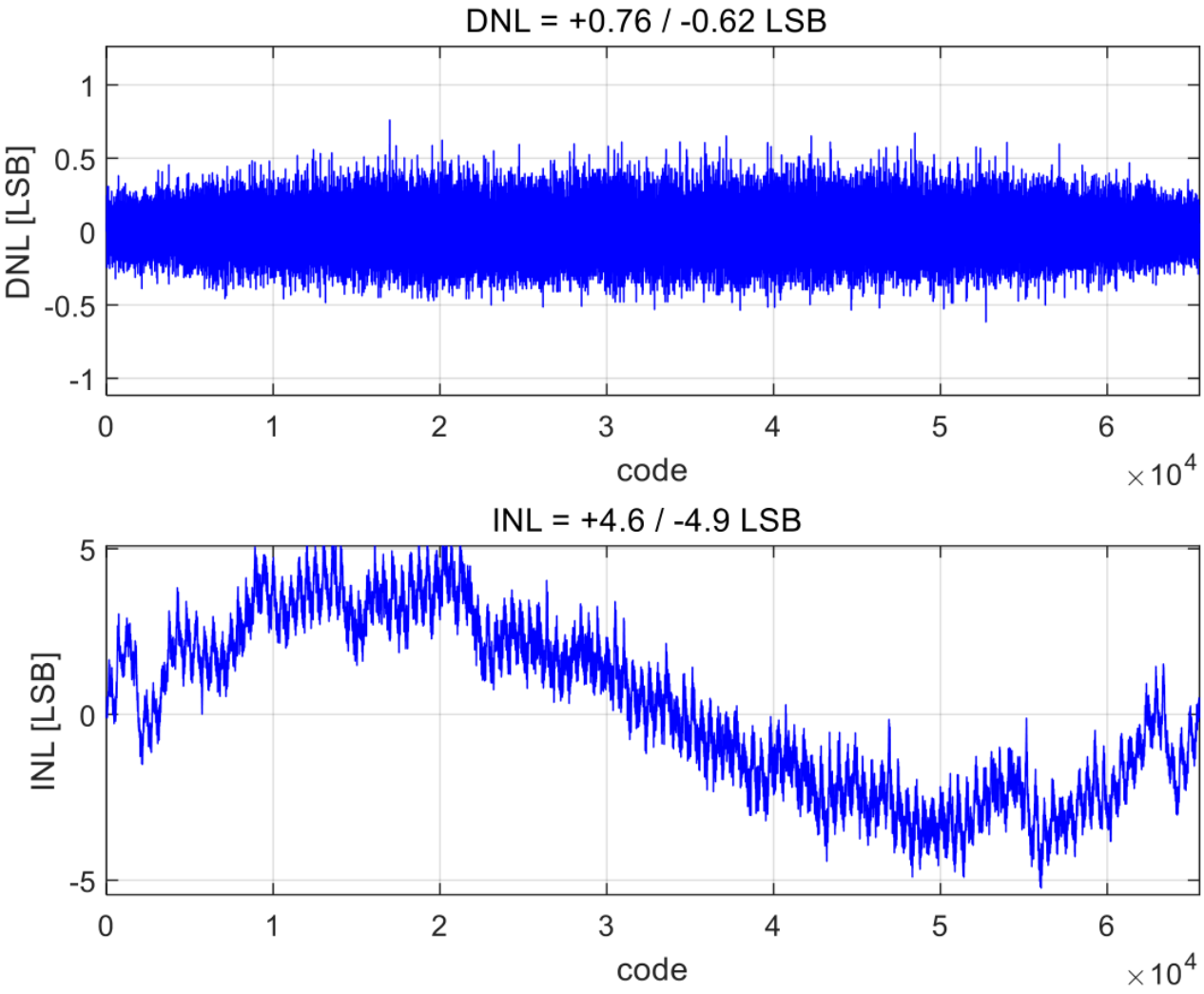


Figure 6: DNL and INL Performance / 图6 DNL 和INL 性能图

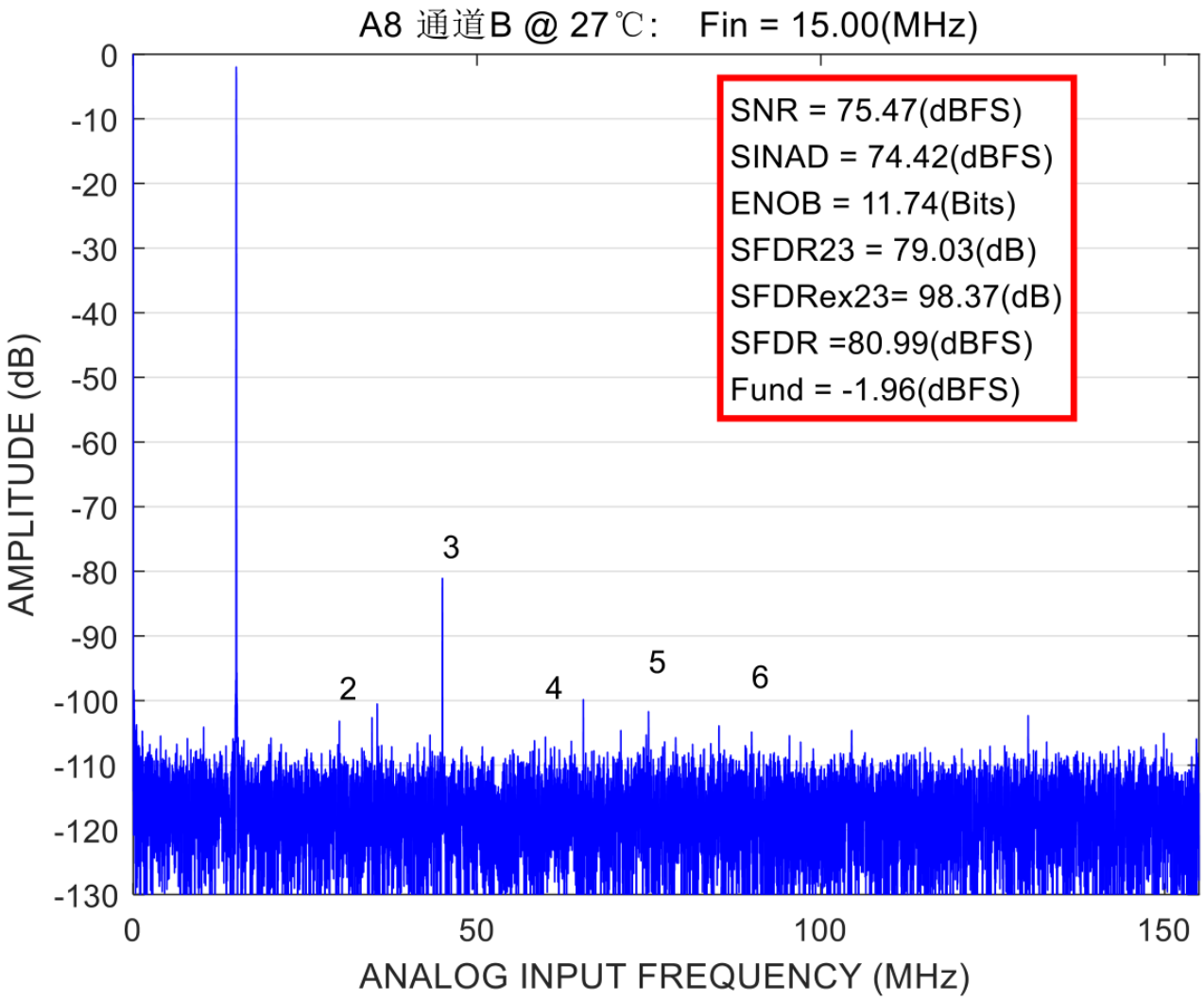


Figure 7: fIN = 15 MHz / 图7 fIN =15MHz

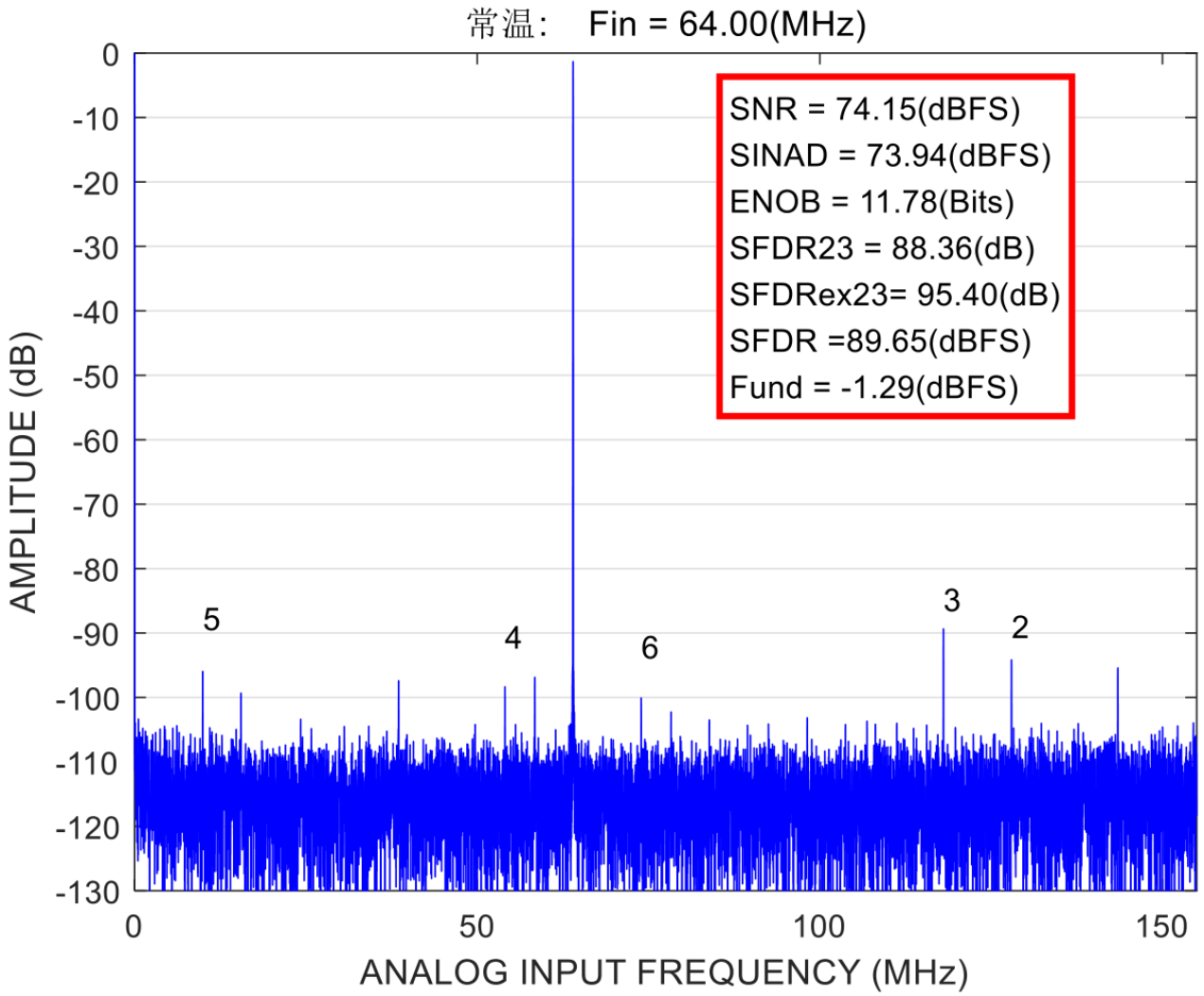


Figure 8: fIN = 64 MHz / 图8 fIN =64MHz

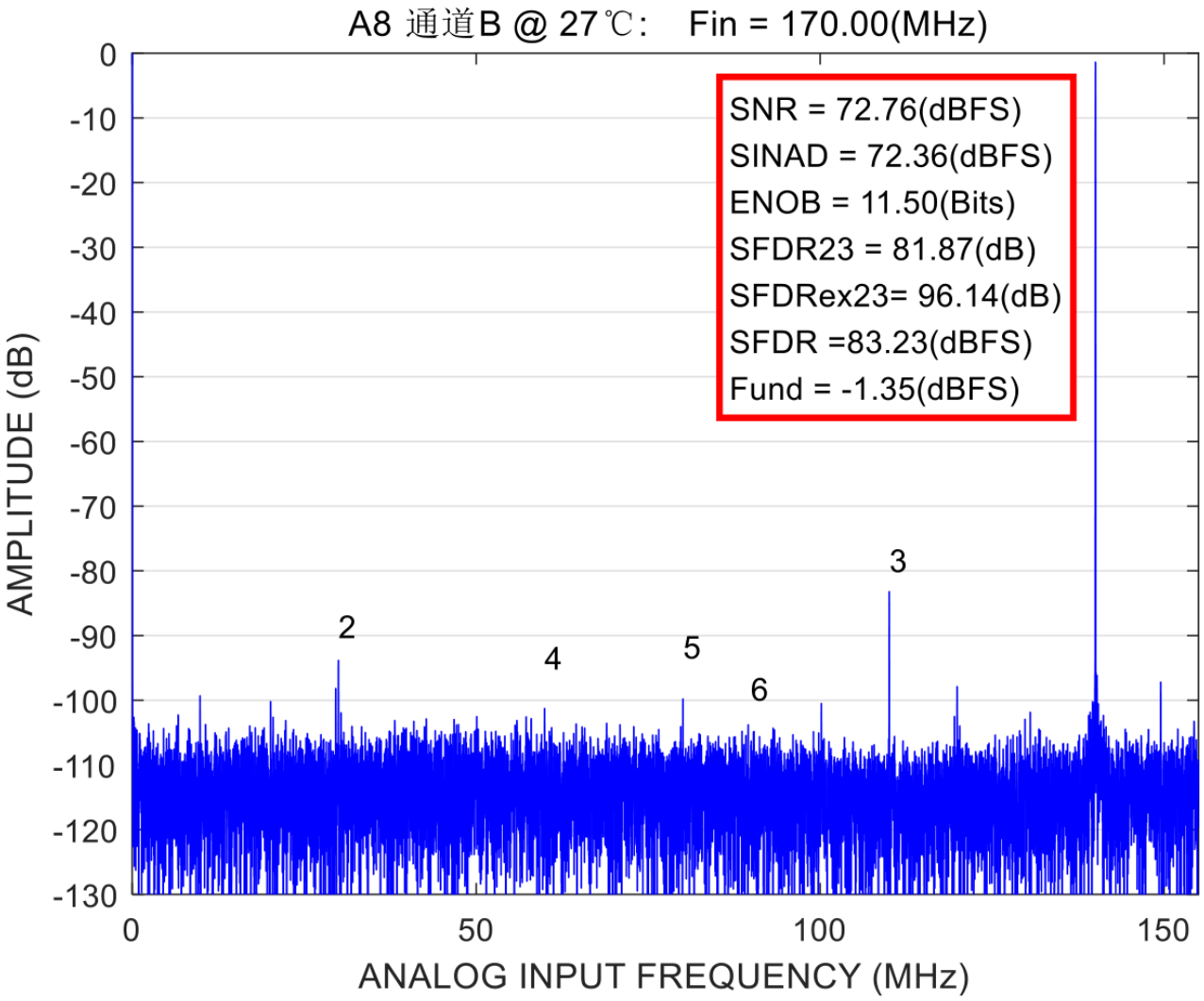


Figure 9: fIN = 170 MHz / 图9 fIN =170MHz

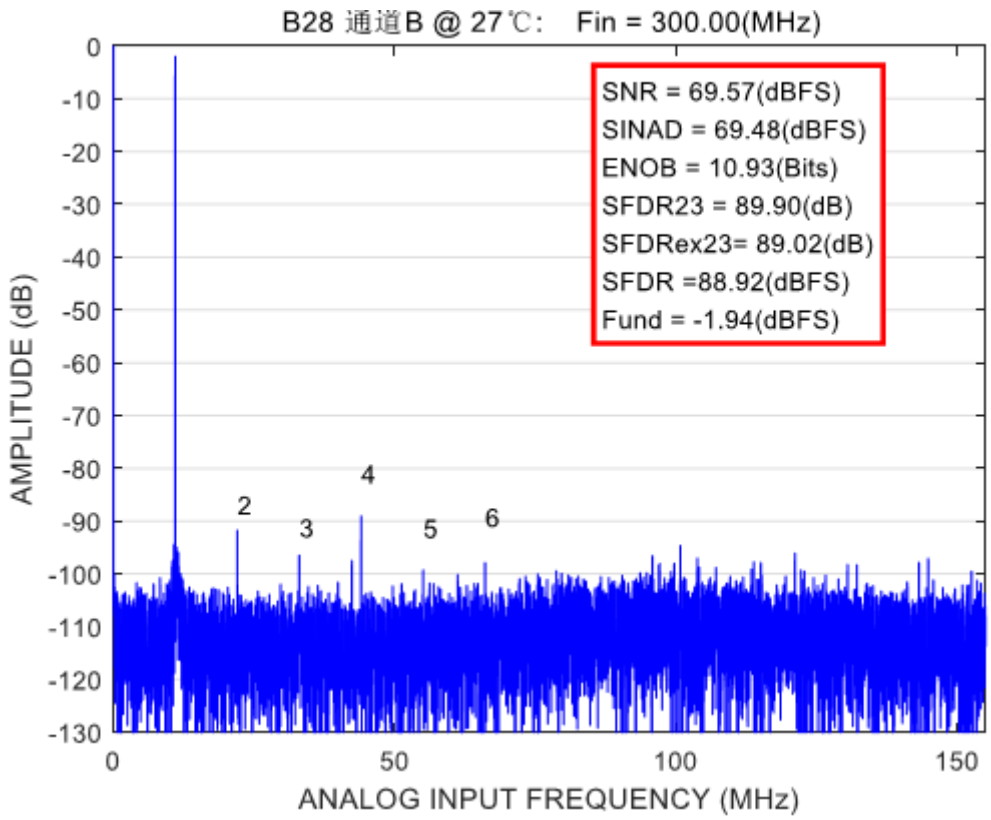


Figure 10: fIN = 300 MHz / 图10 fIN =300MHz

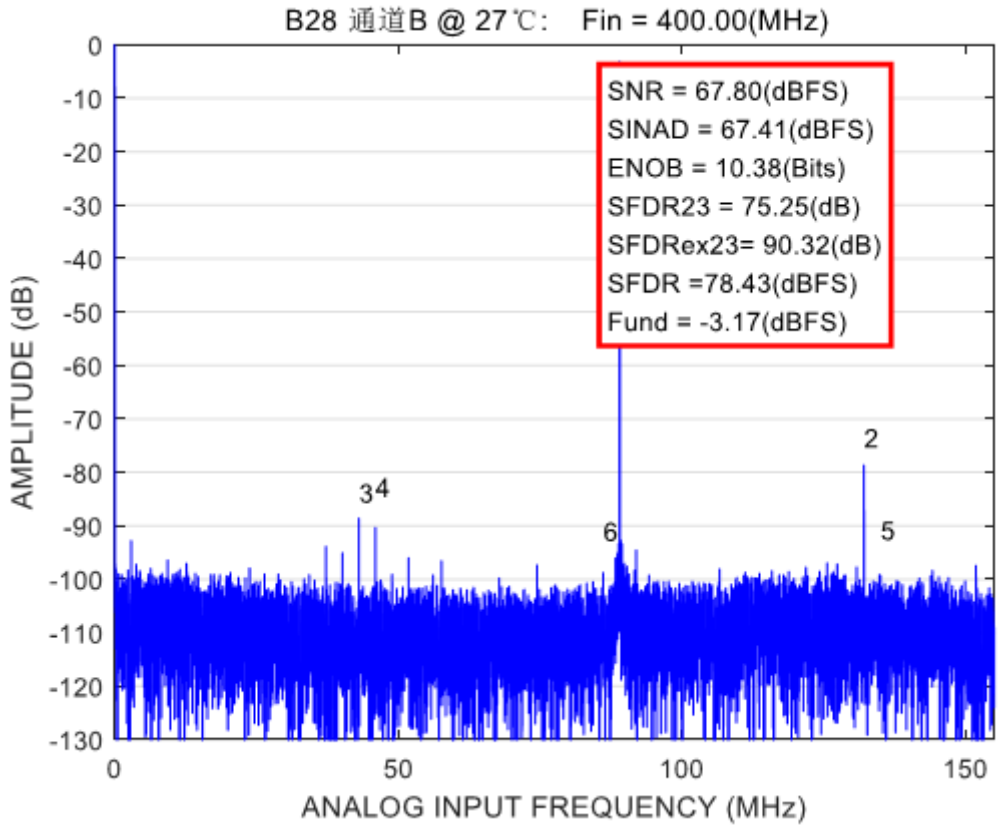


Figure 11: fIN = 400 MHz / 图11 fIN =400MHz

Control Functions / 控制功能

English: The control functions of this device are mainly implemented through the SPI. The SPI register definitions are shown in Table 2.

中文： 该产品控制功能主要通过 SPI 实现，SPI 寄存器定义如表 2 所示。

Table 2. SPI Pins / 表2 SPI 引脚

引脚 / Pin	功能 / Function
SCLK	串行时钟。串行移位时钟输入，同步串行接口的读写。 / Serial clock. Serial shift clock input; synchronizes the read/write operations of the serial interface.
SDIO	串行数据输入/输出。双用引脚，根据所发送的指令和时序中的相对位置，通常作为输入或输出。 / Serial data input/output. Dual-purpose pin; functions as an input or an output depending on the instruction sent and its relative position in the timing sequence.
CSB	片选。低电平控制读写周期，上电时必须拉到逻辑高。 / Chip select. A low level controls the read/write cycle; the pin must be pulled to logic high at power-up.

Memory Map Registers / 存储器映射寄存器

Table 3. Memory Map Registers / 表3 存储器映射寄存器

地址（16 进制） / Address (Hex)	寄存器 / Register	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB	默认值（16 进制） / Default (Hex)	默认说明/注释 / Default Description/Comments
芯片配置寄存器 / Chip Configuration Registers											
0x00	SPI 端口配置（全局） / SPI Port Configuration (Global)	0	LSB first	软件重置 / Software reset	1	1	软件重置 / Software reset	LSB first	0	0x18	无论转换模式如何，LSB first 模式或 MSB first 模式都能正确写入 / The LSB first or MSB first mode can be written correctly regardless of the conversion mode
0x01	芯片 ID（全局） / Chip ID (Global)	8 位芯片 ID[7:0]，(SXA026-M1、SXA026-M2、SXA026-M3 = 0xC1)（默认） / 8-bit chip ID[7:0], (SXA026-M1, SXA026-M2, SXA026-M3 = 0xC1) (default)								0xC1	只读 / Read only
0x02	芯片等级（全局） / Chip Grade (Global)			速度等级 ID，0x00：默认 / Speed grade ID, 0x00: default						0x00	速度等级 ID 区分设备；只读 / The speed grade ID distinguishes devices; read only
通道指数和传输寄存器 /											

地址（16 进制） / Address (Hex)	寄存器 / Register	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB	默认值（16 进制） / Default (Hex)	默认说明/注释 / Default Description/Comments
Channel Index and Transfer Registers											
0x05	通道指数（全局） / Channel Index (Global)							通道 B 默认 / Channel B default	通道 A 默认 / Channel A default	0x03	该位被设置来决定芯片上的哪个设备接收下一个写命令；仅适用于本地寄存器 / This bit is set to determine which device on the chip receives the next write command; applies to local registers only
0xFF	传输（全局） / Transfer (Global)								传输 / Transfer	0x00	同步地将数据从主移位寄存器转移到从寄存器 / Synchronously transfers data from the master shift register to the slave register
ADC 功能 / ADC Functions											
0x08	电源模式（本地） / Power Mode (Local)	预设为 1 / Reserved = 1		外部断电引脚功能 0 = 断电 1 = 备用 / External power-down pin function: 0 = power down, 1 = standby				内部断电模式（本地）00 = 正常操作 01 = 全断电 10 = 备用 11 = 预设 / Internal power-down mode (local): 00 = normal operation, 01 = full power down, 10 = standby, 11 = reserved		0x80	控制断电选项 / Controls the power-down options
0x09										0x01	

地址（16 进制） / Address (Hex)	寄存器 / Register	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB	默认值（16 进制） / Default (Hex)	默认说明/注释 / Default Description/Comments
	全局时钟（全局） / Global Clock (Global)								激活 DCS 默认 / Activate DCS, default		
0x0B	时钟分频（全局） / Clock Divider (Global)						时钟分频率 000 = 1 分频 001 = 2 分频 010 = 预设的，未使用 011 = 4 分频 100 = 8 分频 / Clock divide ratio: 000 = divide by 1, 001 = divide by 2, 010 = reserved, unused, 011 = divide by 4, 100 = divide by 8			0x00	
0x10	失调调整（本地） / Offset Adjust (Local)	LSB 失调调整从 +127（0111 1111）到 -128（1000 0000）（2 的补码） / LSB offset adjustment from +127 (0111 1111) to -128 (1000 0000) (two's complement)								0x00	
0x14	输出模式（本地） / Output Mode (Local)							输出格式 00 = 偏移二进制（默认）01 = 2 的补码 10 = 格雷码 11 = 预设 / Output format: 00 = offset binary (default), 01 = two's complement, 10 = Gray code, 11 = reserved		0x00	配置输出和数据格式 / Configures the output and data format

地址（16 进制）/ Address (Hex)	寄存器 / Register	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB	默认值（16 进制）/ Default (Hex)	默认说明/注释 / Default Description/Comments
0x15	输出 LVDS 控制（全局）/ Output LVDS Control (Global)						LVDS 输出驱动电流调整 000 = 3.72mA（ANSI-LVDS 默认）001 = 3.50mA 010 = 3.30mA 011 = 2.96mA 100 = 2.82mA 101 = 2.57mA 111 = 2.20mA（减少摆动 LVDS）/ LVDS output drive current adjustment: 000 = 3.72 mA (ANSI-LVDS default), 001 = 3.50 mA, 010 = 3.30 mA, 011 = 2.96 mA, 100 = 2.82 mA, 101 = 2.57 mA, 111 = 2.20 mA (reduced-swing LVDS)			0x00	
0x16	时钟相位调整（全局）/ Clock Phase Adjust (Global)						输入时钟分频相位调整 000 = 无延迟 001 = 1 个输入时钟周期 010 = 2 个输入时钟周期 011 = 3 个输入时钟周期 100 = 4 个输入时钟周期 101 = 5 个输入时钟周期 110 = 6 个输入时钟周期 111 = 7 个输入时钟周期 / Input clock divider phase adjustment: 000 = no delay, 001 = 1 input clock cycle, 010 = 2 input clock cycles, 011 = 3 input clock cycles, 100 = 4 input clock cycles, 101 = 5 input clock cycles, 110 = 6 input clock cycles, 111 = 7 input clock cycles			0x00	
0x17	DCO± 输出延迟（全局）/ DCO± Output Delay (Global)				DCO± 时钟延迟（Delay =（2500ps × 寄存器值/31））00000 = 0 ps 00001 = 81 ps 00010 = 161 ps … 11110 = 2419 ps 11111 = 2500 ps / DCO± clock delay (Delay = (2500 ps × register value/31)): 00000 = 0 ps, 00001 = 81 ps, 00010 = 161 ps,						0x00

地址（16 进制） / Address (Hex)	寄存器 / Register	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB	默认值（16 进制） / Default (Hex)	默认说明/注释 / Default Description/Comments
					…, 11110 = 2419 ps, 11111 = 2500 ps						
0x18	输入范围选择（全局） / Input Range Select (Global)	预设为 1 / Reserved = 1	预设为 1 / Reserved = 1				VREF 选择 000 = 1.25V（2.5 VP-P 输入），默认 001 = 1.125V（2.25 VP-P 输入）010 = 1.20V（2.4 VP-P 输入）011 = 1.25V（2.5 VP-P 输入）100 = 未使用 101 = 1.0V（2.0 VP-P 输入） / VREF select: 000 = 1.25 V (2.5 VP-P input), default; 001 = 1.125 V (2.25 VP-P input); 010 = 1.20 V (2.4 VP-P input); 011 = 1.25 V (2.5 VP-P input); 100 = unused; 101 = 1.0 V (2.0 VP-P input)			0xC0	
0x30	Dither（本地） / Dither (Local)				激活 Dither / Activate Dither					0x00	
0x100	SYNC 控制（全局） / SYNC Control (Global)						时钟分频器 Next SYNC / Clock divider next SYNC	时钟分频器 SYNC 激活 / Clock divider SYNC enable	控制 SYNC 缓冲激活 / SYNC buffer enable control	0x00	
0x22A	输入频率设定（全局） / Input Frequency Setting (Global)							0：fIN in 1st Nyquist 1：fIN in 2nd Nyquist 2：fIN in 3rd Nyquist 或更高 / 0: fIN in 1st Nyquist zone; 1: fIN in 2nd Nyquist zone; 2:		0x00	

地址（16 进制） / Address (Hex)	寄存器 / Register	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB	默认值（16 进制） / Default (Hex)	默认说明/注释 / Default Description/Comments
								fIN in 3rd Nyquist zone or higher			
0x4FA	校准断电配置（全局） / Calibration Power-Down Configuration (Global)	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	电源关断/备用初始校准行为：0b00：使用以前的校准校正 0b11：启动快速校准 / Power-down/standby initial calibration behavior: 0b00 = use the previous calibration correction; 0b11 = start fast calibration		0x03	
0x4FB	校准断电配置（全局） / Calibration Power-Down Configuration (Global)	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	预设为 0 / Reserved = 0	预设为 1 / Reserved = 1	重置后台校准设为高，再为低 / Reset background calibration: set high, then low	预设为 0 / Reserved = 0	暂停后台校准 / Pause background calibration	0x08	

Typical Application Circuit / 典型应用线路图

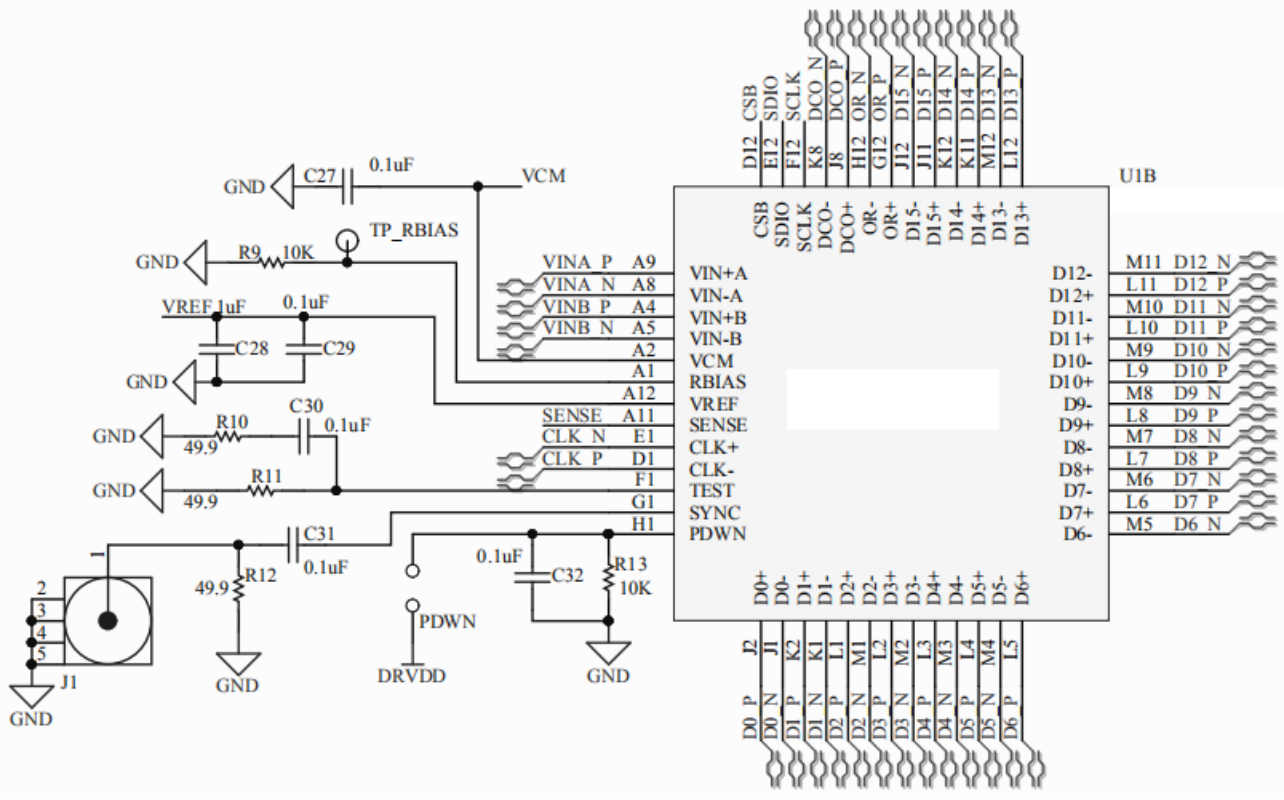


Figure 12: Analog Input Network / 图12 模拟输入网络

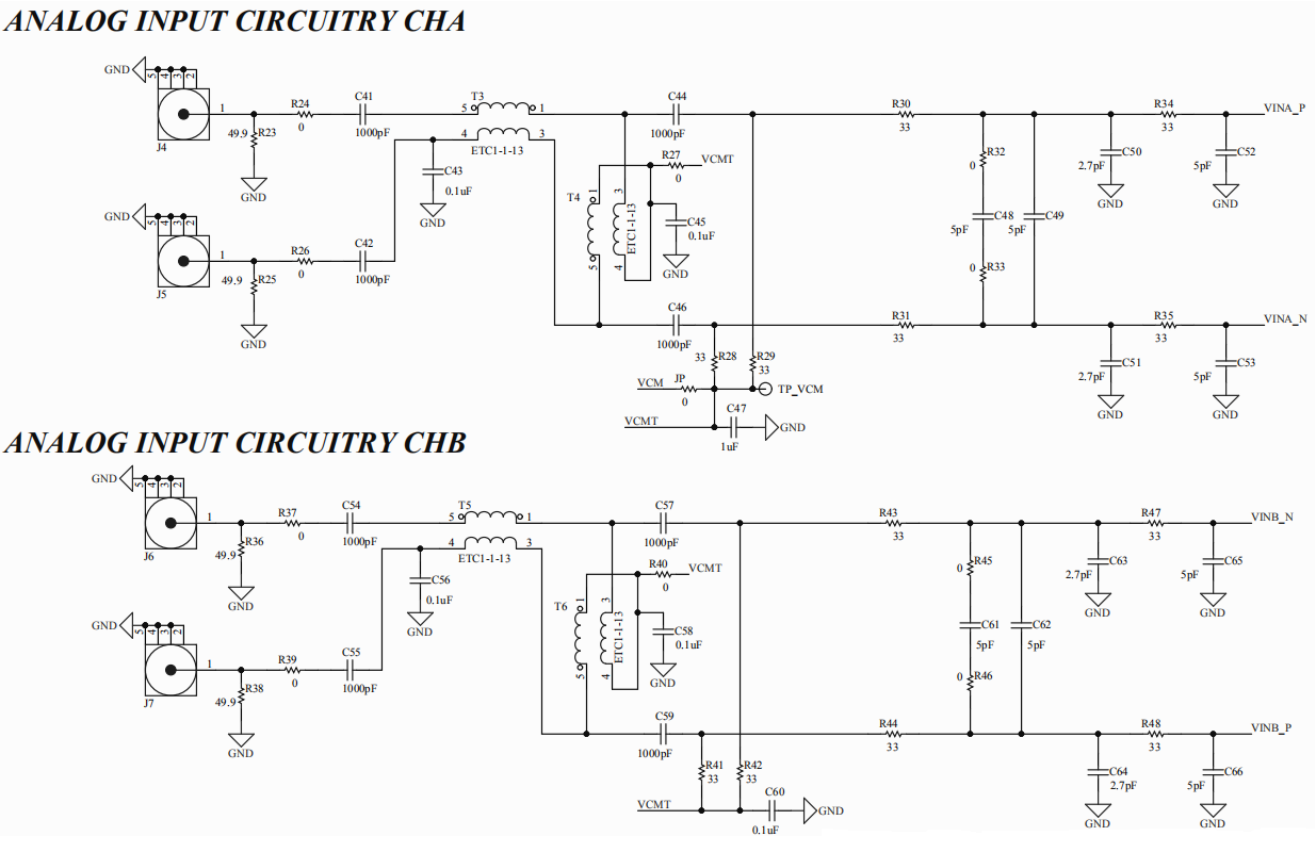


Figure 13: Analog Input Network / 图13 模拟输入网络

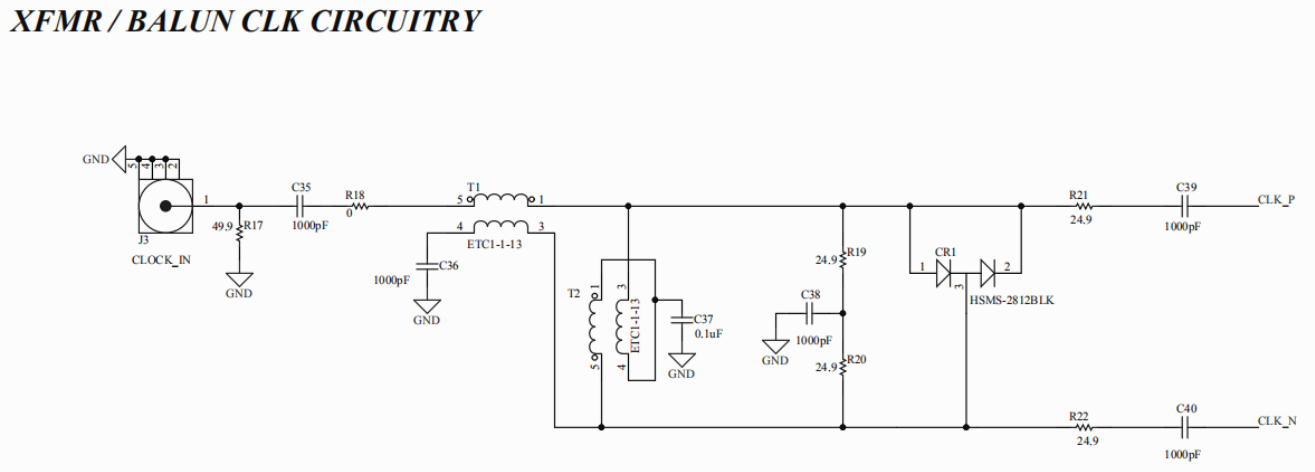


Figure 14: Clock Driver Network / 图14 时钟驱动网络

Additional Application Notes / 其他应用说明

(1) Input Signal / 输入信号

English: The SXA026 analog input is a high-performance differential buffer that isolates the analog input front-end network from the ADC core, giving the ADC consistent input impedance and optimal performance over a wide frequency range. The analog differential input impedance is approximately 54 kΩ, with a parallel capacitance of 5.8 pF, as shown in Figure 15. Depending on the application scenario, passive discrete components can be used to build a low-pass filter network for the ADC. In IF undersampling applications, the parallel capacitance needs to be reduced, as its value limits the input signal bandwidth. Depending on the analog input signal, configure register 0x22A so that the device achieves the best dynamic performance, as shown in Table 4.

中文： SXA026 模拟输入端是高性能差分缓冲器，将模拟输入前端网络和 ADC 内核隔离，使 ADC 在较宽频率范围内具有一致的输入阻抗和具有最优异的性能。模拟差分输入阻抗约为 54KΩ，并联电容为 5.8pF，如图 15 所示。根据使用场景，可以用无源离散元件为 ADC 构建低通滤波网络。在中频欠采样应用中，需要减小并联电容，并联电容的大小会限制输入信号的带宽。根据模拟输入信号的不同，对 0x22A 寄存器进行配置，使器件具有最佳的动态性能，如表 4 所示。

Table 4. Register 0x22A Settings / 表4 寄存器 0x22A 设置

0x22A 设置 / Setting	输入频率范围 / Input Frequency Range
0（默认 / Default）	0-155 MHz（第一奈奎斯特区 / 1st Nyquist zone）
1	155-310 MHz（第二奈奎斯特区 / 2nd Nyquist zone）
2	＞310 MHz（第三奈奎斯特区 / 3rd Nyquist zone）

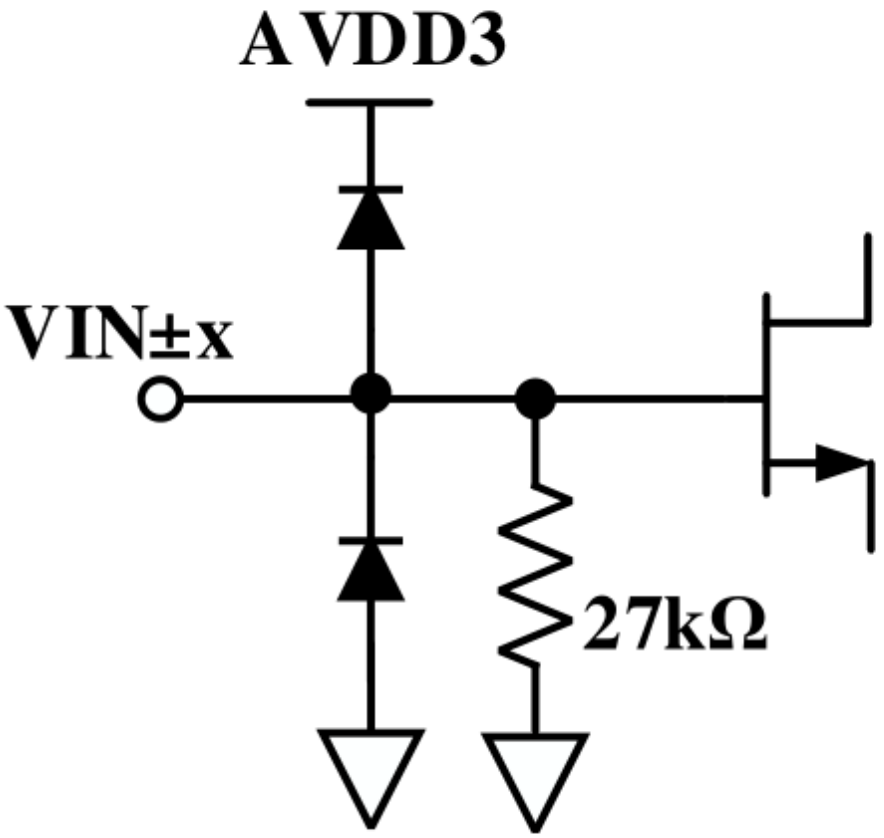


Figure 15: Equivalent Analog Input Circuit / 图15 等效模拟输入电路

(2) Input Common Mode / 输入共模

English: The SXA026 internal analog inputs do not provide DC bias. In AC-coupled applications, the user needs to provide a suitable bias; it is recommended to set the common-mode voltage to 2 V for best performance. The common-mode voltage can be provided through the VCM pin. The VCM pin requires a 0.1 µF capacitor to ground; place the decoupling capacitor as close as possible to the chip pins to minimize the series resistance and inductance between the converter and the decoupling capacitor.

中文： SXA026 内部模拟输入端没有提供直流偏置。在交流耦合应用中，用户需要提供一个合适的偏置，建议将共模电压设置成 2V 以获得最佳性能。共模电压可通过 VCM 引脚提供。VCM 引脚需要使用 0.1µF 的电容接地，尽可能地将去耦电容靠近芯片的引脚，以使转换器与去耦电容之间的串联电阻和电感最小化。

(3) Clock Input Requirements / 时钟输入要求

(3.1) Clock Input / 时钟输入

English: The SXA026 clock input supports CMOS, LVDS, and LVPECL format inputs or a sine-wave signal. Regardless of the clock source format, clock jitter is the primary concern. Figures 16 and 17 provide two recommended clock input structures (the clock frequency can reach 1240 MHz). An RF balun or RF transformer converts the single-ended signal to differential form. For clock frequencies from 125 MHz to 1240 MHz, an RF balun is recommended. For clock frequencies from 80 MHz to 200 MHz, an RF transformer is recommended. Whichever clock input structure is used, back-to-back Schottky diodes must be used

near the SXA026 clock inputs CLK+ and CLK-. On the one hand, this prevents an excessive clock signal amplitude from feeding into other ADC modules and causing effects; on the other hand, a proper amplitude ensures fast clock rise and fall times, which is critical for low clock jitter performance.

中文： SXA026 时钟输入可支持 CMOS、LVDS、LVPECL 形式输入或者正弦波信号。不管哪种形式的时钟信号源，时钟抖动是最需要关注的。图 16 和图 17 中提供了两种较好的时钟输入结构（时钟频率可达到 1240 MHz）。采用射频巴伦或射频变压器将单端转换成差分形式。时钟频率在 125MHz 到 1240MHz 范围时，推荐使用射频巴伦。时钟频率在 80MHz 到 200MHz 时，推荐使用射频变压器。无论采用那种形式的时钟输入结构，都要求在靠近 SXA026 时钟输入端 CLK+ 和 CLK- 端使用背连接的肖特基二极管，一方面，防止时钟信号幅度过大或馈入 ADC 其他模块造成影响，另一方面，合理幅度保证时钟快速上升与下降，这对时钟低抖动性能至关重要。

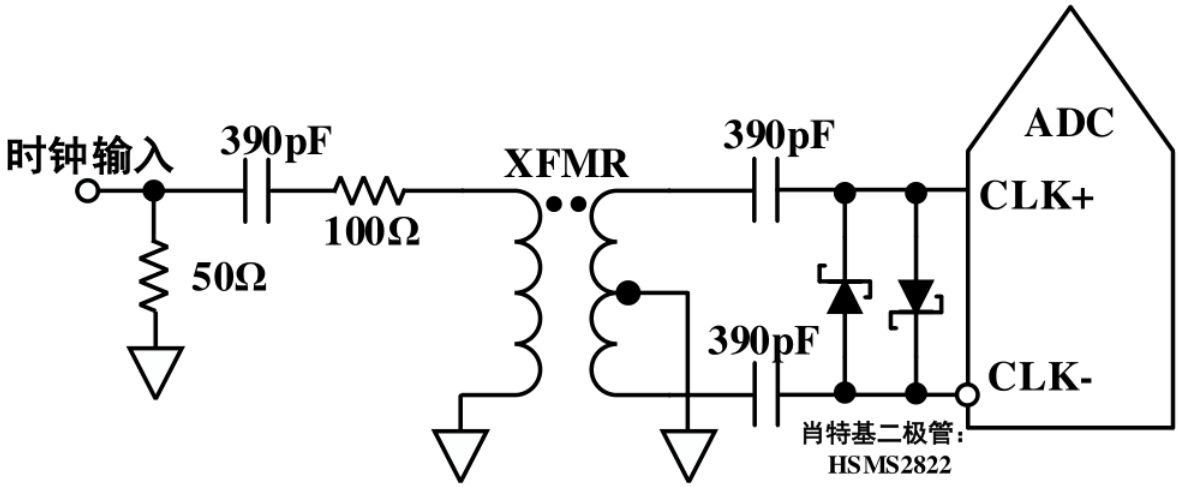


Figure 16: Transformer-Coupled Differential Clock (above 200 MHz) / 图16 变压器耦合差分时钟（超过200MHz）

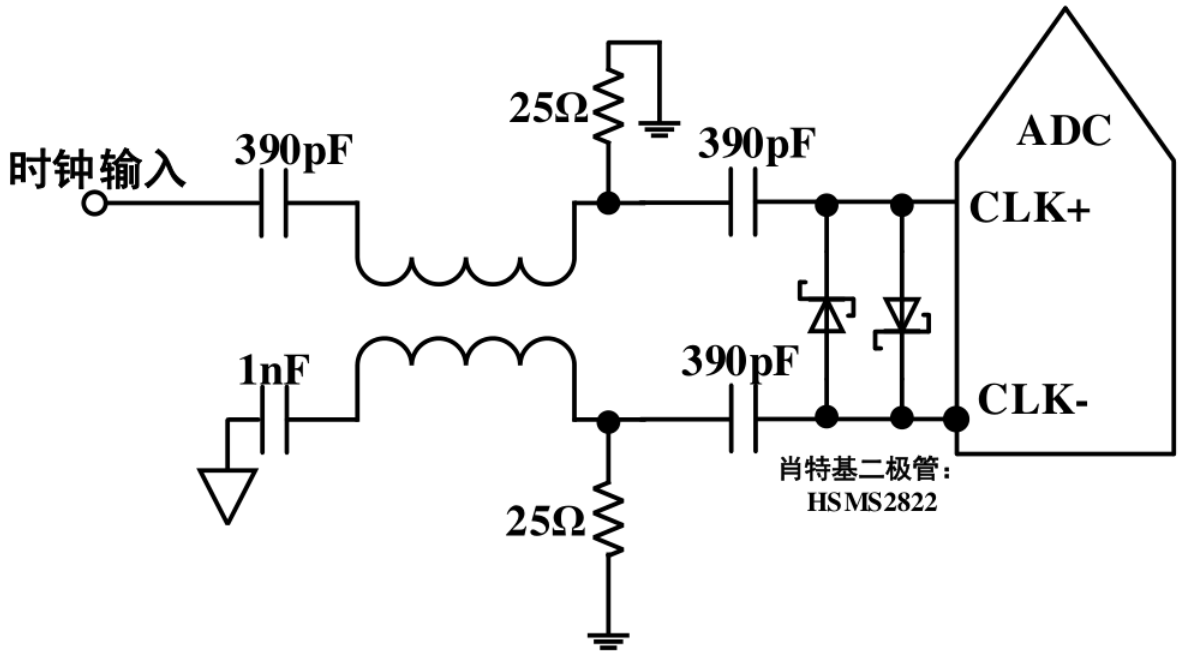


Figure 17: Balun-Coupled Differential Clock (above 1240 MHz) / 图17 巴伦耦合差分时钟（超过1240MHz）

(3.2) Clock Duty Cycle / 时钟占空比

English: High-speed ADCs use both clock edges to generate the internal clock signals they need. Pipeline ADCs are sensitive to duty cycle; to maintain reasonable dynamic performance, a pipeline ADC duty cycle of 50% ±5% is usually required. The SXA026 has a duty-cycle stabilization function; even when the external input clock duty cycle varies over a wide range, it can output a clock signal with the nominal 50% duty cycle. Jitter on the rising edge of the input clock remains a primary concern and must not be affected by the duty-cycle control circuit. The duty-cycle control loop cannot operate effectively when the clock frequency is below 80 MHz.

中文： 高速 ADC 都会使用时钟的两个沿来产生满足内部需求的时钟信号。流水线 ADC 对占空比很敏感，为保持合理的动态性能，通常要求流水线 ADC 的占空比达到 50%±5%。SXA026 具有占空比稳定功能，当外部输入时钟的占空比范围较大时，也能输出额定 50% 占空比的时钟信号。输入时钟上升沿的抖动依然是最为关心的一个问题，并且不能受占空比控制电路的影响。占空比控制环路在时钟频率低于 80MHz 时不能有效地工作。

(3.3) Dither / 抖动

English: The ADC has an optional internal dither circuit that especially improves SFDR for small signals; dither improves the local linearity of the ADC transfer function. In essence, dither injects a known random white-noise sequence into the ADC, as shown in Figure 18. The dither DAC full scale is small and does not limit the normal ADC input amplitude. The pseudo-random sequence is converted by the DAC and added to the ADC core for conversion, and then the pseudo-random sequence is subtracted in the digital domain. Dither causes some reduction in the ADC SNR and SINAD. Dither improves SFDR at the cost of reducing the ADC SNR and SINAD. In the first Nyquist zone, the SNR decreases by approximately 0.5 dB. Using dither does not affect the full-scale dynamic range.

中文： ADC 具有可选的内部抖动电路，尤其能提升小信号状态下的 SFDR，抖动可以改善 ADC 传递函数的局部线性度。抖动的实质就是将已知的随机白噪声序列注入到 ADC 中，如图 18 所示。抖动 DAC 的满量程很小，不会限制 ADC 的正常输入幅度。伪随机序列经过 DAC 转换后加入到 ADC 内核进行转换，然后再数字域将伪随机序减去，抖动引起 ADC 的信噪比和信噪失真比有一定的减少。抖动提升了 SFDR，但代价是降低了 ADC 的信噪比和信噪失真比。在第一奈奎斯特区，信噪比降低大约 0.5dB。使用抖动也不会影响满量程动态范围。

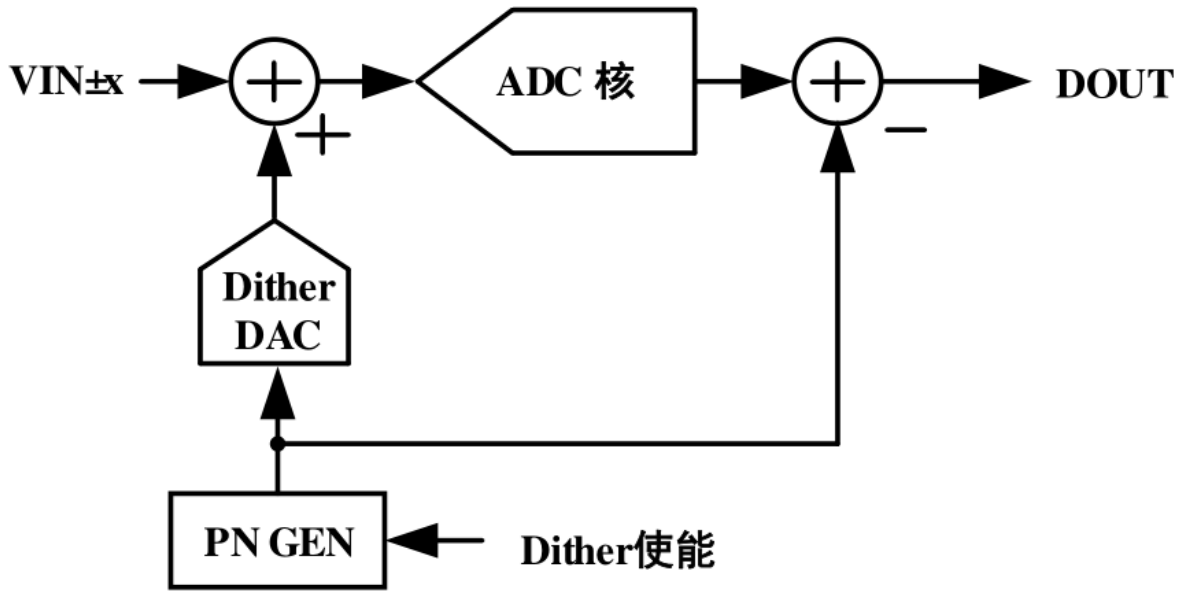


Figure 18: Dither Block Diagram / 图18 Dither 框图

Precautions / 注意事项

English: 1. Product installation precautions:

中文： 1. 产品安装注意事项：

English: 2) The application PCB must have a complete, clean ground.

中文： 2) 要求应用对象电路板有一个完整干净的地。

English: 3) The digital ground and analog ground of the application PCB should be separated as much as possible; do not route digital traces next to analog traces.

中文： 3) 要求应用对象电路板的数字地和模拟地尽量分离，不要将数字线布于模拟线旁边。

English: 4) Assembly instructions:

中文： 4) 电装说明：

English: ① This product has a moisture sensitivity level of MSL3. The allowable time the product may be exposed to the external environment after removal from the moisture barrier bag, dry storage, or baking, before reflow soldering, is: ≤30°C/60% RH, 168 h;

中文： ①本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h；

English: ② If the device storage conditions cannot be controlled or traced, bake strictly at 125°C for 8 h before assembly;

中文： ②若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤；

English: ③ If the assembly environment temperature and humidity cannot be guaranteed at ≤30°C/60% RH, complete soldering within 12 h after baking;

中文： ③若电装环境温湿度无法保证 ≤30°C/60RH%，请在烘烤后 12h 内完成焊接；

English: ④ After baking, the product easily generates static electricity; ESD protection is required during all handling;

中文： ④产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护；

English: ⑤ For board-level assembly with leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C~220°C, the maximum peak temperature should not exceed 235°C, the time within ±5°C of the peak temperature is ≤20 s, the time above the liquidus is 60~90 s, the ramp-up rate is 2~4°C/s, and the ramp-down rate is 2~6°C/s;

中文： ⑤板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~220°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s；

English: ⑥ For board-level assembly with lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C~245°C, the maximum peak temperature should not exceed 260°C, the time within ±5°C of the peak temperature is ≤20 s, the time above the liquidus is 60~90 s, the ramp-up rate is 2~4°C/s, and the ramp-down rate is ≤2°C~6°C;

中文： ⑥板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 ≤2°C~6°C；

English: ⑦ If a mixed assembly process requires a higher temperature, ensure that the device body temperature does not exceed 260°C at most. (The device body temperature measurement point is on the top surface of the device during reflow soldering);

中文： ⑦若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C。（器件本体温度测量点位于回流焊时器件上表面）；

English: ⑧ This product uses lead-free or leaded solder balls, of SAC305 or Sn63Pb37 material.

中文： ⑧本产品采用无铅或有铅焊球，材料为 SAC305 或 Sn63Pb37。

English: 2. Product application precautions: At every power-up of the product: first, perform a reset operation through register 0x00; then, configure the relevant registers (as required by the user).

中文： 2. 产品应用注意事项：产品每次上电：首先，通过 0x00 寄存器进行复位操作；然后，进行相关寄存器（用户所需）配置。

English: 3. Product protection precautions:

中文： 3. 产品防护注意事项：

English: 1) All pins of the product are designed with ESD protection structures; however, large-energy electrical pulses may still damage the circuit, so ESD protection must be observed during testing, handling, and storage.

中文： 1) 产品所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。

English: 2) Exceeding the absolute maximum ratings may cause permanent damage to the device.

中文： 2) 超出绝对最大额定值可能会导致器件永久性损坏。

Common Faults and Troubleshooting / 常见故障及处理办法

English: 1. No signal output: check whether the supply voltage, input signal, and clock are correctly applied. 2. Overflow signal occurs: check whether the common-mode voltage configuration of the analog input positive and negative terminals is correct, and whether the input signal amplitude is correct. 3. Device operates unstably: check the power supply and ensure the supply voltage is stable.

中文： 1. 无信号输出：检查电源电压、输入信号、时钟是否正确加载。2. 出现溢出信号：检查模拟输入正端和负端的共模电压配置是否正确，输入信号幅度是否正确。3. 器件工作不稳定：检查电源，保证电源电压稳定。

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Additional Notes / 附加说明

English: 1. This manual was first released on May 5, 2023.

中文： 1、本说明书首次发布日期：2023 年 5 月 5 日；

更改日期 / Change Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
2023.05.05	——	首次发布 / First release	
2024.03.27	标题、标准、产品特点、产品标识、绝对最大额定值、注意事项、电装要求、附加说明 / Title, Standard, Features, Product Marking, Absolute Maximum Ratings, Precautions, Assembly Requirements, Additional Notes	首页标题修改；删除总规范、增加详细规范号并修改质量等级描述；增加产品重量；增加产品标识部分的标识说明项；修改绝对最大额定值为表格显示；增加"产品应用注意事项"；增加"电装要求"章节；增加"替代国外产品情况说明"；页眉修改，其他描述性、格式类修改 / Title page heading revised; general specification removed, detailed specification number added, and quality grade description revised; product weight added; marking description items added to the Product Marking section; absolute maximum ratings changed to table format; "Product Application Precautions" added; "Assembly Requirements" chapter added; "Substitution of Foreign Products" section added; header revised, and other descriptive and formatting changes	——
2024.05.29	——	说明书换版 / Manual reissued	

English: 2. Product status: ■ In production (this model is currently in production, and formal products can be provided) □ Pre-release (this model has not yet entered formal production, but samples can be provided).

中文： 2. 本产品状态：■生产（该产品型号目前已在生产，可以提供正式产品）□预发布（该产品型号尚未投入正式生产，但是可以提供样品）。

Substitution of Foreign Products — Statement / 替代国外产品情况说明

项目 / Item	SXA026	AD9652
生产厂家 / Manufacturer	深信科技 / Shenxin Technology	ADI

项目 / Item	SXA026	AD9652
产品型号（规格） / Model (Specification)	SXA026-M1、SXA026-M2、SXA026-M3	AD9652BBCZ-310

性能指标 / Performance Specifications

参数 / Parameter	条件 / Conditions	SXA026	AD9652BBCZ-310	单位 / Unit
分辨率 / Resolution	—	16	16	Bits
失调误差 / Offset Error	—	—	1.5（典型值 / Typ）	mV
增益误差 / Gain Error	内基准 / Internal reference	—	-0.3（典型值 / Typ）	%FSR
微分线性误差 / Differential Nonlinearity	fIN = 10 MHz	-1.0~1.5	-0.76/1.1（典型值 / Typ）	LSB
积分线性误差 / Integral Nonlinearity	fIN = 10 MHz	-16~+16	-4.5/4.5	LSB
3.3V 模拟电源电流 / Analog Supply Current, 3.3 V	时钟分频 = 1 / Clock divider = 1	—	145（典型值 / Typ）	mA
1.8V 模拟电源电流 / Analog Supply Current, 1.8 V	时钟分频 = 1 / Clock divider = 1	—	701（典型值 / Typ）	mA
1.8V 时钟电源电流 / Clock Supply Current, 1.8 V	时钟分频 = 1 / Clock divider = 1	—	56（典型值 / Typ）	mA
SPI 电源电流 / SPI Supply Current	时钟分频 = 1 / Clock divider = 1	—	0.005（典型值 / Typ）	mA
数字驱动电源电流 / Digital Driver Supply Current	时钟分频 = 1 / Clock divider = 1	—	180（典型值 / Typ）	mA
功耗 / Power Consumption	—	≤2.50	2.16（典型值 / Typ）	W
关断功耗 / Power-Down Power	寄存器 0x08 = 0x81 / Register 0x08 = 0x81	—	1（典型值 / Typ）	mW
数据输出差分电压 / Data Output Differential Voltage	DDR LVDS 输出模式，100Ω 差分负载 / DDR LVDS output mode, 100Ω differential load	—	310~450	mV
数据输出共模电压 / Data Output Common-Mode Voltage	DDR LVDS 输出模式，100Ω 差分负载 / DDR LVDS output mode, 100Ω differential load	—	1.15~1.35	V
通道数 / Number of Channels	—	2	2	CH
信噪比 / SNR	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	≥68.0	73.6（典型值 / Typ）	dBFS
信噪比 / SNR	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	≥68.0	75.0（典型值 / Typ）	dBFS
信噪比 / SNR	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	≥66.0	72.1（典型值 / Typ）	dBFS
信噪比 / SNR	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	≥66.0	73.7（典型值 / Typ）	dBFS
信噪比 / SNR	VP-P = 2.5 V, fIN = 300 MHz, AIN = -1dBFS	68（典型值 / Typ）	70.7（典型值 / Typ）	dBFS
信噪比 / SNR	VP-P = 2.5 V, fIN = 400 MHz, AIN = -1dBFS	66.0（典型值 / Typ）	68（典型值 / Typ）	dBFS
信噪失真比 / SINAD	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	≥67.5	73.5（典型值 / Typ）	dBFS
信噪失真比 / SINAD	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	≥67.5	74.6（典型值 / Typ）	dBFS
信噪失真比 / SINAD	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	≥65.5	72.0（典型值 / Typ）	dBFS

参数 / Parameter	条件 / Conditions	SXA026	AD9652BBCZ-310	单位 / Unit
信噪失真比 / SINAD	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	⩾65.5	72.6（典型值 / Typ）	dBFS
信噪失真比 / SINAD	VP-P = 2.5 V, fIN = 300 MHz, AIN = -1dBFS	66（典型值 / Typ）	68.5（典型值 / Typ）	dBFS
信噪失真比 / SINAD	VP-P = 2.5 V, fIN = 400 MHz, AIN = -1dBFS	64（典型值 / Typ）	65.8（典型值 / Typ）	dBFS
有效位数 / ENOB	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	⩾10.9	12（典型值 / Typ）	Bits
有效位数 / ENOB	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	⩾10.9	12.1（典型值 / Typ）	Bits
有效位数 / ENOB	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	⩾10.6	11.7（典型值 / Typ）	Bits
有效位数 / ENOB	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	⩾10.6	11.8（典型值 / Typ）	Bits
有效位数 / ENOB	VP-P = 2.5 V, fIN = 300 MHz, AIN = -1dBFS	10.6（典型值 / Typ）	11.1（典型值 / Typ）	Bits
有效位数 / ENOB	VP-P = 2.5 V, fIN = 400 MHz, AIN = -1dBFS	10.3（典型值 / Typ）	10.6（典型值 / Typ）	Bits
无杂散动态范围 / SFDR	VP-P = 2 V, fIN = 70 MHz, AIN = -1dBFS	⩾77	90（典型值 / Typ）	dBFS
无杂散动态范围 / SFDR	VP-P = 2.5 V, fIN = 70 MHz, AIN = -1dBFS	⩾77	87（典型值 / Typ）	dBFS
无杂散动态范围 / SFDR	VP-P = 2 V, fIN = 170 MHz, AIN = -1dBFS	⩾75	84（典型值 / Typ）	dBFS
无杂散动态范围 / SFDR	VP-P = 2.5 V, fIN = 170 MHz, AIN = -1dBFS	⩾75	85（典型值 / Typ）	dBFS
无杂散动态范围 / SFDR	VP-P = 2.5 V, fIN = 300 MHz, AIN = -1dBFS	78（典型值 / Typ）	86（典型值 / Typ）	dBFS
无杂散动态范围 / SFDR	VP-P = 2.5 V, fIN = 400 MHz, AIN = -1dBFS	74（典型值 / Typ）	77（典型值 / Typ）	dBFS
逻辑输入高电平 / Logic Input High Level	—	—	1.2~AVDD_CLK	V
逻辑输入低电平 / Logic Input Low Level	—	—	GNDA~0.6	V
通道隔离度 / Channel Isolation	—	⩾80	90（典型值 / Typ）	dB
全功率带宽 / Full Power Bandwidth	—	—	485（典型值 / Typ）	MHz
输入时钟范围 / Input Clock Range	—	80~1240	80~1240	MHz
工作时钟 / Operating Clock	—	80~310	80~310	MHz

English: Package and dimensions: SXA026 — plastic BGA144, outline dimensions (L × W × H ⩽ 10.10 mm × 10.10 mm × 1.40 mm); AD9652 — plastic CSP_BGA (BC-144-6), outline dimensions (L × W × H ⩽ 10.10 mm × 10.10 mm × 1.40 mm). Substitution recommendation: □ Direct substitution □ Effective substitution ■ Functional substitution. Remarks (AD9652): None.

中文： 封装形式和尺寸：SXA026 为塑封 BGA144，外形尺寸（长 × 宽 × 高 ⩽10.10mm × 10.10mm × 1.40mm）；AD9652 为塑封 CSP_BGA（BC-144-6），外形尺寸（长 × 宽 × 高 ⩽10.10mm × 10.10mm × 1.40mm）。替代建议：□直接替代 □有效替代 ■功能替代。备注（国外产品）：无。

English: The SXA026 operates over a temperature range of -40°C to +85°C, and its electrical specifications are given as limit values, whereas the imported device operates over -40°C to +85°C with specifications given as typical values; the specifications of this device are therefore somewhat relaxed relative to the imported device. The SXA026 and the imported product AD9652BBCZ-310 have compatible package outlines and port definitions and can be interchanged in the socket.

中文： SXA026 产品工作温度范围为 -40°C~85°C，电参数指标为极限值，而进口器件工作温度范围为 -40°C~85°C 且参数指标为典型值，因而国产器件指标相对进口器件有一定放宽。SXA026 和进口产品 AD9652BBCZ-310 封装形式、端口定义兼容，可进行插拔替换。