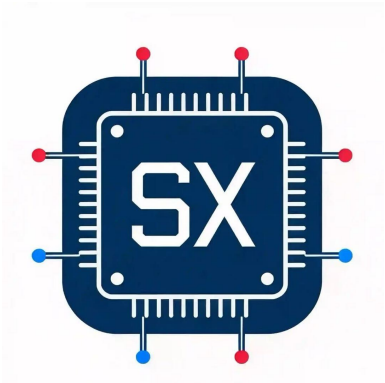


SXA030

8-Channel 24-Bit, 16 kSPS A/D Converter

八通道 24 位 16kSPS A/D 转换器

24-bit | 8 channels | 16 kSPS | QFN64 | Serial CMOS (SPI)
24 位 | 八通道 | 16kSPS | QFN64 | 串行 CMOS（SPI）

对标 / Cross Reference: AD7779 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

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SXA030 8-Channel 24-Bit 16KSPS A/D Converter — Product Manual (Bilingual)

SXA030 型 8 通道 24 位 16KSPS A/D 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深信科技 **V1.20260811**

对标 / Cross Reference: AD7779 — pin-to-pin compatible alternative

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版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V.120260811	2026.8.11	/	首次发布 / Initial release	

产品用途及应用范围 / Applications and Scope

English: Precision measurement instruments; industrial automation and process control; medical electronics; high-precision audio monitoring; seismic data monitoring.

中文： 精密测量仪器；工业自动化及过程控制；医疗电子；高精度音频监测；地震数据监测。

标准 / Standards

English: Quality grade: enterprise standard.

中文： 质量等级：企标级。

产品特点 / Features

English: - Analog supply voltage: 3.3V - Digital supply voltage: 3.3V - Maximum sampling rate: 16KSPS - Signal-to-noise ratio (SNR): ≥100dB @ Fin=60Hz, -0.5dBFS, high-resolution mode (typical 105dB) - Spurious-free dynamic range (SFDR): ≥90dB @ Fin=60Hz, -0.5dBFS, high-resolution mode (typical 113dB) - Integral nonlinearity error (INL): ±150ppm of FSR - Power consumption: ≤500mW (typical 285mW) - Analog input range: ±VREF/PGAGAIN - Circuit interface: CMOS - ESD rating: Class 1C, HBM model, 1000V - Product weight: 0.22g±0.04g - Moisture sensitivity level and package: MSL3, QFN64

中文： - 模拟电源电压：3.3V - 数字电源电压：3.3V - 最高采样率：16KSPS - 信噪比：≥100dB@Fin=60Hz，-0.5dBFS，高分辨率（典型值 105dB） - 无杂散动态范围：≥90dB@Fin=60Hz，-0.5dBFS，高分辨率（典型值 113dB） - 积分线性误差：±150ppm of FSR - 功耗：≤500mW(典型值 285 mW) - 模拟输入范围：±VREF/PGAGAIN - 电路接口：CMOS - ESD 等级：1C，HBM，1000V - 重量：0.22g±0.04g - 湿敏等级和封装形式：MSL3，QFN64

产品描述 / Product Description

English: The SXA030 8-channel 24-bit 16KSPS A/D converter is a monolithic integrated circuit manufactured in a CMOS process. The product uses a sigma-delta (Σ-Δ) architecture, and the circuit internally includes a programmable gain amplifier (PGA), a Σ-Δ ADC, reference generation circuitry, clock circuitry, and a digital filter.

The circuit uses a 64-pin quad flat no-lead package, package code QFN64, with outline dimensions of 9.0mm (L) × 9.0mm (W) × 0.75mm (H).

The functional block diagram of this product is shown in Figure 1.

中文： SXA030 型 8 通道 24 位 16KSPS A/D 转换器是采用 CMOS 工艺制造的单片集成电路。该产品采用 sigma-delta（Σ-Δ）结构，电路内部包含可编程增益放大器（PGA）、Σ-Δ 型 ADC、基准产生电路、时钟电路和数字滤波器等电路。

该电路采用 64 引脚的四边扁平无引线封装，外壳代号 QFN64，外形尺寸为长 9.0mm×宽 9.0mm×高 0.75mm。

该产品功能框图如图 1 所示。

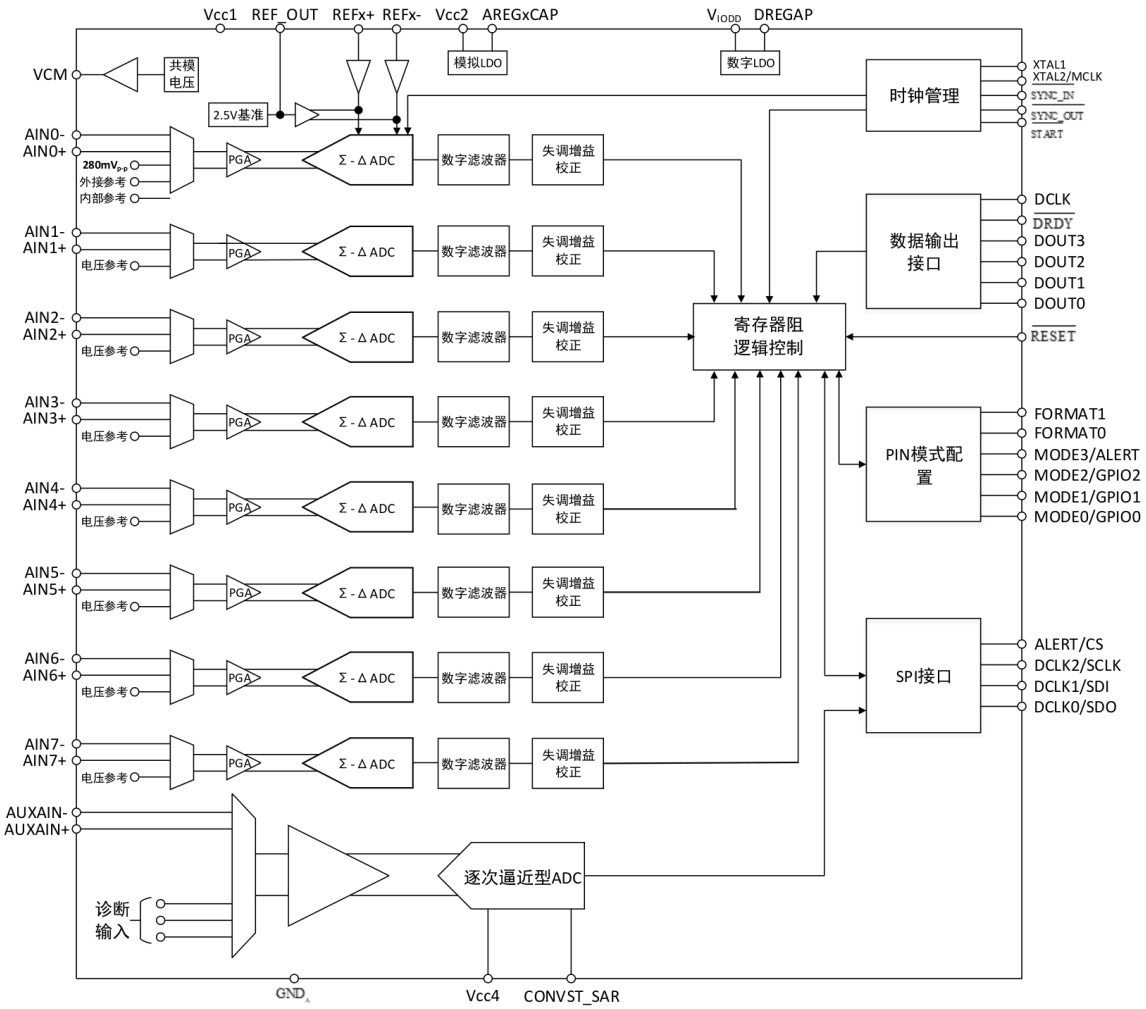


图1 功能框图

Figure 1: Functional block diagram

English: The DOUTx operating timing of this product is as follows:

中文： 该产品 DOUTx 工作时序如下：

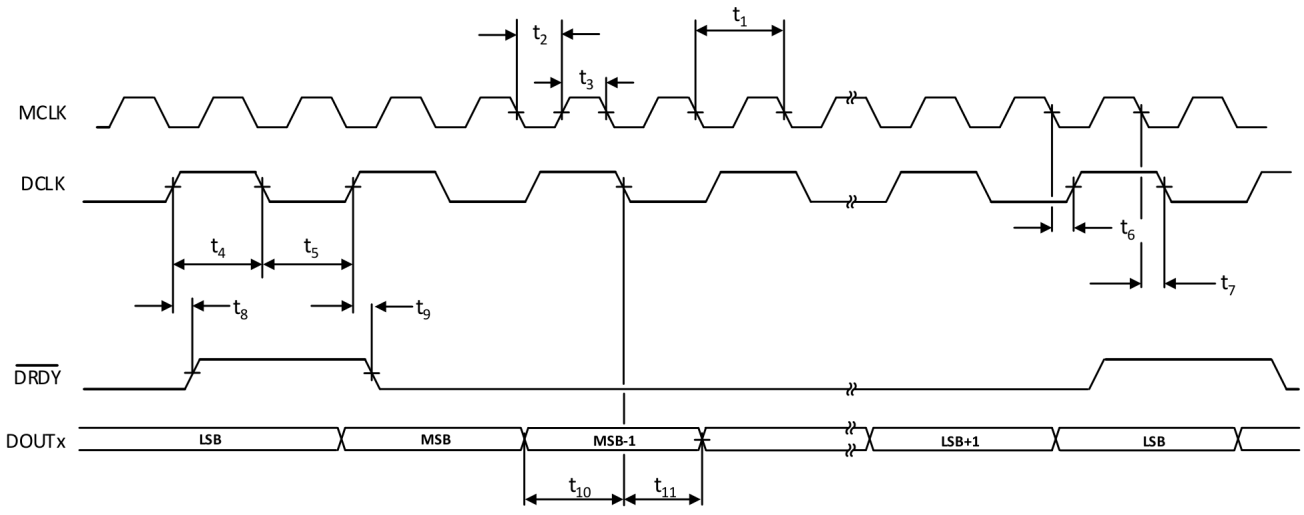


Figure 2: DOUTx operating timing diagram

表1 SPI 时序特性 / Table 1. SPI Timing Characteristics

描述 / Description	参数 / Parameter	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
MCLK 周期 / MCLK period	t1	1/8.192	--	1/0.655	μs
MCLK 低电平时间 / MCLK low time	t2	60	--	--	ns
MCLK 高电平时间 / MCLK high time	t3	60	--	--	ns
DCLK 低电平时间 / DCLK low time	t4	121	--	--	ns
DCLK 高电平时间 / DCLK high time	t5	121	--	--	ns
MCLK 下降沿到 DCLK 上升沿 / MCLK falling edge to DCLK rising edge	t6	--	--	45	ns
MCLK 下降沿到 DCLK 下降沿 / MCLK falling edge to DCLK falling edge	t7	--	--	45	ns
DCLK 上升沿到 DRDY 上升沿 / DCLK rising edge to DRDY rising edge	t8	2	--	--	ns
DCLK 上升沿到 DRDY 下降沿 / DCLK rising edge to DRDY falling edge	t9	1	--	--	ns
DOUTx 建立时间 / DOUTx setup time	t10	20	--	--	ns
DOUTx 保持时间 / DOUTx hold time	t11	20	--	--	ns

产品外形图和实物图片 / Package Outline and Product Photos

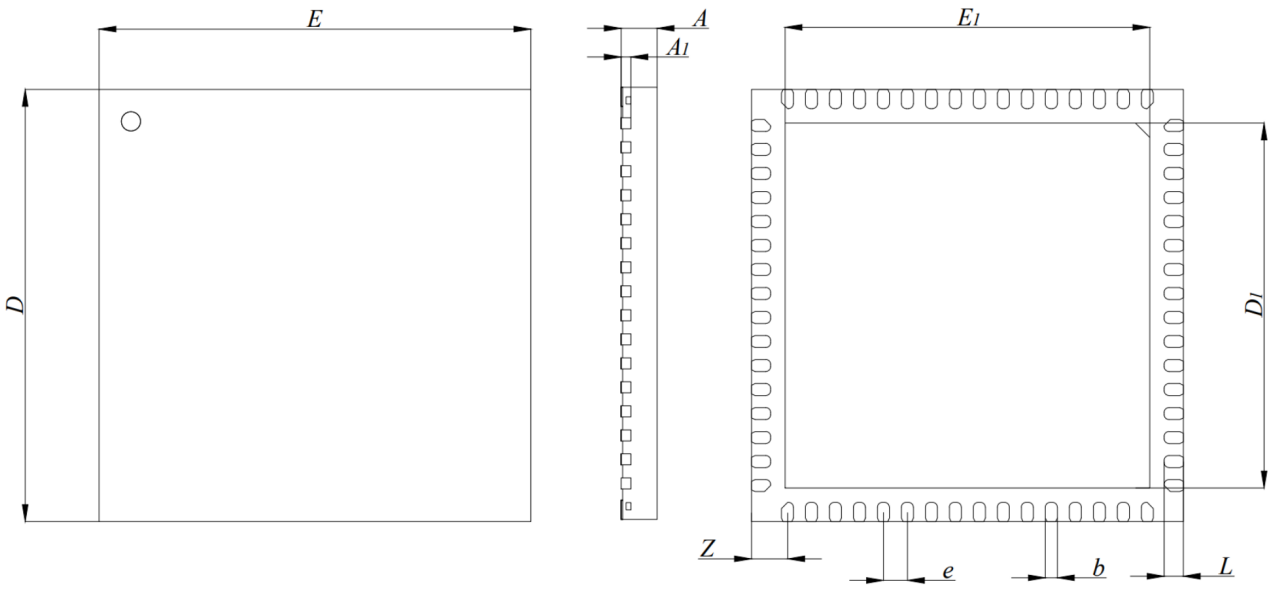


Figure 3: Package outline dimensions

单位为毫米 / Units in mm

尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max	尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max
A	0.60	0.75[a]	0.90	D	8.80	9.00[a]	9.20
A1	—	0.20[a]	—	E	8.80	9.00[a]	9.20
b	0.20	0.25[a]	0.30	D1	7.40	7.60[a]	7.80
e	—	0.50	—	E1	7.40	7.60[a]	7.80
L	0.30	0.40[a]	0.50	Z	—	0.75[a]	0.85

[a] 外壳实际公称值，推荐用户参考该尺寸设计使用；/ Actual nominal package values; users are advised to design with reference to these dimensions.

注：推荐焊盘设计详见电装说明。/ Note: see the assembly instructions for recommended pad layout.

引出端排列（俯视图）/ Pin Arrangement (Top View)

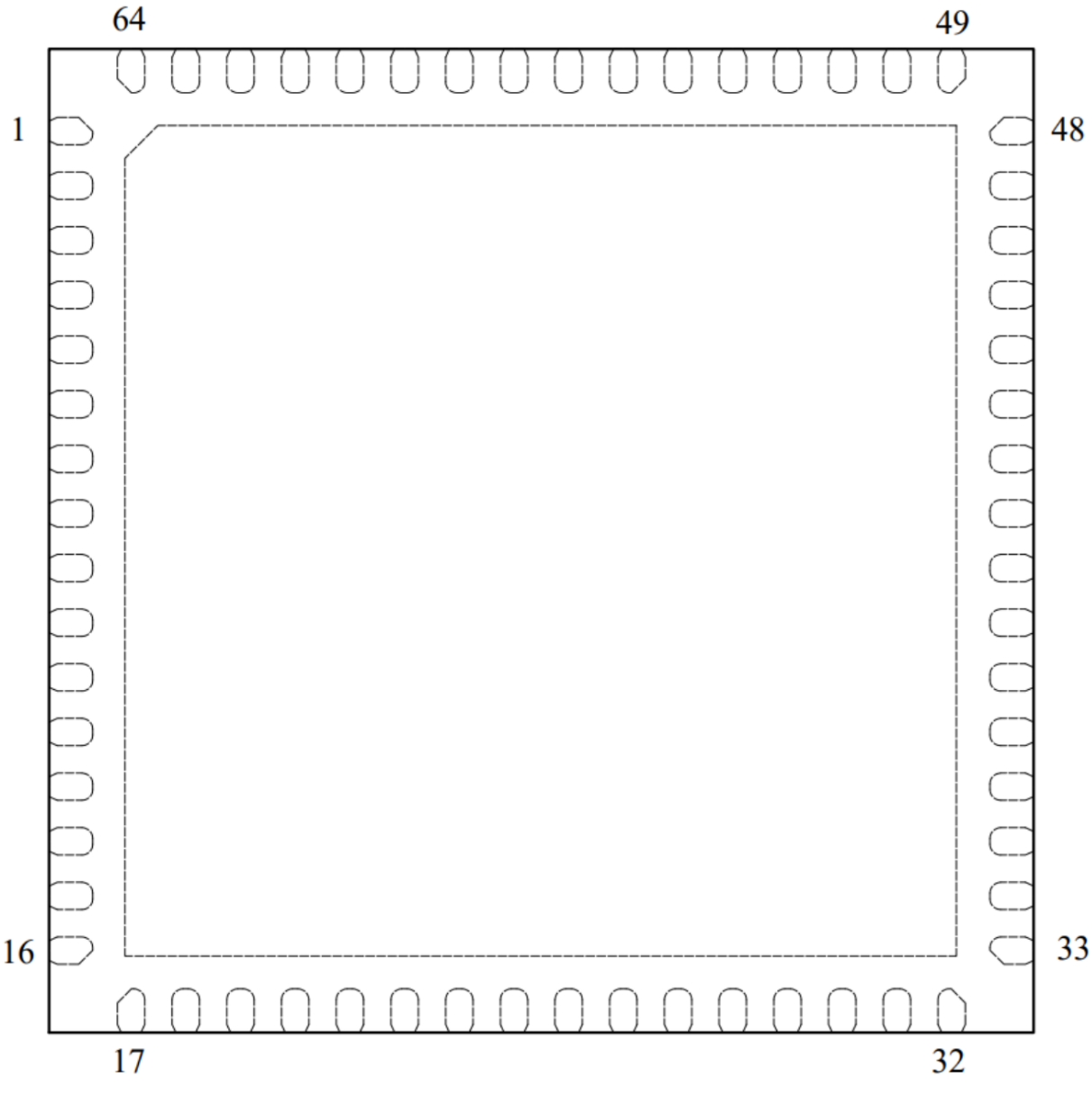


Figure 4: Pin arrangement (top view)

引出端功能符号表 / Pin Function Table

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
1	AIN0-	模拟输入通道 0（负端）/ Analog input channel 0 (negative)	I	33	START	同步脉冲 / Synchronization pulse	I
2	AIN0+	模拟输入通道 0（正端）/ Analog input channel 0 (positive)	I	34	SYNC_OUT	同步信号 / Synchronization signal	O

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
3	AIN1-	模拟输入通道 1（负端）/ Analog input channel 1 (negative)	I	35	SYNC_IN	内部数字模块与多器件同步 / Internal digital module and multi-device synchronization	I
4	AIN1+	模拟输入通道 1（正端）/ Analog input channel 1 (positive)	I	36*	RESET	异步复位信号 / Asynchronous reset signal	I
5	GNDA	模拟地 / Analog ground	/	37	AIN7+	模拟输入通道 7（正端）/ Analog input channel 7 (positive)	I
6	VCC1	模拟电源 1 / Analog supply 1	/	38	AIN7-	模拟输入通道 7（负端）/ Analog input channel 7 (negative)	I
7	REF1-	通道 0 至通道 3 的负基准电压输入 1 / Negative reference voltage input 1 for channels 0 to 3	I	39	AIN6+	模拟输入通道 7（正端） / Analog input channel 7 (positive)	I
8	REF1+	通道 0 至通道 3 的正基准电压输入 1 / Positive reference voltage input 1 for channels 0 to 3	I	40	AIN6-	模拟输入通道 7（负端） / Analog input channel 7 (negative)	I
9	AIN2-	模拟输入通道 2（负端）/ Analog input channel 2 (negative)	I	41	REF2+	通道 4 至通道 7 的正基准电压输入 2 / Positive reference voltage input 2 for channels 4 to 7	I
10	AIN2+	模拟输入通道 2（正端）/ Analog input channel 2 (positive)	I	42	REF2-	通道 4 至通道 7 的负基准电压输入 2 / Negative reference voltage input 2 for channels 4 to 7	I
11	AIN3-	模拟输入通道 3（负端）/ Analog input channel 3 (negative)	I	43	VCC1	模拟电源 1 / Analog supply 1	/
12	AIN3+	模拟输入通道 3（正端）/ Analog input channel 3 (positive)	I	44	GNDA	模拟地 / Analog ground	/
13	MODE0	模式 0 输入引脚 / Mode 0 input pin	I	45	AIN5+	模拟输入通道 5（正端）/ Analog input channel 5 (positive)	I
14	MODE1	模式 1 输入引脚 / Mode 1 input pin	I	46	AIN5-	模拟输入通道 5（负端）/ Analog input channel 5 (negative)	I
15	MODE2	模式 2 输入引脚 / Mode 2 input pin	I	47	AIN4+	模拟输入通道 4（正端）/ Analog input channel 4 (positive)	I
16	MODE3	模式 3 输入引脚 / Mode 3 input pin	I	48	AIN4-	模拟输入通道 4（负端）/ Analog input channel 4 (negative)	I
17	CONVST_SAR	SAR 转换的启动信号 / SAR conversion start signal	I	49	REF_OUT	基准电压输出 / Reference voltage output	O
18	ALERT/CS	报警信号/SPI 片选信号 / Alert signal / SPI chip-select signal	I	50	GNDA	模拟地 / Analog ground	/
19	DCLK2/SCLK	频率选择信号 2/SPI 时钟信号 / Frequency select signal 2 / SPI clock signal	I	51	AREG2CAP	模拟 LDO 输出 2 / Analog LDO output 2	O
20	DCLK1/SDI	频率选择信号 1/SPI 数据输入 / Frequency select signal 1 / SPI data input	I	52	VCC2	模拟电源 2 / Analog supply 2	/

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
21	DCLK0/SDO	频率选择信号 0/SPI 数据输出 / Frequency select signal 0 / SPI data output	O	53	GNDA	模拟地 / Analog ground	/
22	GNDD	数字地 / Digital ground	/	54	FORMAT1	输出数据帧 1 / Output data frame 1	I
23	DREGCAP	数字 LDO 输出 / Digital LDO output	O	55	FORMAT0	输出数据帧 1 / Output data frame 1	I
24	VIODD	IO 电源/数字 LDO 电源 / I/O supply / digital LDO supply	/	56	CLK_SEL	时钟选择信号引脚 / Clock select signal pin	I
25	DOUT3	数据输出引脚 3 / Data output pin 3	I/O	57	VCM	共模电压输出 / Common-mode voltage output	O
26	DOUT2	数据输出引脚 2 / Data output pin 2	I/O	58	VCC2	模拟电源 2 / Analog supply 2	/
27	DOUT1	数据输出引脚 1 / Data output pin 1	O	59	AREG1CAP	模拟 LDO 输出 1 / Analog LDO output 1	O
28	DOUT0	数据输出引脚 0 / Data output pin 0	O	60	GNDA	模拟地 / Analog ground	/
29	DCLK	数据输出时钟 / Data output clock	O	61	GNDA	模拟地 / Analog ground	/
30	DRDY	数据输出就绪引脚 / Data output ready pin	O	62	VCC4	模拟电源 4 / Analog supply 4	/
31	XTAL1	晶振 1 输入连接 / Crystal 1 input connection	I	63	AUXAIN+	SAR 模拟输入（正端）/ SAR analog input (positive)	I
32	XTAL1/MCLK	晶振 2 输入连接/CMOS 时钟输入（MCLK）/ Crystal 2 input connection / CMOS clock input (MCLK)	I	64	AUXAIN-	SAR 模拟输入（负端）/ SAR analog input (negative)	I

*此引脚可将所有寄存器复位至默认值。由于电源的慢速压摆率可能在数字模块中生成不正确的初始化状态，建议器件上电后在此引脚上生成一个脉冲。/ *This pin can reset all registers to their default values. Because a slow supply slew rate may generate an incorrect initialization state in the digital module, it is recommended to generate a pulse on this pin after device power-up.

推荐工作条件 / Recommended Operating Conditions

English: - VCC1 to GNDA: 3.0V~3.6V - VCC2 to GNDA: 3.0V~3.6V - VCC4 to GNDA: VCC1-0.3 ~ VCC1 - GNDA to GNDD: -1.8V~0V - VIODD to GNDD: 1.8V~3.6V - Operating temperature (TA): -40°C~125°C

中文： - VCC1 to GNDA：3.0V~3.6V - VCC2 to GNDA：3.0V~3.6V - VCC4 to GNDA：VCC1-0.3 ~ VCC1 - GNDA to GNDD：-1.8V~0V - VIODD to GNDD：1.8V~3.6V - 工作温度（TA）：-40°C~125°C

绝对最大额定值 / Absolute Maximum Ratings

English: - Any supply voltage to GNDA: -0.3V~3.96V - GNDA to GNDD: -1.98V~0.3V - AREGxCAP to GNDA: -0.3V~1.98V - DREGCAP to GNDD: -0.3V~1.98V - VIODD to GNDD: -0.3V~3.96V - VIODD to GNDA: -0.3V~5.94V - VCC4 to GNDA: VCC1-0.3V~3.96V - Storage temperature (TA): -65°C~150°C

Note: see the cross-reference notes vs. the foreign product in the Additional Notes.

中文： - 任何电源电压 to GNDA：-0.3V~3.96V - GNDA to GNDD：-1.98V~0.3V - AREGxCAP to GNDA：-0.3V~1.98V - DREGCAP to GNDD：-0.3V~1.98V - VIODD to GNDD：-0.3V~3.96V - VIODD to GNDA：-0.3V~5.94V - VCC4 to GNDA：VCC1-0.3V~3.96V - 贮存温度（TA）：-65°C~150°C

注：请查看附件说明中替代国外产品情况说明。

性能指标 / Performance Specifications

Conditions / 条件（除另有规定外 / unless otherwise specified）: VCC1 = VCC2 = VCC4 = 3.3V, VIODD = 3.3V, GNDA = GNDD = 0V, MCLK = 8192KHz, -40°C≤TA≤125°C.

特性 / Parameter	符号 / Symbol	条件 / Conditions	极限值 / Limits — 最小 / Min	极限值 / Limits — 典型 / Typ	极限值 / Limits — 最大 / Max	单位 / Unit
通道数 / Number of channels	L	TA=25°C		8		通道 / channels
输出数据率 / Output data rate	ODR	TA=25°C	--	--	16	KSPS
信噪比 / SNR	SNR	PGA=1，fIN=60Hz	100	105	--	dB
信噪比 / SNR	SNR	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	95	100	--	dB
信噪失真比 / SINAD	SINAD	PGA=1，fIN=60Hz	95	103	--	dB
信噪失真比 / SINAD	SINAD	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	93	99	--	dB
总谐波失真 / Total harmonic distortion	THD	PGA=1，fIN=60Hz	--	-110	-100	dB
总谐波失真 / Total harmonic distortion	THD	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	--	-106	-98	dB
无杂散动态范围 / SFDR	SFDR	PGA=1，fIN=60Hz	90	113	--	dB
无杂散动态范围 / SFDR	SFDR	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	90	108	--	dB
积分非线性 / Integral nonlinearity	INL	TA=25°C	-15	±5	15	ppm
	INL	TA=-55°C、125°C	-150	--	150	ppm

特性 / Parameter	符号 / Symbol	条件 / Conditions	极限值 / Limits — 最小 / Min	极限值 / Limits — 典型 / Typ	极限值 / Limits — 最大 / Max	单位 / Unit
积分非线性 / Integral nonlinearity						
失调误差 / Offset error	EO	TA=25℃	-150	±90	150	uV
失调误差 / Offset error	EO	TA=-55℃、125℃	-300	--	300	uV
增益误差 / Gain error	EG	TA=25℃	-0.5	±0.2	0.5	%FS
增益误差 / Gain error	EG	TA=-55℃、125℃	-1	--	1	%FS
基准电压 / Reference voltage	VREF	TA=25℃	2.45	2.5	2.55	V
逻辑输出高电平电压 / Logic output high voltage	VOH		2.6	--	--	V
逻辑输出低电平电压 / Logic output low voltage	VOL		--	--	0.4	V
逻辑输入高电平电压 / Logic input high voltage	VIH		2.4	--	--	V
逻辑输入低电平电压 / Logic input low voltage	VIL		--	--	0.4	V
功耗 / Power consumption	PW	8 通道 / 8 channels	--	285	500	mW
信噪比（SAR ADC）/ SNR (SAR ADC)	SNRSAR	TA=25℃	60	63	--	dBFS

注：典型值为常温测试数据。/ Note: typical values are room-temperature test data.

主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

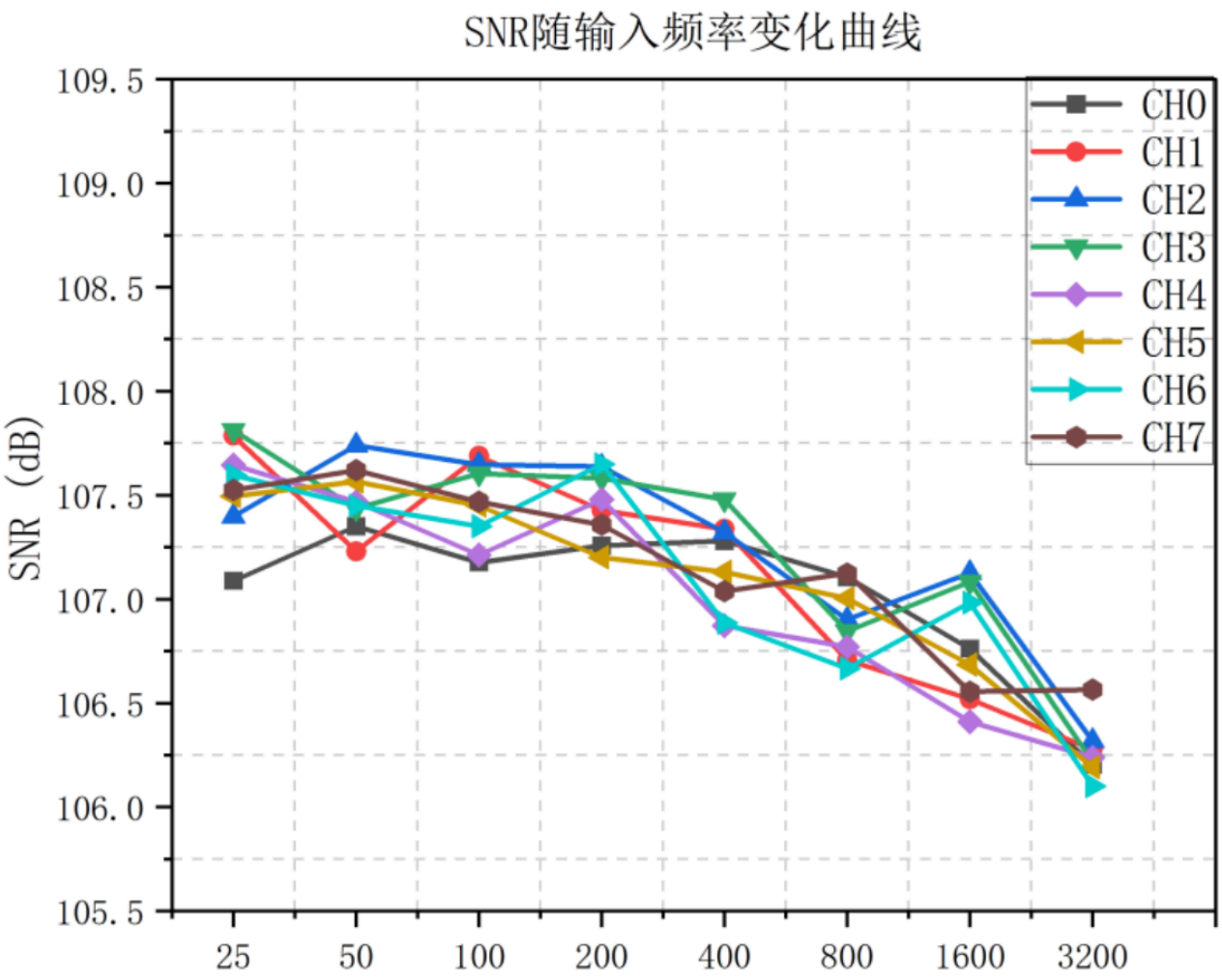


Figure 5: SNR vs. input frequency, ODR=16KSPS, -0.5dBFS, TA=25°C

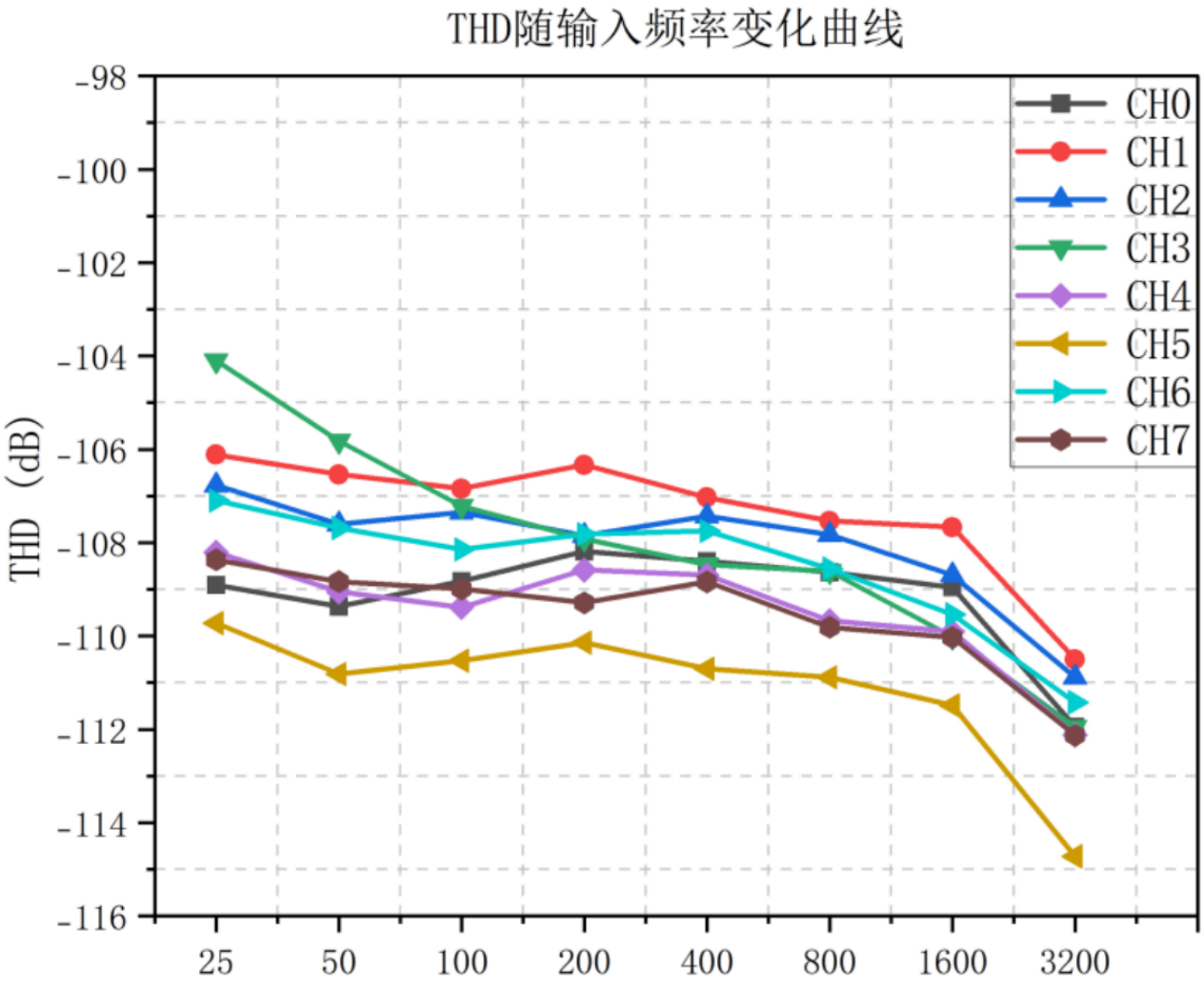


Figure 6: THD vs. input frequency, ODR=16KSPS, -0.5dBFS, TA=25°C

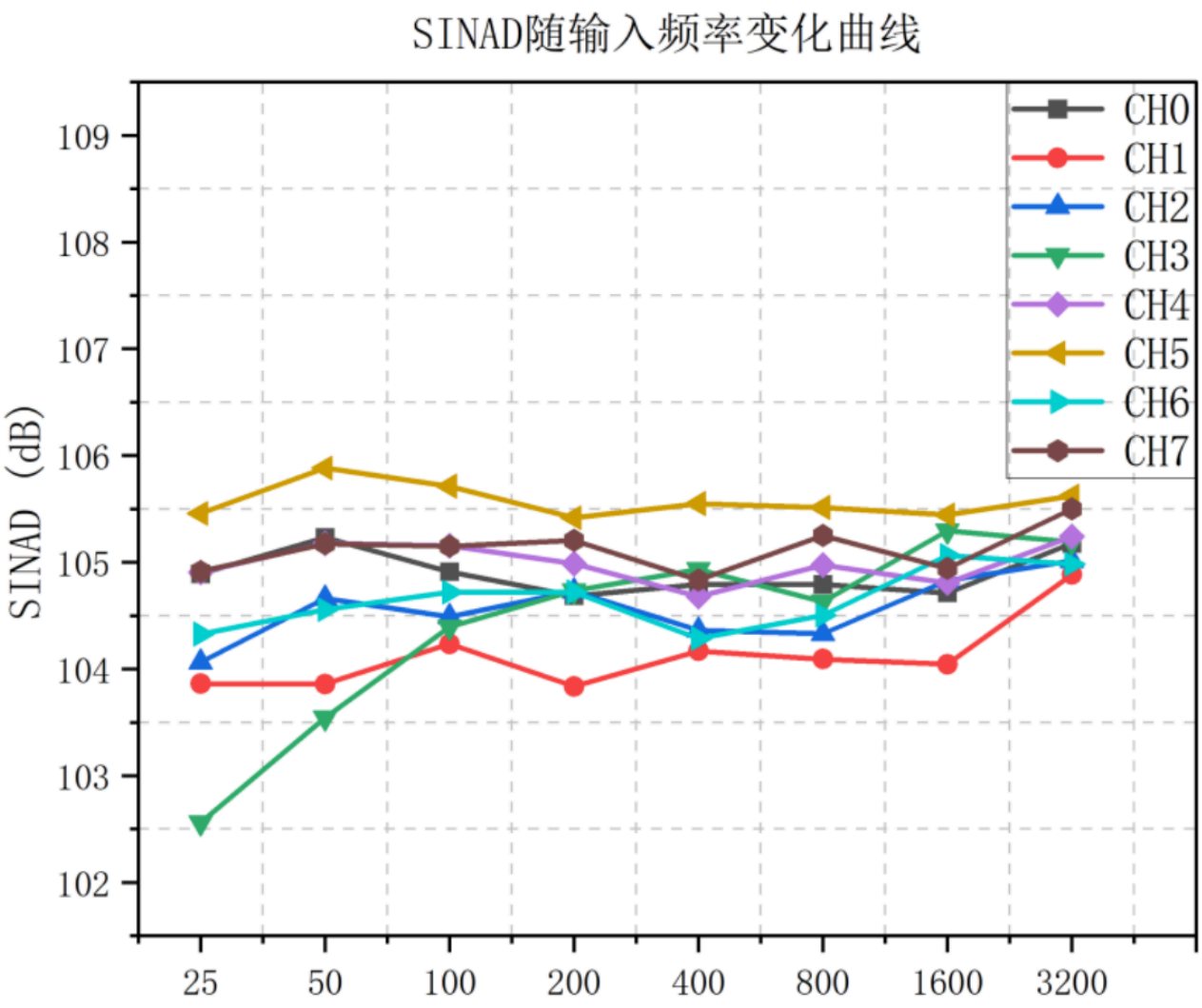


Figure 7: SINAD vs. input frequency, ODR=16KSPS, -0.5dBFS, TA=25°C

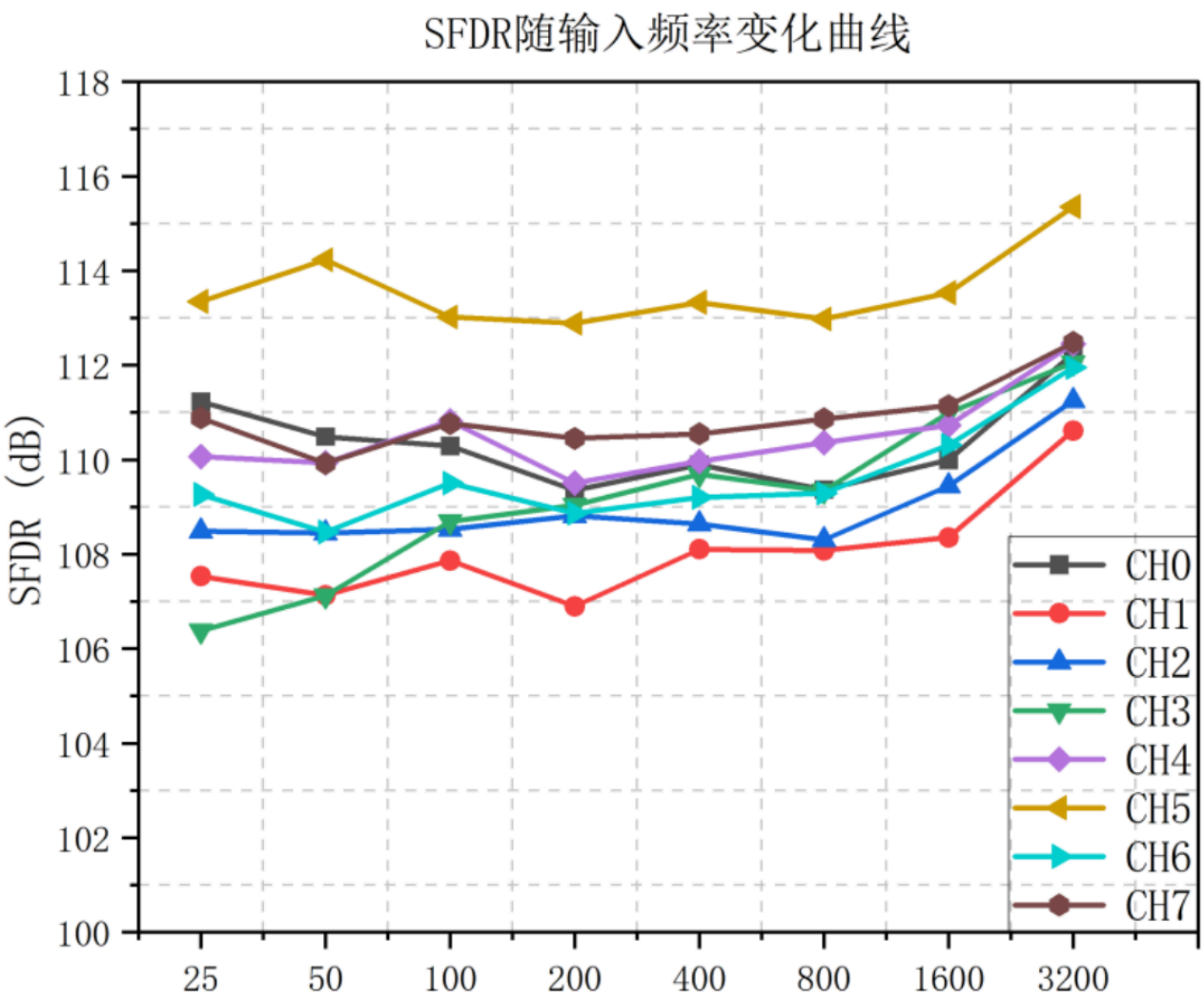


Figure 8: SFDR vs. input frequency, ODR=16KSPS, -0.5dBFS, TA=25°C

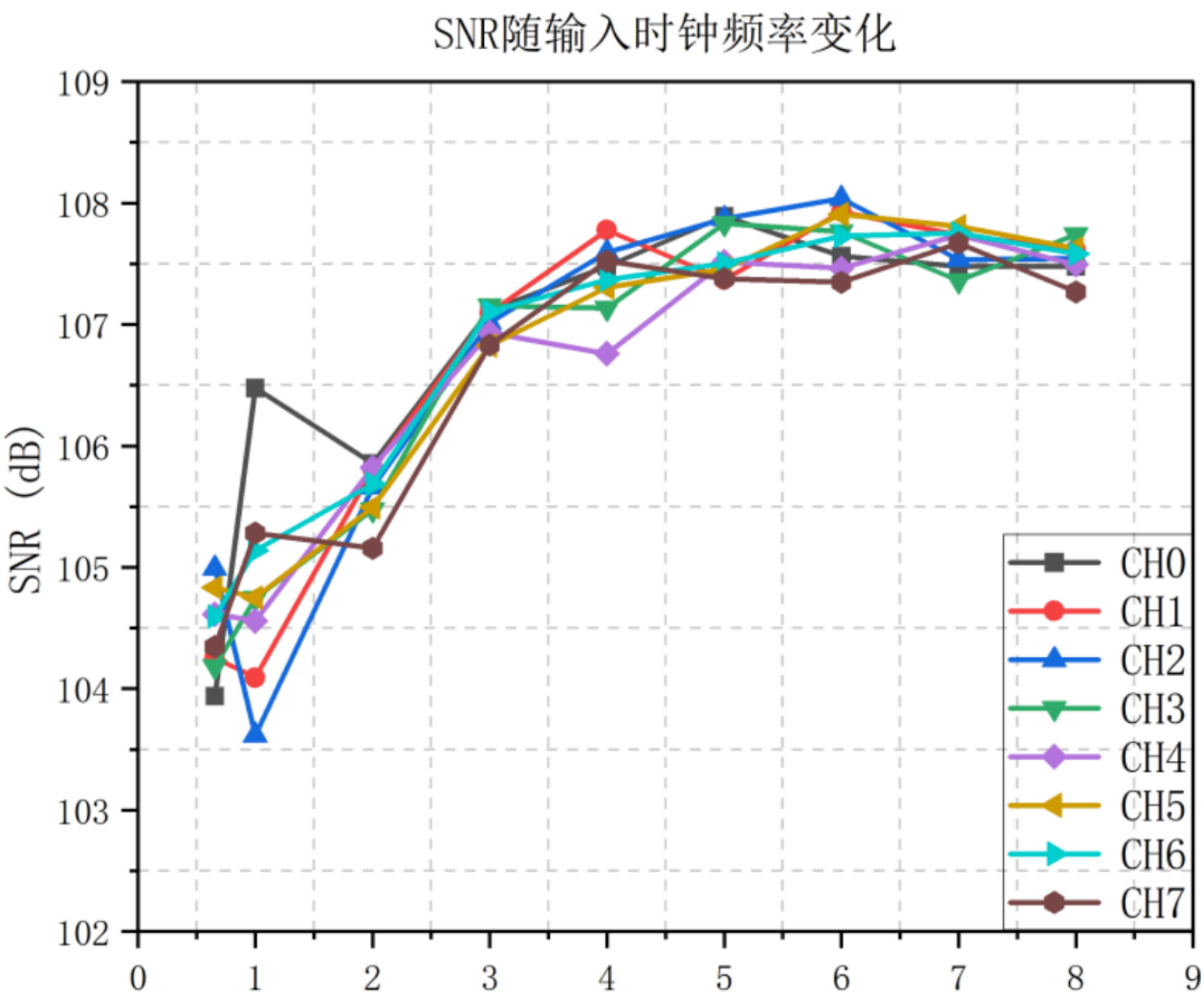


Figure 9: SNR vs. input clock frequency, Fin=1KHz, -0.5dBFS, TA=25°C

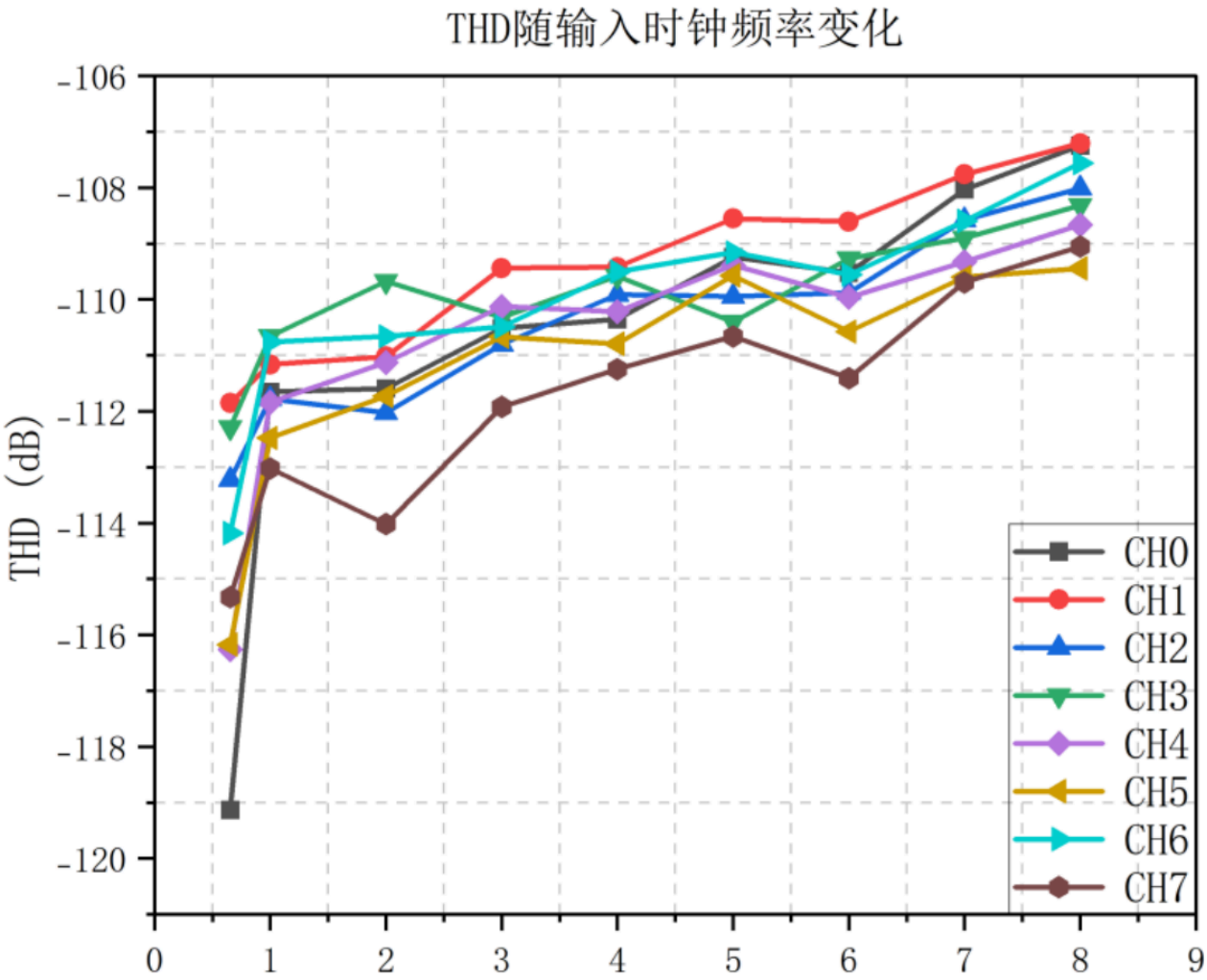


Figure 10: THD vs. input clock frequency, Fin=1KHz, -0.5dBFS, TA=25°C

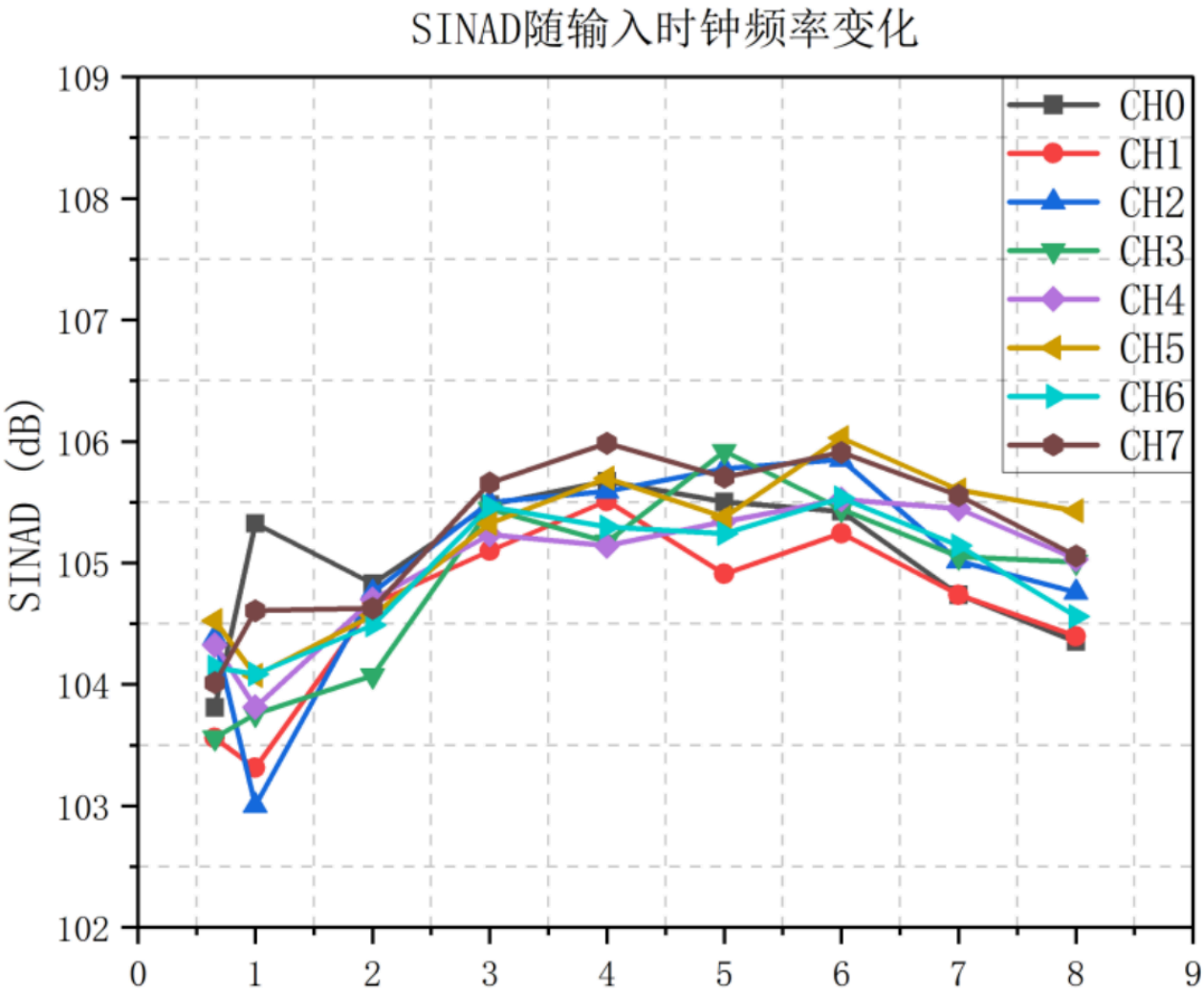


Figure 11: SINAD vs. input clock frequency, Fin=1KHz, -0.5dBFS, TA=25°C

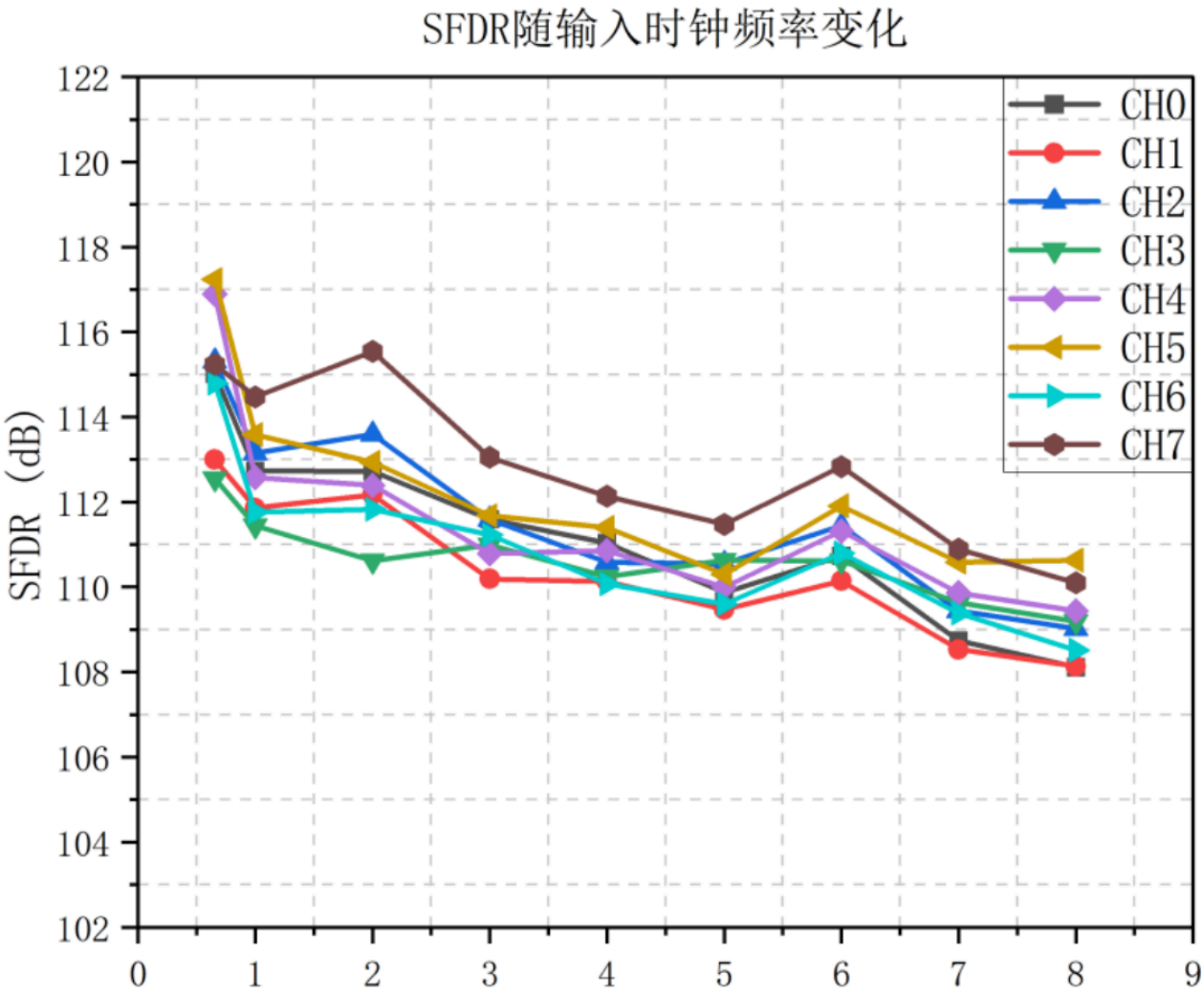


Figure 12: SFDR vs. input clock frequency, Fin=1KHz, -0.5dBFS, TA=25°C

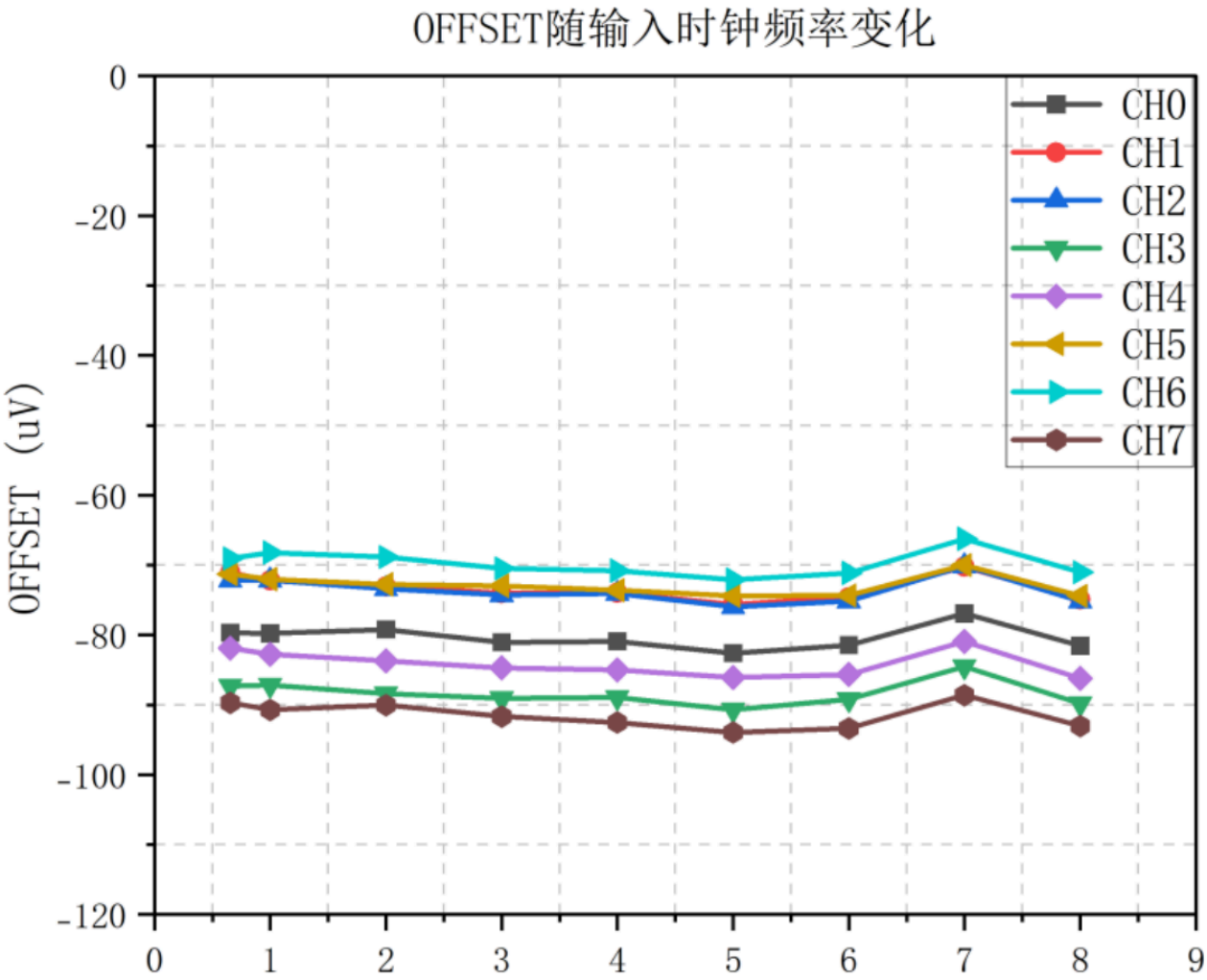


Figure 13: OFFSET vs. input clock frequency, TA=25°C

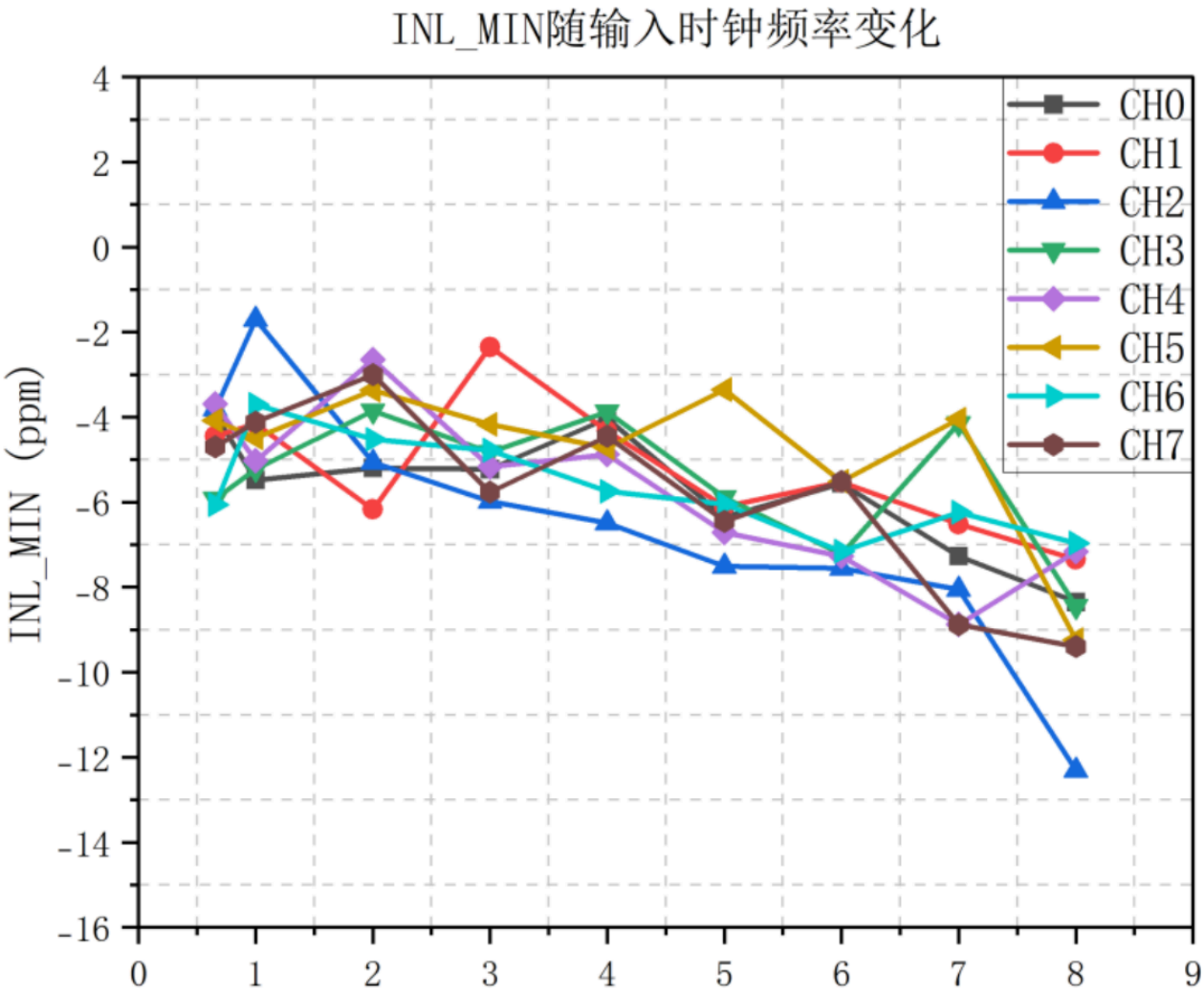


Figure 14: INL_MIN vs. input clock frequency, TA=25℃

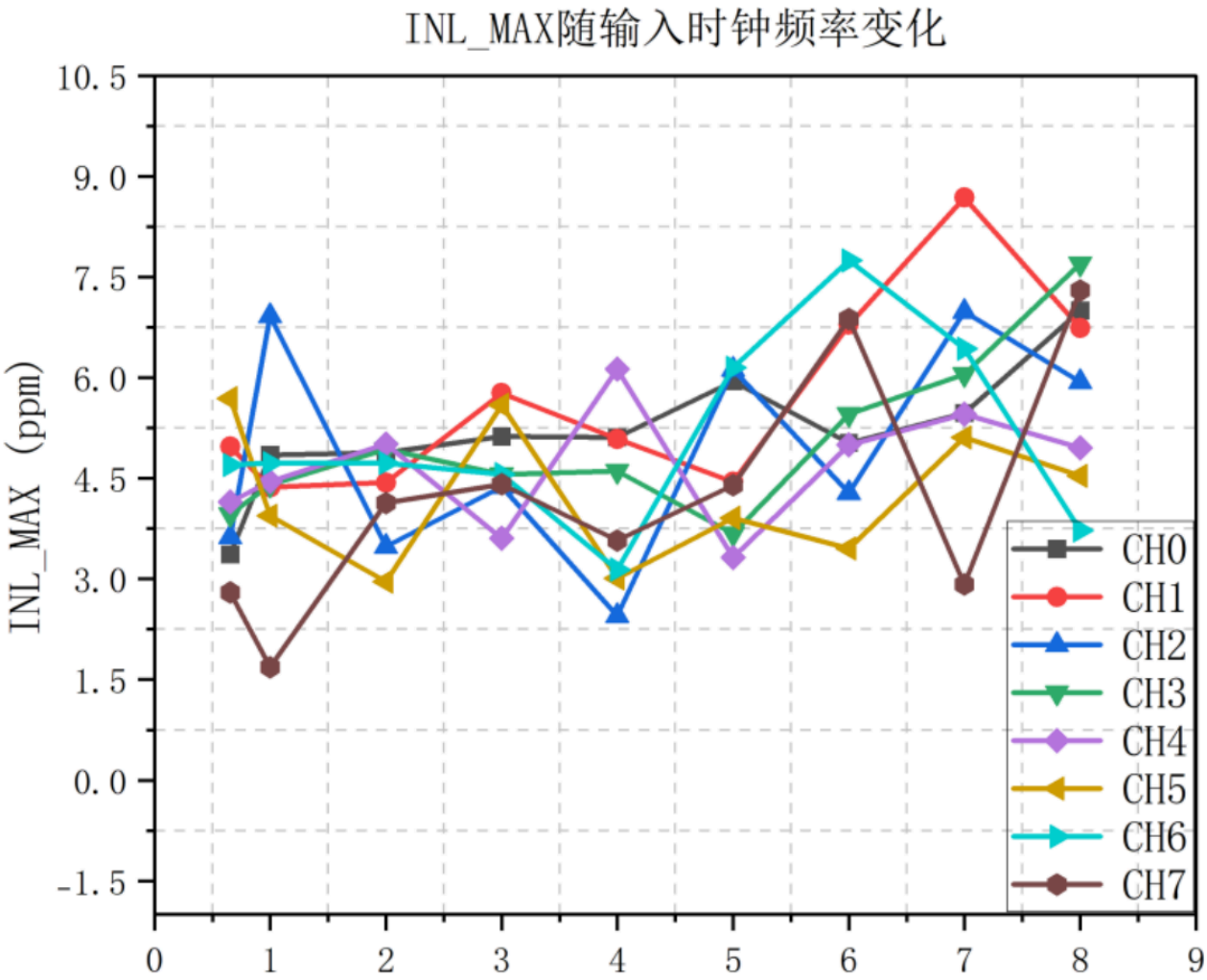


Figure 15: INL_MAX vs. input clock frequency, TA=25°C

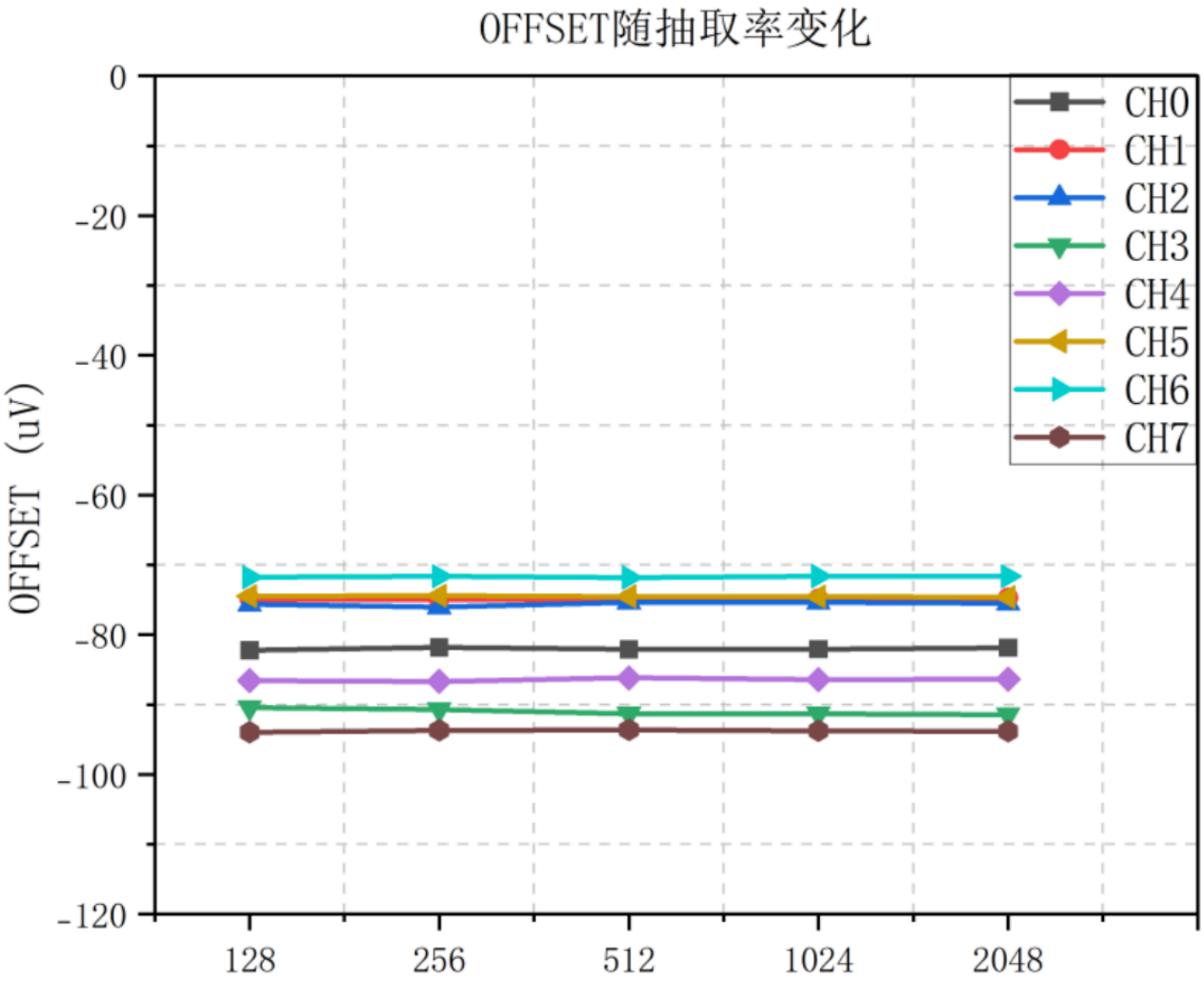


Figure 16: OFFSET vs. decimation rate, TA=25°C

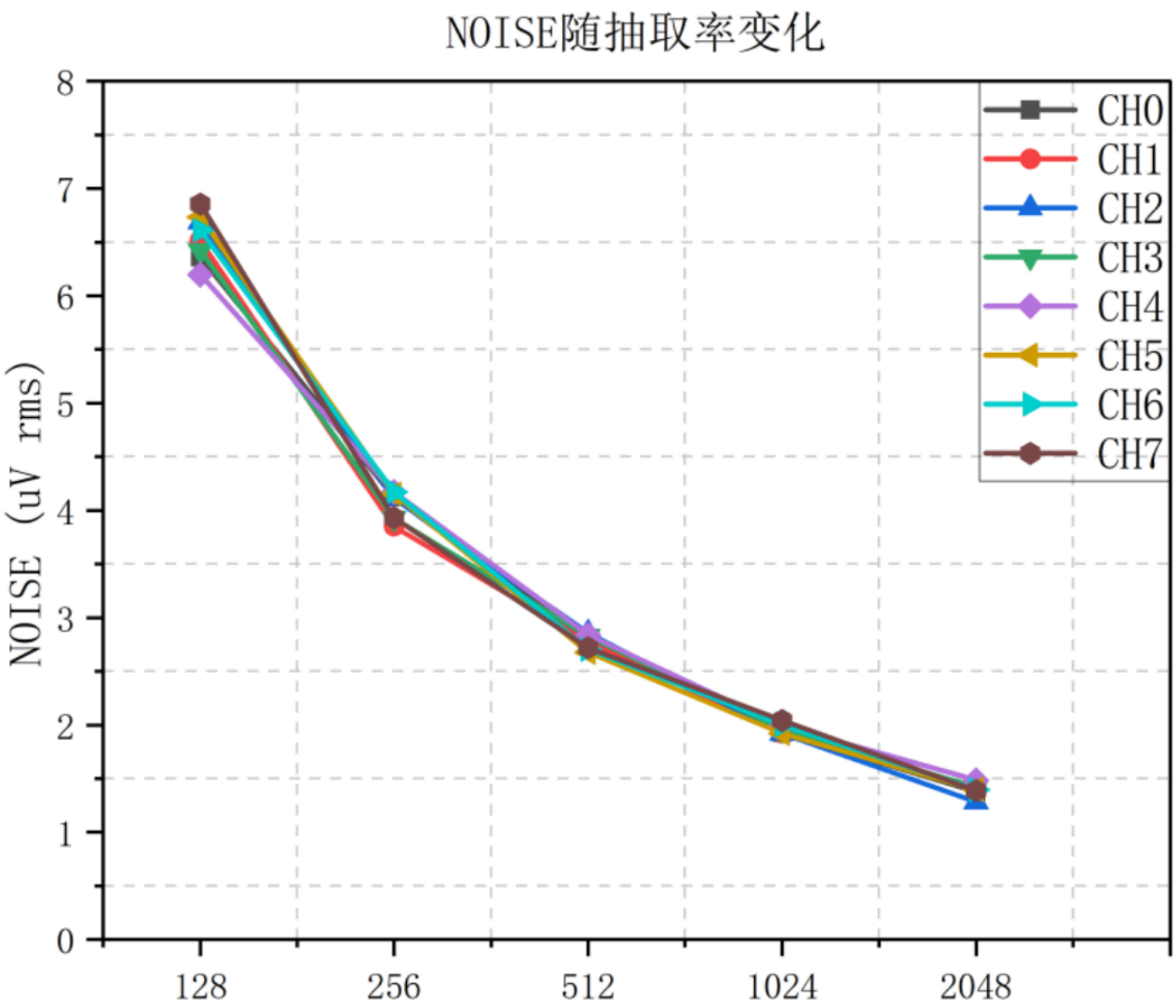


Figure 17: NOISE vs. decimation rate, TA=25°C

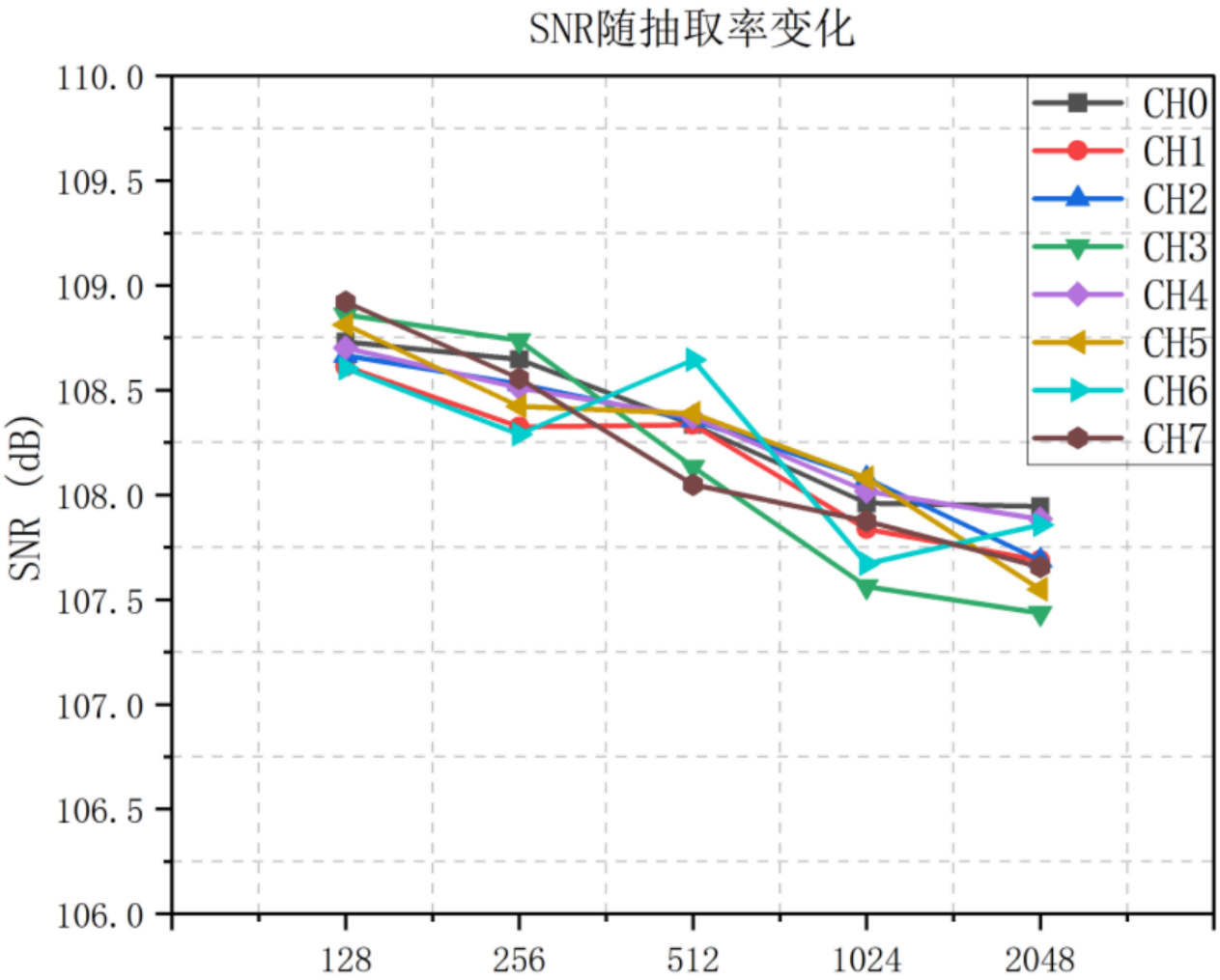


Figure 18: SNR vs. decimation rate, Fin=1KHz, -0.5dBFS, TA=25°C

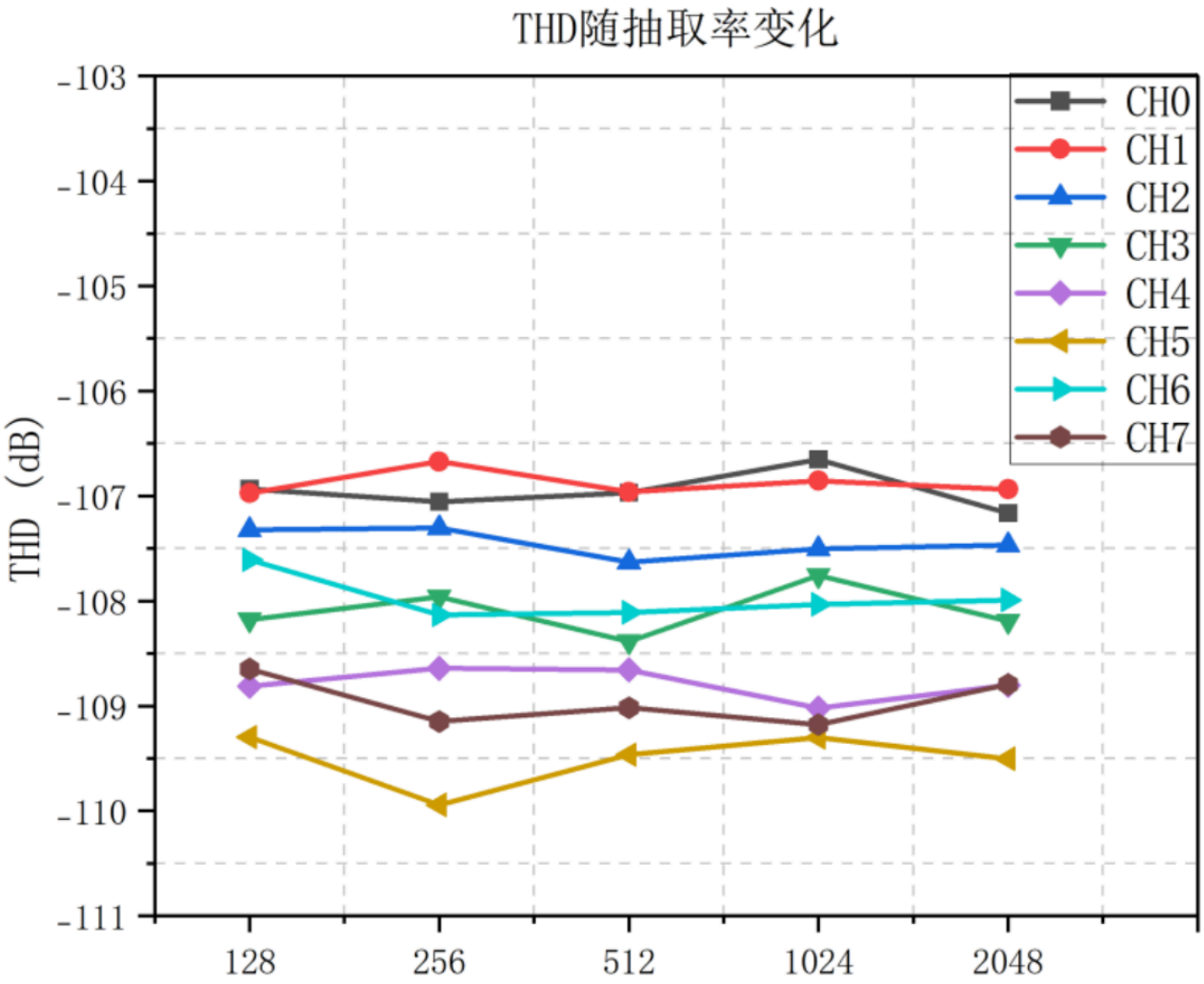


Figure 19: THD vs. decimation rate, Fin=1KHz, -0.5dBFS, TA=25℃

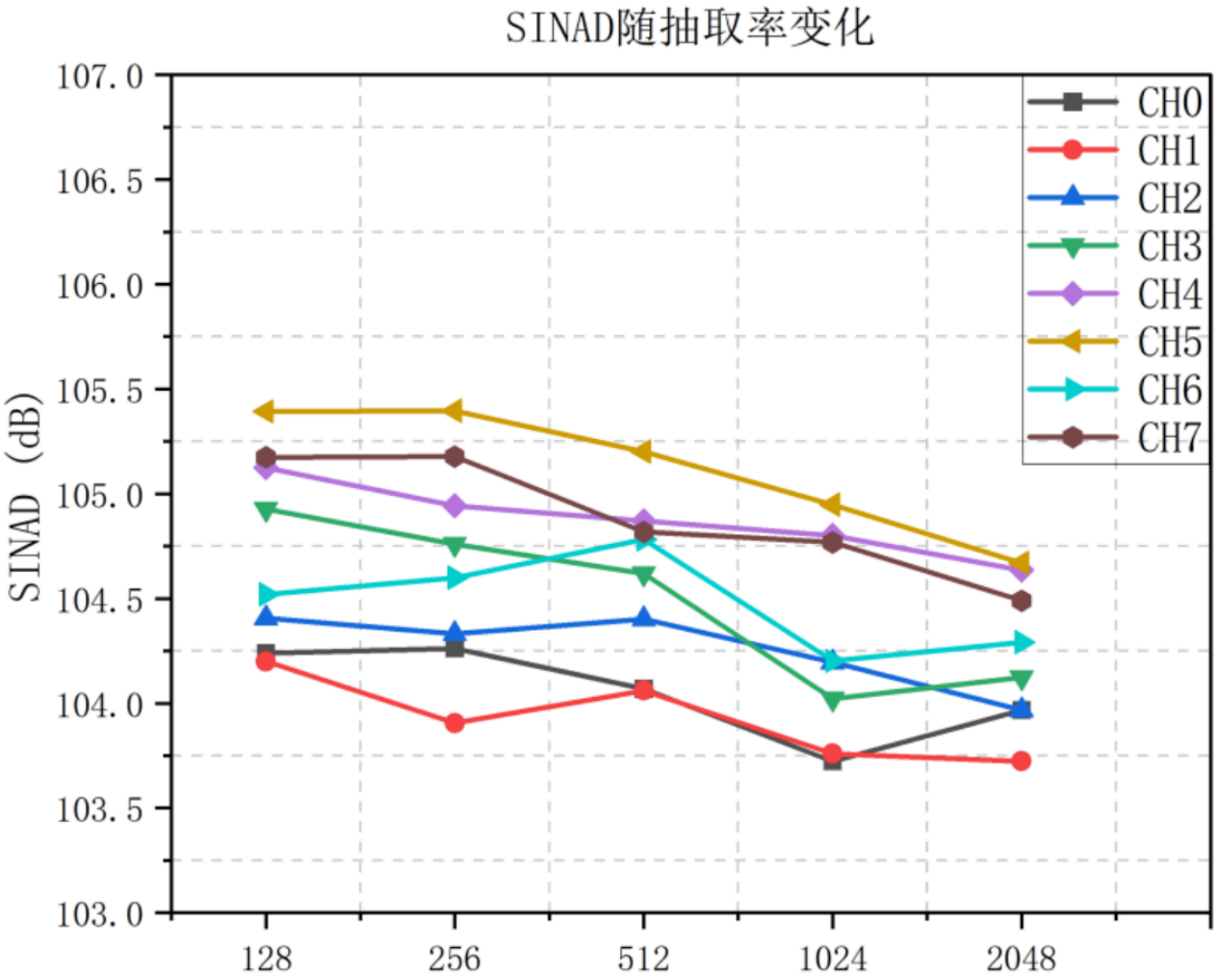


Figure 20: SINAD vs. decimation rate, Fin=1KHz, -0.5dBFS, TA=25°C

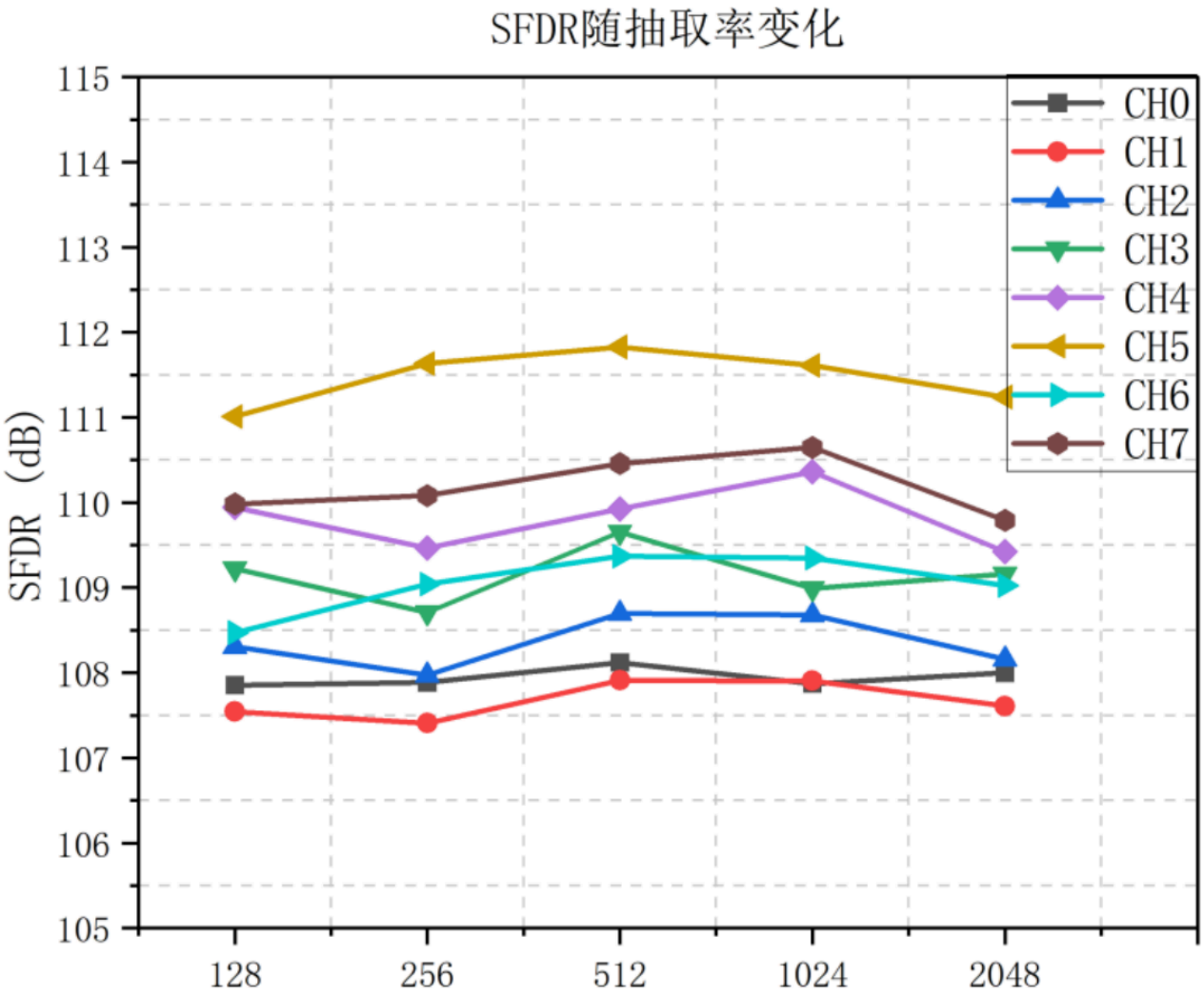


Figure 21: SFDR vs. decimation rate, Fin=1KHz, -0.5dBFS, TA=25°C

典型应用线路图 / Typical Application Circuit

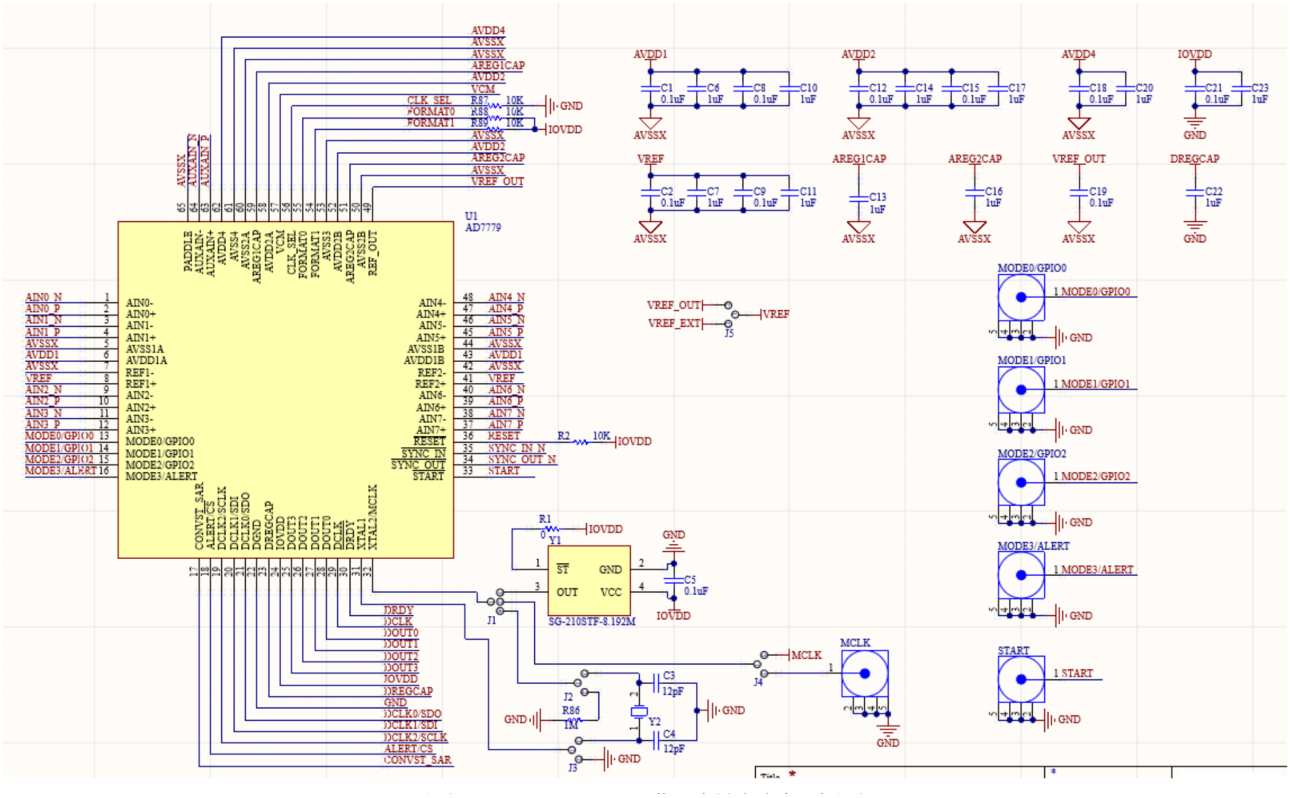


Figure 22: SXA030 typical peripheral circuit

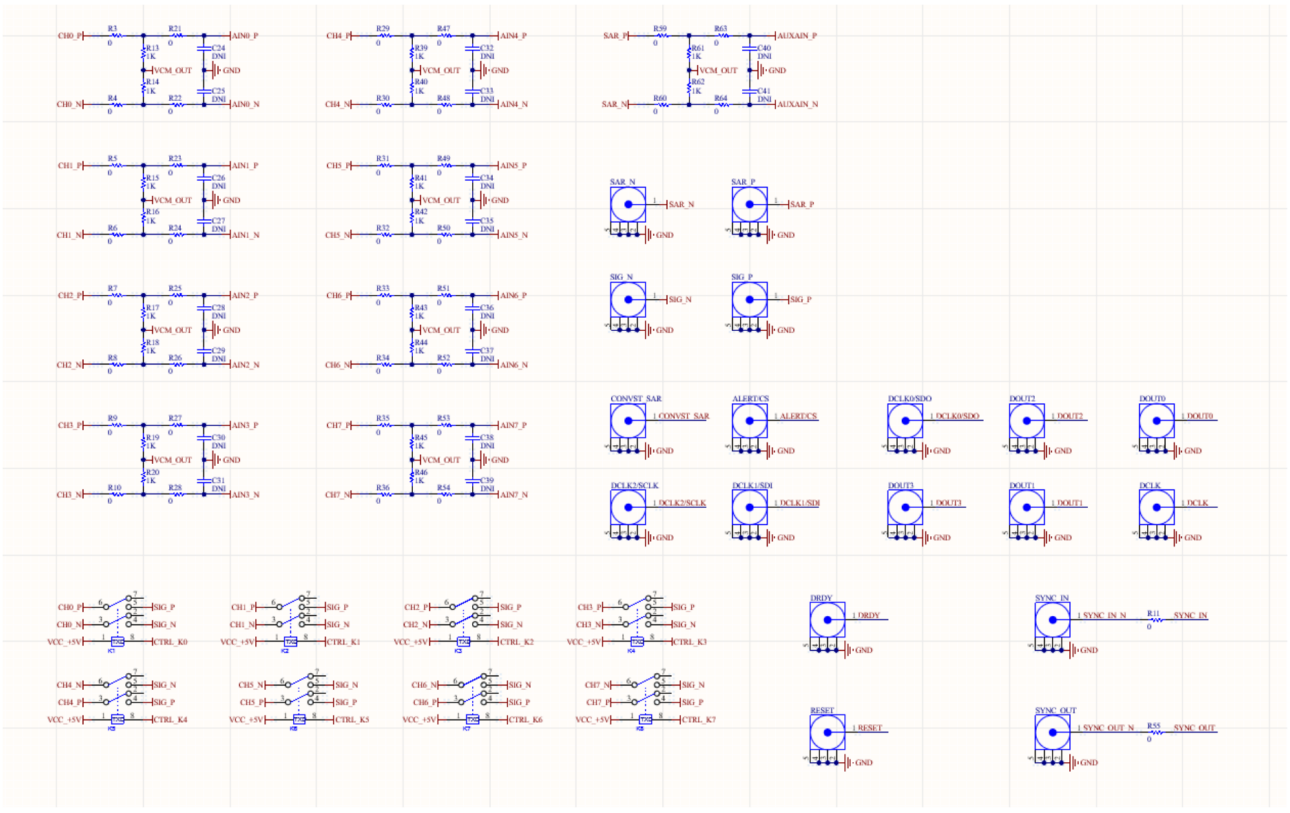


Figure 23: Analog front-end circuit

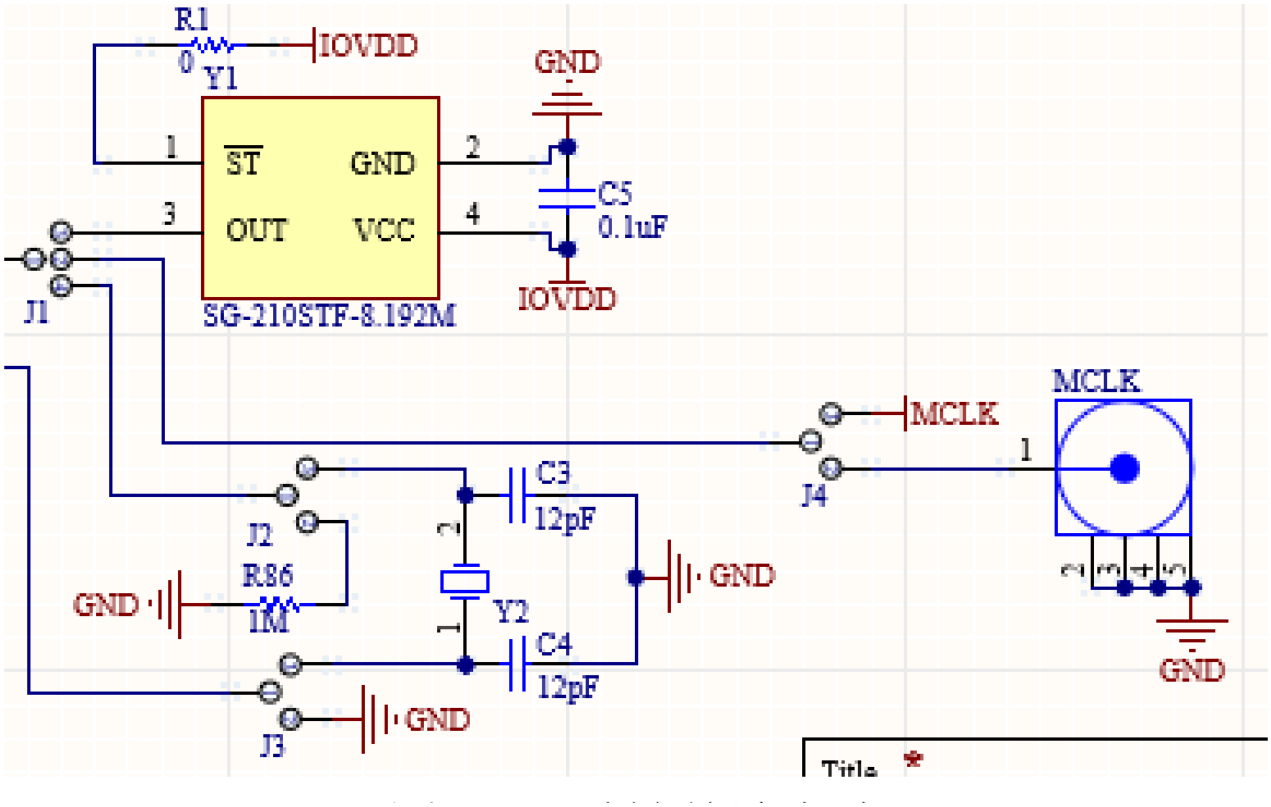


Figure 24: Clock front-end circuit

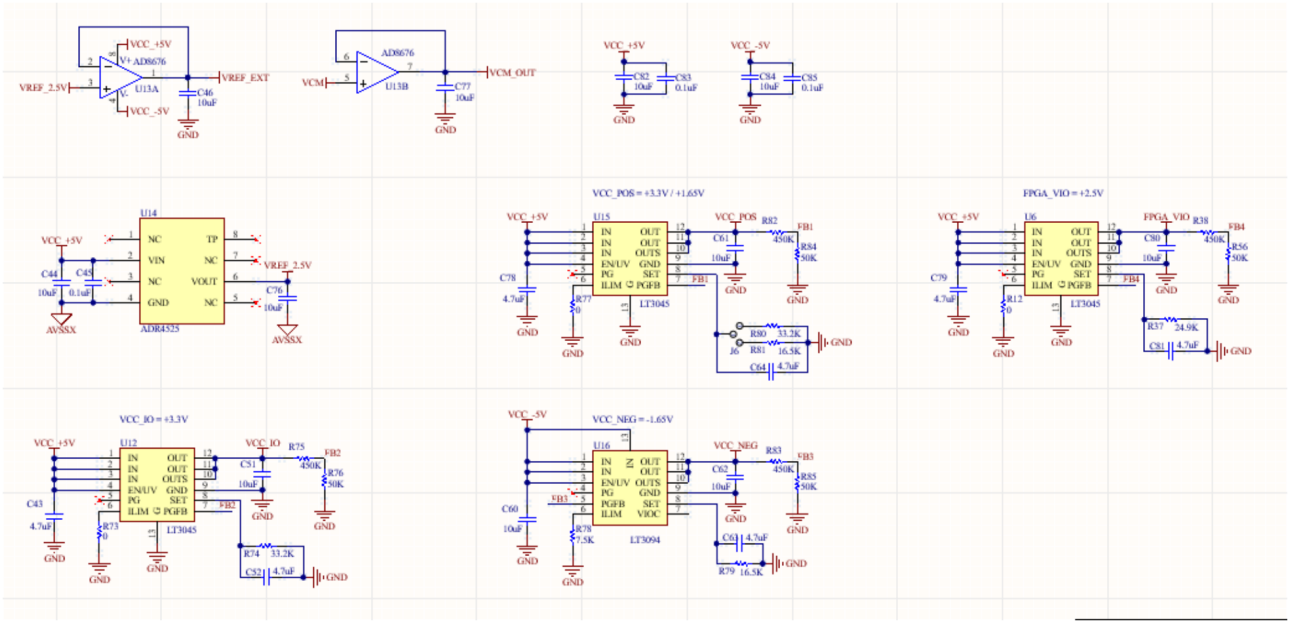


Figure 25: Power supply filtering

单元模块及工作原理 / Functional Blocks and Operating Principles

1、模拟输入 / 1. Analog Input

English: The SXA030 can operate in bipolar or unipolar mode and supports true differential, pseudo-differential, and single-ended input signals, as shown in the figures.

中文： SXA030 可工作在双极性或单极性模式下，支持真差分、伪差分和单端输入信号，如图所示。

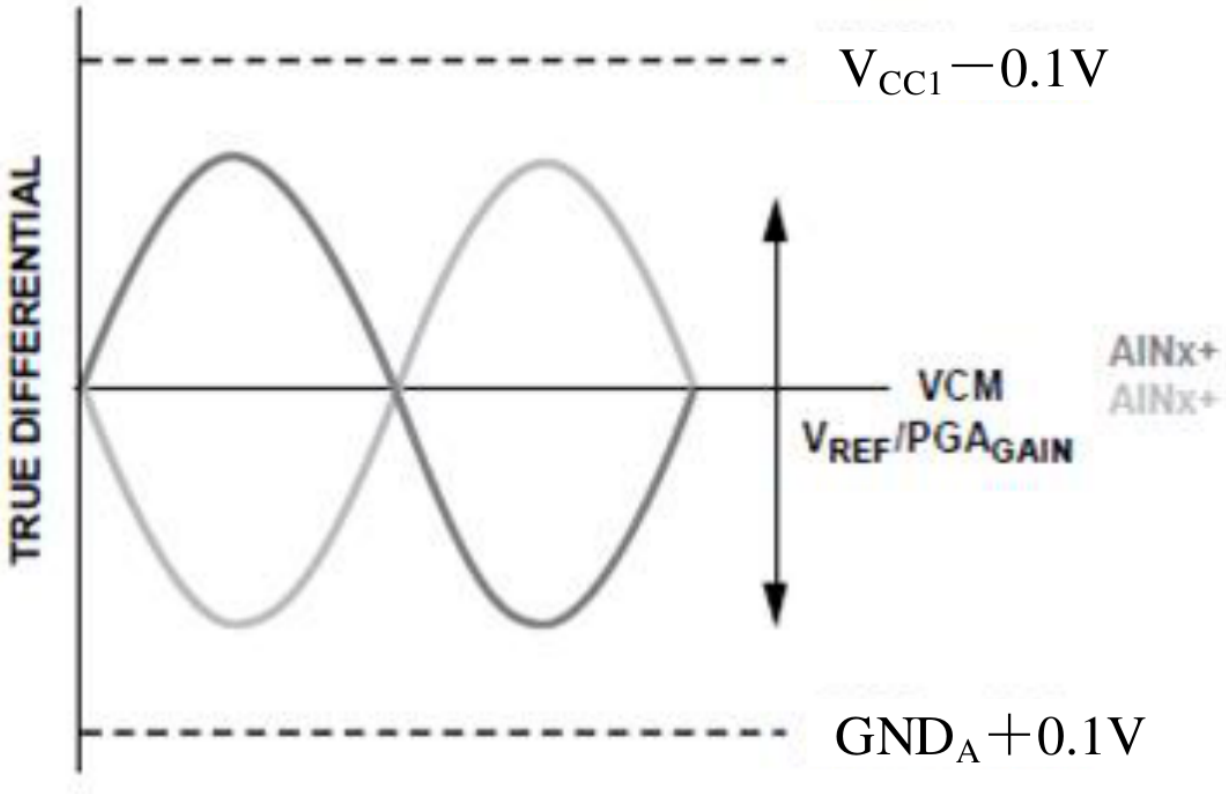


Figure 26: Σ-Δ ADC input signal configuration, true differential

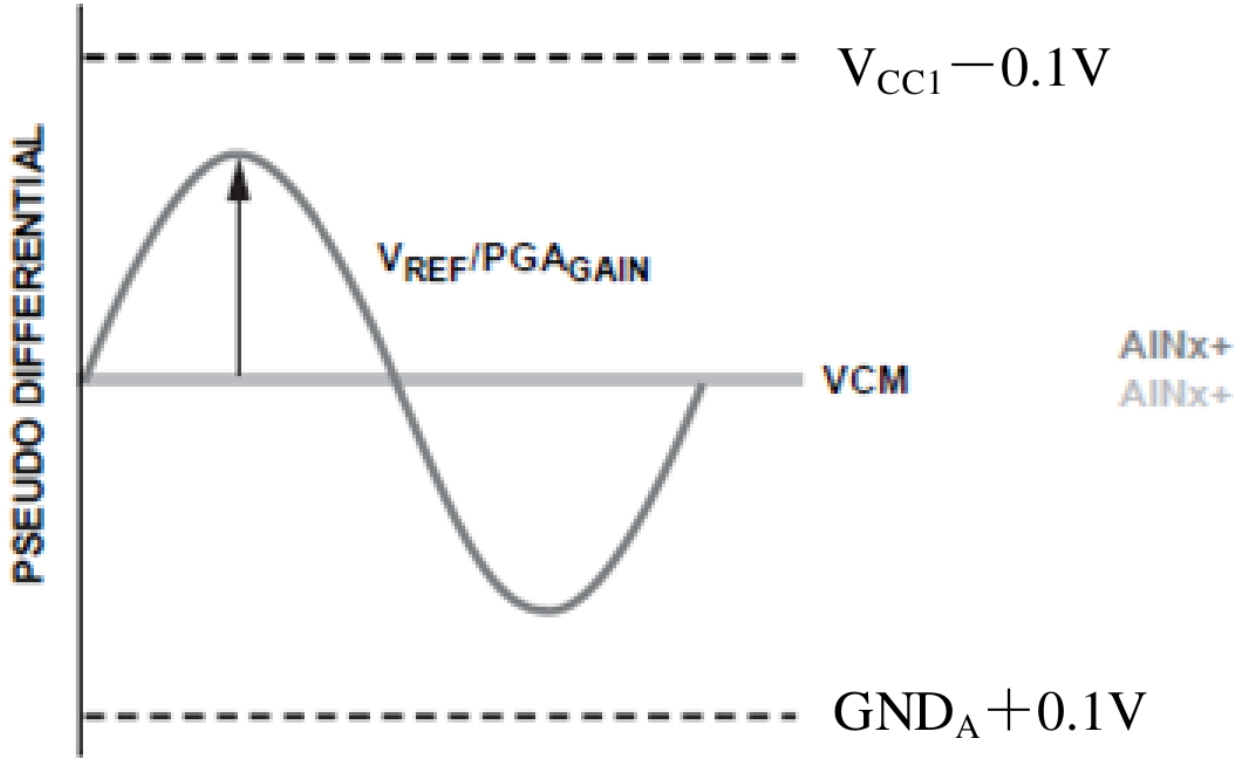


Figure 27: Σ-Δ ADC input signal configuration, pseudo-differential

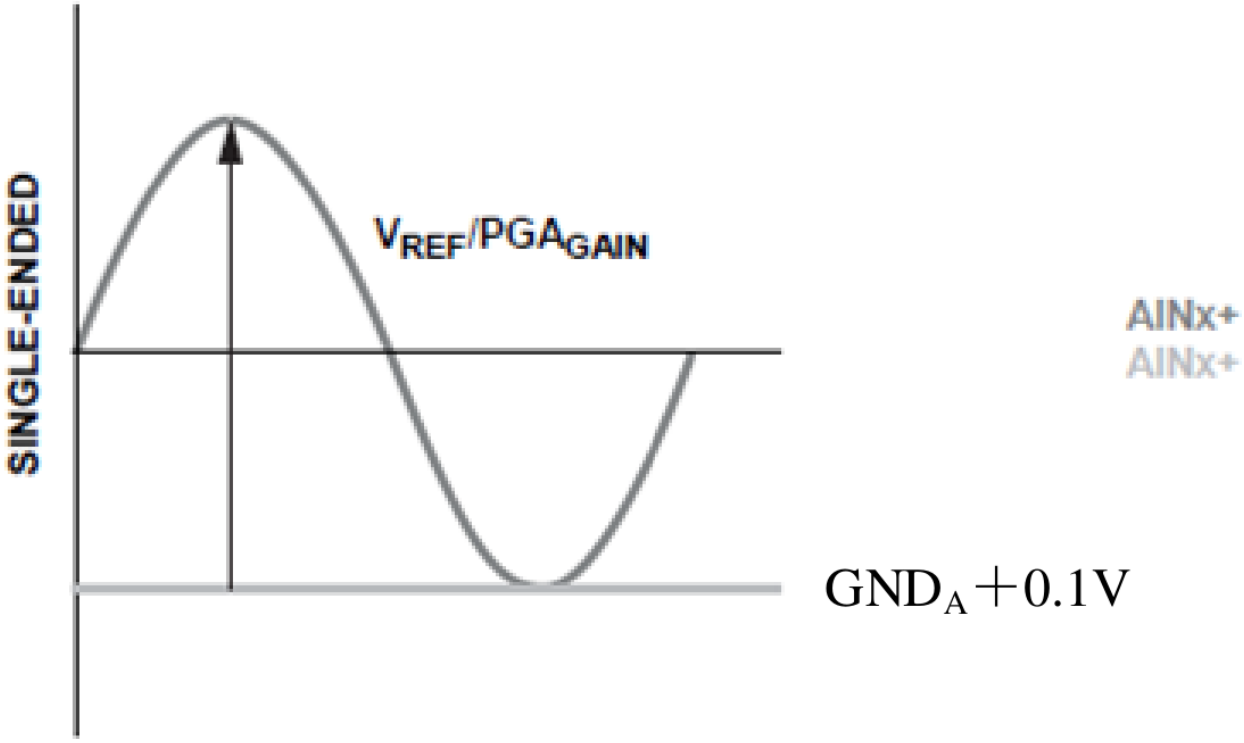


Figure 28: Σ-Δ ADC input signal configuration, single-ended bipolar

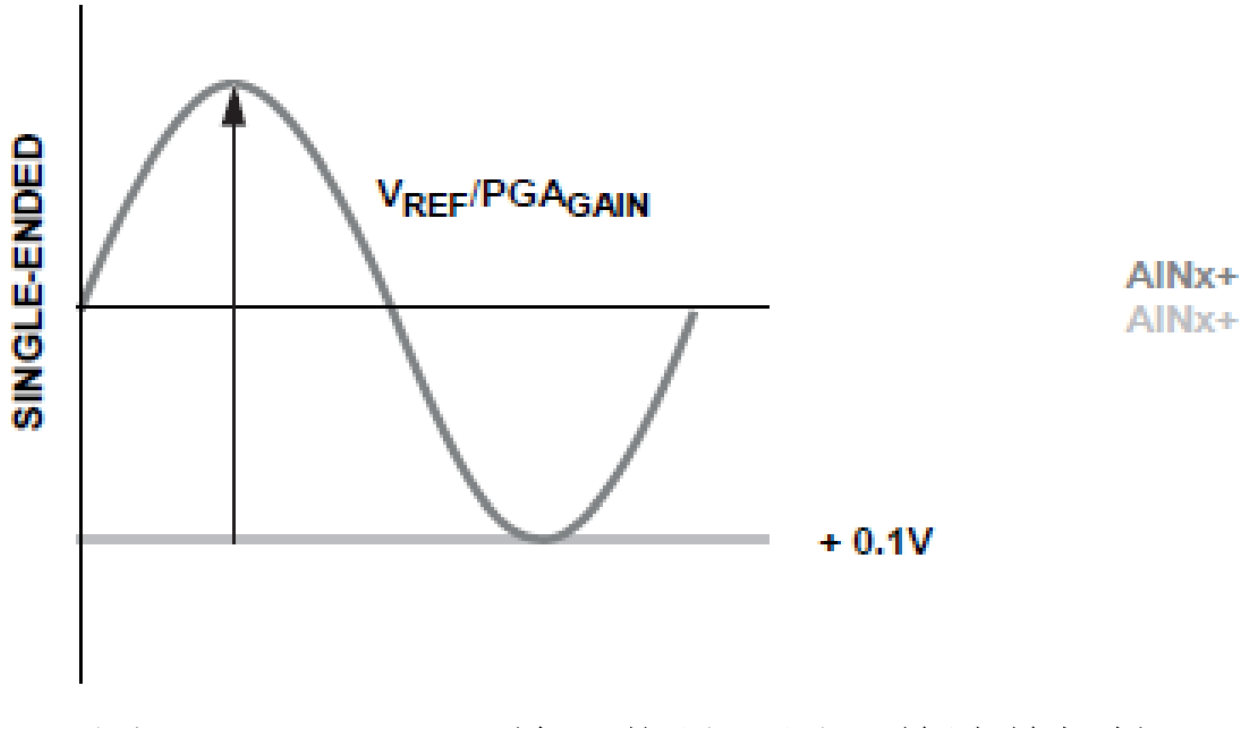


Figure 29: Σ-Δ ADC input signal configuration, single-ended unipolar

English: The table below summarizes the maximum differential input signal and dynamic range for the different input modes.

中文： 下表总结了不同输入模式下的最大差分输入信号和动态范围。

表2 输入信号模式 / Table 2. Input Signal Modes

输入信号模式 / Input Signal Mode	PGA 增益 / PGA Gain	最大差分信号 / Maximum Differential Signal	最大峰峰值信号 / Maximum Peak-to-Peak Signal
真差分 / True differential	所有增益 / All gains	±VREF/PGA	2×VREF/PGA
伪差分 / Pseudo-differential	所有增益 / All gains	±VREF/PGA	2×VREF/PGA
单端 / Single-ended	所有增益 / All gains	VREF/PGA	VREF/PGA

English: The input signal common mode is unrestricted, but the absolute input signal voltage on any AINx± pin shall remain between GNDA+100mV and Vcc1–100mV; otherwise the linearity of the input signal degrades, and if the signal voltage exceeds the absolute maximum signal rating, the device will be damaged.

Figure 30 shows the maximum and minimum voltage common-mode ranges for different PGA gains at the maximum differential input voltage.

中文： 输入信号共模无限制，但任意 AINx±引脚上的绝对输入信号电压应保持在 GNDA+100mV 和 Vcc1–100mV 之间，否则输入信号的线性度会下降，而且如果信号电压超过了绝对最大信号额定值，器件会受损。

图 30 显示了最大差分输入电压情况下，不同 PGA 增益时的最大和最小电压共模范围。

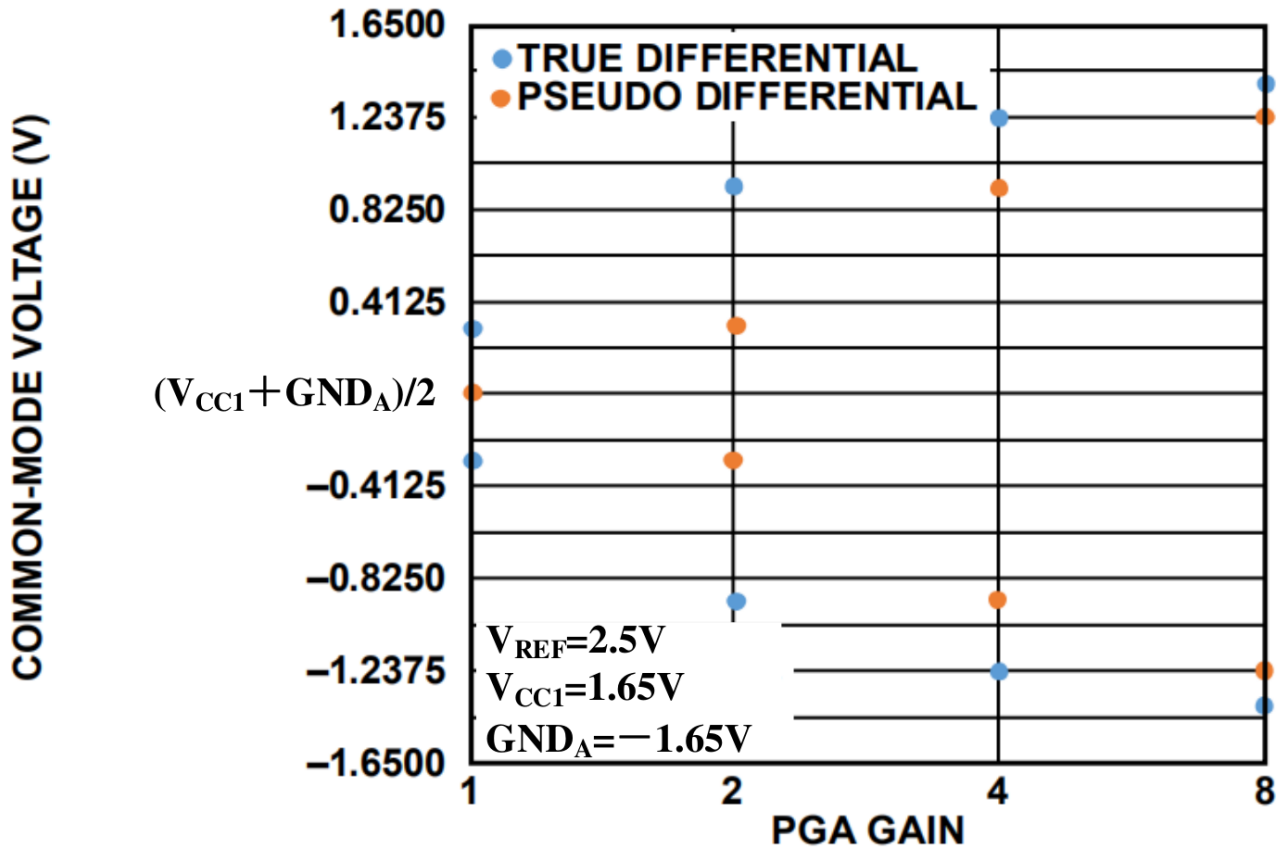


Figure 30: Maximum common-mode voltage range at maximum differential input signal

2、传递函数 / 2. Transfer Function

English: The SXA030 can use a reference voltage of up to 3.6 V (typical value 2.5 V) and converts the differential voltage between the analog inputs (AINx+ and AINx−) into a digital output. The ADC converts the voltage difference between the analog input pins (AINx+ − AINx−) into a digital code at the output. The 24-bit conversion result is provided MSB-first in two's complement format, as shown in Table 3 and Figure 31.

中文： SXA030 可使用最高 3.6 V 的基准电压(典型值为 2.5 V)，并可将模拟输入(AINx+和 AINx−)之间的差分电压转换为数字输出。ADC 将模拟输入引脚之间的电压差(AINx+ − AINx−)转换为输出端的数字码。24 位转换结果以 MSB 优先、二进制补码格式提供，如表 3 和图 31 所示。

表3 PGA=1×的输出码和理想输入电压 / Table 3. Output Codes and Ideal Input Voltages for PGA=1×

条件 / Condition	模拟输入(AINx+ -AINx-)，VREF=2.5V / Analog Input (AINx+ – AINx−), VREF=2.5V	以二进制补码形式表示的数字输出代码（十六进制数）/ Digital Output Code in Two's Complement (Hex)
FS-1LSB	+2.4999999702V	0x7FFFFF
中间电平+1LSB / Midscale +1LSB	+298nV	0x000001
中间电平 / Midscale	0V	0x000000
中间电平-1LSB / Midscale −1LSB	-298nV	0xFFFFFF
-FS+1LSB	-2.4999999702V	0x800001

条件 / Condition	模拟输入(AINx+ -AINx-)，VREF=2.5V / Analog Input (AINx+ – AINx–), VREF=2.5V	以二进制补码形式表示的数字输出代码（十六进制数）/ Digital Output Code in Two's Complement (Hex)
-FS	-2.5V	0x800000

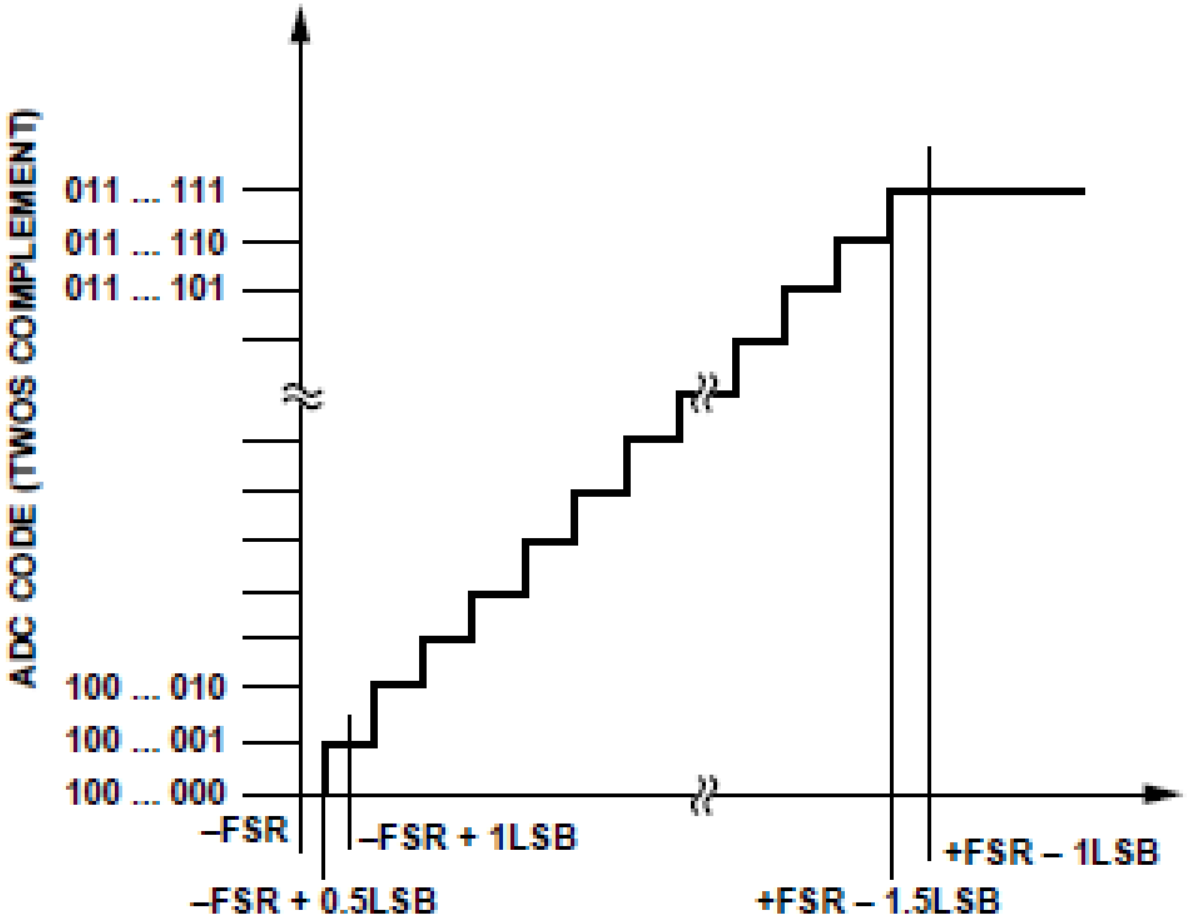


Figure 31: Transfer function

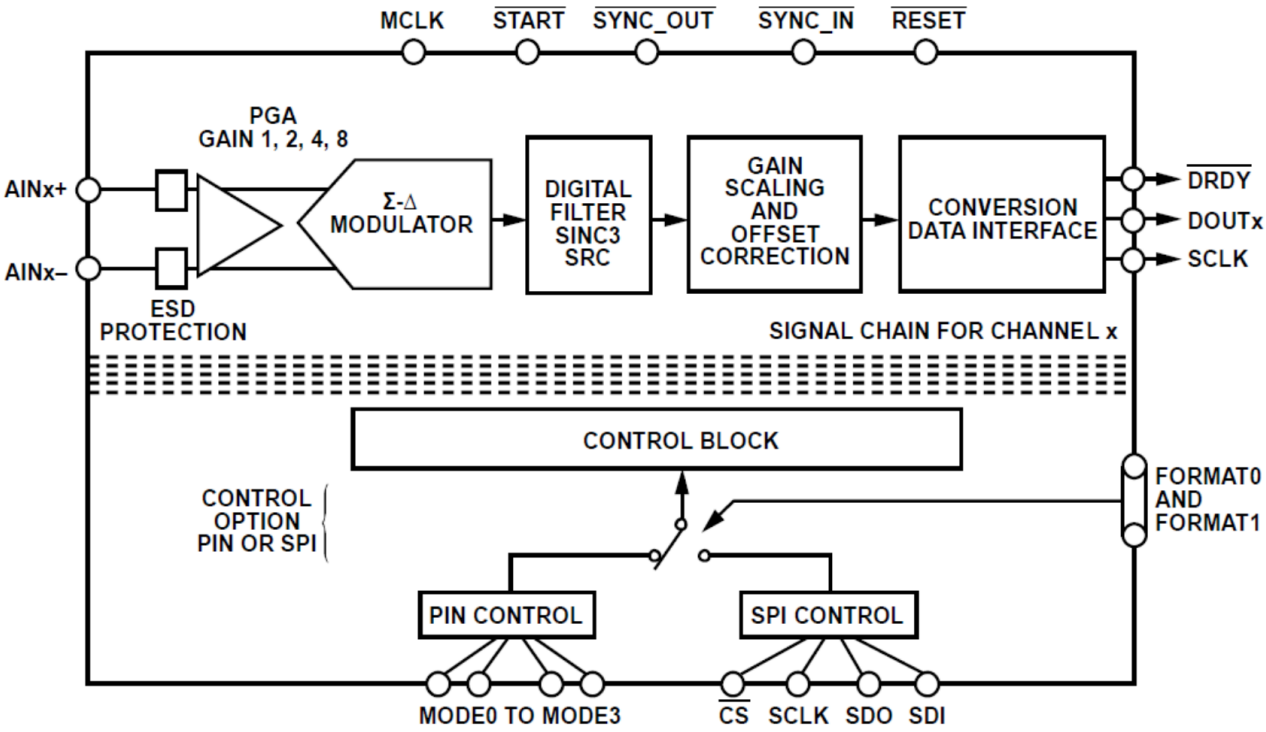


Figure 32: Core signal chain simplified diagram

3、核心信号链 / 3. Core Signal Chain

English: Each Σ-Δ ADC channel of the SXA030 has an identical signal path, which starts at the analog input pins and ends at the digital output pins. Figure 32 shows the top-level deployment of this signal chain. Before each Σ-Δ ADC there is a PGA, used to map the sensor output to the ADC input, thereby providing low input current at DC (±4 nA input current and ±1.5 nA differential input current), an 8 pF input capacitance at AC, and configurable gains of 1, 2, 4, and 8. Each ADC channel has its own Σ-Δ modulator, which oversamples the analog input and conveys the digital representation to the digital filter module. This data is filtered, gain-adjusted, and offset-processed, and then output to the data interface.

To minimize power consumption, channels can also be individually disabled.

中文： SXA030 的每个 Σ-Δ 型 ADC 通道都有一个完全相同的信号路径，此路径起始于模拟输入引脚，终止于数字输出引脚。图 32 所示为此信号链的顶层部署。在每个 Σ-Δ 型 ADC 之前，有一个 PGA，用来将传感器输出映射到 ADC 输入，从而在直流中提供低输入电流(±4 nA 输入电流和±1.5 nA 差分输入电流)，在交流中提供 8 pF 输入电容，以及可配置增益 1、2、4、8。每个 ADC 通道都有自己的 Σ-Δ 调制器，其对模拟输入进行过采样，并将数字表示传送到数字滤波器模块。该数据经过滤波、增益调节和失调处理，然后输出至数据接口。

为了最大程度降低功耗，通道还可单独禁用。

4、容性 PGA / 4. Capacitive PGA

English: Each Σ-Δ ADC has a dedicated PGA providing a gain range of 1, 2, 4, and 8. This PGA requires no external input buffer and allows the user to amplify small sensor signals so as to use the full dynamic range of the SXA030.

This PGA can maximize the signal-chain dynamic range of weak sensor output signals.

The SXA030 uses PGA chopping to minimize the input amplifier offset and offset drift, and can additionally reduce 1/f noise. For the SXA030, the chopping frequency is 64 kHz (high-resolution mode) and 16 kHz (low-power mode). The chopping signal tones are suppressed by the SINC filter.

To minimize intermodulation effects so as to avoid generating images in the target band, it is recommended to limit the input signal bandwidth to 2/3 of the chopping frequency.

The capacitive PGA common-mode voltage is independent of gain, and as long as the input signal voltage is within the range GNDA + 100 mV to VCC1 – 100 mV, it can be any value. For the maximum common-mode voltage at the maximum differential input signal, see Figure 30.

中文： 每个 Σ-Δ 型 ADC 有一个专用 PGA，其提供的增益范围是 1、2、4 和 8。此 PGA 无需外部输入缓冲器，允许用户放大传感器的小信号，以便使用 SXA030 的全部动态范围。

该 PGA 可最大程度增加微弱传感器输出信号的信号链动态范围。

SXA030 通过 PGA 斩波来最大程度减少输入放大器的失调和失调漂移，另外还能降低 1/f 噪声。对于 SXA030，斩波频率为 64 kHz(高分辨率模式)以及 16 kHz(低功耗模式)。斩波信号音由 SINC 滤波器抑制。

为了最大程度降低交调效应，以免在目标频段中产生镜像，建议将输入信号带宽限制为斩波频率的 2/3。

容性 PGA 共模电压与增益无关，且只要输入信号电压处于 GNDA + 100 mV 至 VCC1 – 100 mV 范围内，它就可以是任意值。关于最大差分输入信号下的最大共模电压，请参见图 30。

5、内部基准电流源和基准电压缓冲器 / 5. Internal Reference Current Source and Reference Voltage Buffer

English: The SXA030 integrates a 2.5 V reference voltage source with a typical value of 10 ppm/°C, which is disabled at power-up. The buffered reference voltage is located at pin 49 and provides up to 10 mA of continuous current. Enabling this reference voltage source requires a 100 nF capacitor.

In applications requiring a low-noise reference voltage source, it is recommended to connect a low-pass filter (LPF) with a cutoff frequency (fCUTOFF) below 10 Hz to REF, connect the output of this filter to REFx+, and connect GNDA to REFx−.

In this case, configure the Σ-Δ reference voltage source as external. Performance examples with and without the output filter are shown in Figure 33.

中文： SXA030 集成一个 2.5 V、10 ppm/°C典型值的基准电压源，其在上电时是禁用的。缓冲基准电压位于引脚 49，提供最高 10 mA 连续电流。使能该基准电压源需要一个 100 nF 电容。

在需要低噪声基准电压源的应用中，建议将一个截止频率(f CUTOFF)低于 10 Hz 的低通滤波器(LPF)连接到 REF 将此滤波器的输出连接到 REFx+，并将 GNDA 连接到 REFx−。

这种情况下，将 Σ-Δ 基准电压源配置为外部。使用和不使用输出滤波器时的性能示例如图 33 所示。

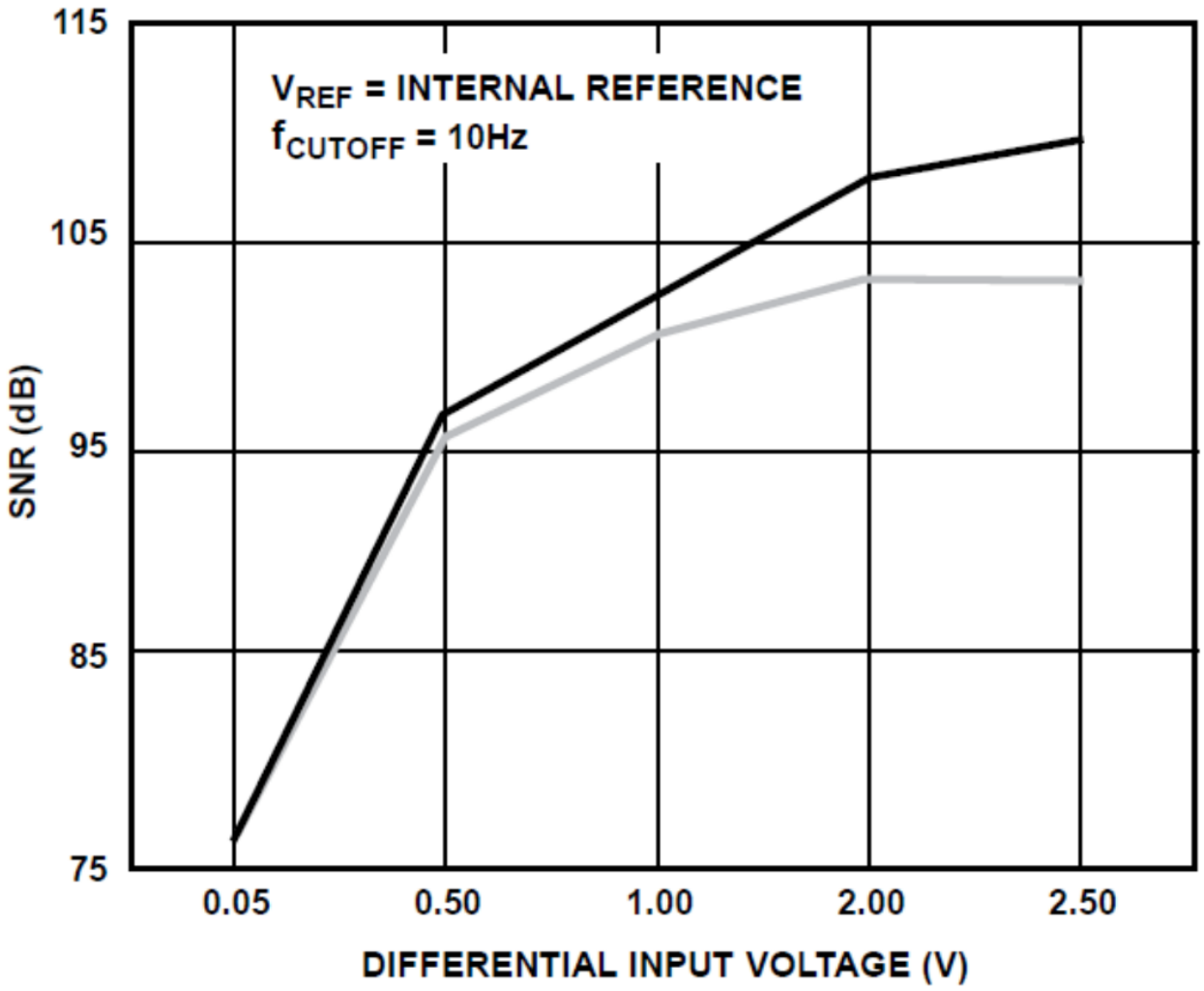


Figure 33: SNR with external LPF added, vREF = internal reference source, fCUTOFF = 10 Hz

English: The SXA030 can use an external reference voltage source, connected between the REFx+ and REFx− pins. Recommended reference voltage sources for the SXA030 include the ADR441 and ADR4525 series low-noise, high-precision reference voltage sources.

中文： SXA030 可以使用外部基准电压源，其连接在 REFx+和 REFx−引脚之间。SXA030 的推荐基准电压源包括 ADR441 和 ADR4525 系列低噪声、高精度基准电压源。

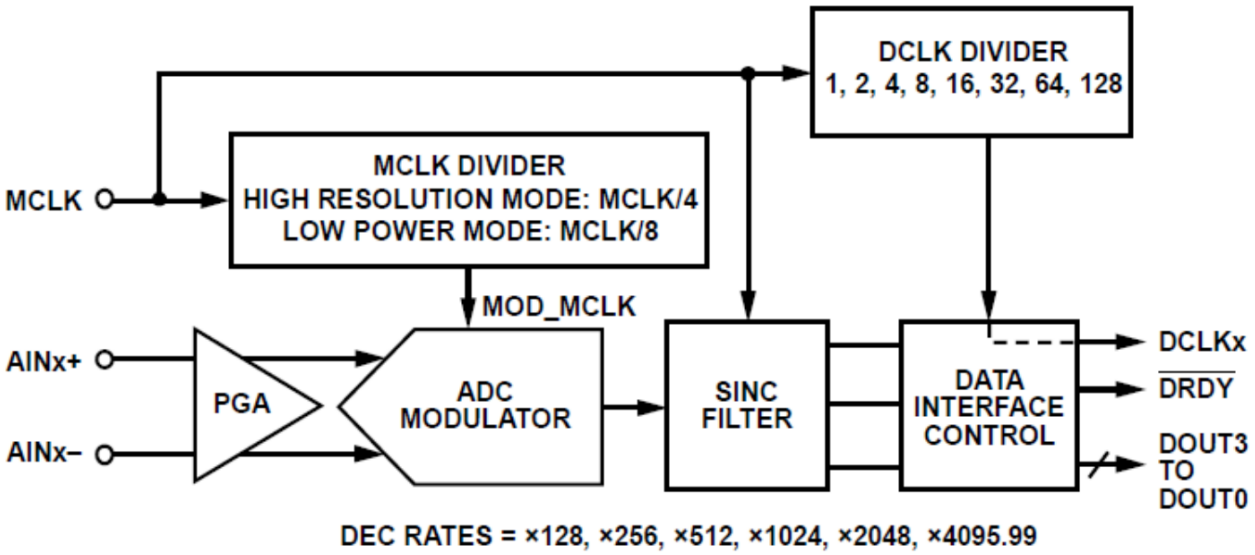


Figure 34: Clock generation on the SXA030

English: The reference voltage source buffer has three different operating modes: buffer enable mode, buffer bypass mode, and buffer precharge mode.

In buffer enable mode, the buffer is fully enabled, minimizing the current requirement on the external reference voltage source. Note that the buffer output voltage headroom is ±100 mV from the supply rails.

In buffer bypass mode, the external reference voltage source is connected directly to the ADC reference capacitance. The reference voltage source must provide sufficient current to correctly charge the internal ADC reference capacitance. In this operating mode, crosstalk performance degrades because the ADC channels are not isolated from each other.

Buffer precharge (pre-Q) mode is the default operating mode. It is a hybrid mode: the internal reference voltage source buffer is connected during initial acquisition to precharge the internal ADC reference capacitance. During the final phase of acquisition, the reference voltage source is connected directly to the ADC capacitance. Compared with buffer enable and buffer bypass modes, this mode has some advantages. In buffer precharge mode: - Lowest reference current requirement (compared with buffer bypass mode) - Eliminates the noise contribution of the internal reference voltage source buffer (compared with buffer enable mode)

In buffer precharge mode, the upper/lower headroom of the reference voltage source buffer does not apply, because the reference voltage source determines the final voltage of the ADC reference capacitance.

中文： 基准电压源缓冲器有三种不同的工作模式：缓冲器使能模式、缓冲器旁路模式和缓冲器预充电模式。

在缓冲器使能模式下，缓冲器完全使能，最大程度降低外部基准电压源的电流要求。注意，缓冲器输出电压裕量为离开供电轨±100 mV。

在缓冲器旁路模式下，外部基准电压源直接连接 ADC 基准电容。基准电压源必须提供足够的电流，从而正确为内部 ADC 基准电容充电。在这种工作模式下，串扰性能会下降，因为 ADC 通道互相之间不隔离。

缓冲器预充电(pre-Q)模式是默认工作模式。它是一种混合模式，内部基准电压源缓冲器在初始采集时连接，对内部 ADC 基准电容预充电。在采集的最终阶段，基准电压源直接连接 ADC 电容。相比缓冲器使能和缓冲器旁路

模式，该模式有一些优势。在缓冲器预充电模式下， • 基准电流要求最低(与缓冲器旁路模式相比) • 消除了内部基准电压源缓冲器的噪声贡献(与缓冲器使能模式相比)

在缓冲器预充电模式下，基准电压源缓冲器的上裕量/下裕量不适用，因为基准电压源决定 ADC 基准电容的最终电压。

6、集成 LDO / 6. Integrated LDO

English: The SXA030 integrates 3 LDOs that regulate the internal supplies: 2 LDOs for the analog modules and 1 LDO for the digital core. The internal LDOs require an external 1µF decoupling capacitor on the DREGCAP, AREG1CAP, and AREG2CAP pins.

The LDO slew rate may be low because it is determined by the main supply slew rate; therefore, to ensure correct initialization of the digital module, a pulse must be sent to the RESET pin at power-up to generate a hardware reset.

中文： SXA030 集成 3 个调节内部电源的 LDO：2 个 LDO 用于模拟模块，1 个 LDO 用于数字核心。内部 LDO 在 DREGCAP、AREG1CAP 和 AREG2CAP 引脚上需要一个外部 1µF 去耦电容。

LDO 压摆率可能较低，因为它由主电源压摆率决定；因此，为了保证数字模块正确初始化，要求在上电时向 RESET 引脚发送脉冲以产生一次硬件复位。

7、时钟和采样速率 / 7. Clock and Sampling Rate

English: The SXA030 integrates 8 Σ-Δ ADC cores. Each ADC receives the same master clock signal. The SXA030 requires maximum external MCLK frequencies of 8192 kHz and 4096 kHz for high-resolution mode and low-power mode, respectively. MCLK is internally divided by 4 (high-performance mode) and by 8 (low-power mode), and the resulting modulator MCLK (MOD_MCLK) signal is used as the modulator sampling clock of the ADC. If the minimum ODR selectable for the SINC filter is not low enough, MCLK can be reduced to accommodate a lower ODR. If the external clock is below 250 kHz, the CLK_QUAL_DIS bit shall be set (SPI control mode only).

The SXA030 integrates an internal oscillator clock, which initializes the internal registers at power-up. After initialization, the CLK_SEL pin determines which external clock is used (see Table 4).

中文： SXA030 集成 8 个 Σ-Δ 型 ADC 内核。各 ADC 接收相同的主时钟信号。SXA030 针对高分辨率模式和低功耗模式分别需要 8192 kHz 和 4096 kHz 的最高外部 MCLK 频率。MCLK 在内部进行 4 分频(高性能模式)和 8 分频(低功耗模式)，产生的调制器 MCLK (MOD_MCLK)信号用作 ADC 的调制器采样时钟。如果 SINC 滤波器选择的最小 ODR 不够低，则可降低 MCLK，以便适应较低的 ODR。如果外部时钟低于 250 kHz，则应设置 CLK_QUAL_DIS 位(仅限 SPI 控制模式)。

SXA030 集成内部振荡器时钟，其在上电时初始化内部寄存器。初始化之后，CLK_SEL 引脚决定使用哪个外部时钟(参见表 4)。

表4 时钟源 / Table 4. Clock Sources

CLK_SEL 状态 / CLK_SEL State	时钟源 / Clock Source	连接 / Connection
0	CMOS	输入至 XTAL2/MCLK，IOVDD 逻辑电平。XTAL1 必须连接 DGND。/ Input to XTAL2/MCLK, IOVDD logic level. XTAL1 must be connected to DGND.

CLK_SEL 状态 / CLK_SEL State	时钟源 / Clock Source	连接 / Connection
1	晶振 / Crystal	连接在 XTAL 和 XTAL2/MCLK 之间。 / Connected between XTAL and XTAL2/MCLK.

English: The MCLK signal generates the DCLK output signal, which serves as the clock signal with which the SXA030 outputs Σ-Δ conversion data, as shown in Figure 34.

中文： MCLK 信号产生 DCLK 输出信号，后者作为 SXA030 输出 Σ-Δ 转换数据的时钟信号，如图 34 所示。

8、数字复位和同步引脚 / 8. Digital Reset and Synchronization Pins

English: Sending an external pulse to the SYNC_IN pin causes an internal reset of the digital module; this pulse does not affect the data in the internal registers. A pulse is required on this pin in the following two cases: - After updating one or more registers directly related to the sinc3 filter. This includes power mode, offset, gain, and phase compensation. - Synchronizing multiple devices.

The SYNC_IN pin pulse must be synchronized with MCLK.

If the controller/processor cannot generate a synchronization pulse, there are two methods to implement a synchronization pulse: - Apply an asynchronous pulse on the START pin, which is then internally synchronized to the external MCLK clock, and the resulting synchronization signal is output to the SYNC_OUT pin. - Trigger SYNC_OUT internally. When the SXA030 is configured in SPI control mode, toggling bit 0 of the GEN_USER_CONFIG_2 register generates a synchronization pulse on the SYNC_OUT pin.

If internal synchronization is used, the SYNC_IN and SYNC_OUT pins must be connected externally.

To synchronize multiple SXA030 devices, the SYNC_OUT pin of one device can be connected to multiple devices. This synchronization method requires the same MCLK signal to be used for all connected SXA030 devices, as shown in Figure 35.

If the START pin is not used, it shall be connected to DGND.

中文： 将一个外部脉冲发送至 SYNC_IN 引脚会使数字模块发生内部复位；此脉冲不影响内部寄存器中的数据。在如下两种情况下，该引脚需要一个脉冲： • 更新与 sinc3 滤波器直接相关的一个或多个寄存器之后。这包括功耗模式、失调、增益和相位补偿。 • 同步多个器件。

SYNC_IN 引脚脉冲必须与 MCLK 同步。

如果控制器/处理器无法生成同步脉冲，则有两种方法可以实现同步脉冲： • 将异步脉冲施加在 START 引脚上，然后再内部同步至外部 MCLK 时钟，得到的同步信号输出至 SYNC_OUT 引脚。 • 内部触发 SYNC_OUT。当 SXA030 配置为 SPI 控制模式时，切换 GEN_USER_CONFIG_2 寄存器的位 0 将在 SYNC_OUT 引脚上产生一个同步脉冲。

如果使用了内部同步，则 SYNC_IN 和 SYNC_OUT 引脚必须外部相连。

如需同步多个 SXA030，则一个器件的 SYNC_OUT 引脚可以连接多个器件。这种同步方式要求对所有连接的 SXA030 器件使用同一 MCLK 信号，如图 35 所示。

如果 START 引脚不用，应将其连至 DGND。

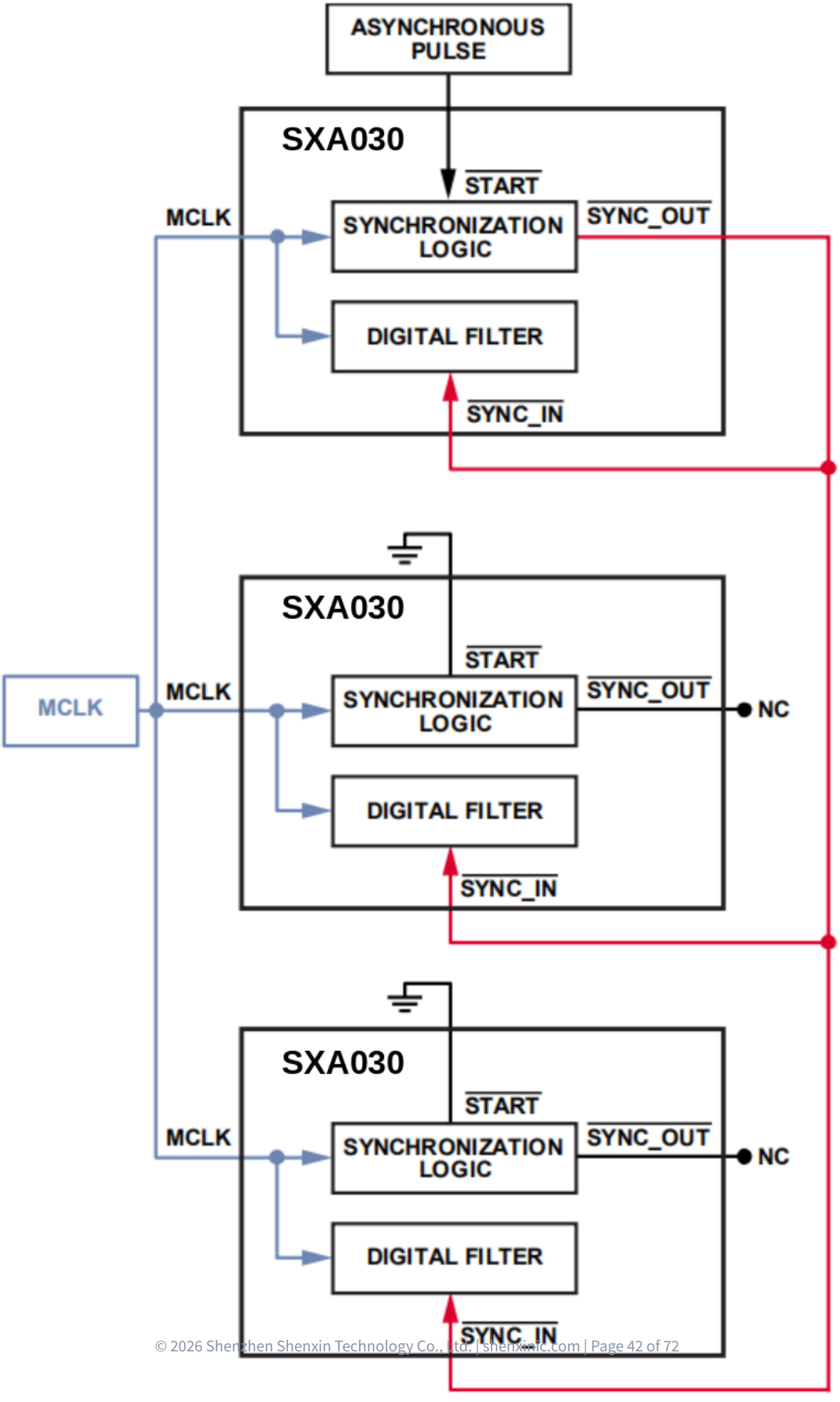

ASYNCHRONOUS PULSE
SXA030
START
MCLK
SYNCHRONIZATION LOGIC
SYNC_OUT
DIGITAL FILTER
SYNC_IN
SXA030
START
MCLK
MCLK
SYNCHRONIZATION LOGIC
SYNC_OUT
NC
DIGITAL FILTER
SYNC_IN
SXA030
START
MCLK
SYNCHRONIZATION LOGIC
SYNC_OUT
NC
DIGITAL FILTER
SYNC_IN

Figure 35: Synchronization of multiple SXA030 devices

9、数字滤波 / 9. Digital Filtering

English: The SXA030 provides a low-latency sinc3 filter. Most precision Σ-Δ ADCs use a sinc3 filter, because the sinc3 filter can provide a low-latency path for applications requiring low-bandwidth signals, such as control loops or situations requiring dedicated post-processing. The digital filter adds notches at multiples of the sampling frequency.

The digital filter implements three main notches: one at the maximum ODR (16 kHz or 8 kHz, depending on the power mode), and two more at ODR frequencies selected to prevent noise from aliasing into the passband.

Figure 36 shows the typical filter transfer function using a decimation rate of 256 samples in both high-resolution and low-power modes.

中文： SXA030 提供低延迟 sinc3 滤波器。大多数精密 Σ-Δ 型 ADC 采用 sinc3 滤波器，因为 sinc3 滤波器能为需要低带宽信号的应用提供低延迟路径，比如控制环路或需要专用后处理的情况。数字滤波器增加的陷波为采样频率的倍数。

数字滤波器实现了三个主陷波：一个在最大 ODR 处(16 kHz 或 8 kHz，具体取决于功耗模式)，另外两个在为阻止噪声混叠进入通带而选择的 ODR 频率处。

图 36 显示了高分辨率和低功耗两种模式下使用 256 样本抽取率的典型滤波器传递函数。

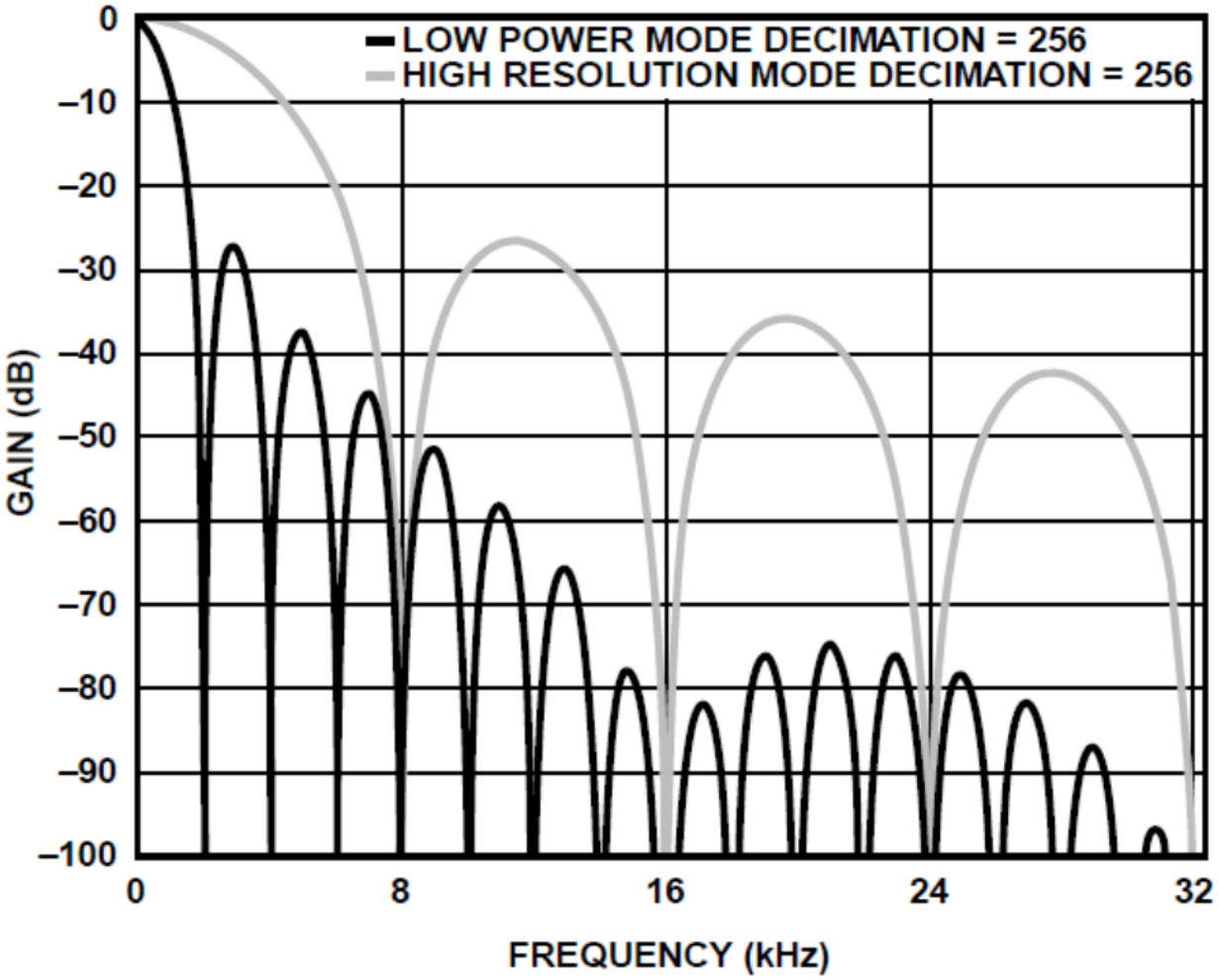


Figure 36: Sinc3 frequency response

English: The sample rate converter characteristics allow fine adjustment of the decimation rate, even to non-integer multiples of the decimation rate.

中文： 采样速率转换器特性允许微调抽取率，甚至可以不是抽取率的整数倍。

10、关断模式 / 10. Shutdown Mode

English: Pulling VCC2 to ground and connecting a 1 MΩ pull-down resistor to XTAL2 places the SXA030 in shutdown mode.

中文： 将 VCC2 拉至地，并将一个拉低的 1 MΩ 电阻连接到 XTAL2，可以将 SXA030 置于关断模式。

11、控制 SXA030 / 11. Controlling the SXA030

English: The SXA030 can be controlled via pin control mode or SPI control mode.

Pin control mode allows the SXA030 to be hardwired to predefined settings to provide a subset of the overall SXA030 functionality. In this mode, the SRC and diagnostic functions or extended error sources are not available.

Controlling the SXA030 through the SPI interface allows the user to access all monitoring, diagnostic, and Σ-Δ control functions. SPI control mode provides additional functions, such as per-channel offset, gain, and phase correction, and can additionally use a flexible SRC to achieve coherent sampling.

For more details on the different configurations, see Table 5.

中文： SXA030 可通过引脚控制模式或 SPI 控制模式进行控制。

引脚控制模式允许 SXA030 硬连线至预定义设置，以提供 SXA030 整体功能的一部分。这种模式下，SRC 和诊断功能或扩展误差源不可用。

通过 SPI 接口控制 SXA030 可让用户访问全部监控、诊断和 Σ-Δ 控制功能。SPI 控制模式可提供额外的功能，比如各通道的失调、增益和相位校正，此外还可利用灵活的 SRC 来实现相干采样。

有关不同配置的更多详细信息，请参见表 5。

12、引脚控制模式 / 12. Pin Control Mode

English: In pin control mode, the SXA030 is configured at power-up according to the mode pins (MODE0, MODE1, MODE2, MODE3). These four pins set the following SXA030 functions: operating mode, decimation rate/ODR, PGA gain, and reference voltage source, as shown in Table 6.

Due to the limited number of mode pins and the number of available options, the PGA gain control is organized into 4 groups ; the ODR selects the maximum value determined by the decimation rate, and the ODR (kHz) in high-resolution mode and low-power mode is 2048/decimation rate and 512/decimation rate, respectively.

Depending on the selected mode, the device is configured to use an external or internal reference voltage source. Conversion data can be read back through the SPI interface or the data output interface, as shown in Table 6. If the data output interface is used to read back conversion data, the number of enabled DOUTx lines and the number of clocks required for Σ-Δ data transmission are determined by the logic levels of the CONV_SAR, FORMAT0, and FORMAT1 pins. In this case, the DCLK2, DCLK1, and DCLK0 pins select the Σ-Δ output interface and control the DCLKx divider function (a divisor of MCLK), as shown in Table 7. The DCLKx divider function sets the frequency of the data output interface DCLKx signal. The minimum DCLK frequency depends on the decimation rate and operating mode.

All pins that determine the SXA030 configuration mode are re-evaluated each time the SYNC_IN pin receives a pulse. A typical connection diagram for pin control mode is shown in Figure 37.

中文： 在引脚控制模式下，SXA030 根据模式引脚(MODE0、MODE1、MODE2、MODE3)上电时进行配置。这四个引脚设置 SXA030 的下列功能：工作模式、抽取率/ODR、PGA 增益和基准电压源，如表 6 所示。

由于模式引脚数量以及可用选项数量的限制，PGA 增益控制组成 4 个模块，ODR 选择抽取率所确定的最大值，高分辨率模式和低功耗模式下的 ODR (kHz)分别为 2048/抽取率和 512/抽取率。

根据所选模式，器件配置为使用外部或内部基准电压源。转换数据可通过 SPI 接口或数据输出接口回读，如表 6 所示。如果利用数据输出接口回读转换数据，则使能的 DOUTx 线数和 Σ-Δ 数据传输所需的时钟数由 CONV_SAR、FORMAT0 和 FORMAT1 引脚的逻辑电平决定。这种情况下，DCLK2、DCLK1 和 DCLK0 引脚选择 Σ-Δ 输出接口并控制 DCLKx 分频功能(MCLK 的约数)，如表 7 所示。DCLKx 分频功能设置数据输出接口 DCLKx 信号的频率。DCLK 最小频率取决于抽取率和工作模式。

确定 SXA030 配置模式的所有引脚在每次 SYNC_IN 引脚获得脉冲时都会重新评估。引脚控制模式的典型连接图如图 37 所示。

表5 数据接口格式 / Table 5. Data Interface Formats

CONV_SAR 状态 / CONV_SAR State	FORMAT1	FORMAT0	控制模式 / Control Mode	数据输出模式 / Data Output Mode
1	0	0	引脚 / Pin	SPI 输出 / SPI output
	0	1	引脚 / Pin	SPI 输出 / SPI output
	1	1	引脚 / Pin	SPI 输出 / SPI output
	1	1	SPI	寄存器 0x14 定义 / Defined by register 0x14
0	0	0	引脚 / Pin	DOUT0，通道 0 至通道 1；DOUT1，通道 2 至通道 3；DOUT2，通道 4 至通道 5；DOUT3，通道 5 至通道 7 / DOUT0, channels 0 to 1; DOUT1, channels 2 to 3; DOUT2, channels 4 to 5; DOUT3, channels 5 to 7
	0	1	引脚 / Pin	DOUT0，通道 0 至通道 3；DOUT1，通道 4 至通道 7 / DOUT0, channels 0 to 3; DOUT1, channels 4 to 7
	1	0	引脚 / Pin	DOUT0，通道 0 至通道 7 / DOUT0, channels 0 to 7
	1	1	SPI	寄存器 0x014 定义 / Defined by register 0x014

表6 引脚模式选择 / Table 6. Pin Mode Selection

MODE3	MODE2	MODE1	MODE0	抽取速率 / Decimation Rate	抽取速率类型 / Decimation Rate Type	PGA 增益通道 0 至通道 3 / PGA Gain, Channels 0 to 3	PGA 增益通道 4 至通道 7 / PGA Gain, Channels 4 to 7	基准电压源 / Reference Source
0	0	0	0	1024	高分辨率 / High resolution	1	1	外部 / External
0	0	0	1	512	高分辨率 / High resolution	1	1	外部 / External
0	0	1	0	256	高分辨率 / High resolution	1	1	外部 / External
0	0	1	1	128	高分辨率 / High resolution	1	1	外部 / External
0	1	0	0	256	高分辨率 / High resolution	1	2	外部 / External
0	1	0	1	512	高分辨率 / High resolution	1	4	外部 / External
0	1	1	0	256	高分辨率 / High resolution	1	4	外部 / External
0	1	1	1	128	高分辨率 / High resolution	1	4	外部 / External
1	0	0	0	512	高分辨率 / High resolution	1	1	内部 / Internal
1	0	0	1	256	高分辨率 / High resolution	1	1	内部 / Internal

MODE3	MODE2	MODE1	MODE0	抽取速率 / Decimation Rate	抽取速率类型 / Decimation Rate Type	PGA 增益通道 0 至通道 3 / PGA Gain, Channels 0 to 3	PGA 增益通道 4 至通道 7 / PGA Gain, Channels 4 to 7	基准电压源 / Reference Source
1	0	1	0	128	高分辨率 / High resolution	1	1	内部 / Internal
1	0	1	1	512	低功耗 / Low power	1	1	外部 / External
1	1	0	0	256	低功耗 / Low power	1	1	外部 / External
1	1	0	1	128	低功耗 / Low power	1	1	外部 / External
1	1	1	0	128	低功耗 / Low power	1	1	内部 / Internal
1	1	1	1	256	低功耗 / Low power	1	1	内部 / Internal

表7 引脚控制模式的 DCLKx 选择 / Table 7. DCLKx Selection in Pin Control Mode

DCLK2/SCLK 状态 / State	DCLK1/SDI 状态 / State	DCLK0/SDO 状态 / State	MCLK 分频器 / MCLK Divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

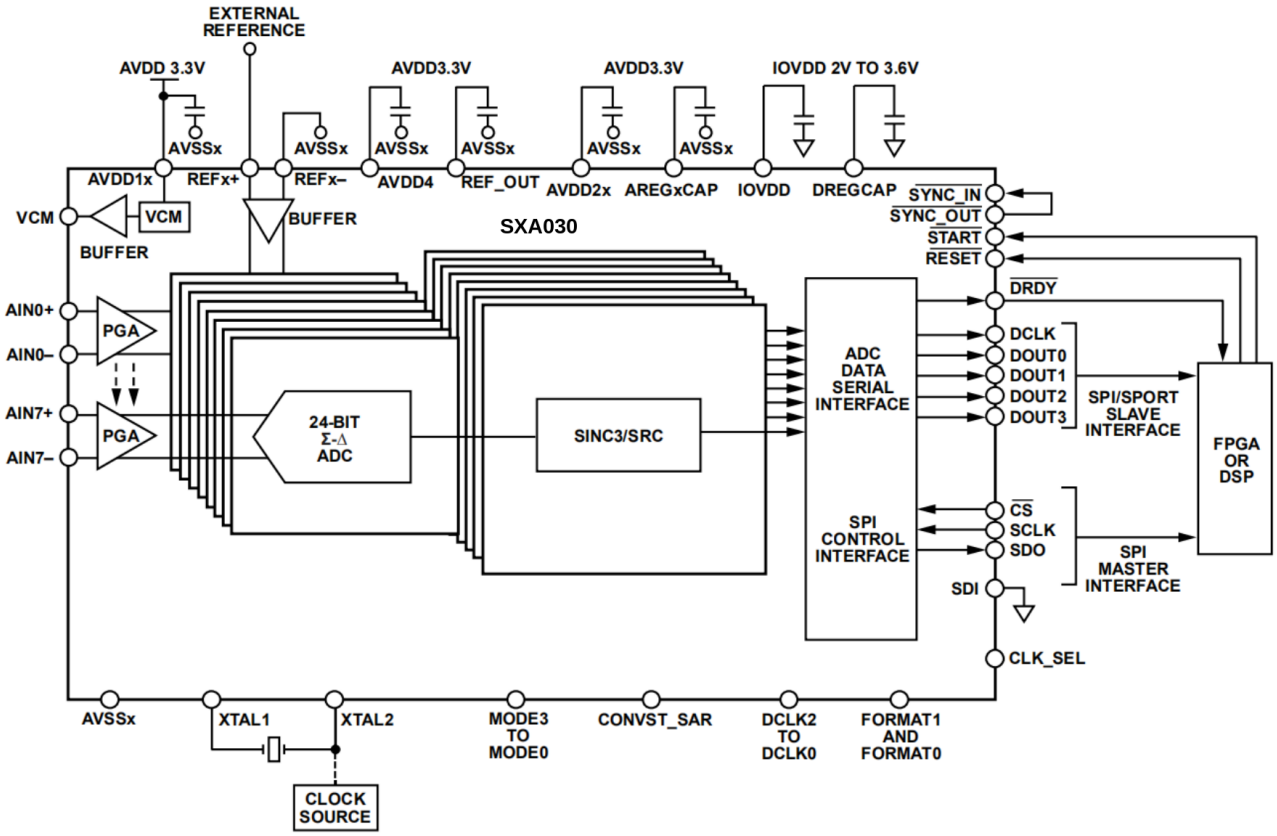


Figure 37: Pin-mode connection diagram using an external reference source

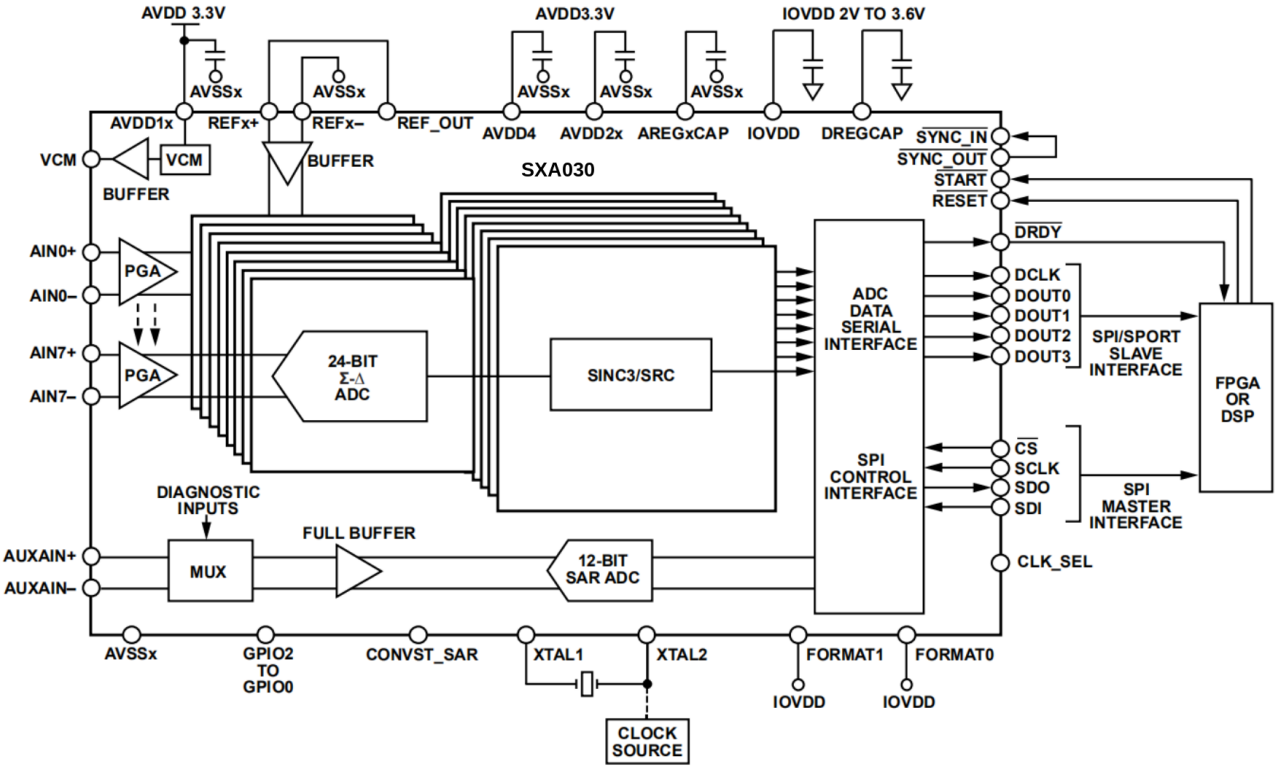


Figure 38: SPI control mode connection diagram using an internal reference source

13、SPI 控制 / 13. SPI Control

English: The second method of controlling and monitoring the SXA030 is through the SPI interface. This option enables the full functionality of the SXA030, including the SAR converter, phase synchronization, offset and gain adjustment, diagnostics, and SRC. To use SPI control, the FORMAT0 and FORMAT1 pins must be set to logic high.

In this mode, by setting the SPI_SLAVEMODE_EN bit, the SPI interface can also be used to read Σ-Δ conversion data.

A typical connection diagram for SPI control mode is shown in Figure 38, in which the SCLK frequency is up to 30MHz.

中文： 控制和监测 SXA030 的第二种方法是通过 SPI 接口。该选项可开启 SXA030 的全部功能，包括 SAR 转换器、相位同步、失调和增益调整、诊断以及 SRC。如需使用 SPI 控制，须将 FORMAT0 和 FORMAT1 引脚设为逻辑高电平。

在该模式下，通过置位 SPI_SLAVEMODE_EN 位，SPI 接口还可用于读取 Σ-Δ 转换数据。

SPI 控制模式的典型连接图如图 38 所示，其中 SCLK 频率最高为 30MHz。

English: Functions available in SPI mode: The SPI control mode of the SXA030 provides a rich set of functions and diagnostic capabilities.

中文： SPI 模式下的可用功能：SXA030 的 SPI 控制模式提供了丰富的功能集和诊断能力。

13.1、失调和增益矫正 / 13.1. Offset and Gain Correction

English: Offset and gain registers are provided for system calibration. The gain registers are preprogrammed during final production for a PGA gain of 1, but can be overwritten with new values if required.

The gain register is 24 bits long, split into 3 registers: CHx_GAIN_UPPER_BYTE, CHx_GAIN_MID_BYTE, and CHx_GAIN_LOWER_BYTE, with the gain set on a per-channel basis. The gain value is relative to 0x555555, which represents a gain of 1.

The offset register is 24 bits long, split into 3 byte registers: CHx_OFFSET_UPPER_BYTE, CHx_OFFSET_MID_BYTE, and CHx_OFFSET_LOWER_BYTE. The power-up default value is 0x000000. The offset shall be programmed as a signed 24-bit two's complement number. If the channel gain is set to the nominal value 0x555555, a 1 LSB adjustment of the offset register changes the digital output by −4/3 LSB.

A calibration example: the measured offset is −200 LSB (both AINx± pins connected to the same potential). An offset adjustment of −150 changes the digital output by −150 × (−4/3) = 200 LSB (gain value = 0x555555); expressed in two's complement this value is 0xFFFFFF –0x96 + 1 = 0xFFFF70. - CHx_OFFSET_UPPER_BYTE = 0xFF - CHx_OFFSET_MID_BYTE = 0xFF - CHx_OFFSET_LOWER_BYTE = 0x70

Note: offset compensation shall precede gain compensation. The gain is set at final test so that PGAGAIN = 1. The gain register values can be overwritten. However, after a reset or power cycling, the gain register values return to the hard-coded factory settings.

If the required gain is 0.75 of the nominal value (0x555555), the following value must be written: 0x555555 × 0.75 = 0x400000. In this way, a 1 LSB adjustment of the offset register changes the digital output by −4/3 ×0.75 = 1 LSB. - CHx_GAIN_UPPER_BYTE = 0x40 - CHx_GAIN_MID_BYTE = 0x00 - CHx_GAIN_LOWER_BYTE = 0x00

中文： 提供失调和增益寄存器，可用于系统校准。增益寄存器在最终生产期间预编程为 PGA 增益 1，但如有需要，可以用新值覆盖。

增益寄存器长度为 24 位，分割为 3 个寄存器：CHx_GAIN_UPPER_BYTE、CHx_GAIN_MID_BYTE 和 CHx_GAIN_LOWER_BYTE，以各通道为基础进行增益设置。增益值相对于 0x555555 而言，后者代表增益 1。

失调寄存器长度为 24 位，分割为 3 个字节寄存器：CHx_OFFSET_UPPER_BYTE、CHx_OFFSET_MID_BYTE 和 CHx_OFFSET_LOWER_BYTE。上电时的默认值为 0x000000。失调应编程设置为二进制补码带符号 24 位数。如果通道增益设置为标称值 0x555555，则失调寄存器调整的 1 LSB 将使数字输出改变−4/3 LSB。

举一个校准示例：失调测量值为−200 LSB(两个 AINx±引脚连接相同的电位)。失调调整−150 将使数字输出改变 −150 × (−4/3) = 200 LSB(增益值 = 0x555555)，此值表示为二进制补码即为 0xFFFFFF –0x96 + 1 = 0xFFFF70。 • CHx_OFFSET_UPPER_BYTE = 0xFF • CHx_OFFSET_MID_BYTE = 0xFF • CHx_OFFSET_LOWER_BYTE = 0x70

注意：失调补偿要先于增益补偿。增益在最终测试时设置，以使 PGAGAIN = 1。增益寄存器值可以覆盖。然而，在复位或周期供电之后，增益寄存器值会回到硬编码的出厂设置。

如果所需增益为标称值(0x555555)的 0.75，则必须写入如下值：0x555555 × 0.75 = 0x400000。这样，失调寄存器调整的 1 LSB 将使数字输出改变 −4/3 ×0.75 = 1 LSB。 • CHx_GAIN_UPPER_BYTE = 0x40 • CHx_GAIN_MID_BYTE = 0x00 • CHx_GAIN_LOWER_BYTE = 0x00

13.2、SPI 控制功能 / 13.2. SPI Control Functions

13.2.1、全局控制功能 / 13.2.1. Global Control Functions

English: The global control functions of the SXA030 are listed in detail below: - High-resolution and low-power operating modes - Output data rate: sample rate converter (SRC) - VCM buffer shutdown - Internal/external reference voltage source selection - Enable, precharge, or bypass reference voltage source buffer mode - Internal reference voltage source shutdown - SAR diagnostic multiplexing - SAR shutdown - GPIO write/read - SPI SAR conversion readback - SPI slave mode — read results - SDO and DOUT drive strength - DOUT mode - DCLK division - Internal LDO bypass - CRC protection: enable or disable

中文： 下面详细列出了 SXA030 的全局控制功能： • 高分辨率和低功耗工作模式 • 输出数据速率：采样速率转换器(SRC) • VCM 缓冲器关断 • 内部/外部基准电压源选择 • 使能、预充电或旁路基准电压源缓冲器模式 • 内部基准电压源关断 • SAR 诊断复用 • SAR 关断 • GPIO 写/读 • SPI SAR 转换回读 • SPI 从机模式—读取结果 • SDO 和 DOUT 驱动强度 • DOUT 模式 • DCLK 分频 • 内部 LDO 旁路 • CRC 保护：使能或禁用

13.2.2、各通道功能 / 13.2.2. Per-Channel Functions

English: The per-channel functions of the SXA030 are listed in detail below: - PGA gain. - Σ-Δ channel shutdown. - Phase delay: synchronous phase offset per channel. - Offset calibration. - Gain calibration. - Σ-Δ input signal multiplexing. - Channel error registers.

中文： 下面详细列出了 SXA030 的各通道功能： • PGA 增益。 • Σ-Δ 通道关断。 • 相位延迟：每通道的同步相位偏移。 • 失调校准。 • 增益校准。 • Σ-Δ 输入信号复用。 • 通道错误寄存器。

13.3、相位调整 / 13.3. Phase Adjustment

English: The SXA030 phase delay can be adjusted to compensate for inter-channel phase mismatch caused by phase errors of sensors or signal channels connected to the SXA030. Phase adjustment is implemented by programming the CHx_SYNC_OFFSET register. This programming delays the synchronization signal by a number of modulator clocks MOD_CLK, so as to initialize the digital filter of each Σ-Δ ADC separately.

The phase adjustment register is read during the pulse; any subsequent change to the register has no effect unless a pulse is generated.

The phase offset register is internally multiplied by a coefficient determined by the decimation rate, as shown in Table 8.

中文： 可以调节 SXA030 相位延迟，以补偿连接到 SXA030 的传感器或信号通道相位误差所导致的通道间相位失配。相位调整通过 CHx_SYNC_OFFSET 寄存器编程实现。这种编程将使同步信号延迟一定数量的调制器时钟 MOD_CLK，以便分别对每一个 Σ-Δ 型 ADC 的数字滤波器进行初始化。

在脉冲期间读取相位调整寄存器，之后的寄存器任何变化都不会有影响，除非生成一个脉冲。

相位失调寄存器内部乘以一个系数，该系数由抽取率决定，如表 8 所示。

表8 相位调整与抽取率 / Table 8. Phase Adjustment vs. Decimation Rate

相位调整补偿 / Phase Adjustment Compensation	抽取率 / Decimation Rate
X1	≤255
X2	≤511
X4	≤1023
X8	≤2047
X16	≤4095

English: The maximum phase delay must not equal or exceed the decimation rate. If it does, the value internally becomes the decimation rate value minus 1.

中文： 最大相位延迟不可等于或高于抽取率。若如此，该值会在内部变为抽取率值减 1。

13.4、PGA 增益 / 13.4. PGA Gain

English: By appropriately selecting bits [7:6] of the CHx_CONFIG register, the PGA gain can be independently selected, as shown in Table 9.

中文： 适当选择 CHx_CONFIG 寄存器的位[7:6]，便可独立选择 PGA 增益，如表 9 所示。

表9 通过 CHx_CONFIG 设置 PGA 增益 / Table 9. PGA Gain Setting via CHx_CONFIG

CHx_CONFIG	PGA 增益设置 / PGA Gain Setting
00	X1
01	X2
10	X4
11	X8

English: If the Σ-Δ reference voltage source is updated, it is recommended to apply a pulse to the pin to eliminate invalid samples during the reference voltage source transition.

中文： 如果更新 Σ-Δ 基准电压源，建议将一个脉冲施加于引脚，以消除基准电压源过渡期间的无效采样。

13.5、抽取 / 13.5. Decimation

English: The decimation determines the sampling frequency, as described below: - In high-resolution mode, sampling frequency = MCLK/(4 × decimation) - In low-power mode, sampling frequency = MCLK/(8 × decimation)

中文： 抽取决定了采样频率，如下所述： • 在高分辨率模式下，采样频率 = MCLK/(4 × 抽取) • 在低功耗模式下，采样频率 = MCLK/(8 × 抽取)

13.6、GPIO 引脚 / 13.6. GPIO Pins

English: If the SXA030 operates in SPI control mode, the mode pins serve as GPIO pins, as shown in Figure 39. The GPIO pins can be configured as input or output pins, regardless of the configuration order.

中文： 如果 SXA030 工作在 SPI 控制模式下，则模式引脚用作 GPIO 引脚，如图 39 所示。GPIO 引脚可配置为输入或输出引脚，与配置顺序无关。

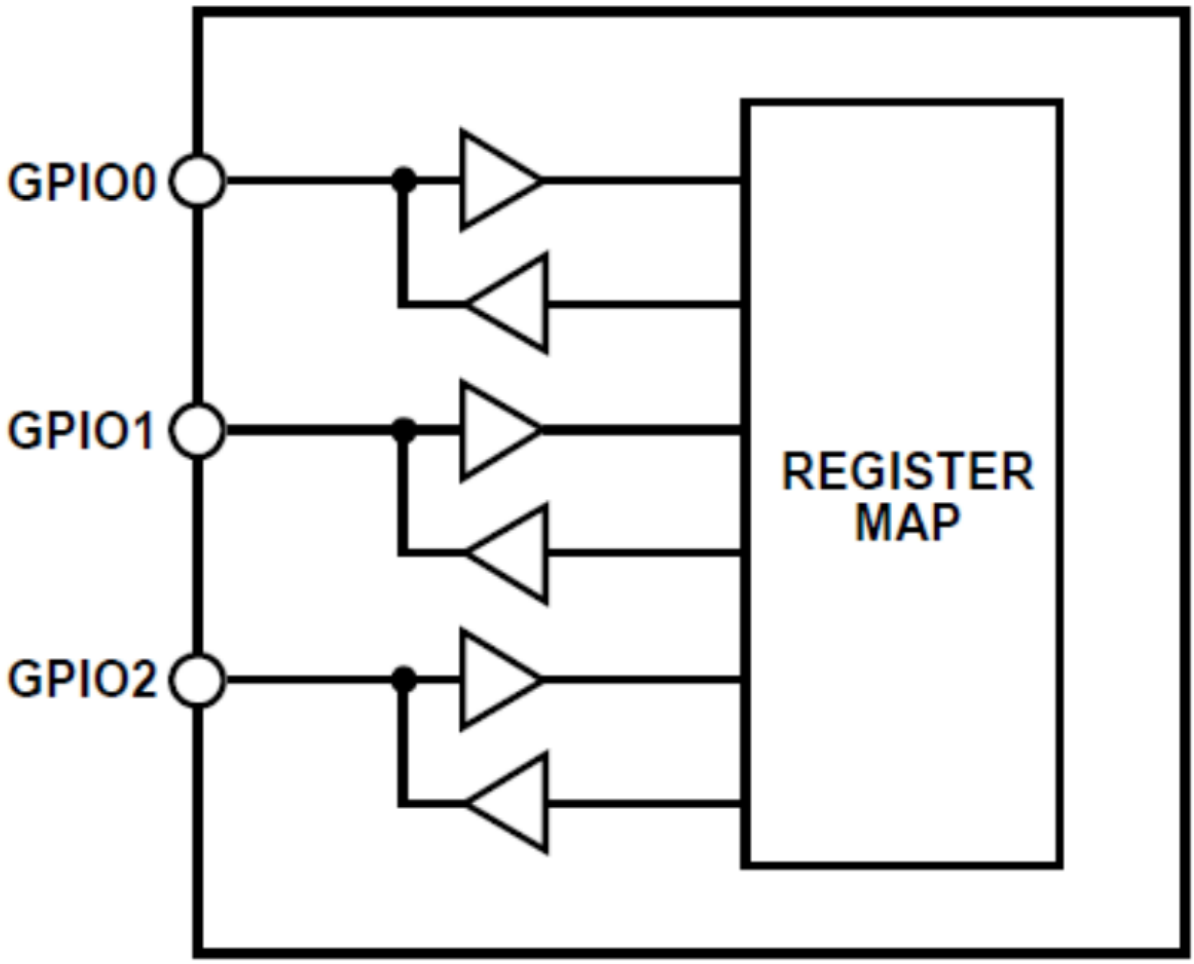


Figure 39: GPIO pin functions

English: The configuration control and readback of the GPIO pins are handled by bits [2:0] of the GPIO_CONFIG register (0 = input, 1 = output) and the GPIO_DATA register. In addition to these uses, the GPIO can also control the external multiplexer connected to the SAR ADC auxiliary input. Use this multiplexer to verify the results of the Σ-Δ ADC.

In addition, the GPIO pins can be used to externally trigger a new decimation rate.

中文： GPIO 引脚的配置控制和回读由 GPIO_CONFIG 寄存器的位2:0和 GPIO_DATA 寄存器来处理。除了这些用途，GPIO 还可控制连接 SAR ADC 辅助输入的外部复用。使用此多路复用器来验证 Σ-Δ 型 ADC 的结果。

另外，GPIO 引脚可用于外部触发新的抽取率。

13.7、Σ-Δ 基准电压源设置 / 13.7. Σ-Δ Reference Voltage Source Setting

English: The SXA030 can operate with an internal or external reference voltage source. In addition, when performing diagnostics, the analog supply can be used as the reference voltage source, as shown in Table 10.

中文： SXA030 可采用内部或外部基准电压源工作。此外，当进行诊断时，模拟电源可以用作基准电压源，如表 10 所示。

表10 Σ-Δ 基准电压源 / Table 10. Σ-Δ Reference Voltage Sources

ADC_MUX_CONFIG 位[7:6]的设置 / ADC_MUX_CONFIG Bits[7:6] Setting	通道 0 至通道 3 / Channels 0 to 3	通道 4 至通道 7 / Channels 4 to 7
00	REF1+/REF1−	REF2+/REF2−
01	内部基准电压源 / Internal reference source	内部基准电压源 / Internal reference source
10	AVDD1A/AVSS1A	AVDD1B/AVSS1B
11	REF1−/REF1+	REF2−/REF2+

English: The operation of the reference voltage source buffer is described in Table 11. The selected reference voltage source and buffer operating mode affect all channels.

If the reference voltage source is updated, it is recommended to apply a pulse to the SYNC_IN pin to eliminate invalid samples during the reference voltage source transition.

中文： 基准电压源缓冲器的工作情况说明参见表 11。选中的基准电压源和缓冲器工作模式影响所有通道。

如果更新基准电压源，建议将一个脉冲施加于 SYNC_IN 引脚，以消除基准电压源过渡期间的无效采样。

表11 基准电压源缓冲器工作模式 / Table 11. Reference Voltage Source Buffer Operating Modes

基准电压源缓冲器工作模式 / Reference Buffer Operating Mode	REFx+	REFx−
使能 / Enable	BUFFER_CONFIG_1，位 4 = 1；BUFFER_CONFIG_2，位 7 = 0 / BUFFER_CONFIG_1, bit 4 = 1; BUFFER_CONFIG_2, bit 7 = 0	BUFFER_CONFIG_1，位 3 = 1；BUFFER_CONFIG_2，位 6 = 0 / BUFFER_CONFIG_1, bit 3 = 1; BUFFER_CONFIG_2, bit 6 = 0
预充电 / Precharge	BUFFER_CONFIG_1，位 4 = 1；BUFFER_CONFIG_2，位 7 = 1 / BUFFER_CONFIG_1, bit 4 = 1; BUFFER_CONFIG_2, bit 7 = 1	BUFFER_CONFIG_1，位 3 = 1；BUFFER_CONFIG_2，位 6 = 1 / BUFFER_CONFIG_1, bit 3 = 1; BUFFER_CONFIG_2, bit 6 = 1
禁用 / Disable	BUFFER_CONFIG_1，位 4 = 0 / BUFFER_CONFIG_1, bit 4 = 0	BUFFER_CONFIG_1，位 3 = 0 / BUFFER_CONFIG_1, bit 3 = 0

表12 可额外禁用的关断模块 / Table 12. Additional Shutdown Modules That Can Be Disabled

模块 / Module	寄存器 / Register	注释 / Notes
VCM	GENERAL_USER_CONFIG_1，位 5 / bit 5	默认使能 / Enabled by default
基准电压源缓冲器 / Reference buffer	BUFFER_CONFIG_1，位[4:3] / bits[4:3]	默认为预充电模式 / Precharge mode by default
内部基准电压源缓冲器 / Internal reference buffer	GENERAL_USER_CONFIG_1，位 4 / bit 4	默认禁用 / Disabled by default
Σ-Δ 通道 / Σ-Δ channels	CH_DISABLE，位[7:0] / bits[7:0]	

模块 / Module	寄存器 / Register	注释 / Notes
		默认通道使能 / Channels enabled by default
SAR	GENERAL_USER_CONFIG_1，位 3 / bit 3	默认禁用 / Disabled by default
内部振荡器 / Internal oscillator	GENERAL_USER_CONFIG_1，位 2 / bit 2	默认使能 / Enabled by default

13.8、功耗模式 / 13.8. Power Modes

English: The SXA030 provides different power modes to improve power efficiency, namely high-resolution mode and low-power mode, which can be controlled via bit 6 of GENERAL_USER_CONFIG_1. To further reduce power consumption, other modules can also be independently disabled, as shown in Table 12.

When the power mode changes, a pulse must be applied to the SYNC_IN pin.

中文： SXA030 提供不同功耗模式来改善电源效率，即高分辨率模式和低功耗模式，这可通过 GENERAL_USER_CONFIG_1 的位 6 来控制。如需进一步降低功耗，还可独立禁用其他模块，如表 12 所示。

功耗模式改变时，需要将一个脉冲施加于 SYNC_IN 引脚。

13.9、LDO 旁路 / 13.9. LDO Bypass

English: The internal LDOs can be independently bypassed, applying an external supply directly to the AREG1CAP, AREG2CAP, or DREGCAP pins. Table 13 shows the minimum and maximum supply voltages for these pins, and the related registers used to bypass the regulators.

中文： 内部 LDO 可以独立旁路，而将外部电源直接施加于 AREG1CAP、AREG2CAP 或 DREGCAP 引脚。表 13 显示了这些引脚的最小和最大电源电压，以及用来旁路稳压器的相关寄存器。

表13 LDO 旁路 / Table 13. LDO Bypass

LDO	BUFFER_CONFIG_2，位[2:0][1] / BUFFER_CONFIG_2, Bits[2:0][1]	电源最大值(V) / Supply Maximum (V)	电源最小值(V) / Supply Minimum (V)
AREG1CAP	1XX	1.9	1.85
AREF1CAP	X1X	1.9	1.85
DREGCAP	XX1	1.98	1.65

[1] X 表示无关。/ [1] X indicates don't care.

14、数字 SPI 接口 / 14. Digital SPI Interface

English: The SPI serial interface of the SXA030 consists of four signals: CS, SDI, SCLK, and SDO. A typical connection diagram of the SPI interface is shown in Figure 40.

中文： SXA030 的 SPI 串行接口由四个信号组成：CS、SDI、SCLK 和 SDO。SPI 接口的典型连接图如图 40 所示。

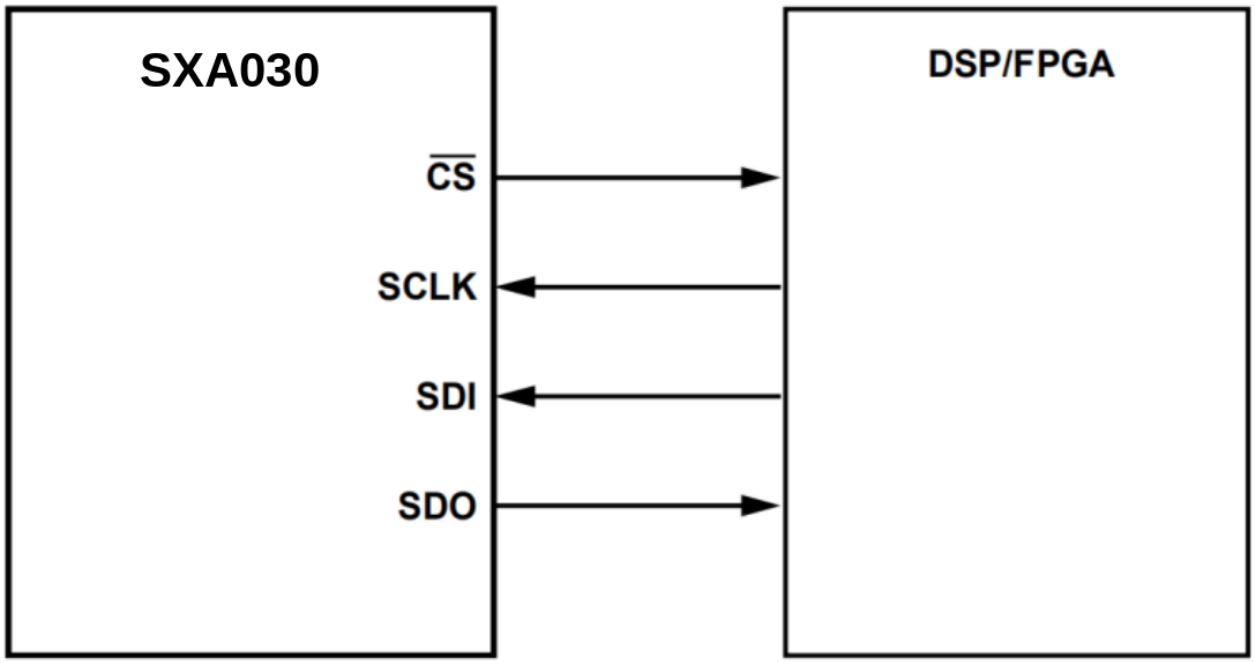


Figure 40: SPI control interface — SXA030 as SPI slave, digital signal processor (DSP) / field-programmable gate array (FPGA) as master

English: The SPI interface operates in mode 0 and mode 3, CPOL = 0, CPHA = 0 (mode 0) or CPOL = 1, CPHA = 1 (mode 3).

In pin control mode, SDI can be used to read back results, depending on the level of the CONV_SAR pin, as shown in Table 5.

In SPI control mode, the SPI interface transfers data to the on-chip registers, and SDO reads back data from the on-chip registers, or reads SAR or Σ-Δ conversion results, depending on the selected operating mode.

In SPI control mode, the SDO data source is determined by the registers GENERAL_USER_CONFIG_2 and GENERAL_USER_CONFIG_3, as shown in Table 14.

中文： SPI 接口工作在模式 0 和模式 3，CPOL = 0、CPHA = 0(模式 0)或 CPOL = 1、CPHA = 1(模式 3)。

在引脚控制模式下，SDI 可用来回读结果，具体取决于 CONV_SAR 引脚的电平，如表 5 所示。

在 SPI 控制模式下，SPI 接口将数据传输至片内寄存器，而 SDO 从片内寄存器回读数据，或者读取 SAR 或 Σ-Δ 转换结果，具体取决于所选工作模式。

SPI 控制模式下的 SDO 数据源由寄存器 GENERAL_USER_CONFIG_2 和 GENERAL_USER_CONFIG_3 决定，如表 14 所示。

表14 SPI 控制模式下的 SPI 工作模式 / Table 14. SPI Operating Modes in SPI Control Mode

GENERAL_USER_CONFIG_2 位 5 设置 / GENERAL_USER_CONFIG_2 Bit 5 Setting	GENERAL_USER_CONFIG_3 位 4 设置 / GENERAL_USER_CONFIG_3 Bit 4 Setting	模式 / Mode
AREG1CAP	0	内部寄存器 / Internal registers

GENERAL_USER_CONFIG_2 位 5 设置 / GENERAL_USER_CONFIG_2 Bit 5 Setting	GENERAL_USER_CONFIG_3 位 4 设置 / GENERAL_USER_CONFIG_3 Bit 4 Setting	模式 / Mode
AREF1CAP	1	Σ-Δ 数据转换 / Σ-Δ data conversion
DREGCAP	X	SAR 转换 / SAR conversion

English: In SPI control mode, the SDO pin has four different levels of I/O strength, selectable via bits [4:3] of GENERAL_USER_CONFIG_2, as shown in Table 15.

中文： 在 SPI 控制模式下，SDO 引脚具有四种不同电平的 I/O 强度，可通过 GENERAL_USER_CONFIG_2 的位[4:3]选择，如表 15 所示。

表15 SPI 控制模式下的 SPI 工作模式 / Table 15. SPI Operating Modes in SPI Control Mode

GENERAL_USER_CONFIG_2，位[4:3]设置 / GENERAL_USER_CONFIG_2 Bits[4:3] Setting		模式 / Mode
0	0	标称值 / Nominal
0	1	强 / Strong
1	0	弱 / Weak
1	1	极强 / Very strong

English: SCLK is the serial clock input of this device. All data transfers (whether on SDO or SDI) are relative to this SCLK signal.

The SPI interface can handle multiples of 8 bits. For example, in SPI control mode, if the SDO pin is used to read back data from the internal registers or the SAR ADC, the data frame is 16 bits wide (CRC disabled, as shown in Figure 41) or 24 bits wide (CRC enabled, as shown in Figure 42). In this case, the controller can generate 1 frame of 16-bit/24-bit data (CRC enabled and disabled), or 2/3 frames of 8-bit data (CRC enabled and disabled). When the SDO pin is used to read back data from the Σ-Δ channels, 64 bits must be read back from the controller (in this case, the controller can generate 1 frame of 64-bit data — 2 × 32 bits, 4 × 16 bits, or 8 × 8 bits).

中文： SCLK 是该器件的串行时钟输入。所有数据传输(无论是 SDO 上还是 SDI 上)均相对于该 SCLK 信号进行。

SPI 接口可处理 8 位的倍数。例如，在 SPI 控制模式下，若 SDO 引脚用于从内部寄存器或 SAR ADC 回读数据，则数据帧为 16 位宽(CRC 禁用，如图 41 所示)或 24 位宽(CRC 使能，如图 42 所示)。这种情况下，控制器可产生 1 帧的 16 位/24 位数据(CRC 使能和禁用)，或 2/3 帧的 8 位数据(CRC 使能和禁用)。当 SDO 引脚用于从 Σ-Δ 通道回读数据时，必须从控制器回读 64 位(这种情况下，控制器可产生 1 帧的 64 位数据—2 × 32 位、4 × 16 位或 8 × 8 位)。

14.1、SPI CRC—校验和保护(SPI 控制模式) / 14.1. SPI CRC — Checksum Protection (SPI Control Mode)

English: The SXA030 has a checksum mode that can be used to improve the robustness of the SPI interface in SPI control mode. Using a checksum ensures that only valid data is written to the registers, and that data read from the device can be verified. Setting the SPI_CRC_TEST_EN bit enables SPI CRC. If an error occurs during a register write, the SPI_CRC_ERR of the error register is set.

Enabling the SPI_CRC_TEST_EN bit causes the CRC checksum to be performed on all R/W operations. When SPI_CRC_TEST_EN is enabled, for SAR and register map operations, an 8-bit CRC word is appended to each SPI transaction.

To ensure a successful register write, it is recommended to read back the register and verify the checksum.

The CRC checksum calculation always uses the following polynomial: x8 + x2 + x + 1.

中文： SXA030 具有校验和模式，可用来改善 SPI 控制模式下的 SPI 接口鲁棒性。使用校验和可确保仅将有效数据写入寄存器，并且可以对从器件读取的数据进行验证。置位 SPI_CRC_TEST_EN 位即可使能 SPI CRC。如果寄存器写入期间发生错误，错误寄存器的 SPI_CRC_ERR 会置位。

使能 SPI_CRC_TEST_EN 位将导致 CRC 校验和对所有 R/W 操作执行。当 SPI_CRC_TEST_EN 使能时，对于 SAR 和寄存器映射操作，每次 SPI 处理都会附加一个 8 位 CRC 字。

为确保寄存器写入成功，建议回读寄存器并验证校验和。

CRC 校验和计算始终使用如下多项式：x8 + x2 + x + 1。

14.2、SPI 读/写寄存器模式(SPI 控制模式) / 14.2. SPI Register Read/Write Mode (SPI Control Mode)

English: The SXA030 is configured and controlled through on-chip registers. These registers have a 7-bit address — the 7-bit register address on the SDI line is used to select the register for the read/write function. This 7-bit register address follows the R/W bit in the SDI data. If the SPI transfer is a write operation transfer, the 8 bits following the 7-bit register address on the SDI line are the data to be written to the selected register. Data on the SDI line is read into the SXA030 on the SCLK rising edge.

During an SPI transfer, the data on the SDO line contains an 8-bit 0010 0000 header: 8-bit register data (read (R) operation) or eight zeros (write (W) operation).

When CRC is disabled, the basic data frame on the SDI line during transfer is 16 bits long, as shown in Figure 41. When CRC is enabled, the minimum frame length required for an SPI transfer is 24 SCLK. The 24-bit data on the SDO line consists of an 8-bit header (0010 0000), 8-bit data, and an 8-bit CRC (see Figure 42).

中文： SXA030 通过片内寄存器来配置和控制器件。这些寄存器具有 7 位地址—SDI 线路上的 7 位寄存器地址用来选择读/写功能的寄存器。该 7 位寄存器地址在 SDI 数据中的 R/W 位之后。如果 SPI 传输是写操作传输，则 SDI 线路上的 7 位寄存器地址之后的 8 位是待写入所选寄存器的 数据。SDI 线路上的数据在 SCLK 上升沿读入 SXA030。

SPI 传输期间，SDO 线路上的数据包含 8 位 0010 0000 报头：8 位寄存器数据(读(R)操作)或 8 个零(写 (W)操作)。

CRC 禁用时，传输期间 SDI 线路上的基本数据帧为 16 位长，如图 41 所示。CRC 使能时，SPI 传输要求的最小帧长度为 24 SCLK。SDO 线路上的 24 位数据由 8 位报头(0010 0000)、8 位数据和 8 位 CRC 组成(见图 42)。

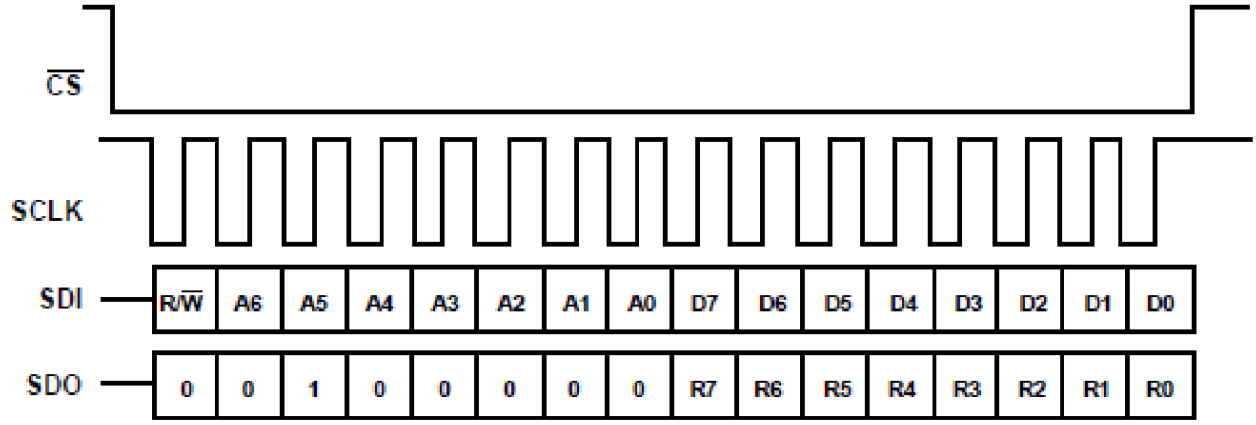


Figure 41: 16-bit SPI transfer — CRC disabled

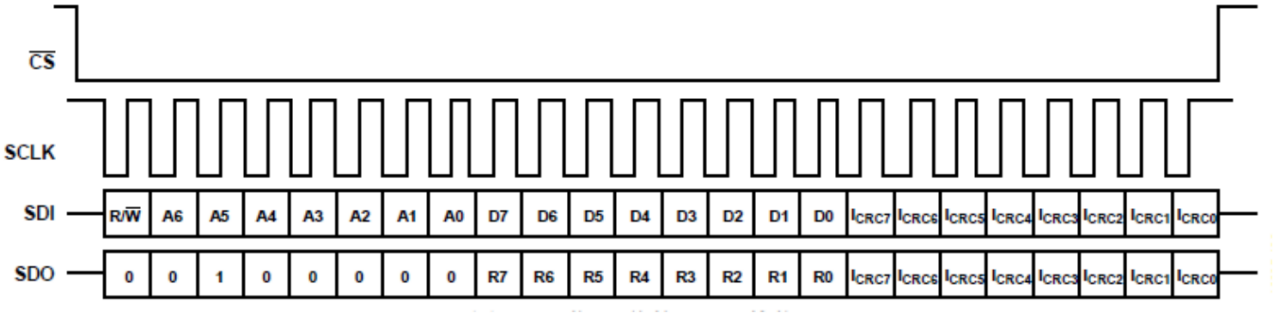


Figure 42: 24-bit SPI transfer — CRC enabled

14.3、SPI SAR 诊断模式(SPI 控制模式) / 14.3. SPI SAR Diagnostic Mode (SPI Control Mode)

English: Setting bit 5 in the GENERAL_USER_CONFIG_2 register configures the SDO line to shift out data from SAR ADC conversions, as shown in Table 14.

In SAR mode, the SXA030 internal registers can be written, but all readback commands are ignored, because the SDO data frame is dedicated to shifting out conversion results from the SAR ADC.

To exit this operating mode, reset bit 5 of the GENERAL_USER_CONFIG_2 register.

During an SPI transfer, if CRC is disabled, the data on the SDO line contains a 4-bit 0010 header and a 12-bit SAR conversion result.

When CRC is enabled, the minimum frame length required for an SPI transfer is 24 SCLK. The 24-bit data on the SDO line consists of a 4-bit header (0010), 12-bit data, and an 8-bit CRC, as shown in Figure 43.

According to the SPI register read/write mode (see the "SPI Register Read/Write Mode" section), the SDI line contains the R/W bit, a 7-bit register address, 8-bit data, and an 8-bit CRC (if enabled). When reading back SAR conversion results via the SDO line, to avoid unnecessarily writing to the internal registers, it is recommended to send a readback command to the device, such as 0x8000, which will be ignored because the SDO pin is being used to shift out the contents of the SAR ADC.

If the SAR ADC performs conversions continuously, the previous conversion result shall be read back before a new conversion result is generated, otherwise the result will be corrupted.

中文： 置位 GENERAL_USER_CONFIG_2 寄存器中的位 5 可将 SDO 线路配置为移出来自 SAR ADC 转换的数据，如表 14 所示。

在 SAR 模式下，SXA030 内部寄存器可以写入，但会忽略一切回读命令，因为 SDO 数据帧专用于从 SAR ADC 移出转换结果。

如需退出此工作模式，请复位 GENERAL_USER_CONFIG_2 寄存器的位 5。

SPI 传输期间，若 CRC 禁用，则 SDO 线路上的数据包含 4 位 0010 报头和 12 位 SAR 转换结果。

CRC 使能时，SPI 传输要求的最小帧长度为 24 SCLK。SDO 线路上的 24 位数据由 4 位报头(0010)、12 位数据和 8 位 CRC 组成，如图 43 所示。

根据 SPI 读/写寄存器模式(参见"SPI 读/写寄存器模式"部分)，SDI 线路包含 R/W 位、7 位寄存器地址、8 位数据和 8 位 CRC(若使能)。当通过 SDO 线路回读 SAR 转换结果时，为了避免不必要地写入内部寄存器，建议向器件发送一个回读命令，如 0x8000，该命令会被忽略，因为 SDO 引脚正用于移出 SAR ADC 的内容。

如果 SAR ADC 连续执行转换，应在产生新转换结果之前回读前一转换的结果，否则结果会被破坏。

14.4、Σ-Δ 数据，ADC 模式 / 14.4. Σ-Δ Data, ADC Mode

English: In pin control mode, the SPI interface can be used to read back Σ-Δ conversion results, as shown in Table 5. In SPI control mode, by setting bit 4 of GENERAL_USER_CONFIG_3, the SPI interface can read back conversion results, as shown in Table 14. In this mode, the SXA030 internal registers can be written, but all readback commands are ignored, because the SDO data frame is dedicated to shifting out conversion results from the Σ-Δ ADC. To avoid unnecessarily writing to the internal registers, it is recommended to send a readback command to the device, such as 0x8000, which will be ignored because the SDO pin is being used to shift out the contents of the Σ-Δ ADC.

The SDO pin data can be read back in any multiple of 8 bits, for example 64 bits, 2 × 32 bits, 4 × 16 bits, or 8 × 8 bits.

中文： 在引脚控制模式下，SPI 接口可用来回读 Σ-Δ 转换结果，如表 5 所示。在 SPI 控制模式下，通过置位 GENERAL_USER_CONFIG_3 的位 4，SPI 接口便可回读转换结果，如表 14 所示。在此模式下，SXA030 内部寄存器可以写入，但会忽略一切回读命令，因为 SDO 数据帧专用于从 Σ-ΔADC 移出转换结果。为了避免不必要地写入内部寄存器，建议向器件发送一个回读命令，如 0x8000，该命令会被忽略，因为 SDO 引脚正用于移出 Σ-Δ ADC 的内容。

SDO 引脚数据可以 8 位的任意倍数回读，例如 64 位、2 × 32 位、4 × 16 位或 8 × 8 位。

14.5、SPI 软件复位 / 14.5. SPI Software Reset

English: If the SDI pin is held high for 64 consecutive clocks, a software reset is generated.

中文： 若在连续 64 个时钟期间让 SDI 引脚保持高电平，则会产生软件复位。

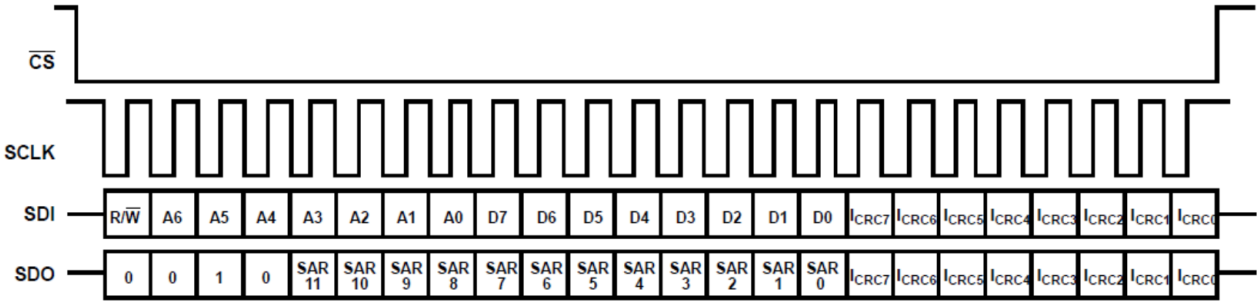


Figure 43: SAR ADC / diagnostic mode — CRC enabled

寄存器 / Registers

English: The register table is summarized as follows.

中文： 寄存器表汇总如下。

寄存器 / Register	名称 / Name	位 / Bits	主要位域 / Principal Bit Fields	复位 / Reset	R/W
0x000	CH0_CONFIG	[7:0]	CH0_GAIN, CH0_REF_MONITOR, CH0_RX, 保留 / Reserved	0x00	/WR
0x001	CH1_CONFIG	[7:0]	CH1_GAIN, CH1_REF_MONITOR, CH1_RX, 保留 / Reserved	0x00	R/W
0x002	CH2_CONFIG	[7:0]	CH2_GAIN, CH2_REF_MONITOR, CH2_RX, 保留 / Reserved	0x00	R/W
0x003	CH3_CONFIG	[7:0]	CH3_GAIN, CH3_REF_MONITOR, CH3_RX, 保留 / Reserved	0x00	R/W
0x004	CH4_CONFIG	[7:0]	CH4_GAIN, CH4_REF_MONITOR, CH4_RX, 保留 / Reserved	0x00	R/W
0x005	CH5_CONFIG	[7:0]	CH5_GAIN, CH5_REF_MONITOR, CH5_RX, 保留 / Reserved	0x00	R/W
0x006	CH6_CONFIG	[7:0]	CH6_GAIN, CH6_REF_MONITOR, CH6_RX, 保留 / Reserved	0x00	R/W
0x007	CH7_CONFIG	[7:0]	CH7_GAIN, CH7_REF_MONITOR, CH7_RX, 保留 / Reserved	0x00	R/W
0x008	CH_DISABLE	[7:0]	CH7_DISABLE, CH6_DISABLE, CH5_DISABLE, CH4_DISABLE, CH3_DISABLE, CH2_DISABLE, CH1_DISABLE, CH0_DISABLE	0x00	R/W
0x009	CH0_SYNC_OFFSET	[7:0]	CH0_SYNC_OFFSET	0x00	R/W
0x00A	CH1_SYNC_OFFSET	[7:0]	CH1_SYNC_OFFSET	0x00	R/W
0x00B	CH2_SYNC_OFFSET	[7:0]	CH2_SYNC_OFFSET	0x00	R/W
0x00C	CH3_SYNC_OFFSET	[7:0]	CH3_SYNC_OFFSET	0x00	R/W

寄存器 / Register	名称 / Name	位 / Bits	主要位域 / Principal Bit Fields	复位 / Reset	R/W
0x00D	CH4_SYNC_OFFSET	[7:0]	CH4_SYNC_OFFSET	0x00	R/W
0x00E	CH5_SYNC_OFFSET	[7:0]	CH5_SYNC_OFFSET	0x00	R/W
0x00F	CH6_SYNC_OFFSET	[7:0]	CH6_SYNC_OFFSET	0x00	R/W
0x010	CH7_SYNC_OFFSET	[7:0]	CH7_SYNC_OFFSET	0x00	R/W
0x011	GENERAL_USER_CONFIG_1	[7:0]	ALL_CH_DIS_MCLK_EN, POWER_MODE, PDB_VCM, PDB_REFOUT_BUF, PDB_SAR, PDB_RC_OSC, SOFT_RESET	0x24	R/W
0x012	GENERAL_USER_CONFIG_2	[7:0]	保留 / Reserved, SDO_DRIVE_STR, DOUT_DRIVE_STR, SPI_SYNC_MODE_EN	0x09	R/W
0x013	GENERAL_USER_CONFIG_3	[7:0]	CONVST_DEGLITCH_DIS, 保留 / Reserved, MODE_EN, QUAL_DIS	0x80	R/W
0x014	DOUT_FORMAT	[7:0]	DOUT_FORMAT, DOUT_HEADER_FORMAT, 保留 / Reserved		
0x015	ADC_MUX_CONFIG	[7:0]	REF_MUX_CTRL, MTR_MUX_CTRL, 保留 / Reserved	0x00	R/W
0x016	GLOBAL_MUX_CONFIG	[7:0]	GLOBAL_MUX_CTRL, 保留 / Reserved	0x00	R/W
0x017	GPIO_CONFIG	[7:0]	保留 / Reserved, GPIO_OP_EN	0x00	R/W
0x018	GPIO_DATA	[7:0]	IO_WRITE_DATA	0x00	R/W
0x019	BUFFER_CONFIG_1	[7:0]	保留 / Reserved, REF_BUF_POS_EN, REF_BUF_NEG_EN, 保留 / Reserved		
0x01A	BUFFER_CONFIG_2	[7:0]	REF_BUFP_PREQ, REF_BUFN_PREQ, RESERVED, PDB_ALDO1_OVRDRV, PDB_ALDO2_OVRDRV, PDB_DLDO_OVRDRV	0xC0	R/W
0x01C	CH0_OFFSET_UPPER_BYTE	[7:0]	CH0_OFFSET_ALL[23:16]	0x00	R/W
0x01D	CH0_OFFSET_MID_BYTE	[7:0]	CH0_OFFSET_ALL[15:8]	0x00	R/W
0x01E	CH0_OFFSET_LOWER_BYTE	[7:0]	CH0_OFFSET_ALL[7:0]	0x00	R/W
0x01F	CH0_GAIN_UPPER_BYTE	[7:0]	CH0_GAIN_ALL[23:16]	0x00	R/W
0x020	CH0_GAIN_MID_BYTE	[7:0]	CH0_GAIN_ALL[15:8]	0x00	R/W
0x021	CH0_GAIN_LOWER_BYTE	[7:0]	CH0_GAIN_ALL[7:0]	0x00	R/W
0x022	CH1_OFFSET_UPPER_BYTE	[7:0]	CH1_OFFSET_ALL[23:16]	0x00	R/W
0x023	CH1_OFFSET_MID_BYTE	[7:0]	CH1_OFFSET_ALL[15:8]	0x00	

寄存器 / Register	名称 / Name	位 / Bits	主要位域 / Principal Bit Fields	复位 / Reset	R/W
					R/W
0x024	CH1_OFFSET_LOWER_BYTE	[7:0]	CH1_OFFSET_ALL[7:0]	0x00	R/W
0x025	CH1_GAIN_UPPER_BYTE	[7:0]	CH1_GAIN_ALL[23:16]	0x00	R/W
0x026	CH1_GAIN_MID_BYTE	[7:0]	CH1_GAIN_ALL[15:8]	0x00	R/W
0x027	CH1_GAIN_LOWER_BYTE	[7:0]	CH1_GAIN_ALL[7:0]	0x00	R/W
0x028	CH2_OFFSET_UPPER_BYTE	[7:0]	CH2_OFFSET_ALL[23:16]	0x00	R/W
0x029	CH2_OFFSET_MID_BYTE	[7:0]	CH2_OFFSET_ALL[15:8]	0x00	R/W
0x02A	CH2_OFFSET_LOWER_BYTE	[7:0]	CH2_OFFSET_ALL[7:0]	0x00	R/W
0x02B	CH2_GAIN_UPPER_BYTE	[7:0]	CH2_GAIN_ALL[23:16]	0x00	R/W
0x02C	CH2_GAIN_MID_BYTE	[7:0]	CH2_GAIN_ALL[15:8]	0x00	R/W
0x02D	CH2_GAIN_LOWER_BYTE	[7:0]	CH2_GAIN_ALL[7:0]	0x00	R/W
0x02E	CH3_OFFSET_UPPER_BYTE	[7:0]	CH3_OFFSET_ALL[23:16]	0x00	R/W
0x02F	CH3_OFFSET_MID_BYTE	[7:0]	CH3_OFFSET_ALL[15:8]	0x00	R/W
0x030	CH3_OFFSET_LOWER_BYTE	[7:0]	CH3_OFFSET_ALL[7:0]	0x00	R/W
0x031	CH3_GAIN_UPPER_BYTE	[7:0]	CH3_GAIN_ALL[23:16]	0x00	R/W
0x032	CH3_GAIN_MID_BYTE	[7:0]	CH3_GAIN_ALL[15:8]	0x00	R/W
0x033	CH3_GAIN_LOWER_BYTE	[7:0]	CH3_GAIN_ALL[7:0]	0x00	R/W
0x034	CH4_OFFSET_UPPER_BYTE	[7:0]	CH4_OFFSET_ALL[23:16]	0x00	R/W
0x035	CH4_OFFSET_MID_BYTE	[7:0]	CH4_OFFSET_ALL[15:8]	0x00	R/W
0x036	CH4_OFFSET_LOWER_BYTE	[7:0]	CH4_OFFSET_ALL[7:0]	0x00	R/W
0x037	CH4_GAIN_UPPER_BYTE	[7:0]	CH4_GAIN_ALL[23:16]	0x00	R/W
0x038	CH4_GAIN_MID_BYTE	[7:0]	CH4_GAIN_ALL[15:8]	0x00	

寄存器 / Register	名称 / Name	位 / Bits	主要位域 / Principal Bit Fields	复位 / Reset	R/W
					R/W
0x039	CH4_GAIN_LOWER_BYTE	[7:0]	CH4_GAIN_ALL[7:0]	0x00	R/W
0x03A	CH5_OFFSET_UPPER_BYTE	[7:0]	CH5_OFFSET_ALL[23:16]	0x00	R/W
0x03B	CH5_OFFSET_MID_BYTE	[7:0]	CH5_OFFSET_ALL[15:8]	0x00	R/W
0x03C	CH5_OFFSET_LOWER_BYTE	[7:0]	CH5_OFFSET_ALL[7:0]	0x00	R/W
0x03D	CH5_GAIN_UPPER_BYTE	[7:0]	CH5_GAIN_ALL[23:16]	0x00	R/W
0x03E	CH5_GAIN_MID_BYTE	[7:0]	CH5_GAIN_ALL[15:8]	0x00	R/W
0x03F	CH5_GAIN_LOWER_BYTE	[7:0]	CH5_GAIN_ALL[7:0]	0x00	R/W
0x040	CH6_OFFSET_UPPER_BYTE	[7:0]	CH6_OFFSET_ALL[23:16]	0x00	R/W
0x041	CH6_OFFSET_MID_BYTE	[7:0]	CH6_OFFSET_ALL[15:8]	0x00	R/W
0x042	CH6_OFFSET_LOWER_BYTE	[7:0]	CH6_OFFSET_ALL[7:0]	0x00	R/W
0x043	CH6_GAIN_UPPER_BYTE	[7:0]	CH6_GAIN_ALL[23:16]	0x00	R/W
0x044	CH6_GAIN_MID_BYTE	[7:0]	CH6_GAIN_ALL[15:8]	0x00	R/W
0x045	CH6_GAIN_LOWER_BYTE	[7:0]	CH6_GAIN_ALL[7:0]	0x00	R/W
0x046	CH7_OFFSET_UPPER_BYTE	[7:0]	CH7_OFFSET_ALL[23:16]	0x00	R/W
0x047	CH7_OFFSET_MID_BYTE	[7:0]	CH7_OFFSET_ALL[15:8]	0x00	R/W
0x048	CH7_OFFSET_LOWER_BYTE	[7:0]	CH7_OFFSET_ALL[7:0]	0x00	R/W
0x049	CH7_GAIN_UPPER_BYTE	[7:0]	CH7_GAIN_ALL[23:16]	0x00	R/W
0x04A	CH7_GAIN_MID_BYTE	[7:0]	CH7_GAIN_ALL[15:8]	0x00	R/W
0x04B	CH7_GAIN_LOWER_BYTE	[7:0]	CH7_GAIN_ALL[7:0]	0x00	R/W
0x04C	CH0_ERR_REG	[7:0]	保留 / Reserved, CH0_ERR_AINM_UV, CH0_ERR_AINM_OV, CH0_ERR_AINP_UV, CH0_ERR_AINP_OV, CH0_ERR_REF_DET	0x00	R
0x04D	CH1_ERR_REG	[7:0]		0x00	R

寄存器 / Register	名称 / Name	位 / Bits	主要位域 / Principal Bit Fields	复位 / Reset	R/W
			保留 / Reserved, CH1_ERR_AINM_UV, CH1_ERR_AINM_OV, CH1_ERR_AINP_UV, CH1_ERR_AINP_OV, CH1_ERR_REF_DET		
0x04E	CH2_ERR_REG	[7:0]	保留 / Reserved, CH2_ERR_AINM_UV, CH2_ERR_AINM_OV, CH2_ERR_AINP_UV, CH2_ERR_AINP_OV, CH2_ERR_REF_DET	0x00	R
0x04F	CH3_ERR_REG	[7:0]	保留 / Reserved, CH3_ERR_AINM_UV, CH3_ERR_AINM_OV, CH3_ERR_AINP_UV, CH3_ERR_AINP_OV, CH3_ERR_REF_DET	0x00	R
0x050	CH4_ERR_REG	[7:0]	保留 / Reserved, CH4_ERR_AINM_UV, CH4_ERR_AINM_OV, CH4_ERR_AINP_UV, CH4_ERR_AINP_OV, CH4_ERR_REF_DET	0x00	R
0x051	CH5_ERR_REG	[7:0]	保留 / Reserved, CH5_ERR_AINM_UV, CH5_ERR_AINM_OV, CH5_ERR_AINP_UV, CH5_ERR_AINP_OV, CH5_ERR_REF_DET	0x00	R
0x052	CH6_ERR_REG	[7:0]	保留 / Reserved, CH6_ERR_AINM_UV, CH6_ERR_AINM_OV, CH6_ERR_AINP_UV, CH6_ERR_AINP_OV, CH6_ERR_REF_DET	0x00	R
0x053	CH7_ERR_REG	[7:0]	保留 / Reserved, CH7_ERR_AINM_UV, CH7_ERR_AINM_OV, CH7_ERR_AINP_UV, CH7_ERR_AINP_OV, CH7_ERR_REF_DET	0x00	R
0x054	CH0_1_SAT_ERR	[7:0]	保留 / Reserved, CH1_ERR_MOD_SAT, CH1_ERR_FILTER_SAT, CH1_ERR_OUTPUT_SAT, CH0_ERR_MOD_SAT, CH0_ERR_FILTER_SAT, CH0_ERR_OUTPUT_SAT	0x00	R
0x055	CH2_3_SAT_ERR	[7:0]	保留 / Reserved, CH3_ERR_MOD_SAT, CH3_ERR_FILTER_SAT, CH3_ERR_OUTPUT_SAT, CH2_ERR_MOD_SAT, CH2_ERR_FILTER_SAT, CH2_ERR_OUTPUT_SAT	0x00	R
0x056	CH4_5_SAT_ERR	[7:0]	保留 / Reserved, CH5_ERR_MOD_SAT, CH5_ERR_FILTER_SAT, CH5_ERR_OUTPUT_SAT, CH4_ERR_MOD_SAT, CH4_ERR_FILTER_SAT, CH4_ERR_OUTPUT_SAT	0x00	R
0x057	CH6_7_SAT_ERR	[7:0]	保留 / Reserved, CH7_ERR_MOD_SAT, CH7_ERR_FILTER_SAT, CH7_ERR_OUTPUT_SAT, CH6_ERR_MOD_SAT, CH6_ERR_FILTER_SAT, CH6_ERR_OUTPUT_SAT	0x00	R
0x058	CHX_ERR_REG_EN	[7:0]	OUTPUT_SAT_TEST_EN, FILTER_SAT_TEST_EN, MOD_SAT_TEST_EN, AINM_UV_TEST_EN, AINM_OV_TEST_EN, AINP_UV_TEST_EN, AINP_OV_TEST_EN, REF_DET_TEST_EN	0xFE	R/W
0x059	GEN_ERR_REG_1	[7:0]	保留 / Reserved, ROM_CRC_ERR, SPI_CLK_COUNT_ERR, SPI_INVALID_READ_ERR, SPI_INVALID_WRITE_ERR, SPI_CRC_ERR	0x00	R
0x05A	GEN_ERR_REG_1_EN	[7:0]	保留 / Reserved, ROM_CRC_TEST_EN, SPI_CLK_COUNT_TEST_EN, SPI_INVALID_READ_TEST_EN, SPI_INVALID_WRITE_TEST_EN, SPI_CRC_TEST_EN	0x3E	R/W
0x05B	GEN_ERR_REG_2	[7:0]	保留 / Reserved, EXT_MCLK_SWITCH_ERR, RESERVED, ALDO1_PSM_ERR, ALDO2_PSM_ERR, DLDO_PSM_ERR	0x00	R
0x05C	GEN_ERR_REG_2_EN	[7:0]	保留 / Reserved, EXT_MCLK_SWITCH_DETECT_EN	0x00	R
0x060	SRC_N_MSB	[7:0]	保留 / Reserved, SRC_N_ALL[11:8]	0x00	R/W
0x061	SRC_N_LSB	[7:0]	SRC_N_ALL[7:0]	0x80	R/W
0x062	SRC_IF_MSB	[7:0]	SRC_IF_ALL[15:8]	0x00	R/W
0x063	SRC_IF_LSB	[7:0]	SRC_IF_ALL[7:0]	0x00	

寄存器 / Register	名称 / Name	位 / Bits	主要位域 / Principal Bit Fields	复位 / Reset	R/W
					R/W
0x064	SRC_UPDATE	[7:0]	SRC_LOAD_SOURCE, 保留 / Reserved, SRC_LOAD_UPDATE	0x00	R/W

电源地间保护 / Power-to-Ground Protection

English: To improve the anti-static capability of the device, the following ESD protection loops exist between the various supply pins inside the device. The forward conduction voltage drop of each ESD protection device is approximately 0.3V; during power-up and normal use, prolonged forward conduction of these ESD protection devices should be avoided.

中文： 为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.3V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。

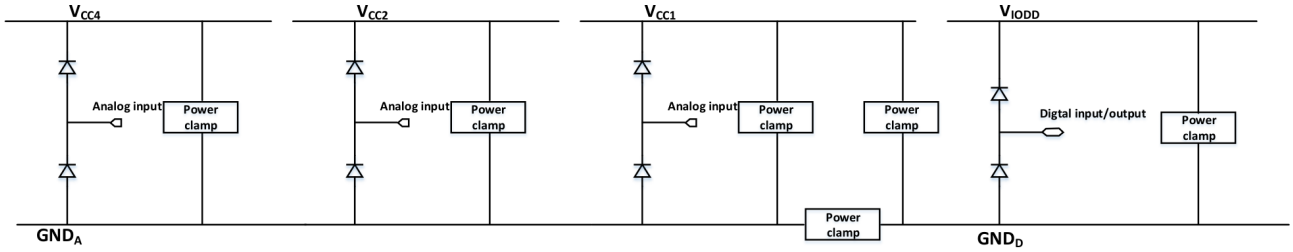


Figure 44: Internal ESD protection circuits between supplies

注意事项 / Precautions

1、产品安装注意事项 / 1. Product Installation Precautions

English: 1) Pay attention to device orientation during soldering to avoid soldering it in the wrong orientation. 2) Instruments and meters used for debugging the circuit must share a good common ground. PCB design must maintain good grounding and power-supply decoupling. 3) Take care not to reverse the power supply or short the input/output ends to the power supply, which can easily damage the circuit.

中文： 1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2、产品使用注意事项 / 2. Product Usage Precautions

English: 1) It is recommended to reset the circuit first after power-up before use. 2) It is recommended to pay attention to the ambient temperature during actual use, and to pay attention to heat dissipation. 3) If the input signal exceeds the input rating range, after it returns to the normal input range, a data-path soft reset is recommended. 4) Pay attention to all ports marked with positive and negative signs (such as REF1±, etc.); use them accurately according to the positive and negative markings. 5) If a change in the circuit peripheral configuration (such as a non-continuous change in input clock frequency, a sudden

interruption of the input clock, or a supply voltage exceeding the rating) causes an interruption of ADC functionality, the circuit may be in an abnormal state caused by the peripheral configuration change; even if the peripheral configuration returns to normal again, the circuit may still remain in a non-normal operating state. Therefore, after the peripheral configuration has stabilized, it is recommended to soft-reset the data path (register 0x011[1:0] first write 0x11 then write 0x10), so as to ensure normal ADC operation. 6) For the supply voltage range, refer to the Recommended Operating Conditions section. 7) Do not use beyond the maximum limit conditions of the product, otherwise irreversible damage to the circuit will result. 8) The circuit operating frequency is 1.3MHz~8.192MHz. 9) The heat sink is analog ground; unused pins are recommended to be left floating. 10) It is recommended to filter the power supply, and to appropriately isolate the analog and digital supplies.

中文： 1) 推荐上电后首先对电路进行复位，再进行使用。 2) 建议实际使用时关注环境温度，并注意散热。 3) 如果输入信号超出输入额定范围，当恢复到正常输入范围后，建议数据路径软复位。 4) 注意所有标注了正负的端口（如 REF1±等），请准确按照正负标注使用。 5) 如果电路外围配置变化（如输入时钟频率非连续变化、输入时钟突然中断或者电源电压超出额定值等情况），导致 ADC 功能中断，电路可能处于因外围配置变化而导致的异常状态，即使外围配置重新恢复正常，电路任然可能处于非正常工作状态。因此，建议外围配置稳定后，对数据路径软复位（0x011[1:0]寄存器先写 0x11 再写 0x10），从而保证 ADC 正常工作。 6) 供电电压范围参考推荐工作条件部分。 7) 不能超过产品最大限定条件使用，否者将会对电路造成不可逆的损坏。 8) 电路工作频率为 1.3MHz~8.192MHz。 9) 热沉为模拟地，未使用引脚建议悬空。 10) 建议对电源进行滤波，且将模拟和数字电源进行适当隔离。

3、产品防护注意事项 / 3. Product Protection Precautions

English: 1) Storage temperature and humidity and environmental requirements for the finished-product warehouse: temperature 10°C～25°C, relative humidity 25%～70%, electrostatic discharge sensitivity Class 1C (1000~1999V). All pins of this circuit have ESD protection structures; however, high-energy electrical pulses can still damage the circuit, so ESD protection should be observed during testing, handling, and storage. 2) Product storage period: counted from the inspection batch identification code date; when warehoused products have been stored for more than 36 months, the products shall be stored in a special cabinet for expired products, and the products must pass re-inspection before they can be used. 3) It is recommended to use within 4 hours after unpacking; if exposed to air for more than 4 hours, it is recommended to perform high-temperature baking at 150°C for 8h, then vacuum-package and store in a dry cabinet. 4) Avoid dropping during use to avoid mechanical stress damage. 5) Exceeding the absolute maximum ratings may cause permanent damage to the device. The maximum ratings do not indicate that the device can operate normally under these conditions or under any other conditions beyond those shown in this product manual. Long-term operation under absolute maximum rating conditions will affect the reliability of the device. 6) Plastic-packaged circuits easily absorb moisture, causing delamination; keep the surrounding environment dry during use, and store vacuum-packaged at room temperature in a dry environment.

中文： 1) 成品库贮存的温湿度和环境要求：温度 10°C～25°C，相对湿度 25%～70%、静电放电敏感度 1C 等级（1000~1999V）。该电路所有引出端均有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 2) 产品贮存期：从检验批识别代码日期算起，入库产品贮存期超过 36 个月时产品应归入超期产品专柜存放，产品须复检合格后方能使用。 3) 建议拆封后 4 小时内使用，如在空气中暴露超过 4 小时，建议进行 150°C，8h 的高温烘焙后抽真空包装，放置于干燥柜中存放。 4) 在使用过程中应避免跌落以免造成机械应力损伤。 5) 超出绝对最大额定值可能会导致器件永久性损坏。额定最大值不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。长期在绝对最大额定值条件下工作会

影响器件的可靠性。 6) 塑封电路易吸潮导致分层，使用时应注意保持周围环境干燥，存储时应真空包装储存于常温、干燥环境下。

4、电装说明 / 4. Assembly Instructions

English: 1) The moisture sensitivity level of this product is MSL3. After removing the product from the moisture-barrier bag, performing dry storage, or baking, the allowable floor life before reflow soldering is: ≤30°C/60RH%, 168h; 2) If device storage conditions cannot be controlled or traced, bake strictly at 125°C for 8h before assembly; 3) If the assembly environment temperature/humidity cannot be guaranteed at ≤30°C/60RH%, complete soldering within 12h after baking; 4) After baking, the product is highly susceptible to static electricity; observe ESD protection throughout all operations; 5) For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C~235°C; the maximum peak temperature should not exceed 235°C; time within ±5°C of the peak temperature ≤20s; time above liquidus 60~90s. Ramp-up rate 2~4°C/s, ramp-down rate 2~6°C/s; 6) For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C~245°C; the maximum peak temperature should not exceed 260°C; time within ±5°C of the peak temperature ≤20s; time above liquidus 60~90s. Ramp-up rate 2~4°C/s, ramp-down rate 2~6°C/s; 7) If a mixed assembly process requires elevated temperature, ensure the device body temperature does not exceed 260°C (device body temperature is measured at the top surface of the device during reflow); 8) The solder terminal surface treatment of this product is nickel-palladium-gold, but with a content of less than 3%, no gold brittleness will occur, and no tinning is required; 9) If there is a mandatory tinning requirement, perform tinning in accordance with the national aerospace industry standard QJ3267, Process Technical Requirements for Tinning of Electronic Components. Note that the device must be dried before tinning, the tinning temperature setting shall not exceed 300°C, the heating time per side of the quad pins shall be less than 5s, the heat-sink surface heating time shall be less than 30s, and the number of tinning operations shall not exceed 1.

中文： 1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； 3) 若电装环境温湿度无法保证≤30°C/60RH%，请在烘烤后 12h 内完成焊接； 4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s。升温速率 2~4°C/s，降温速率 2~6°C/s； 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s。升温速率 2~4°C/s，降温速率 2~6°C/s； 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）； 8) 本产品焊接端表面处理方式为镍钯金，但含量小于 3%，不会出现金脆现象，不需要搪锡； 9) 若有强制搪锡需求，按《国家航天行业标准 QJ3267 电子元器件搪锡工艺技术要求》标准进行搪锡。应注意搪锡前器件需烘干，搪锡设置温度不超过 300°C，四边引脚每边受热时间小于 5s，热沉表面受热时间小于 30s，搪锡次数不超过 1 次。

5、热阻 / 5. Thermal Resistance

表16 封装热阻 / Table 16. Package Thermal Resistance

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard and Method
	21.41 K/W	JESD51-2 得到 / Obtained per JESD51-2

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)		
Rthjt(结到器件顶面的热阻) / Rthjt (junction-to-package-top thermal resistance)	1.283 K/W	JESD51-14 得到 / Obtained per JESD51-14
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-package-bottom thermal resistance)	1.461 K/W	JESD51-14 拐点理论得到 / Obtained per the JESD51-14 inflection-point theory

常见故障及处理办法 / Common Faults and Troubleshooting

English: 1. No output signal: check whether the clock pins have clock input, check whether the power and ground signal connections are normal, and ensure the input voltage and reference voltage are accurate; 2. Output data jitter: check the external circuit and connections, and ensure the reference voltage is stable. 3. Unstable device operation: check the power supply and ensure the supply voltage is stable.

中文： 1、无输出信号：检查时钟引出端是否有时钟输入，检查电源、地信号连接是否正常，保证输入电压、基准电压准确； 2、输出数据抖动：检查外部电路和连接，保证基准电压稳定。 3、器件工作不稳定：检查电源，保证电源电压稳定。

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附加说明 / Additional Notes

English: 1. First release date of this manual: August 2026. 2. Product status: ☑ Production (this model is currently in production; formal products are available). ☐ Pre-release (this model has not yet entered formal production; samples are available). 3. Model suffix difference explanation (for series products, explain model suffixes as in the example below; add this section when needed): None. 4. Cross-reference notes vs. the foreign product: The power-supply absolute maximum ratings of the SXA030 are consistent with the foreign product; the recommended power-supply operating conditions are consistent with the foreign product except as noted ; the outline dimensions are consistent with the foreign product; the dynamic range DR in low-power mode and the spurious-free dynamic range SFDR in high-performance mode are lower than the foreign product; the integral nonlinearity, offset error, and gain error specifications are slightly higher than the foreign product; the operating temperature range is consistent with the foreign product. The SXA030 is pin-compatible with the foreign product and can achieve a functional replacement of the foreign product. For a detailed description of the main functions of the foreign product, refer to the foreign product datasheet; where there is any inconsistency with the foreign product datasheet, this product manual shall prevail. If you have any questions, please contact technical support personnel to obtain technical support.

中文： 1. 本说明书首次发布日期：2026 年 8 月。 2. 本产品状态：☑生产 （该产品型号目前已在生产，可以提供正式产品） □预发布（该产品型号尚未投入正式生产，可以提供样品） 3. 型号后缀差异性说明（系列化产品需对型号后缀说明如下示例，需要时增加此部分）：无 4. 替代国外产品情况说明：SXA030 电源绝对最大额定值与国外产品一致，电源推荐工作条件除以外与国外产品一致，外形尺寸与国外产品一致，低功耗模式的动态范围 DR 和高性能模式的无杂散动态范围 SFDR 比国外产品低，积分非线性、失调误差和增益误差指标略高于国外产品，工作温度范围与国外产品一致。SXA030 与国外产品管脚兼容，可实现对国外产品的功能替换。国外产品主要功能的详细描述可以参考国外产品数据手册，当与国外产品数据手册不一致时，以本产品说明书为准，如有疑问请联系技术支持人员，以获得技术支持。

1）绝对最大额定值对比 / 1) Absolute Maximum Ratings Comparison

附表1 绝对最大额定值对比 / Appendix Table 1. Absolute Maximum Ratings Comparison

参数 / Parameter	SXA030 规范要求 / SXA030 Specification	国外产品器件手册 / Foreign Product Datasheet	比对结果 / Comparison Result
VCC1	3.96V	3.96V	一致 / Consistent
VCC2	3.96V	3.96V	一致 / Consistent
VCC4	3.96V	3.96V	一致 / Consistent
VIODD	3.96V	3.96V	一致 / Consistent

2）推荐工作条件对比 / 2) Recommended Operating Conditions Comparison

附表2 推荐工作条件对比 / Appendix Table 2. Recommended Operating Conditions Comparison

参数 / Parameter	SXA030 规范要求 / SXA030 Specification	国外产品器件手册 / Foreign Product Datasheet	比对结果 / Comparison Result
VCC1	3.0V~3.6V	3.0V~3.6V	一致 / Consistent
VCC2	3.0V~3.6V	2.0V~3.6V	一致 / Consistent
VCC4	3.0V~3.6V	3.0V~3.6V	一致 / Consistent
VIODD	1.8V~3.6V	1.8V~3.6V	一致 / Consistent
工作温度范围（性能）/ Operating temperature range (performance)	-40°C≤TA≤125°C	-40°C≤TA≤105°C	有差异 / Different
工作温度范围（功能）/ Operating temperature range (functional)	-40°C≤TA≤125°C	-40°C≤TA≤125°C	一致 / Consistent

3）性能指标对比 / 3) Performance Specifications Comparison

附表3 主要性能指标对比 / Appendix Table 3. Main Performance Specifications Comparison

参数 / Parameter	条件 / Conditions	SXA030（TA=-40°C~125°C，MCLK=8192 KSPS）— 最小 / Min	SXA030 — 典型值 / Typ	SXA030 — 最大 / Max	国外产品（器件手册）（TA=-40°C~105°C，MCLK=8192 KSPS）— 最小 / Min	国外产品 — 典型值 / Typ	国外产品 — 最大 / Max	单位 / Unit	比对结果 / Comparison Result
信噪比 / SNR	PGA=1，fIN=60Hz	100	105	--	--	--	--	dB	/

参数 / Parameter	条件 / Conditions	SXA030（TA=-40℃~125℃，MCLK=8192 KSPS）— 最小 / Min	SXA030 — 典型值 / Typ	SXA030 — 最大 / Max	国外产品（器件手册）（TA=-40℃~105℃，MCLK=8192 KSPS）— 最小 / Min	国外产品 — 典型值 / Typ	国外产品 — 最大 / Max	单位 / Unit	比对结果 / Comparison Result
信噪比 / SNR	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	95	100	--	--	--	--	dB	/
信噪失真比 / SINAD	PGA=1，fIN=60Hz	95	103	--	--	106	--	dB	基本一致 / Essentially consistent
信噪失真比 / SINAD	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	93	99	--	--	--	--	dB	/
总谐波失真 / THD	PGA=1，fIN=60Hz	--	-110	-100	--	-109	--	dB	基本一致 / Essentially consistent
总谐波失真 / THD	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	--	-106	-98	--	-105	--	dB	基本一致 / Essentially consistent
无杂散动态范围 / SFDR	PGA=1，fIN=60Hz	90	113	--	--	132	--	dB	有差异 / Different
无杂散动态范围 / SFDR	PGA=1，fIN=60Hz，MCLK=4096KHz，低功耗模式 / low-power mode	90	108	--	--	--	--	dB	/
积分非线性 / INL	TA=25°C	-15	±5	15	-15	±7	15	ppm	有差异 / Different
积分非线性 / INL	TA=-55°C、125°C	-150	--	150				ppm	
失调误差 / Offset error	TA=25°C	-150	±90	150	-125	±40	125	μV	有差异 / Different
失调误差 / Offset error	TA=-55°C、125°C	-300	--	300				μV	
增益误差 / Gain error	TA=25°C	-0.5	±0.2	0.5	--	±0.1	--	%FS	基本一致 / Essentially consistent
增益误差 / Gain error	TA=-55°C、125°C	-1	--	1	--	--	--	%FS	
基准电压 / Reference voltage	TA=25°C	2.45	2.5	2.55	2.495	2.5	2.505	V	有差异 / Different

参数 / Parameter	条件 / Conditions	SXA030（TA=-40℃~125℃，MCLK=8192 KSPS）— 最小 / Min	SXA030 — 典型值 / Typ	SXA030 — 最大 / Max	国外产品（器件手册）（TA=-40℃~105℃，MCLK=8192 KSPS）— 最小 / Min	国外产品 — 典型值 / Typ	国外产品 — 最大 / Max	单位 / Unit	比对结果 / Comparison Result
功耗 / Power consumption	8 通道 / 8 channels	--	285	500	--	--	--	mW	/
信噪比（SAR ADC）/ SNR (SAR ADC)	TA=25°C	60	63	--	--	66	--	dBFS	基本一致 / Essentially consistent

注：SXA030、国外产品典型值均为常温实测值，SXA030 极限值为规范要求，国外某产品极限值为数据手册值。/ Note: the typical values of both the SXA030 and the foreign product are room-temperature measured values; the SXA030 limit values are specification requirements, and the limit values of the foreign product are datasheet values.

English: A comparison of measured data under the same conditions shows that the spurious-free dynamic range SFDR of the SXA030 in high-performance mode is lower than that of the foreign product, the integral nonlinearity, offset error, and gain error specifications are slightly higher than those of the foreign product, and the operating temperature range (performance) is wider than that of the foreign product.

中文： 相同条件下的实测数据对比结果表明，SXA030 高性能模式的无杂散动态范围 SFDR 比国外产品低，积分非线性、失调误差和增益误差指标略高于国外产品，工作温度范围（性能）比国外产品宽。

5）寄存器对比 / 5) Register Comparison

English: None.

中文： 无。

6）其它指标对比 / 6) Other Parameter Comparison

附表4 其它指标对比 / Appendix Table 4. Other Parameter Comparison

参数 / Parameter	SXA030	国外产品 / Foreign Product	比对结果 / Comparison Result
封装形式 / Package	QFN64	LFCSP64（QFN64）	一致 / Consistent
质量等级 / Quality grade	企标级 / Enterprise standard grade	工业级 / Industrial grade	有差异 / Different
尺寸 / Dimensions	9mm×9mm×0.75mm	9mm×9mm×0.75mm	一致 / Consistent
替代建议 / Cross-reference recommendation	☐直接替代 / ☐Direct replacement ☐有效替代 / ☐Effective alternative ☑功能替代 / ☑Functional alternative		

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