SXA031

Quad 16-Bit, 125 MSPS A/D Converter

四通道 16 位 125MSPS A/D 转换器

16-bit | 4 channels | 125 MSPS | QFN48 | Serial LVDS

16位 | 四通道 | 125MSPS | QFN48 | 串行LVDS

对标 / Cross Reference: AD9653 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

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SXA031 Quad-Channel 16-Bit 125MSPS A/D Converter — Product Manual (Bilingual)

SXA031 型四通道 16 位 125MSPS A/D 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深信科技 **V1.20260727**

对标 / Cross Reference: AD9653 — pin-to-pin compatible alternative

目录 / Table of Contents

1. 产品用途及应用范围 / Applications and Scope
2. 标准 / Standards
3. 产品特点 / Features
4. 产品描述 / Product Description
5. 产品外形图和实物图片 / Package Outline and Product Photos
6. 引出端排列（俯视图）/ Pin Arrangement (Top View)
7. 引出端功能符号表 / Pin Function Table
8. 绝对最大额定值 / Absolute Maximum Ratings
9. 推荐工作条件 / Recommended Operating Conditions
10. 性能指标 / Performance Specifications
11. 主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)
12. 典型应用线路图 / Typical Application Circuit
13. 单元模块及工作原理 / Functional Blocks and Operating Principles
14. 寄存器 / Registers
15. 电源地间保护 / Power-to-Ground Protection
16. 注意事项 / Precautions
17. 常见故障及处理办法 / Common Faults and Troubleshooting
18. 联系方式 / Contact Information
19. 附加说明 / Additional Notes

版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20270727	2026.7.27	——	首次发布 / Initial release	

产品用途及应用范围 / Applications and Scope

Medical imaging; high-speed imaging; radio receivers; portable measurement equipment.

医疗成像；高速成像；无线电接受机；便携式测量设备。

标准 / Standards

Detailed specification and approval number: Q/GC 0208-2026 — Detailed Specification for Semiconductor Integrated Circuit SXA031 Quad-Channel 16-Bit 125MSPS A/D Converter. Quality grade: enterprise standard.

详细规范及确认号：Q/GC 0208-2026 《半导体集成电路 SXA031 型四通道 16 位 125MSPS A/D 转换器详细规范》；质量等级：企标。

产品特点 / Features

- Analog supply voltage: 1.8V - Digital supply voltage: 1.8V - Resolution: 16bit - Conversion rate: 125MSPS - Signal-to-noise ratio (SNR): ≥76.5dBFS - Spurious-free dynamic range (SFDR): ≥93dBFS - Differential nonlinearity error (DNL): ±0.5LSB - Integral nonlinearity error (INL): ±5.0LSB - Power consumption: ≤150mW per channel - Analog input range: 2VPP~2.6VPP - Circuit interface: LVDS - ESD rating: Class 1C, HBM model, 1000V - Product weight: 0.20g±0.04g - Moisture sensitivity level and package: MSL3, QFN48

- 模拟电源电压：1.8V - 数字电源电压：1.8V - 分辨率：16bit - 转换速率：125MSPS - 信噪比：≥76.5dBFS - 无杂散动态范围：≥93dBFS - 微分线性误差：±0.5LSB - 积分线性误差：±5.0LSB - 功耗：≤150mW/每通道 - 模拟输入范围：2VPP～2.6VPP - 电路接口：LVDS - ESD 等级：1C 级，HBM 模型，1000V - 产品重量：0.20g±0.04g - 湿敏等级和封装形式：MSL3，QFN48

产品描述 / Product Description

This product is a 4-channel, 16-bit analog-to-digital converter (ADC) with a 125 MSPS sampling rate, developed specifically for low power consumption, small size, and application flexibility. The device supports conversion rates up to 125 MSPS, with excellent dynamic performance and ultra-low power characteristics, suitable for a wide range of applications.

The ADC operates from a single 1.8 V supply with an LVPECL/CMOS/LVDS-compatible sampling clock signal. No external reference source or drivers are required.

Each internal channel can be independently powered down; with all channels disabled, typical power consumption is less than 14 mW. The ADC integrates multiple functions, including programmable clock output, data alignment, and generation of digital test patterns. Available digital test patterns include built-in fixed test patterns and pseudo-random test patterns, and user-defined test patterns via the serial port interface (SPI) are also supported.

This product is packaged in a 48-pin plastic quad flat no-lead package (QFN48) with outline dimensions of 7.0 mm (L) × 7.0 mm (W) × 0.75 mm (H).

The functional block diagram of this product is shown in Figure 1.

本产品是一款 4 通道，16 位，125 MSPS 采样率的模数转换器(Analog-to-Digital Converter，ADC)，专门针对低功耗、小尺寸和使用灵活性进行开发设计。该产品转换速率最高可达到 125 MSPS，具有优异的动态性能和超低功耗特性，适用多种应用场景。

该 ADC 采用 1.8 V 单电源供电和 LVPECL /CMOS/LVDS 兼容型采样时钟信号。无需外部基准电压源和驱动器即可满足需求。

支持独立关闭内部各通道功能；禁用全部通道后，典型功耗小于 14mW。该 ADC 内置多种功能，包括可编程时钟输出、数据对齐、生成数字测试码等。可获得的数字测试码包括：内置固定测试码和伪随机测试码，也支持用户通过串行端口接口(SPI)自定义测试码的方式。

本产品采用 48 引脚塑料四边无引线扁平封装（QFN48），外形尺寸为长 7.0mm×宽 7.0mm×高 0.75mm。

该产品功能框图如图 1 所示。

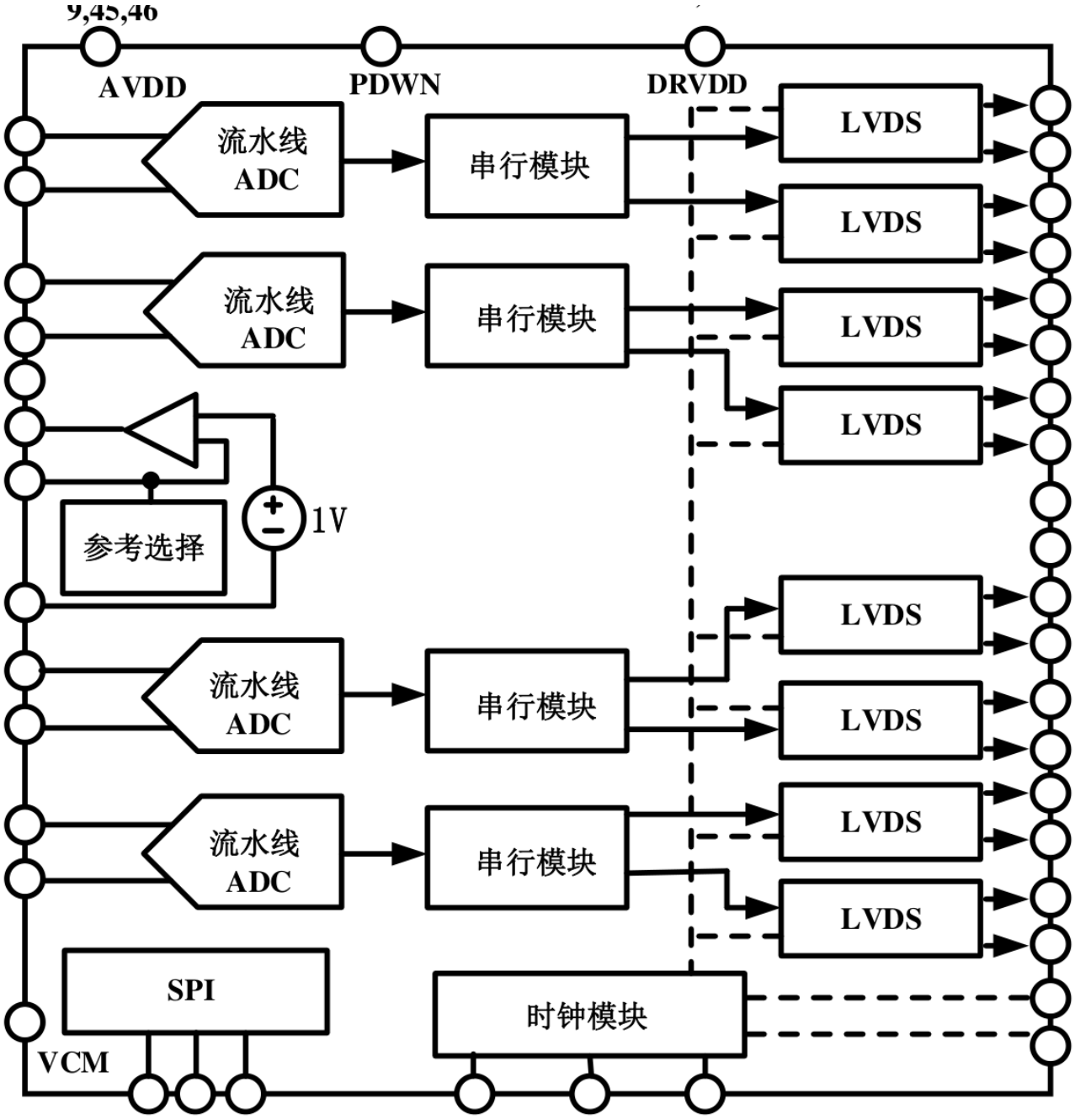


Figure 1: SXA031 functional block diagram

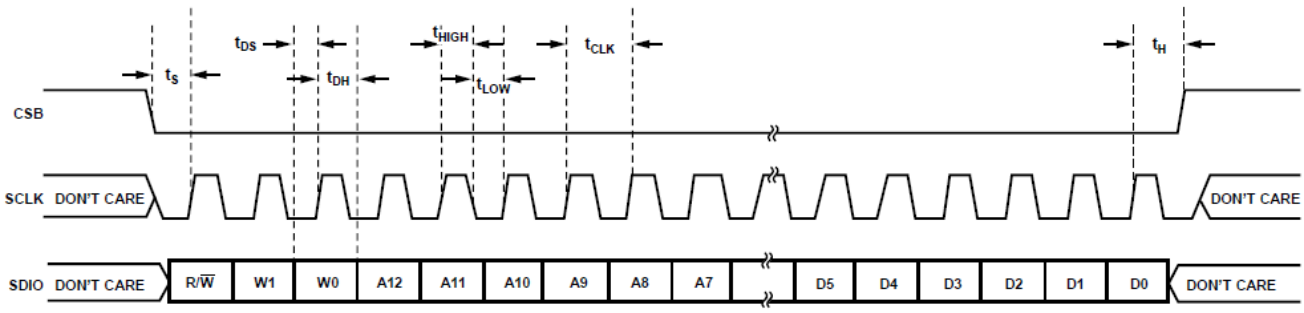


Figure 2: SPI timing diagram

产品外形图和实物图片 / Package Outline and Product Photos

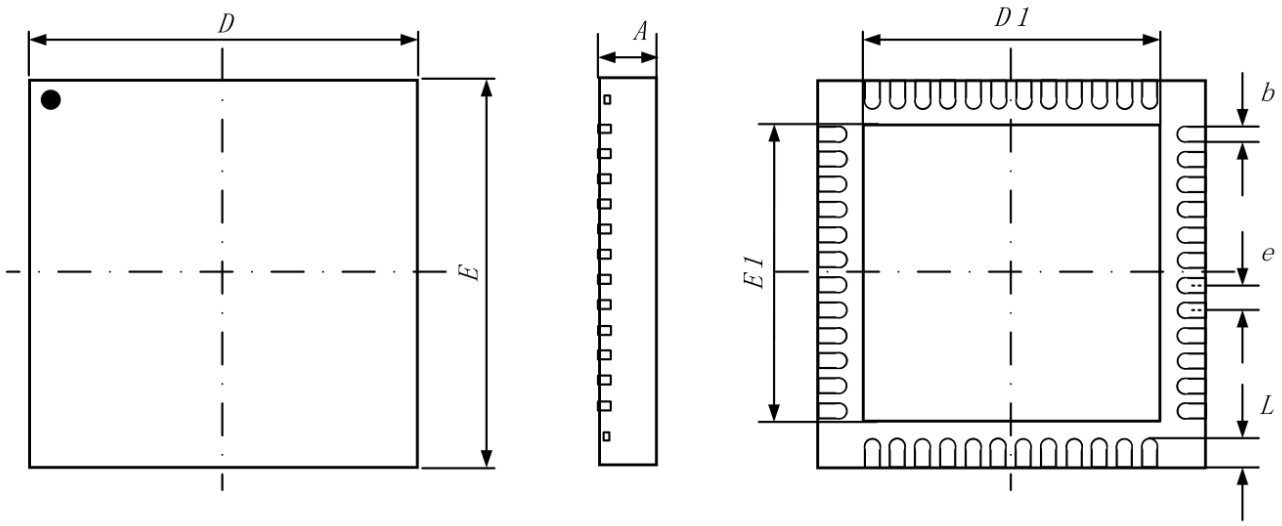


Figure 3: Package outline dimensions and product photo

单位为毫米 / Units in mm

尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max	尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max
A	0.70	0.75[a]	0.80	D	6.90	7.00[a]	7.10
b	0.18	0.25[a]	0.30	D1	5.50	5.60[a]	5.70
e	—	0.50	—	E	6.90	7.00[a]	7.10
L	0.35	0.40[a]	0.45	E1	5.50	5.60[a]	5.70

[a] 外壳实际公称值，推荐用户参考该尺寸设计使用；/ Actual nominal package values; users are advised to design with reference to these dimensions.

注：推荐焊盘设计详见电装说明。/ Note: see the assembly instructions for recommended pad layout.

引出端排列（俯视图）/ Pin Arrangement (Top View)

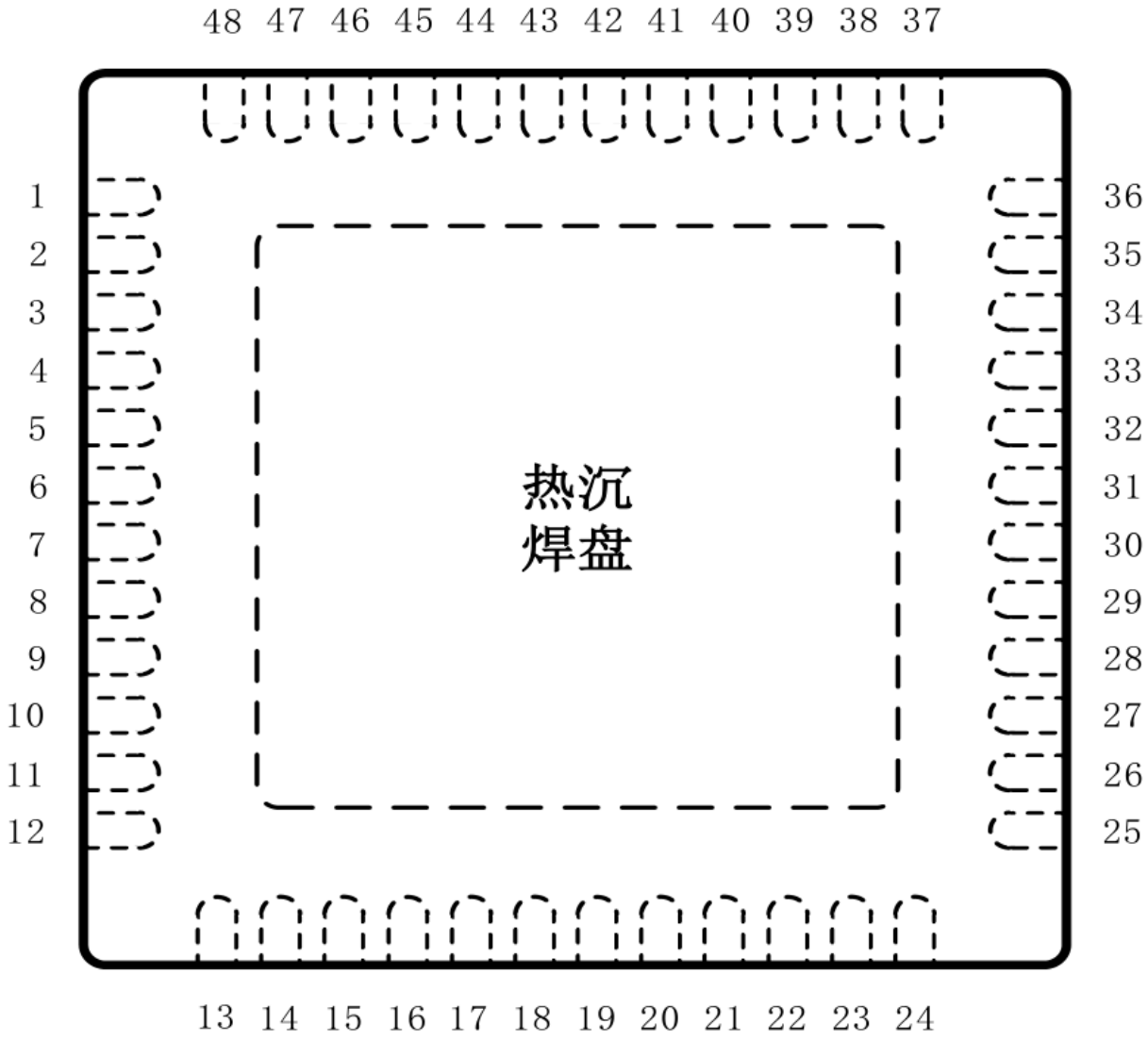


Figure 4: Pin arrangement (top view)

引出端功能符号表 / Pin Function Table

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q
0	AGND	模拟地 / Analog ground	/	25	D1A-	A 通道数字输出（-）/ Channel A digital output (-)	O
1	VIND+	ADC D 通道模拟输入(+) / ADC channel D analog input (+)	I	26	D1A+	A 通道数字输出（+）/ Channel A digital output (+)	O
2	VIND-	ADC D 通道模拟输入(-) / ADC channel D analog input (-)	I	27	D0A-	A 通道数字输出（-）/ Channel A digital output (-)	O

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q
3	AVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/	28	D0A+	A 通道数字输出（+）/ Channel A digital output (+)	O
4	AVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/	29	DRVDD	数字输出驱动器电源 / Digital output driver supply	/
5	CLK-	差分时钟(-) / Differential clock (-)	I	30	SCLK/DTP	SPI 时钟输入/数字测试码 / SPI clock input / digital test pattern	I
6	CLK+	差分时钟(+) / Differential clock (+)	I	31	SDIO/OLM	SPI 数据输入和输出 / SPI data input and output	I
7	AVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/	32	CSB	SPI 片选信号 / SPI chip-select signal	I
8	DRVDD	数字输出驱动器电源 / Digital output driver supply	/	33	PDWN	数字输入(高电平=关断；低电平=工作) / Digital input (high = power-down; low = operation)	I
9	D1D-	D 通道数字输出（-）/ Channel D digital output (-)	O	34	AVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
10	D1D+	D 通道数字输出（+）/ Channel D digital output (+)	O	35	VINA-	ADC A 通道模拟输入(-) / ADC channel A analog input (-)	I
11	D0D-	D 通道数字输出（-）/ Channel D digital output (-)	O	36	VINA+	ADC A 通道模拟输入(+) / ADC channel A analog input (+)	I
12	D0D+	D 通道数字输出（+）/ Channel D digital output (+)	O	37	VINB+	ADC B 通道模拟输入(+) / ADC channel B analog input (+)	I
13	D1C-	C 通道数字输出（-）/ Channel C digital output (-)	O	38	VINB-	ADC B 通道模拟输入(-) / ADC channel B analog input (-)	I
14	D1C+	C 通道数字输出（+）/ Channel C digital output (+)	O	39	AVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
15	D0C-	C 通道数字输出（-）/ Channel C digital output (-)	O	40	RBIAS	设置模拟电流偏置 / Analog current bias setting	I
16	D0C+	C 通道数字输出（+）/ Channel C digital output (+)	O	41	SENSE	基准电压模式选择 / Reference voltage mode select	I
17	DCO-	数据时钟输出（-）/ Data clock output (-)	O	42	VREF	基准电压输入和输出引脚 / Reference voltage input/output pin	O
18	DCO+	数据时钟输出（+）/ Data clock output (+)	O	43	VCM	模拟输入共模电压 / Analog input common-mode voltage	O
19	FCO-	帧时钟输出（-）/ Frame clock output (-)	O	44	SYNC	数字输入，时钟分频器的 SYNC 输入 / Digital input, SYNC input of the clock divider	I

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q
20	FCO+	帧时钟输出（+）/ Frame clock output (+)	O	45	AVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
21	D1B-	B 通道数字输出（-）/ Channel B digital output (-)	O	46	AVDD	1.8V 模拟电源引脚 / 1.8V analog supply pin	/
22	D1B+	B 通道数字输出（+）/ Channel B digital output (+)	O	47	VINC-	ADC C 通道模拟输入(-) / ADC channel C analog input (-)	I
23	D0B-	B 通道数字输出（-）/ Channel B digital output (-)	O	48	VINC+	ADC C 通道模拟输入(+) / ADC channel C analog input (+)	I
24	D0B+	B 通道数字输出（+）/ Channel B digital output (+)	O				

绝对最大额定值 / Absolute Maximum Ratings

- Analog supply voltage (VDDA): 2V - Digital supply voltage (VDDD): 2V - Storage temperature (Tstg): -55°C~125°C - Junction temperature (TJ): 150°C

- 模拟电源电压（VDDA）：2V - 数字电源电压（VDDD）：2V - 贮存温度（Tstg）：-55°C~125°C - 结温（TJ）：150°C

推荐工作条件 / Recommended Operating Conditions

- Operating frequency (fCLK): 20MHz~125MHz - Analog supply voltage (VDDA): 1.75V~1.9V - Digital supply voltage (VDDD): 1.75V~1.9V - Input signal amplitude range (peak-to-peak): ≤2V - Analog input common-mode voltage: 0.8V~1.0V - Operating ambient temperature (TC): -40°C~85°C

- 工作频率（fCLK）：20MHz~125MHz - 模拟电源电压（VDDA）：1.75V~1.9V - 数字电源电压（VDDD）：1.75V~1.9V - 输入信号幅度范围（峰峰值）：≤2V - 模拟输入共模电压：0.8V~1.0V - 工作环境温度（TC）：-40°C~85°C

性能指标 / Performance Specifications

Conditions / 条件（除另有规定外 / unless otherwise specified）: VPP=2.0V, VAVDD = VDRVDD = 1.8V, AGND=0V, Fs=125MSPS, -40°C≤TA≤85°C.

特性 / Parameter	符号 / Symbol	条件 / Conditions	典型值 / Typical	极限值 / Limits — 最小 / Min	极限值 / Limits — 最大 / Max	单位 / Unit
分辨率 / Resolution	RES		16	16		bits
通道数 / Number of channels	N		4	4		—
失调误差 / Offset error	Eo		-0.25	-0.6	+0.3	%FSR

特性 / Parameter	符号 / Symbol	条件 / Conditions	典型值 / Typical	极限值 / Limits — 最小 / Min	极限值 / Limits — 最大 / Max	单位 / Unit
增益误差 / Gain error	Eg		-6.5	-14	+5	%FSR
微分线性误差 / Differential nonlinearity	EDL	fIN=10MHz	±0.5	-0.99	+1.5	LSB
积分非线性误差 / Integral nonlinearity	EIL	fIN=10MHz	±5	-10	+10	LSB
内部基准电压源 / Internal reference voltage	Vref		1	0.95	1.05	V
模拟输入共模电压范围 / Analog input common-mode voltage range	VCM		0.9	0.8	1	V
模拟输入电阻 / Analog input resistance [a]	RIN		2.6	2.3	3.3	kΩ
功耗 / Power consumption	PW	四通道 / Four channels	600	—	750	mW
掉电功耗 / Power-down power [a]	PD		0.6	—	2.5	mW
转换率 / Conversion rate [b]	SR		—	20	125	MSPS
信噪比 / SNR	SNR	-1dBFS，fIN=10MHz	76.5	72	—	dBFS
信噪比 / SNR	SNR	-1dBFS，fIN=128MHz	70.5	69	—	dBFS
信噪失真比 / SINAD	SINAD	-1dBFS，fIN=10MHz	76.3	71	—	dBFS
信噪失真比 / SINAD	SINAD	-1dBFS，fIN=128MHz	69	68	—	dBFS
有效位 / ENOB	ENOB	-1dBFS，fIN=10MHz	12.4	11.5	—	bits
有效位 / ENOB	ENOB	-1dBFS，fIN=128MHz	11.2	11	—	bits
无杂散动态范围 / SFDR	SFDR	-1dBFS，fIN=10MHz	93	80	—	dBFS
无杂散动态范围 / SFDR	SFDR	-1dBFS，fIN=128MHz	81.3	76	—	dBFS
通道隔离度 / Channel isolation [a]	CT	-1dBFS，fIN=10MHz	72	65	—	dB
逻辑输入高电平（SCLK、SDIO、CSB）/ Logic input high (SCLK, SDIO, CSB)	VIH	—	1.2		1.8	V
逻辑输入低电平（SCLK、SDIO、CSB）/ Logic input low (SCLK, SDIO, CSB)	VIL	—	0		0.75	V

[a] 未纳入考核，仅供用户参考使用。/ Not subject to acceptance testing; provided for user reference only. [b] 时钟速率在不分频时最高为 125MSPS，或 8 分频则最高为 1GSPS。/ Maximum clock rate is 125MSPS without division, or up to 1GSPS with divide-by-8.

注：典型值为常温测试数据。/ Note: typical values are room-temperature test data.

主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

1. Spectrum at fs=125MSPS, fIN=10MHz. 2. Spectrum at fs=125MSPS, fIN=70MHz. 3. Spectrum at fs=125MSPS, fIN=125MHz . 4. Spectrum at fs=125MSPS, fIN=200MHz. 5. Differential and integral nonlinearity error plots.

1、fs=125MSPS，fIN=10MHz 条件下频谱图。2、fs=125MSPS，fIN=70MHz 条件下频谱图。3、fs=125MSPS，fIN=125MHz 条件下频谱图 。4、fs=125MSPS，fIN=200MHz 条件下频谱图。5、微分非线性误差和积分非线性误差图。

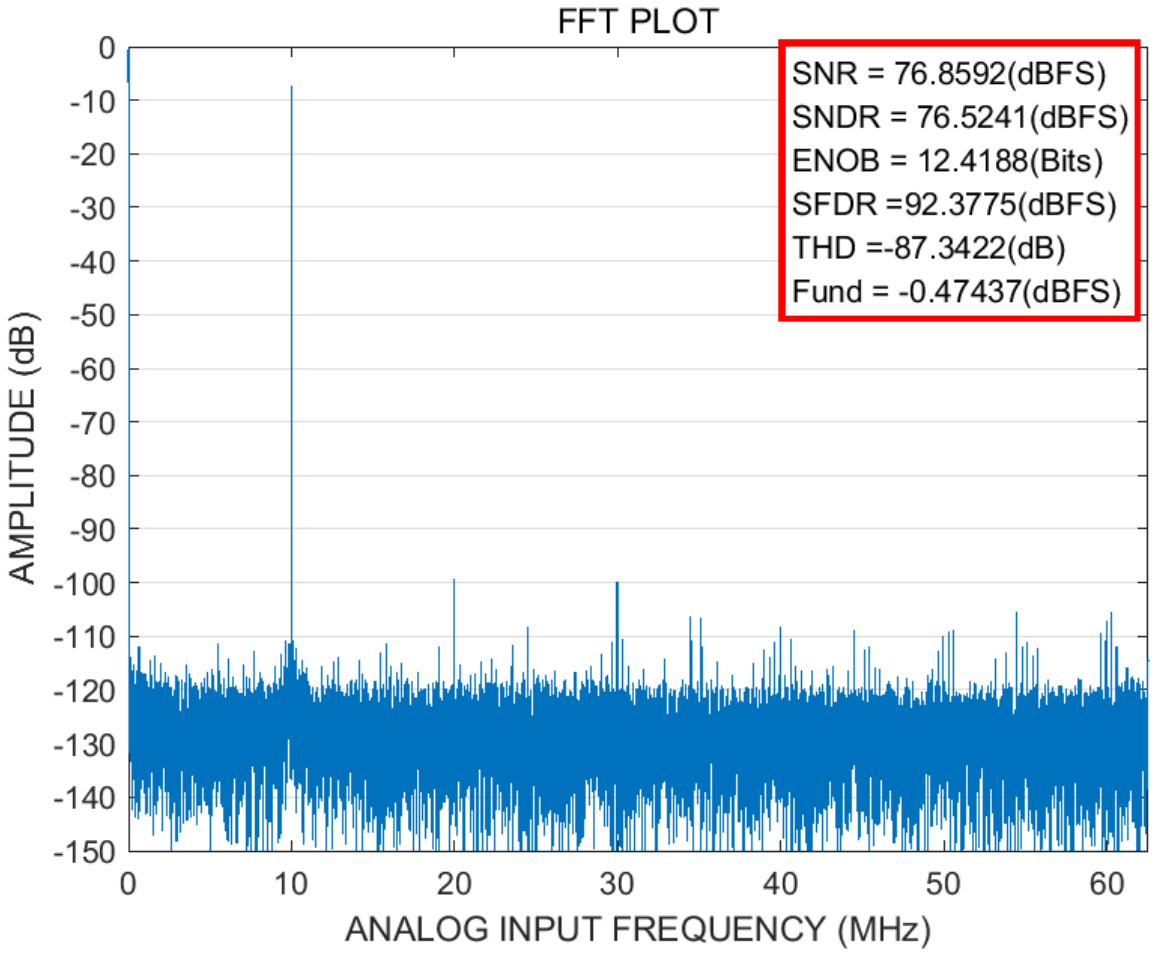


Figure 5: Single-tone 32K spectrum (fIN=10MHz, fS=125MSPS), TA=25°C

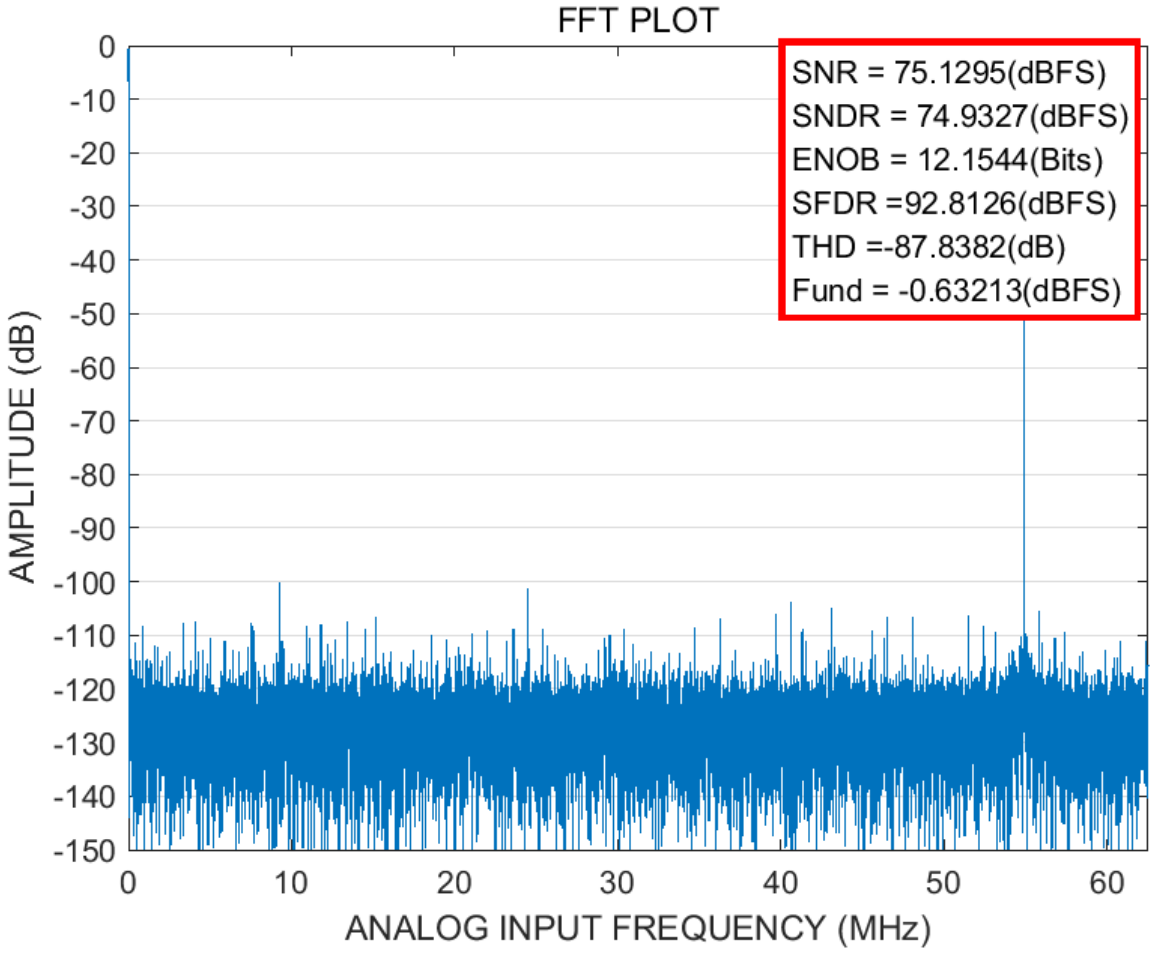


Figure 6: Single-tone 32K spectrum (fIN=70MHz, fS=125MSPS), TA=25°C

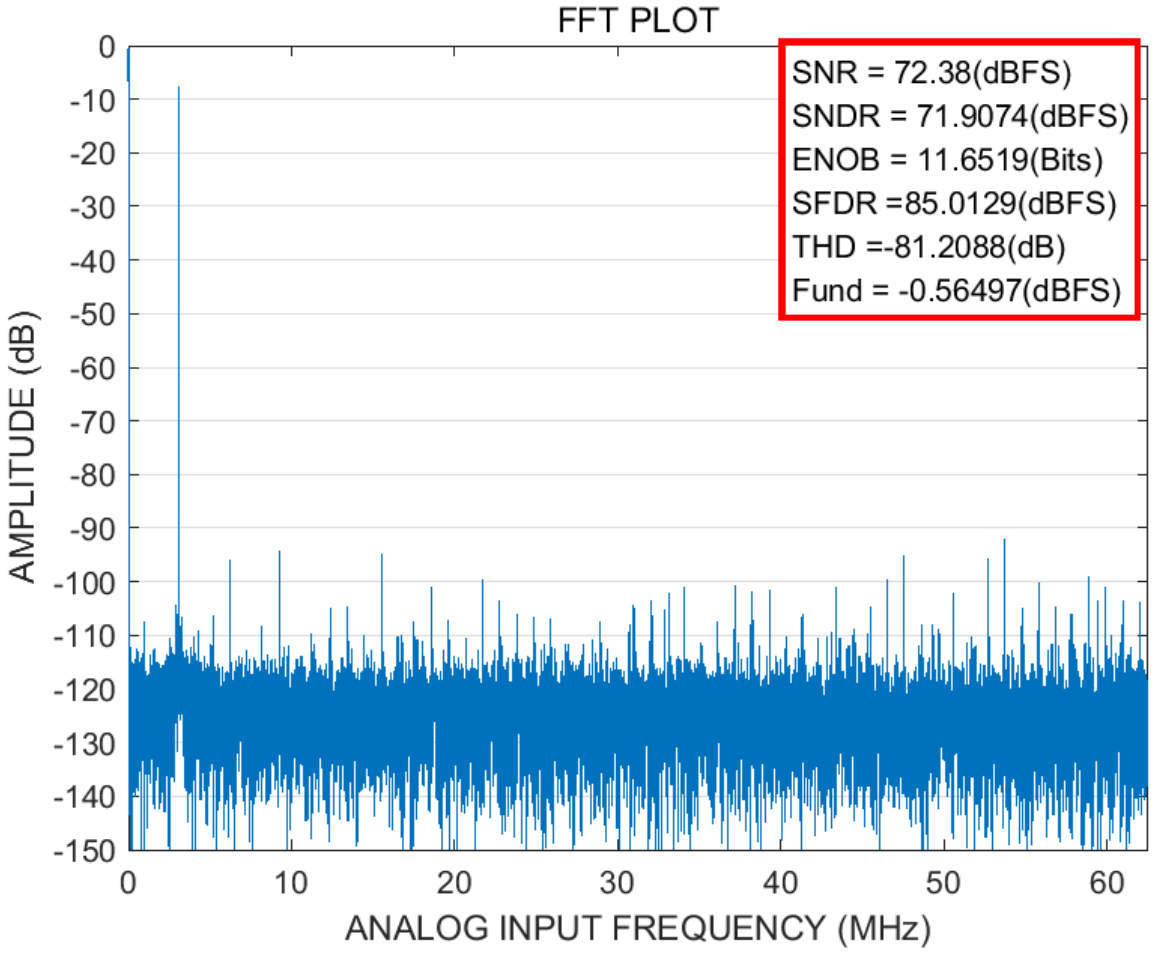


Figure 7: Single-tone 32K spectrum (fIN=128MHz, fS=125MSPS), TA=25°C

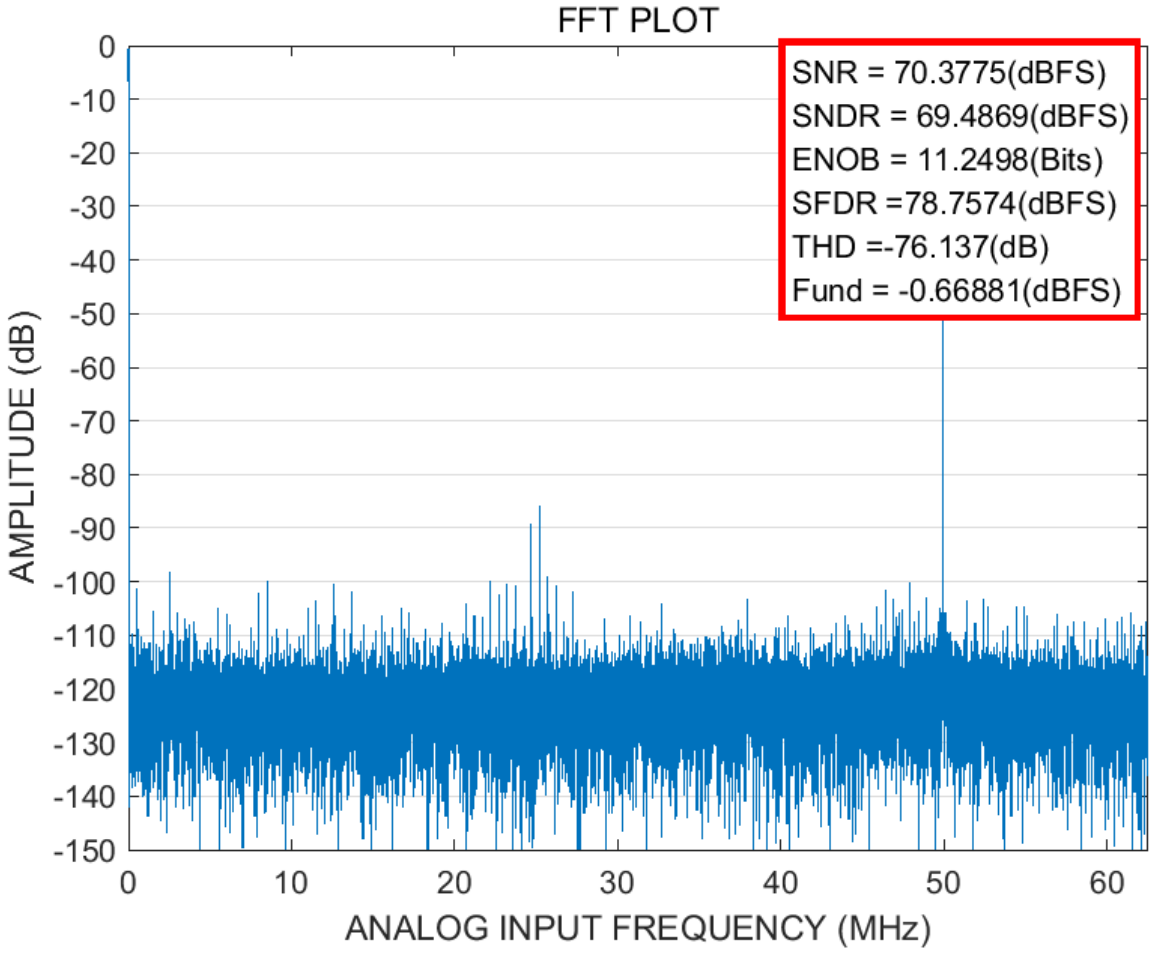


Figure 8: Single-tone 32K spectrum (fIN=200MHz, fS=125MSPS), TA=25°C

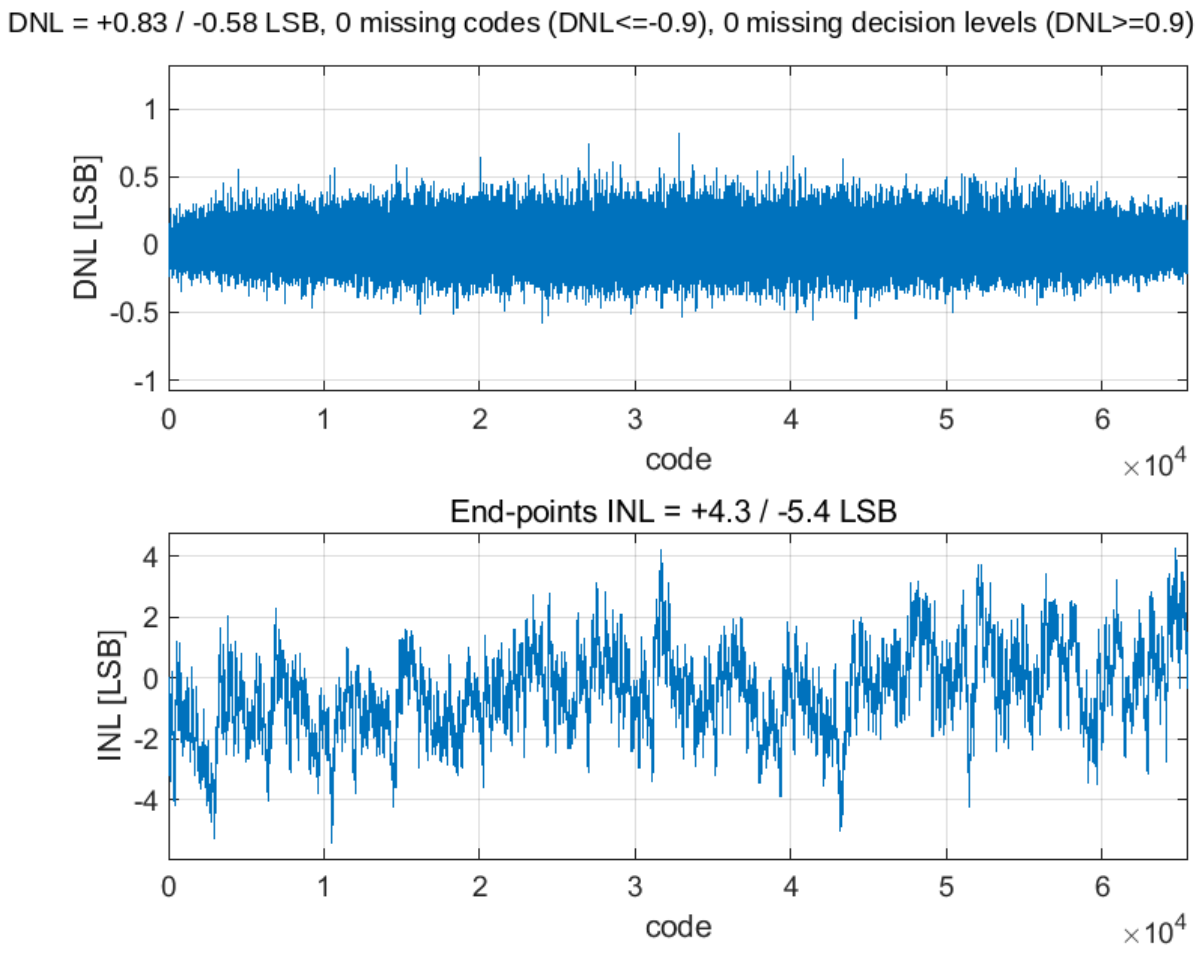


Figure 9: DNL/INL (fIN=10MHz, fS=125MSPS), TA=25°C

典型应用线路图 / Typical Application Circuit

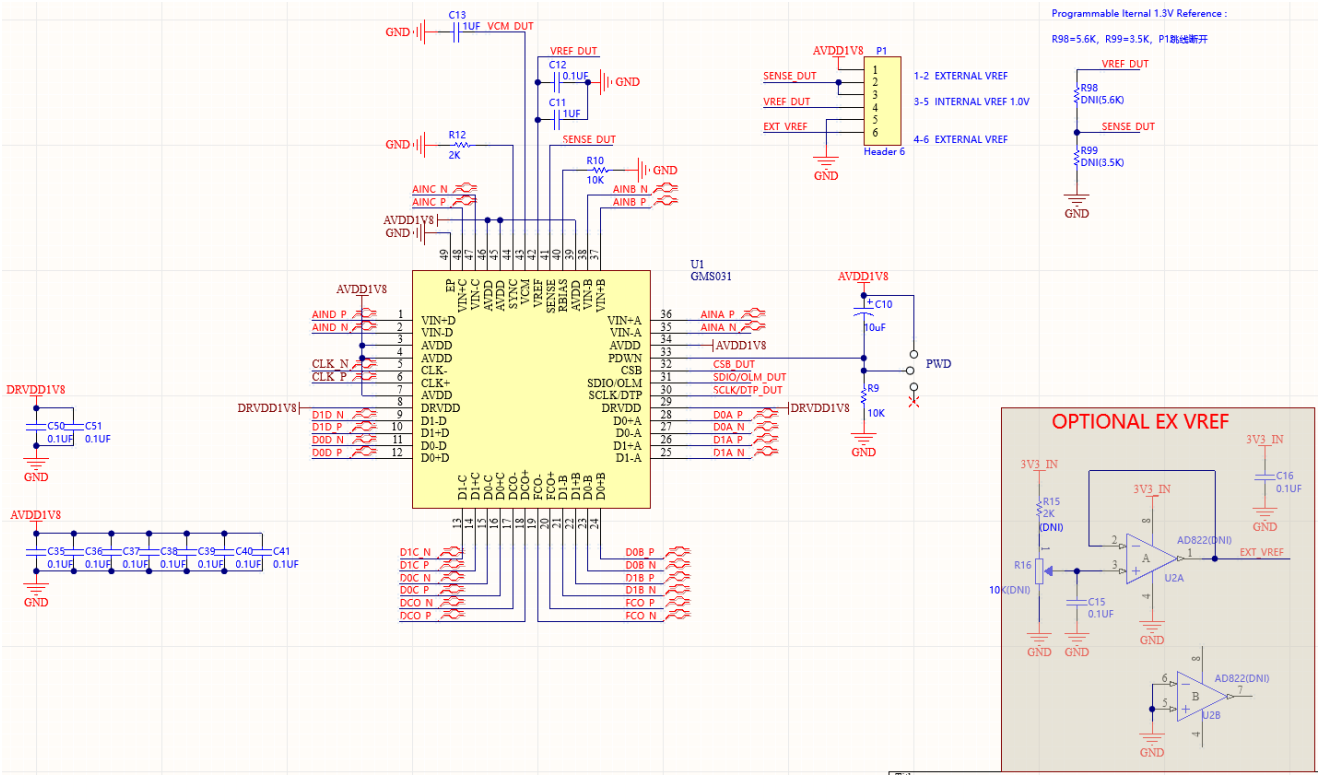


Figure 10: Typical application circuit

单元模块及工作原理 / Functional Blocks and Operating Principles

1、原理概述 / 1. Theory of Operation

Except for the last stage, each stage of the pipeline consists of a low-resolution Flash ADC, a connected switched-capacitor DAC, and an inter-stage residue amplifier (e.g., a multiplying digital-to-analog converter [MDAC]). The residue amplifier amplifies the difference between the reconstructed DAC output and the Flash input for the next pipeline stage. To aid digital correction of Flash errors, each stage is assigned one bit of redundancy. The last stage consists only of a Flash ADC.

除最后一级以外，流水线的每一级都由一个低分辨率 Flash 型 ADC、与之相连的一个开关电容 DAC 和一个级间余量放大器(例如乘法数模转换器[MDAC])组成。余量放大器放大重构 DAC 输出与 Flash 型输入之差，以便提供给流水线的下一级。为了帮助对 Flash 误差进行数字校正，每一级设定了一位的冗余量。最后一级仅由一个 Flash 型 ADC 组成。

2、模拟输入 / 2. Analog Input

The analog input of this product is a differential switched-capacitor circuit designed to process differential input signals. The circuit supports a wide common-mode range while maintaining excellent performance. When the input common-mode voltage is at mid-supply, signal-dependent errors are minimized and optimum performance is achieved.

本产品的模拟输入端为一个差分开关电容电路，设计用于处理差分输入信号。该电路支持宽共模范围，同时能保持出色的性能。当输入共模电压为中间电源电压时，信号相关误差最小，并且能实现最佳性能。

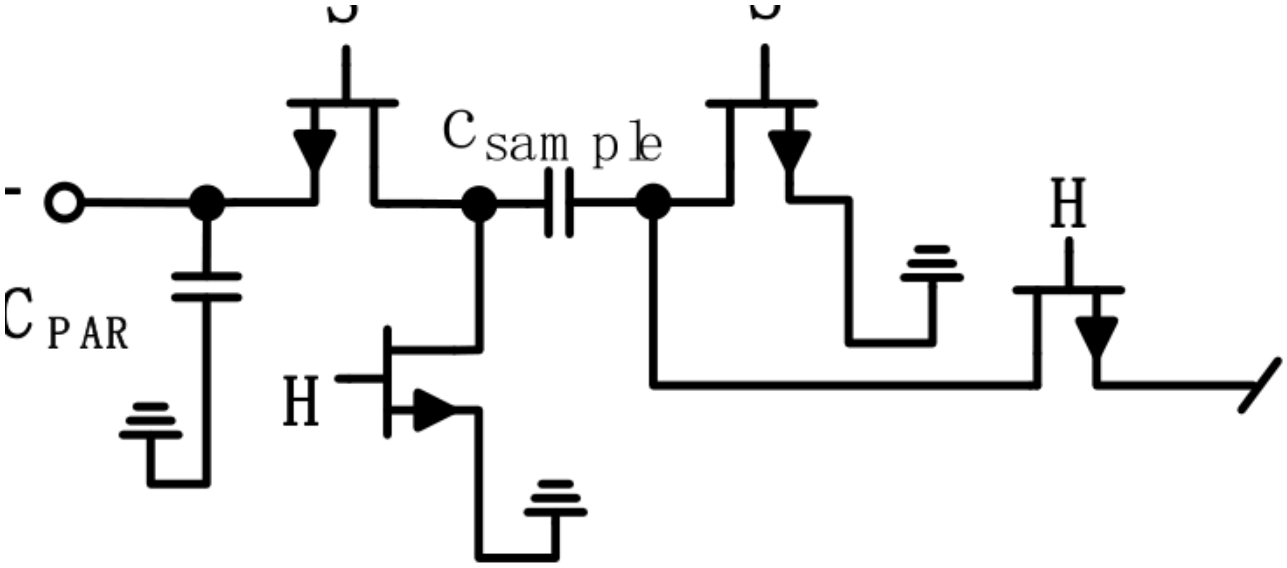


Figure 11: Analog input equivalent circuit

3、输入共模电平 / 3. Input Common-Mode Level

The analog input of this product has no internal DC bias; in AC-coupled applications, the user must provide an external bias. For optimum dynamic performance, the device must be configured so that the input common-mode level VCM = AVDD/2.

This product provides an on-chip reference voltage through the VCM pin, which must be bypassed to ground with a 0.1μF capacitor.

In a differential configuration, setting the device input to maximum range achieves the highest signal-to-noise ratio (SNR) performance. For this product, the input range depends on the reference voltage; performance degrades sharply beyond the input range.

本产品的模拟输入端无内部直流偏置，在交流耦合应用中，用户必须提供外部偏置。为了获得最佳的动态性能，用户必须对器件进行配置，使输入共模电平 VCM=AVDD/2。

本产品通过引脚 VCM 提供片内基准电压，必须使用一个 0.1μF 电容将 VCM 引脚旁路到地。

在差分配置中，将器件输入设置为最大范围可以实现最高的信噪比(SNR)性能，对于本产品输入范围取决于基准电压，超过输入范围性能将急剧恶化。

4、差分输入配置 / 4. Differential Input Configuration

There are various active and passive ways to effectively drive this product; driving differentially suppresses even-order harmonics to achieve optimum performance.

In baseband applications, driving this product with a differential balun configuration provides excellent performance and a flexible interface for the ADC (see Figure 11) .

In applications where SNR is a critical parameter, since the noise performance of most amplifiers is insufficient to meet the true performance of this product, the input configuration requires differential transformer coupling (see Figure 12) .

In both applications above, the value of capacitor C1 must be selected in coordination with the input spectrum; it is recommended to reduce the capacitance of this capacitor or remove it when converting high-frequency analog input signals.

Single-ended input drive of this product is not recommended.

有多种有源和无源方式可以有效驱动本产品，通过差分方式驱动可以抑制偶次谐波从未获得最佳性能。

在基带应用中，利用差分巴伦配置驱动本产品能够为 ADC 提供出色的性能和灵活接口（参考图 11）。

在 SNR 为关键参数的应用中，因为绝大部分放大器的噪声性能不足以满足本产品的真实性能，所以输入配置要求采用差分变压器耦合(参考图 12)。

以上两种应用中的电容 C1 的选值需要和输入频谱配合选择，建议转换高频模拟输入信号时减小该电容容值或者移除该电容。

不建议单端输入方式驱动本产品。

`*C1 是可选择的 / *C1 is optional`

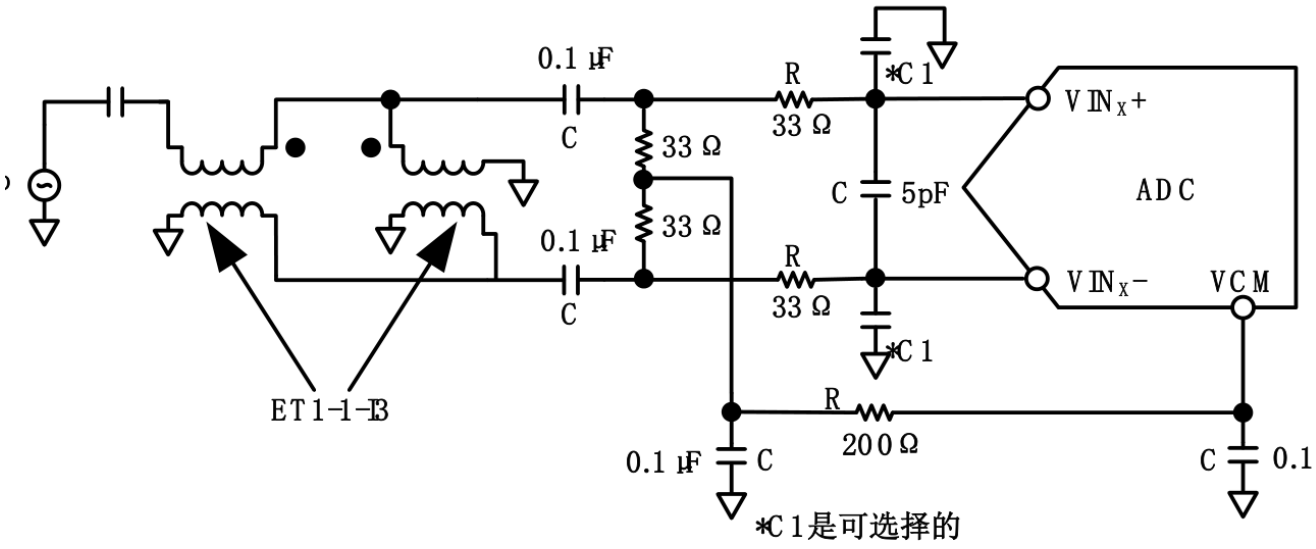


Figure 12: Differential dual-balun configuration

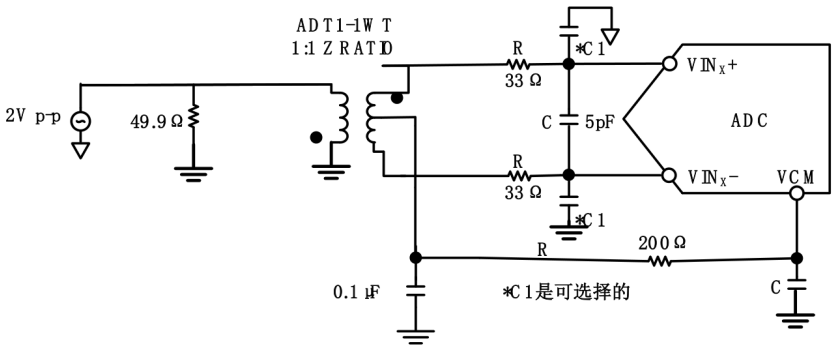


Figure 13: Differential transformer coupling

5、基准电压 / 5. Reference Voltage

This product has a built-in stable, accurate reference voltage source. VREF can be configured using the internal 1.0 V reference, an externally applied 1.0 V to 1.3 V reference, or an external resistor divider acting on the internal reference, to generate a user-selectable reference voltage. See the "Internal Reference Voltage Connection" section and the "External Reference Voltage" section for descriptions of the reference voltage source modes. The VREF pin should be bypassed to ground through an external low equivalent series resistance (ESR) 1.0μF capacitor in parallel with a low-ESR 0.1μF ceramic capacitor.

The built-in comparator of this product detects the voltage on the SENSE pin, thereby configuring the reference voltage into one of three possible modes. If the SENSE pin is grounded, the reference voltage amplifier switch is connected to the internal resistor divider (see Figure 13) , so the VREF pin voltage V is set to 1.0 V. If the SENSE pin is connected to an external resistor divider (see Figure 14) , then VREF is defined as:

VREF = 0.5 × (1 + R2/R1)

where 7 kΩ ≤ (R1 + R2) ≤ 10 kΩ.

If the internal reference voltage of this product is used to drive multiple converters to improve gain matching, the loading of the reference voltage by the other converters must be considered. Figures 15 and 16 show how loading affects the internal reference voltage .

本产品内置稳定、精确的基准电压源。VREF 可以利用内部 1.0 V 基准电压、外部施加的 1.0 V 至 1.3 V 基准电压或作用于内部基准电压的外部电阻分压器来配置，产生用户可选的基准电压。基准电压源模式说明参见"内部基准电压连接"部分和"外部基准电压"部分。VREF 引脚应通过外部一个低等效串联电阻(ESR)1.0μF 电容和一个低 ESR 0.1μF 陶瓷电容的并联旁路至地。

本产品的内置比较器可检测出 SENSE 引脚的电压，从而将基准电压配置成三种可能的模式之一。如果 SENSE 引脚接地，则基准电压放大器开关与内部电阻分压器相连(见图 13)，因而将 VREF 引脚电压 V 设为 1.0 V。如果 SENSE 引脚连接到外部电阻分压器(见图 14)，则 VREF 定义为：

VREF=0.5 x (1 + R2/R1)

其中，7 kΩ ≤ (R1 + R2) ≤ 10 kΩ。

如需利用本产品的内部基准电压来驱动多个转换器，从而提高增益的匹配度，则必须考虑到其它转换器对基准电压的负载。图 15 和图 16 显示负载如何影响内部基准电压 。

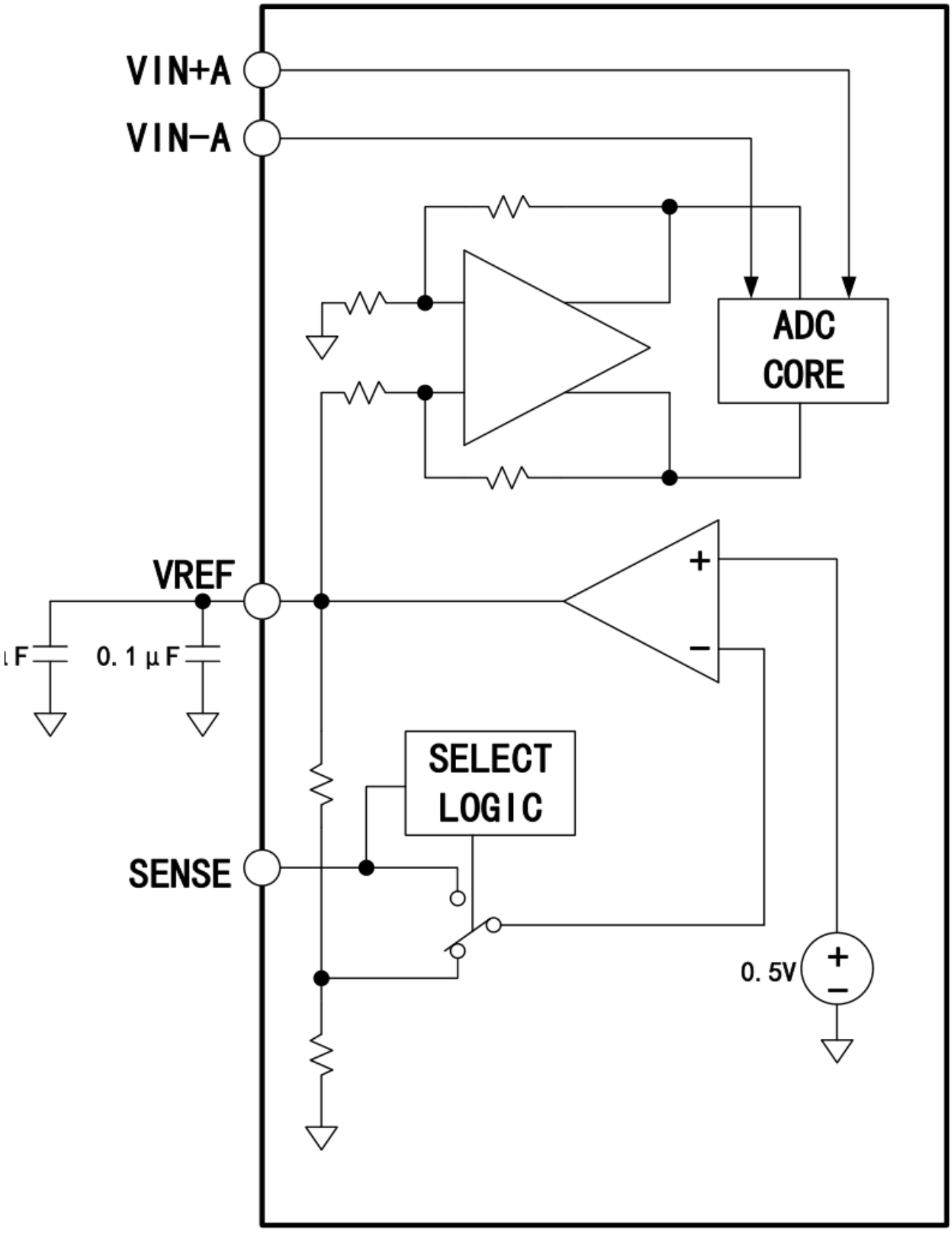


Figure 14: 1.0V reference voltage configuration

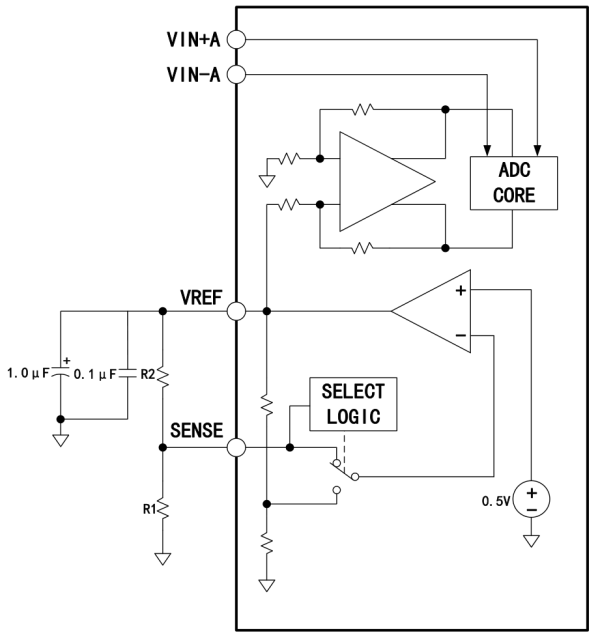


Figure 15: External reference voltage configuration

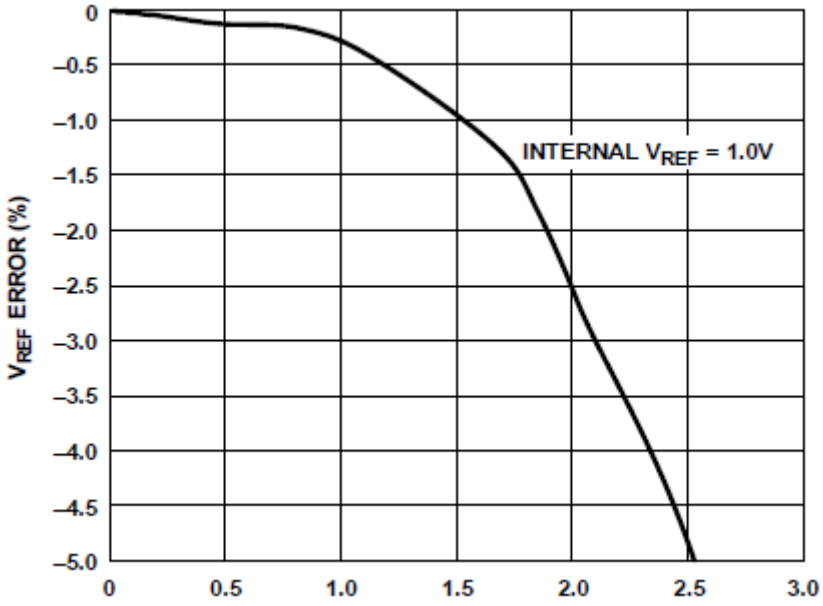


Figure 16: VREF error (internal VREF = 1.0 V) vs. load current

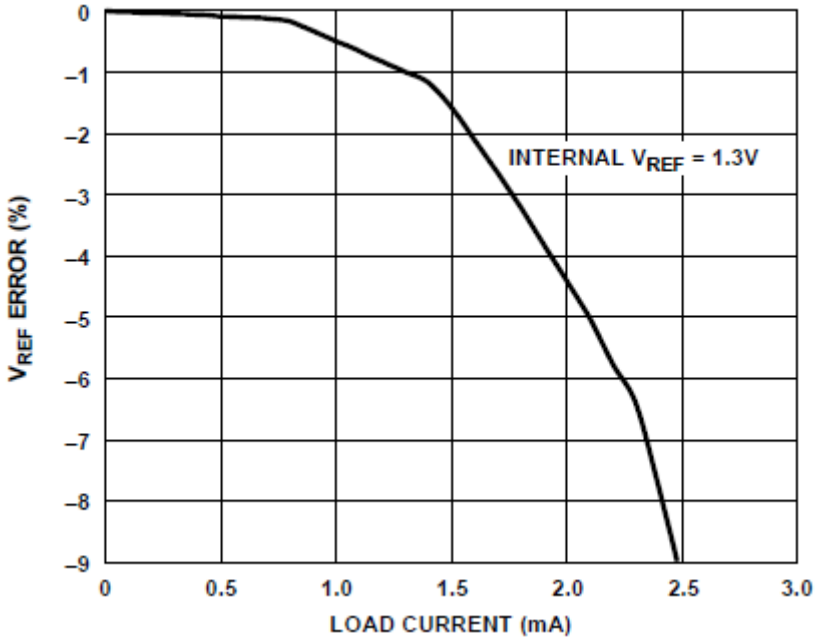


Figure 17: VREF error (internal VREF = 1.3 V) vs. load current

6、外部基准电压 / 6. External Reference Voltage

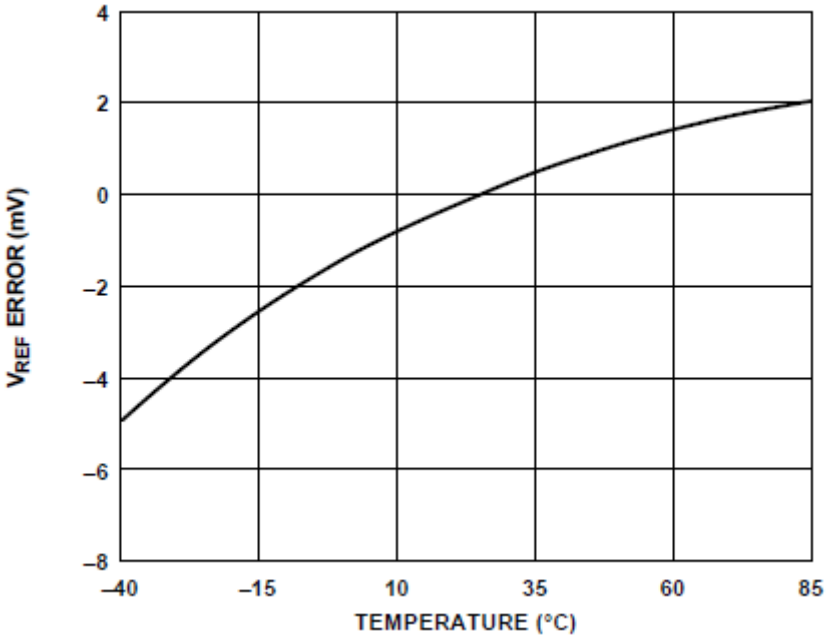


Figure 18: VREF error vs. temperature (VREF = 1.0 V typical drift)

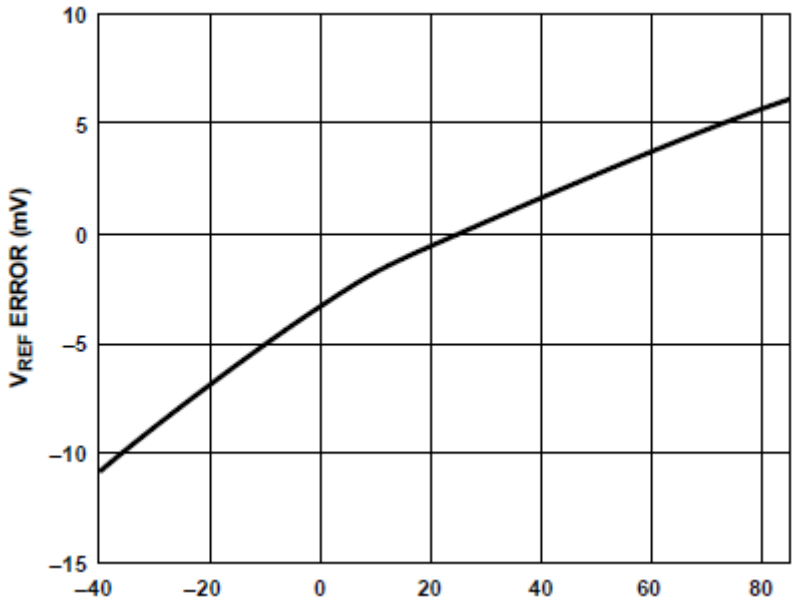


Figure 19: VREF error vs. temperature (VREF = 1.3 V typical drift)

An external reference voltage must be used to further improve ADC gain accuracy and thermal drift characteristics. Figures 17 and 18 show the typical drift characteristics of the internal reference voltage source in 1.0 V mode and 1.3 V mode, respectively . Connecting the SENSE pin to AVDD disables the internal reference voltage source, allowing the use of an external reference voltage source. The loading of the internal reference buffer on the external reference voltage source is equivalent to a 7.5 kΩ load. The internal buffer generates the positive and negative full-scale reference voltages for the ADC core. Floating the SENSE pin is not recommended.

必须采用外部基准电压才可能进一步提高 ADC 增益精度、改善热漂移特性。图 17 和图 18 显示内部基准电压源分别在 1.0 V 模式和 1.3 V 模式下的典型漂移特性 。将 SENSE 引脚与 AVDD 相连时，可以禁用内部基准电压源，从而允许使用外部基准电压源。内部基准电压缓冲器对外部基准电压源的负载相当于 7.5 kΩ 负载。内部缓冲器为 ADC 内核生成正、负满量程基准电压。不建议悬空 SENSE 引脚。

7、时钟输入考虑 / 7. Clock Input Considerations

To fully exploit the performance of the chip, a differential signal should be used as the clock signal for the sampling clock inputs (CLK+ and CLK−) of this product. This signal is typically AC-coupled to the CLK+ and CLK− pins via a transformer or capacitors. These two pins are internally biased and require no external bias.

为了充分发挥芯片的性能，应利用一个差分信号作为本产品采样时钟输入端(CLK+和 CLK−)的时钟信号。该信号通常使用变压器或电容器交流耦合到 CLK+和 CLK−引脚内。这两个引脚有内部偏置，无需外部偏置。

8、时钟输入 / 8. Clock Input

This product has a flexible clock input structure. CMOS, LVDS, LVPECL, or sine-wave signals can all serve as its clock input signal. Regardless of the signal type, clock source jitter must be considered (see the Jitter Considerations section). Using an RF transformer or RF balun, the single-ended signal of a low-jitter clock source can be converted into a differential signal. For clock frequencies from 125 MHz to 1 GHz, the RF balun configuration is recommended; for clock frequencies from 40 MHz to 200 MHz, the RF

transformer configuration is recommended. Schottky diodes connected across the secondary winding of the transformer/balun can limit the clock signal fed into this product to approximately 0.8V peak-to-peak differential (see Figures 19 and 20) .

This both prevents large voltage swings of the clock from feeding through to other parts of this product and preserves fast signal rise and fall times, which is important for achieving low-jitter performance. However, at frequencies above 500 MHz, diode capacitance has an effect. Appropriate signal-limiting diodes must be carefully selected.

If a low-jitter clock source is not available, another approach is to AC-couple a differential PECL signal to the sampling clock input pins (as shown in Figure 21) . AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

Another approach is to AC-couple a differential LVDS signal to the sampling clock input pins (as shown in Figure 22) . AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

本产品具有灵活的时钟输入结构。CMOS、LVDS、LVPECL 或正弦波信号均可作为其时钟输入信号。无论采用哪种信号，都必须考虑到时钟源抖动(见抖动考虑部分说明)。利用射频变压器或射频巴伦，可将低抖动时钟源的单端信号转换成差分信号。对于 125 MHz 至 1 GHz 的时钟频率，建议采用射频巴伦配置；对于 40 MHz 至 200 MHz 的时钟频率，建议采用射频变压器配置。跨接在变压器/巴伦次级绕组上的肖特基二极管可以将输入到本产品中的时钟信号限制为约差分 0.8V 峰峰值(见图 19 和图 20)。

这样，既可以防止时钟的大电压摆幅馈通至本产品的其它部分，还可以保留信号的快速上升和下降时间，这一点对实现低抖动性能来说非常重要。但是，当频率高于 500 MHz 时，二极管电容会产生影响。必须小心选择适当的信号限幅二极管。

如果没有低抖动的时钟源，那么，另一种方法是对差分 PECL 信号进行交流耦合，并传输至采样时钟输入引脚(如图 21 所示)。AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 时钟驱动器具有出色的抖动性能。

另一种方法是将差分 LVDS 信号交流耦合至采样时钟输入引脚(如图 22 所示)。AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 时钟驱动器具有出色的抖动性能。

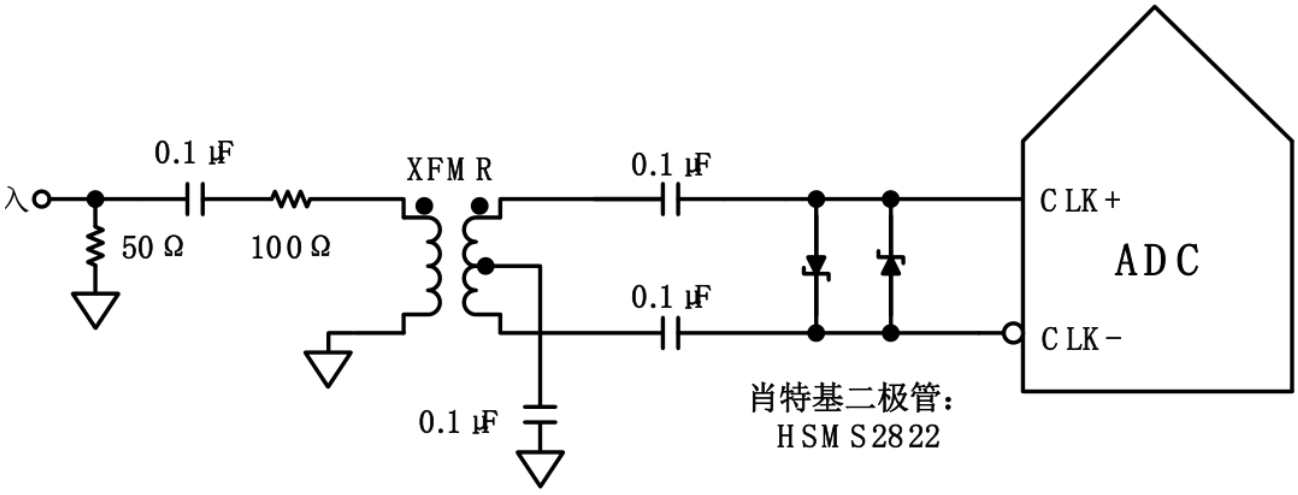


Figure 20: Transformer-coupled differential clock (up to 200 MHz)

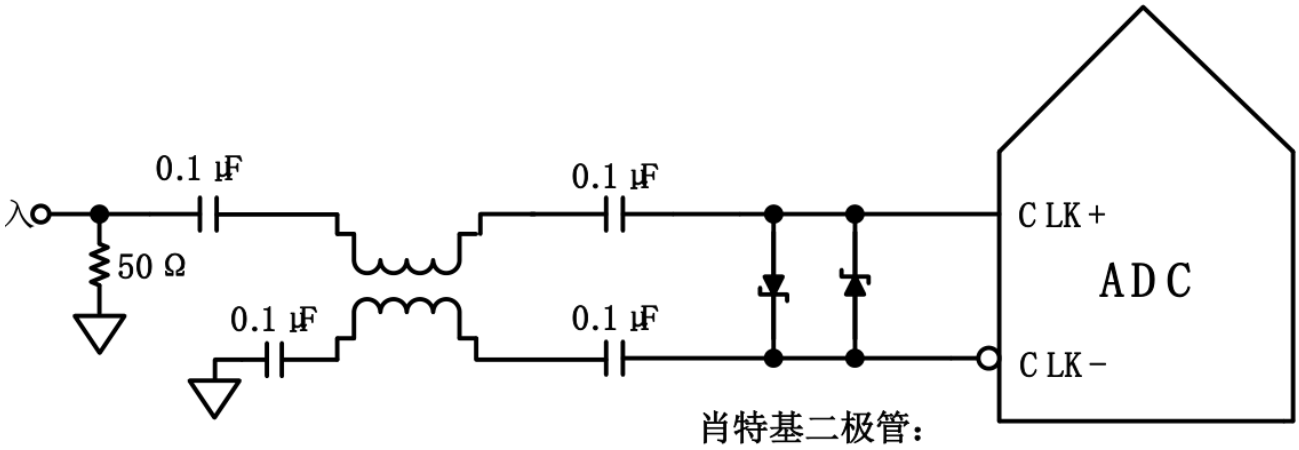


Figure 21: Balun-coupled differential clock (up to 1 GHz)

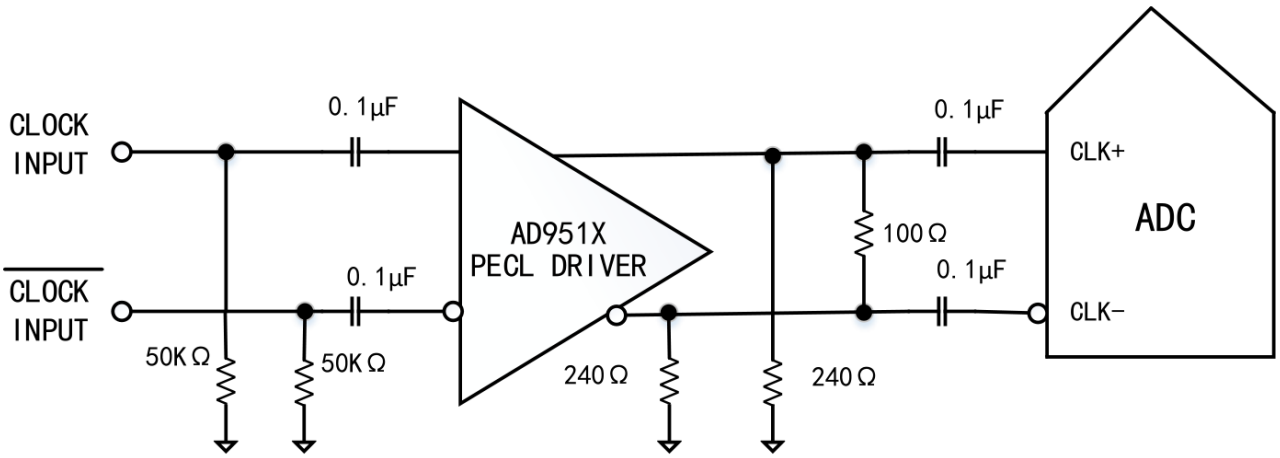


Figure 22: Differential PECL sampling clock (up to 1 GHz)

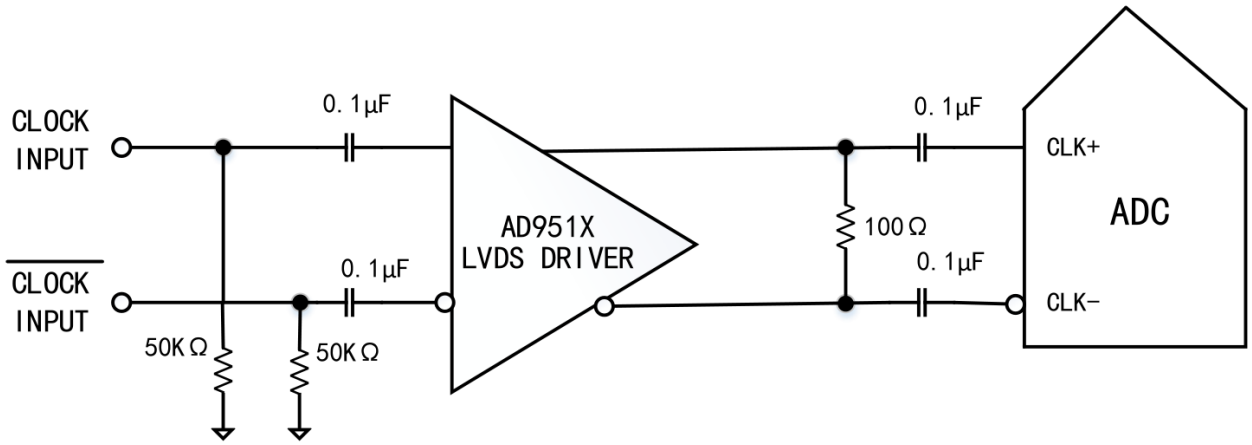


Figure 23: Single-ended 1.8 V CMOS input clock (up to 200 MHz)

9、输入时钟分频器 / 9. Input Clock Divider

This product has a built-in input clock divider that can divide the input clock by an integer factor of 1 to 8. An external SYNC input signal can synchronize the clock divider of this product. Writing to bits 0 and 1 of register 0x109 allows the clock divider to be re-synchronized after each received SYNC signal or

only after the first received SYNC signal. A valid SYNC resets the divider to its initial state. This synchronization feature aligns the clock dividers of multiple devices, ensuring simultaneous input sampling.

本产品内置一个输入时钟分频器，可对输入时钟进行 1 至 8 整数倍分频。利用外部 SYNC 输入信号，可同步本产品时钟分频器。通过对寄存器 0x109 的位 0 和位 1 进行写操作，可以设置每次收到 SYNC 信号或者仅第一次收到 SYNC 信号后对时钟分频器再同步。有效 SYNC 可使分频器复位至初始状态。该同步特性可让多个器件的时钟分频器对准，从而保证同时进行输入采样。

10、时钟占空比 / 10. Clock Duty Cycle

Typical high-speed ADCs use both clock edges to generate different internal timing signals, so they are very sensitive to clock duty cycle. Generally, to maintain ADC dynamic performance, the clock duty-cycle tolerance should be ±5%.

This product has a built-in duty cycle stabilizer (DCS) that re-times the non-sampling edge (falling edge) and provides an internal clock signal with a nominal 50% duty cycle. When the clock input duty cycle deviates from the nominal 50% duty cycle by more than the ±5% rating, this feature minimizes performance degradation. Enabling the DCS function significantly improves noise and distortion performance for clock input duty cycles of 30% to 45% and 55% to 70%.

Jitter on the input rising edge remains a concern and cannot be easily reduced by the internal stabilization circuit. In applications where the clock rate changes dynamically, the time constant associated with this loop must be considered. Before the DCS loop re-locks to the input signal, a wait of 1.5 μs to 5 μs is required.

典型的高速 ADC 利用两个时钟边沿产生不同的内部定时信号，因此，它对时钟占空比非常敏感。通常，为保持 ADC 的动态性能，时钟占空比容差应为±5%。

本产品内置一个占空比稳定器(DCS)，可对非采样边沿(下降沿)进行重新定时，并提供标称占空比为 50%的内部时钟信号。当时钟输入占空比偏离标称 50%占空比的幅度大于±5%额定值时，该特性可最大程度减少性能的下降。使能 DCS 功能可显著改善 30%至 45%和 55%至 70%的时钟输入占空比的噪声和失真性能。

输入上升沿的抖动依然值得关注，且无法借助内部稳定电路来轻易减少这种抖动。在时钟速率动态改变的应用中，必须考虑与该环路相关的时间常量。在 DCS 环路重新锁定输入信号前，都需要等待 1.5 μs 至 5 μs 的时间。

11、抖动考虑 / 11. Jitter Considerations

High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. Intermediate-frequency undersampling applications are particularly sensitive to jitter (see Figure 23) .

When aperture jitter may affect the dynamic range of this product, the clock input signal should be treated as an analog signal. The clock driver supply should be separated from the ADC output driver supply to prevent digital noise from mixing into the clock signal. A low-jitter crystal-controlled oscillator provides the best clock source. If the clock signal comes from other types of clock sources (via gating, frequency division, or other methods), the original clock should be used for re-timing in the final stage.

高速、高分辨率 ADC 对时钟输入信号的质量非常敏感。中频欠采样应用对抖动尤其敏感(见图 23)。

当孔径抖动可能影响本产品的动态范围时，应将时钟输入信号视为模拟信号。将时钟驱动器电源与 ADC 输出驱动器电源分离，以免在时钟信号内混入数字噪声。低抖动的晶体控制振荡器可提供最佳时钟源。如果时钟信号来自其它类型的时钟源(通过门控、分频或其它方法)，则需要在最后一步中利用原始时钟进行重定时。

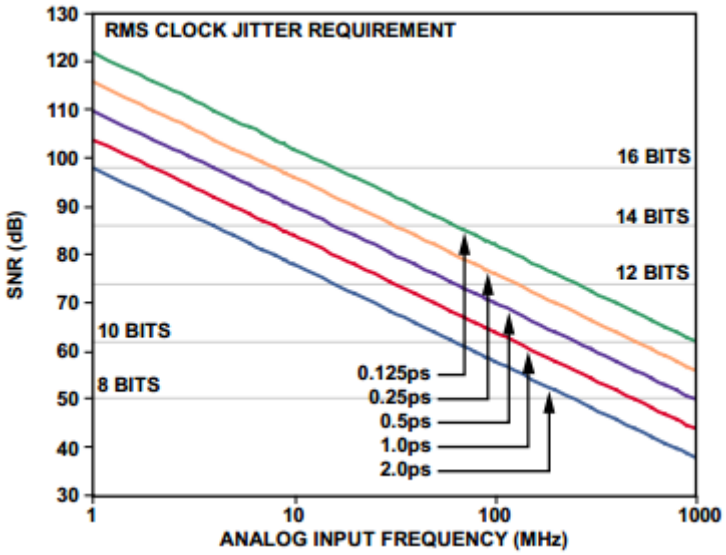


Figure 24: Ideal SNR vs. analog input frequency and jitter

12、功耗和省电模式 / 12. Power Consumption and Power-Saving Modes

As shown in Figure 24 , the power consumption of this product is proportional to its sampling rate. This product can be put into power-saving mode via the SPI port or by setting the PDWN pin high. In power-saving mode, the typical power consumption of the ADC is 2 mW. In power-saving mode, the output drivers are in a high-impedance state. Setting the PDWN pin low returns this product to normal operating mode. Note that PDWN is referenced to the data output driver supply voltage (DRVDD) and must not exceed that supply voltage.

In power-saving mode, low power consumption is achieved by turning off the reference voltage source, reference voltage buffer, bias network, and clock. When entering power-saving mode, internal capacitors discharge; when returning to normal operating mode, internal capacitors must be recharged. Therefore, the wake-up time depends on the time spent in power-saving mode; the shorter the time in power-saving mode, the shorter the corresponding wake-up time. Using the SPI port interface, the user can place the ADC in power-saving mode or standby mode. For shorter wake-up times, standby mode can be used, in which the internal reference voltage circuit remains powered. For more information on using these features, see the "Memory Map" section .

如图 24 所示 ，本产品的功耗与其采样速率成比例关系。通过 SPI 端口或将 PDWN 引脚置位高电平，可使本产品进入省电模式。在省电模式下，ADC 的典型功耗为 2 mW。省电模式下，输出驱动器处于高阻抗状态。将 PDWN 引脚置位低电平时，本产品返回正常工作模式。注意，PDWN 以数据输出驱动器电源电压(DRVDD)为基准，且不得高于该电源电压。

在省电模式下，通过关闭基准电压源、基准电压缓冲器、偏置网络以及时钟，可实现低功耗。进入省电模式时，内部电容放电；返回正常工作模式时，内部电容必须重新充电。因此，唤醒时间与处于省电模式的时间有关；处于省电模式的时间越短，则相应的唤醒时间越短。使用 SPI 端口接口时，用户可将 ADC 置于省电模式或待机模式。如需较短的唤醒时间，可以使用待机模式，该模式下内部基准电压电路处于通电状态。有关使用这些功能的更多信息，请参见"存储器映射"部分 。

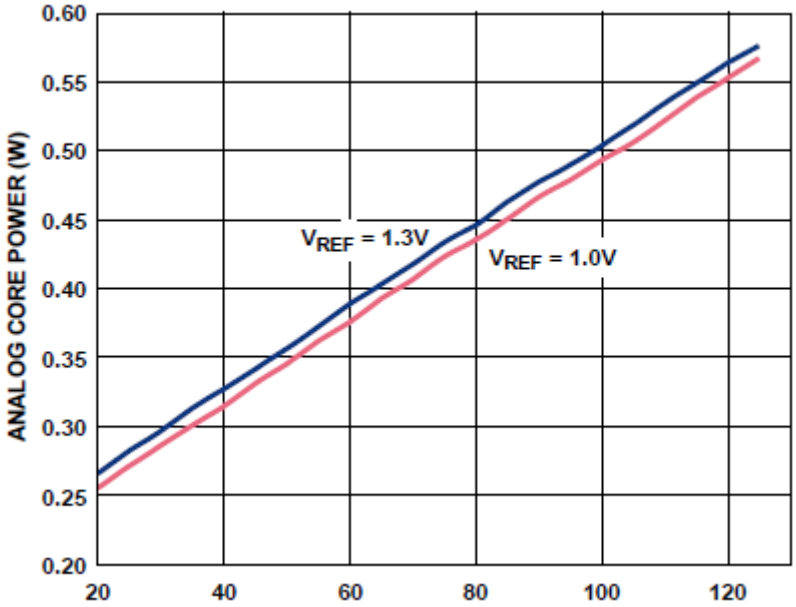


Figure 25: Total power consumption vs. fSAMPLE

13、数字输出 / 13. Digital Outputs

The digital outputs of this product use the ANSI-644 LVDS standard, with an output current of 3.5 mA, a 100-ohm termination resistor load, and a 350 mV swing. In the default mode, the output timing relationship is as shown in Figure 25 .

本产品数字输出采用 ANSI-644 LVDS 标准，输出电流为 3.5mA，负载 100 欧姆的端电阻，摆幅 350mV。默认模式下，输出的时序关系如图 25 所示 。

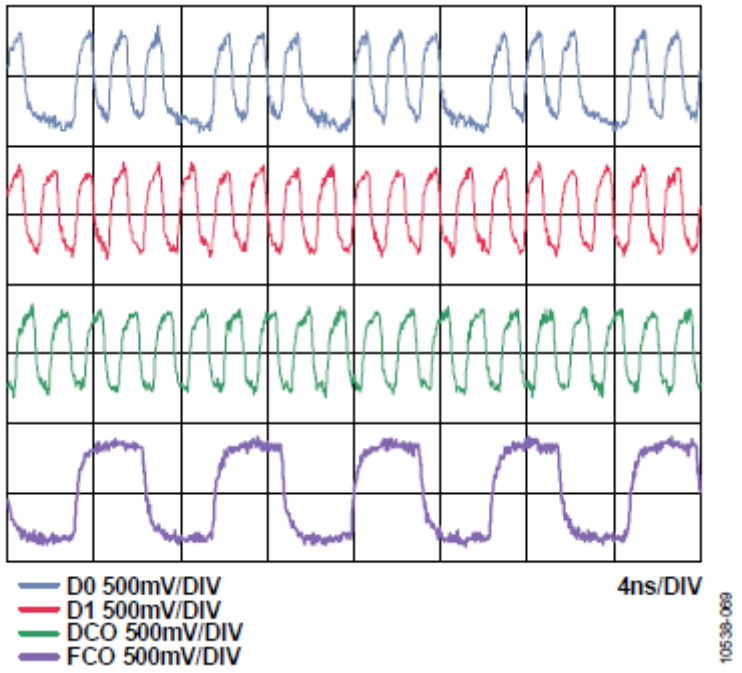


Figure 26: LVDS output timing example

寄存器 / Registers

The SPI of this product is three-wire controlled; the SPI timing control diagram is shown in Figure 2. After power-up, please complete the register reset operation first.

本产品 SPI 为三线控制，SPI 的时序控制图如图 2 所示。上电后，请先完成寄存器复位操作。

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值 (十六进制) / Default (Hex)	注释 / Notes
芯片配置寄存器 / Chip configuration registers											
0x00	SPI 端口配置 / SPI port configuration	0=SDO有效 / 0=SDO valid	LSB优先 / LSB first	软复位 / Soft reset	1=16位地址 / 1=16-bit address	1=16位地址 / 1=16-bit address	软复位 / Soft reset	LSB优先 / LSB first	0=SDO有效 / 0=SDO valid	0x18	半字节之间是镜像关系，使得LSB优先或MSB优先模式寄存器均能正确记录数据。ADC的默认值为16位模式。/ Nibbles are mirrored so that registers can be correctly recorded in both LSB-first and MSB-first modes. The ADC default is 16-bit mode.
0x02	芯片等级(全局) / Chip grade (global)	禁用 / Disabled	速度等级ID[6:4] / Speed grade ID[6:4]: 110 = 125 MSPS			禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled		唯一速度等级ID，用来区分器件等级；只读。/ Unique speed-grade ID for device grade identification; read-only.
器件索引和传送寄存器 /											

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值 (十六进制) / Default (Hex)	注释 / Notes
Device index and transfer registers											
0x05	器件索引 / Device index	禁用 / Disabled	禁用 / Disabled	时钟通道DCO / Clock channel DCO	时钟通道FCO / Clock channel FCO	时钟通道D / Clock channel D	时钟通道C / Clock channel C	时钟通道B / Clock channel B	时钟通道A / Clock channel A	0x3F	设置这些位以决定片内哪个器件接收下一个写命令。默认为片内所有器件。/ Set these bits to determine which on-chip device receives the next write command. Default is all on-chip devices.
0xFF	传输 / Transfer	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	启动覆盖 / Start override	0x00	设置采样速率覆盖。/ Set sample-rate override.
全局ADC功能寄存器 / Global ADC function registers											
0x08	功耗模式(全局) / Power mode (global)	禁用 / Disabled	禁用 / Disabled	外部掉电引脚功能 / External power-down	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	功耗模式 / Power mode: 00=芯片运行 /		0x00	决定芯片的一般工作模式。/ Determines the general operating mode of the chip.

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值 (十六进制) / Default (Hex)	注释 / Notes
				pin function: 0=完全掉电 / 0=full power-down; 1=待机 / 1=standby				00=chip operation; 01=完全掉电 / 01=full power-down; 10=待机 / 10=standby; 11=复位 / 11=reset			
0x09	时钟(全局) / Clock (global)	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	占空比稳定 / Duty cycle stabilizer: 0=开 / 0=on; 1=关 / 1=off	0x01	打开或关闭占空比稳定器。 / Turn the duty cycle stabilizer on or off.
0x0B	时钟分频(全局) / Clock divider (global)	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	时钟分频比[2:0] / Clock division ratio[2:0]: 000=1分频 / 000=divide by 1; 001=2分频 / 001=divide by 2; 010=3分频 / 010=divide by 3; 011=4分频 / 011=divide by 4; 100=5分频 / 100=divide by 5; 101=6分频 / 101=divide by 6; 110=7分频 /			0x00	

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值(十六进制) / Default (Hex)	注释 / Notes
							110=divide by 7; 111=8分频 / 111=divide by 8				
0x0C		禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	斩波模式 / Chopping mode: 0=关 / 0=off; 1=开 / 1=on	禁用 / Disabled	禁用 / Disabled	0x00	使能/禁用斩波模式。/ Enable/ disable chopping mode.
0x0D	测试模式(局部，PN序列复位除外) / Test mode (local, except PN sequence reset)	用户输入测试模式 / User input test mode: 00=单一 / 00=single; 01=交替 / 01=alternate; 10=单一一次 / 10=single once; 11=交替一次 / 11=alternate once（仅影响用户输入测试模式，位[3:0]=1000 / affects user input test mode only, bits[3:0]=1000)		产生复位PN长序列 / Generate/reset PN long sequence	产生复位PN短序列 / Generate/ reset PN short sequence	输出测试模式3:0 / Output test mode[3:0] (local): 0000=关(默认) / 0000=off (default); 0001=中间电平短序列 / 0001=midscale short; 0010=正FS / 0010=+FS; 0011=负FS / 0011=−FS; 0100=交替棋盘形式 / 0100=alternating checkerboard; 0101=PN 23序列 / 0101=PN 23 sequence; 0110=PN 9序列 / 0110=PN 9 sequence; 0111=1/0字反转 / 0111=1/0 word toggle; 1000=用户输入 / 1000=user input; 1001=1/0位反转 / 1001=1/0 bit toggle; 1010=1×同步 / 1010=1× sync; 1011=1位高电平 / 1011=1-bit high; 1100=混合位频率 / 1100=mixed bit frequency				0x00	置1时，测试数据将取代正常数据被置于输出引脚上。/ When set, test data replaces normal data on the output pins.
0x10	失调调整(局部) / Offset adjust (local)	8位器件失调调整，位7:0 / 8-bit device offset adjust, bits[7:0] (local)								0x00	器件失调调整。失调调整以LSB为单位，从+127到−128(二进制补码格式)。/ Device offset adjustment. Offset adjustment in LSB units, from +127 to −128

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值(十六进制) / Default (Hex)	注释 / Notes
											(two's complement format).
0x14	输出模式 / Output mode	禁用 / Disabled	LVDS-ANSI/LVDS-IEEE选项 / LVDS-ANSI/LVDS-IEEE option: 0=LVDS-ANSI; 1=LVDS-IEEE; 缩小范围链路(全局) / reduced-range link (global)	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	输出反向(局部) / Output invert (local)	禁用 / Disabled	输出格式 / Output format: 0=偏移二进制 / 0=offset binary; 1=二进制补码 / 1=two's complement (全局 / global)	0x01	配置输出和数据格式。 / Configure output and data format.
0x15	输出调整 / Output adjust	禁用 / Disabled	禁用 / Disabled	输出驱动器端接[1:0] / Output driver termination[1:0]: 00=无 / 00=none; 01=200Ω; 10=100Ω; 11=100Ω		禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	输出驱动 / Output drive: 0=1×驱动 / 0=1× drive; 1=2×驱动 / 1=2× drive	0x00	决定LVDS或其它输出属性。 / Determines LVDS or other output attributes.
0x16	输出相位 / Output phase	禁用 / Disabled	输入时钟相位调整[6:4] / Input clock phase adjust[6:4]（值			输出时钟相位调整[3:0] / Output clock phase adjust[3:0]（0000至1011 / 0000 to 1011）				0x03	在利用全局时钟分频的器件上，决定使用分频器

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值 (十六进制) / Default (Hex)	注释 / Notes
			为相位延迟的输入时钟周期数 / value is the number of input clock cycles of phase delay)								输出的哪个相位提供输出时钟。内部锁存不受影响。/ On devices using the global clock divider, determines which phase of the divider output provides the output clock. Internal latches are unaffected.
0x18	VREF	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	VREF调节数字方案[2:0] / VREF adjust digital scheme[2:0]: 000=1.0 V p-p (1.3 V p-p); 001=1.14 V p-p (1.48 V p-p); 010=1.33 V p-p (1.73 V p-p); 011=1.6 V p-p (2.08 V p-p); 100=2.0 V p-p (2.6 V p-p)			0x04	选择内部VREF。显示值针对VREF = 1.0 V (1.3 V)。/ Select internal VREF. Displayed values are for VREF = 1.0 V (1.3 V).
0x19	USER_PATT1_LSB(全局) / (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	用户定义的测试码1 LSB。/ User-defined test pattern 1 LSB.
0x1A		B15	B14	B13	B12	B11	B10	B9	B0	0x00	用户定义的测试码1 MSB。/

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值(十六进制) / Default (Hex)	注释 / Notes
	USER_PATT1_MSB(全局) / (global)										User-defined test pattern 1 MSB.
0x1B	USER_PATT2_LSB(全局) / (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	用户定义的测试码2 LSB。/ User-defined test pattern 2 LSB.
0x1C	USER_PATT2_MSB(全局) / (global)	B15	B14	B13	B12	B11	B10	B9	B0	0x00	用户定义的测试码2 MSB。/ User-defined test pattern 2 MSB.
0x21	串行输出数据控制(全局) / Serial output data control (global)	LVDS输出LSB优先 / LVDS output LSB first	SDR/DDR 单通道/双通道、逐位/逐字节 [6:4] / SDR/DDR single/dual-channel, bit-wise/byte-wise[6:4]: 000=SDR双通道、逐位 / 000=SDR dual-channel, bit-wise; 001=SDR双通道、逐字节 / 001=SDR dual-channel, byte-wise; 010=DDR双通道、逐位 / 010=DDR dual-channel, bit-wise; 011=DDR双通道、逐字节 / 011=DDR dual-channel, byte-wise; 100=DDR单通道、逐字 / 100=DDR single-channel, word-wise			禁用 / Disabled	选择2×帧 / Select 2× frame	串行输出位数 / Serial output word length: 00=16位 / 00=16 bits		0x30	串行流控制。默认为MSB优先、原有位流。/ Serial stream control. Default is MSB first, original bit stream.
0x22		禁用 / Disabled	禁用 / Disabled			禁用 / Disabled	禁用 / Disabled			0x00	

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值(十六进制) / Default (Hex)	注释 / Notes
	串行通道状态(局部) / Serial lane status (local)			禁用 / Disabled	禁用 / Disabled			通道输出复位 / Lane output reset	通道掉电 / Lane power-down		用来关断转换器的各个部分。 / Used to power down sections of the converter.
0x100	采样速率覆盖 / Sample rate override	禁用 / Disabled	Always write =01		禁用 / Disabled	采样速率 / Sample rate: 000=20 MSPS; 001=40 MSPS; 010=50 MSPS; 011=65 MSPS; 100=80 MSPS; 101=105 MSPS; 110=125 MSPS				0x00	
0x101	用户I/O控制 2 / User I/O control 2	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	SDIO下拉 / SDIO pull-down	0x00	禁用SDIO下拉电阻。 / Disable SDIO pull-down resistor.
0x102	用户I/O控制 3 / User I/O control 3	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	VCM掉电 / VCM power-down	禁用 / Disabled	禁用 / Disabled	0x00	VCM控制。 / VCM control.
0x106	比较器阈值算法 / Comparator threshold algorithm	保留 / Reserved	保留 / Reserved	保留 / Reserved	保留 / Reserved	保留 / Reserved	保留 / Reserved	00=关闭 / 00=off; 01=打开第1级 / 01=enable stage 1; 10=打开第2级 / 10=enable stage 2; 11=打开第1/2级 / 11=enable stages 1/2		0x00	
0x109	同步 / Sync	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	仅与下一同步脉冲同步 /	使能同步 / Enable sync	0x00	

地址(十六进制) / Address (Hex)	参数名称 / Parameter	位7 (MSB) / Bit7	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0	默认值 (十六进制) / Default (Hex)	注释 / Notes
								Sync with next sync pulse only			

电源地间保护 / Power-to-Ground Protection

To improve the anti-static capability of the device, the following ESD protection loops exist between the various supply pins inside the device. The forward conduction voltage drop of each ESD protection device is approximately 0.35V; during power-up and normal use, prolonged forward conduction of these ESD protection devices should be avoided.

为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.35V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。



Figure 27: Internal ESD protection circuits between supplies

注意事项 / Precautions

1、产品安装注意事项 / 1. Product Installation Precautions

1) Pay attention to device orientation during soldering to avoid soldering it in the wrong orientation. 2) Instruments and meters used for debugging the circuit must share a good common ground. PCB design must maintain good grounding and power-supply decoupling. 3) Take care not to reverse the power supply or short the input/output pins to the power supply, which can easily damage the circuit.

1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2、产品使用注意事项 / 2. Product Usage Precautions

1) Differential inputs should be routed as close together as possible and parallel to each other. 2) Input traces should be as short as possible to minimize parasitic capacitance and noise pickup. 3) For better heat dissipation and electrical performance, the die paddle of the chip should be soldered to a large ground area on the PCB, maximizing the thermal performance of the package. 4) Importantly, the chip ground should be connected to the PCB ground plane through as many vias and as much area as possible. 5) It is recommended to reset the circuit first after power-up before use. 6) When connecting power to this product, it is recommended to use two independent 1.8 V supplies: one for the analog output (AVDD) and another for the digital output (DRVDD and DVDD). Designers may use several different decoupling capacitors for high and low frequencies. Decoupling capacitors should be placed close to the printed-circuit-board (PCB) entry point and close to the device pins, with trace lengths as short as possible. This product requires only one PCB ground plane. Proper decoupling and skillful separation of the PCB analog, digital, and clock sections easily achieve optimum performance. 7) At power-up, this product enters an initial phase in which the internal state machine sets biases and registers so the device can operate normally. During initialization, this product requires a stable clock. If the ADC clock source is absent or unstable during ADC power-up, the state machine will be interrupted, causing the ADC to power up into an unknown state. To correct this state, the initial sequence must be re-invoked after the ADC clock stabilizes.

This can be done by initiating a digital reset via register 0x08. In the default configuration (internal VREF, AC-coupled input), VREF and VCM are provided by the ADC itself, so the clock is sufficiently stable at power-up. When VREF and/or VCM are provided by external sources, they must also be stable at power-up; otherwise, a sequential digital reset via register 0x08 is required. The pseudo-code sequence for the digital reset is as follows: SPI_Write (0x08, 0x03); # Digital Reset; SPI_Write (0x08, 0x00); # Normal Operation. 8) For optimum electrical and thermal performance, the exposed pad at the bottom of the ADC must be connected to analog ground (AGND). A continuous copper plane, exposed (without solder mask), on the PCB must match the exposed pad (pin 0) of this product. The copper plane must have multiple vias to obtain the lowest possible thermal-resistance path for heat dissipation through the bottom of the PCB. These vias should be filled or plugged with insulating epoxy. To maximize coverage and connection between the ADC and the PCB, a silkscreen layer should cover the PCB to divide the continuous plane into multiple equal sections. This prevents solder buildup during reflow and provides multiple connection points between the ADC and the PCB. A continuous, undivided plane guarantees only one connection point between the ADC and the PCB. Refer to the evaluation board for a PCB layout example. 9) Decouple the VCM pin to ground with a 0.1 µF capacitor. 10) The VREF pin should be decoupled to ground through an external low-ESR 0.1 µF ceramic capacitor in parallel with a low-ESR 1.0 µF capacitor. 11) When the converter needs to deliver its full dynamic performance, the SPI port should be disabled. Typically the SCLK, CSB, and SDIO signals are asynchronous to the ADC clock, so noise on these signals degrades converter performance. If other devices use the on-board SPI bus, it may be necessary to connect a buffer between that bus and this product to prevent these signals from changing at the converter's input pins during critical sampling periods. 12) Comparator thresholds may fluctuate due to process or environmental variations; it is recommended to enable the comparator threshold correction function during use. The SPI pseudo-code sequence is as follows: SPI_Write (0x106, 0x03);

1) 差分输入应尽量靠近且相互平行。 2) 输入连线应尽量短以最小化寄生电容和噪声引入。 3) 为了更好的散热并获得更好的电性能，芯片的底板应焊接到 PCB 板的一个大的地端，从而最大限度发挥封装的热性能。 4) 很重要的是，芯片的地应该通过尽量多的渠道和足够多的面积与 PCB 板的地层相连。 5) 推荐上电后首先对电路进行复位，再进行使用。 6) 当连接电源至本产品时，建议使用两个独立的 1.8 V 电源：一个电源用于模拟输出(AVDD)，另一个电源用于数字输出(DRVDD 和 DVDD)。设计人员可以使用多个不同的去耦电容以适用于高频和低频。去耦电容应放置在接近印刷电路板(PCB)入口点和接近器件引脚的位置，并尽可能缩短走线长度。本产品仅需要一个 PCB 接地层。对 PCB 模拟、数字和时钟模块进行合理去耦和巧妙分隔，可以轻松获得最佳性能。 7) 上电时，本产品进入初始相位，内部状态机设置偏置和寄存器，以便器件能正常工作。在初始化过程中，本产品需要稳定的时钟。若 ADC 时钟源不存在，或在 ADC 上电期间不稳定，则会打断状态机，进而导致 ADC 上电至未知状态。要校正这一状态，必须在 ADC 时钟稳定后重新调用初始序列。可通过寄存器 0x08 发起数字复位来完成该操作。在默认配置中(内部 VREF，交流耦合输入)，VREF 和 VCM 由 ADC 自身提供，因此上电时具有足够稳定的时钟。当 VREF 和/或 VCM 由外部源提供时，它们在上电时也必须是稳定的；否则，需要通过寄存器 0x08 进行序列数字复位。数字复位的伪代码序列如下所示：SPI_Write (0x08, 0x03); # Digital Reset SPI_Write (0x08, 0x00); # Normal Operation 8) 为获得最佳的电气性能和热性能，必须将 ADC 底部的裸露焊盘连接至模拟地(AGND)。PCB 上裸露(无阻焊膜)的连续铜平面必须与本产品的裸露焊盘(引脚 0)匹配。铜平面上必须有多个通孔，获得尽可能低的热阻路径以通过 PCB 底部进行散热。应采用绝缘环氧化物来填充或堵塞这些通孔。为了最大化地实现 ADC 与 PCB 之间的覆盖与连接，应在 PCB 上覆盖一个丝印层，以便将 PCB 上的连续平面划分为多个均等的部分。这样，在回流焊过程中，便可防止焊料堆积并在 ADC 与 PCB 之间提供多个连接点。而一个连续的、无分割的平面则仅可保证在 ADC 与 PCB 之间有一个连接点。PCB 布局范例可以参考评估板。 9) VCM 利用一个 0.1 µF 电容将 VCM 引脚去耦至地。 10) VREF 引脚应通过外部一个低 ESR 0.1 µF 陶瓷电容和一个低 ESR 1.0 µF 电容的并联去耦至地。 11) 当需要转换器充分发挥其全部动态性能时，应禁用 SPI 端口。通常 SCLK 信号、CSB 信号和 SDIO 信号与 ADC 时钟是异步的，因此，这些信号中的噪声会降低转换器性能。如果其它器件使用板

上 SPI 总线，则可能需要在该总线与本产品之间连接缓冲器，以防止这些信号在关键的采样周期内，在转换器的输入引脚端发生变化。 12) 受工艺或环境变化等影响，比较器阈值会出现波动，建议使用时打开比较器阈值矫正功能。SPI 伪代码序列如下所示：SPI_Write (0x106, 0x03);

3、产品防护注意事项 / 3. Product Protection Precautions

1) All pins of this circuit are designed with ESD protection structures; however, high-energy electrical pulses can still damage the circuit, so ESD protection should be observed during testing, handling, and storage. 2) Exceeding the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and do not imply that the device can operate normally under these conditions or under any other conditions beyond those shown in this product manual. 3) Under conditions avoiding direct exposure to rain and snow, packages containing the product may be transported by safe means of transport, but they must not be stacked together with acidic, alkaline, or other corrosive materials. Packaging should be secure, using available means of transport. 4) The storage environment for packaged products shall meet the Class I warehouse conditions specified in Section 8.1 of Q/W 657A (temperature: 15°C~25°C, humidity: 25%~65%), with no acids, alkalis, or other corrosive gases nearby, good ventilation, and appropriate anti-static measures.

1) 该电路所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 2) 超出绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。 3) 在避免雨、雪直接影响的条件下，装有产品的包装箱可以用安全的运输工具运输。但不能和带有酸性、碱性和其它腐蚀性物体堆放在一起。包装应是安全的，可以采用现有的运输工具。 4) 包装好的产品贮存环境应满足 Q/W 657A 第 8.1 规定的 I 类库房条件要求（温度：15°C~25°C，湿度：25%~65%），周围没有酸、碱或其它腐蚀性气体，通风良好，且具备相应防静电措施。

4、电装说明 / 4. Assembly Instructions

1) The moisture sensitivity level of this product is MSL3. After removing the product from the moisture-barrier bag, performing dry storage, or baking, the allowable floor life before reflow soldering is: ≤30°C/60RH%, 168 h. 2) If device storage conditions cannot be controlled or traced, bake strictly at 125°C for 8 h before assembly. 3) If the assembly environment temperature/humidity cannot be guaranteed at ≤30°C/60RH%, complete soldering within 12 h after baking. 4) After baking, the product is highly susceptible to static electricity; observe ESD protection throughout all operations. 5) For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C~235°C; the maximum peak temperature should not exceed 235°C; time within ±5°C of the peak temperature ≤20 s; time above liquidus 60~90 s; ramp-up rate 2~4°C/s; ramp-down rate 2~6°C/s. 6) For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C~245°C; the maximum peak temperature should not exceed 260°C; time within ±5°C of the peak temperature ≤20 s; time above liquidus 60~90 s; ramp-up rate 2~4°C/s; ramp-down rate 2~6°C/s. 7) If a mixed assembly process requires elevated temperature, ensure the device body temperature does not exceed 260°C (device body temperature is measured at the top surface of the device during reflow). 8) The solder terminal plating of this product is NiPdAu (nickel-palladium-gold).

1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； 3) 若电装环境温湿度无法保证≤30°C/60RH%，请在烘烤后 12h 内完成焊接； 4) 产品烘烤

后，极易产生静电，所有操作过程需要注意 ESD 防护； 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）； 8) 本产品焊接端镀层为镍钯金。

5、热阻 / 5. Thermal Resistance

表1 封装热阻 / Table 1. Package Thermal Resistance

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)	31.05 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2, natural-convection thermal test environmental requirements and test method for integrated circuits
Rthjt（结到器件顶面的热阻）/ Rthjt (junction-to-package-top thermal resistance)	3.298 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14, two-interface separation method for one-dimensional heat-transfer paths
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-package-bottom thermal resistance)	2.775 K/W	JESD51-14 拐点理论器件内部结构分层得到 / JESD51-14, obtained by inflection-point-theory layering of the device internal structure

常见故障及处理办法 / Common Faults and Troubleshooting

1. No signal output: check that the supply voltage, input signal, and clock are correctly applied. 2. Abnormal device function: identify the device operating mode and confirm the configuration is correct. 3. Unstable device operation: check the power supply and ensure the supply voltage is stable.

1. 无信号输出：检查电源电压、输入信号、时钟是否正确加载。 2. 器件功能不正常：明确器件工作模式，确认配置是否正确。 3. 器件工作不稳定：检查电源，保证电源电压稳定。

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附加说明 / Additional Notes

1. First release date of this manual: July 2026. 2. Product status: ☑ Production (this model is currently in production; formal products are available). ☐ Pre-release (this model has not yet entered formal production; samples are available). 3. Model suffix difference explanation (for series products,

explain model suffixes as in the example below; add this section when needed): This model has no suffix. 4. Cross-reference notes vs. the foreign product:

1. 本说明书首次发布日期：2026 年 7 月。 2. 本产品状态：☑ 生产（该产品型号目前已在生产，可以提供正式产品） □预发布（该产品型号尚未投入正式生产，可以提供样品） 3. 型号后缀差异性说明（系列化产品需对型号后缀说明如下示例，需要时增加此部分）：本型号产品无后缀 4. 替代国外产品情况说明：

1）绝对最大额定值对比 / 1) Absolute Maximum Ratings Comparison

附表1 绝对最大额定值对比 / Appendix Table 1. Absolute Maximum Ratings Comparison

参数 / Parameter	SXA031 规范要求 / SXA031 Specification	AD9653 器件手册 / AD9653 Datasheet	比对结果 / Comparison Result
模拟电源电压（VAVDD）/ Analog supply voltage (VAVDD)	2V	2V	一致 / Consistent
数字电源电压（VDRVDD）/ Digital supply voltage (VDRVDD)	2V	2V	一致 / Consistent
贮存温度（Tstg）/ Storage temperature (Tstg)	-55°C~125°C	-65°C~150°C	不一致 / Not consistent
结温（TJ）/ Junction temperature (TJ)	150°C	150°C	一致 / Consistent

2）推荐工作条件对比 / 2) Recommended Operating Conditions Comparison

附表2 推荐工作条件对比 / Appendix Table 2. Recommended Operating Conditions Comparison

参数 / Parameter	SXA031 规范要求 / SXA031 Specification	AD9653 器件手册 / AD9653 Datasheet	比对结果 / Comparison Result
工作频率（fCLK）/ Operating frequency (fCLK)	20MHz~125MHz	20MHz~125MHz	一致 / Consistent
模拟电源电压（VAVDD）/ Analog supply voltage (VAVDD)	1.75V~1.9V	1.75V~1.9V	一致 / Consistent
数字电源电压（VDRVDD）/ Digital supply voltage (VDRVDD)	1.75V~1.9V	1.75V~1.9V	一致 / Consistent
输入信号幅度范围（峰峰值）/ Input signal amplitude range (peak-to-peak)	≤2V	≤2V	一致 / Consistent
工作环境温度（TA）/ Operating ambient temperature (TA)	-40°C~85°C	-40°C~85°C	一致 / Consistent

3）其它指标对比 / 3) Other Parameter Comparison

附表3 其它指标对比 / Appendix Table 3. Other Parameter Comparison

参数 / Parameter	SXA031	AD9653	比对结果 / Comparison Result
封装形式 / Package	QFN48	QFN48	一致 / Consistent
质量等级 / Quality grade	企标 / Enterprise standard	工业级 / Industrial grade	有差异 / Different

参数 / Parameter	SXA031	AD9653	比对结果 / Comparison Result
尺寸 / Dimensions	7mm×7mm×0.75mm	7mm×7mm×0.75mm	一致 / Consistent
替代建议 / Cross-reference recommendation	□直接替代 / □Direct replacement □有效替代 / □Effective alternative ☑功能替代 / ☑Functional alternative		

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