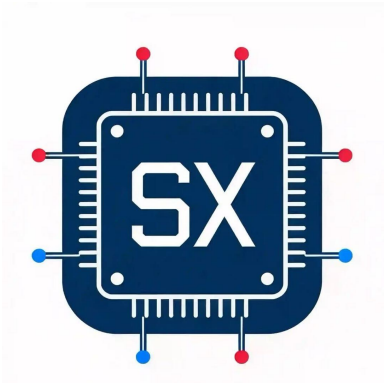


SXA032

Dual-Channel 14-Bit, 1250 MSPS A/D Converter

双通道 14 位 1250MSPS A/D 转换器

14-bit | 2 channels | 1250 MSPS | QFN64 | JESD204B

14 位 | 双通道 | 1250MSPS | QFN64 | JESD204B

对标 / Cross Reference: AD9680 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXA032 Dual-Channel 14-Bit 1250MSPS A/D Converter — Product Manual (Bilingual)

SXA032 型双通道 14 位 1250MSPS A/D 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深信科技 **V1.20260722**

对标 / Cross Reference: AD9680 — pin-to-pin compatible alternative

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版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20260722	2026.07.22	——	首次发布 / Initial release	

1. 产品用途及应用范围 / Product Applications

The SXA032 is suitable for the following applications. / SXA032 适用于以下应用：

- High-end medical imaging equipment / 高端医疗成像设备
- IF signal sampling in communications receivers / 通信接收器中频信号采样
- Portable instruments / 便携式仪表
- Low-power digital oscilloscopes / 低功耗数字示波器

2. 标准 / Standards

- Detailed specification and approval number: Q/GC 0227-2026 "Detailed Specification for SXA032 Dual-Channel 14-Bit 1250MSPS A/D Converter". 详细规范及确认号：Q/GC 0227-2026《半导体集成电路 SXA032 型双通道 14 位 1250MSPS A/D 转换器详细规范》
- Quality grade / quality assurance requirement: Enterprise standard / 质量等级/质量保证要求：企标

3. 产品特点 / Features

English: - Analog supply voltages: 1.3/2.5/3.3V - Digital supply voltage: 1.3V - Sample rate: 1250MSPS - Signal-to-noise ratio (SNR): 61dBFS @ Fin=765MHz (typical) - Spurious-free dynamic range (SFDR): 69dBFS @ Fin=765MHz (typical) - Power consumption: ≤4.8W (dual channel) - Analog input range: 1.46VPP~1.94VPP - Circuit interface: SERDES serial output supporting up to 12.5Gbps - -3dB bandwidth: 2GHz - ESD rating: Class 1B, HBM model, 500V - Weight: 0.22g±0.04g - Moisture sensitivity level: MSL3 - Package: QFN64 - Multi-chip synchronization supported - Fast over-threshold detection of the input signal, supporting efficient automatic gain control (AGC)

中文： - 模拟电源电压：1.3/2.5/3.3V - 数字电源电压：1.3V - 采样率：1250MSPS - 信噪比：61dBFS@Fin=765MHz（典型值） - 无杂散动态范围：69dBFS@Fin=765MHz（典型值） - 功耗：≤4.8W（双通道） - 模拟输入范围：1.46VPP~1.94VPP - 电路接口：支持最高 12.5Gbps 的 SERDES 串行输出 - -3dB 带宽：2GHz - ESD 等级：1B 级，HBM 模型，500V - 重量：0.22g±0.04g - 湿敏等级：MSL3 - 封装形式：QFN64 - 支持多芯片同步 - 输入信号超阈值快速检测功能，支持实现高效自动增益控制

4. 产品描述 / Product Description

English: The SXA032 14-bit 1250MSPS A/D converter is packaged in QFN64. Its functional block diagram is shown in Figure 1. The device integrates an on-chip buffer and sample-and-hold circuit, designed for low power, small size and ease of use. It is designed to sample wideband analog signals up to 2 GHz, and is optimized for wide input bandwidth, high sample rate, excellent linearity, small package and low power.

SXA032 型 14 位 1250MSPS A/D 转换器采用 QFN64 封装，功能框图如图 1 所示。该器件内置片内缓冲器和采样保持电路，专门针对低功耗、小尺寸和易用性而设计。该器件设计用于高达 2 GHz 的宽带模拟信号采样。该器件针对宽输入带宽、高采样速率、出色的线性度和小封装低功耗而优化。

English: The dual-channel ADC core uses a multi-stage, differential pipelined architecture with integrated output error-correction logic. Each ADC features wide-bandwidth inputs supporting user-selectable input ranges. An integrated voltage reference simplifies the design. Both analog inputs and clock signals are differential. Each ADC data output is internally connected to two digital downconverters (DDCs). Each DDC contains four cascaded signal-processing stages: one 12-bit frequency converter (NCO) and four half-band decimation filters.

这款双通道 ADC 内核采用多级、差分流水线架构，并集成了输出纠错逻辑。每个 ADC 均具有宽带宽输入，支持用户可选的各种输入范围。集成基准电压源可简化设计。模拟输入和时钟信号均为差分输入信号。每个 ADC 数据输出均内部连接至两个数字下变频器(DDC)。每个 DDC 均含有四个级联信号处理级：一个 12 位频率转换器(NCO)和四个半带抽取滤波器。

English: In addition to the DDC blocks, the device provides other features that simplify automatic gain control (AGC) in communications receivers. Using the ADC fast-detect output bits, a programmable threshold detector can monitor input signal power. If the input signal level exceeds the programmable threshold, the fast-detect indicator goes high. Because the latency of this threshold indicator is extremely short, the user can quickly reduce system gain, avoiding overrange at the ADC input.

除了 DDC 模块，该器件还具备其他功能，能够简化通信接收机的自动增益控制(AGC)。利用 ADC 的快速检测输出位，可编程阈值检测器可以监控输入信号功率。如果输入信号电平超过可编程阈值，快速检测指示器就会变为高。由于该阈值指示器的延迟极短，因此用户能够快速调低系统增益，从而避免 ADC 输入端出现超量程现象。

English: The user can configure the Subclass 1 JESD204B high-speed serial output as 1, 2 or 4 lanes, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multi-device synchronization is supported via the SYSREF± and SYNCINB± input pins. The product functional block diagram is shown in Figure 1:

用户能将子类 1 JESD204B 高速串行输出配置为 1、2 或 4 通道，具体取决于 DDC 配置和接收逻辑器件的可接受通道速率。通过 SYSREF±和 SYNCINB±输入引脚，可提供多器件同步支持。该产品功能框图如图 1 所示：

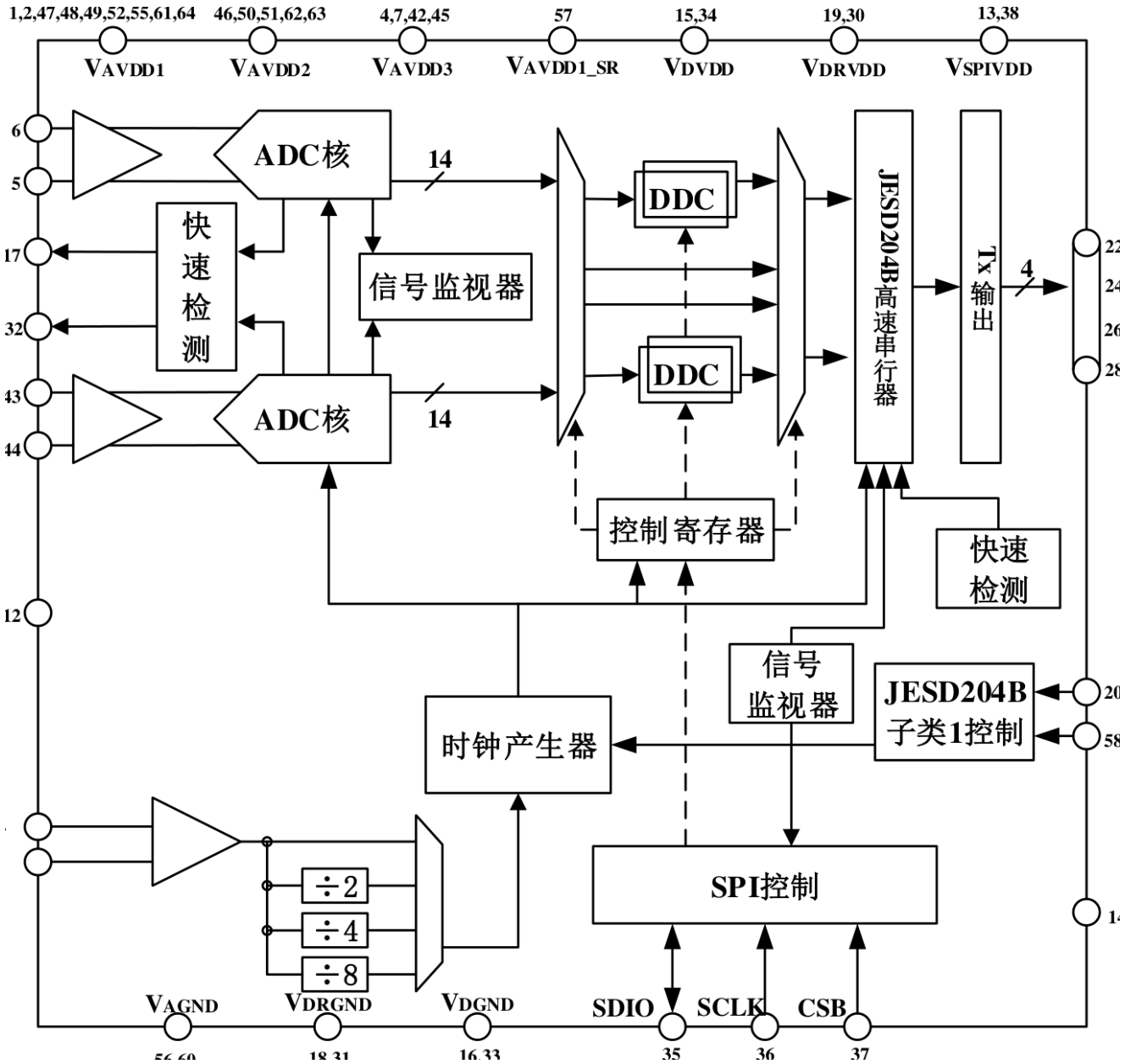


Figure 1: SXA032 functional block diagram

The operating timing of the product is as follows. / 该产品工作时序如下：

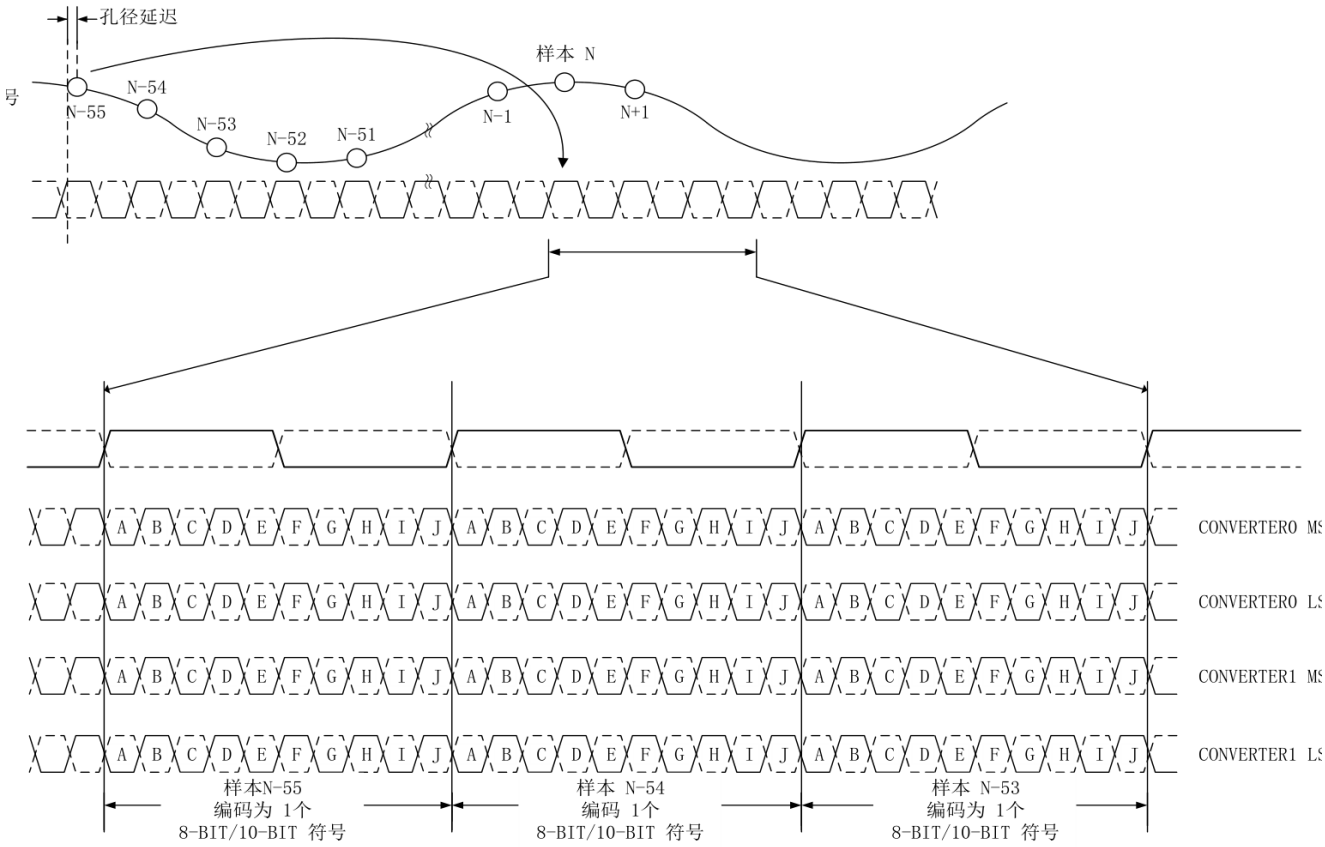


Figure 2: Data output timing (full-bandwidth mode, L=4, M=2, F=1)

表1 工作时序特性 / Table 1 — Operating Timing Characteristics

Parameter / 参数	Symbol/Note / 符号/注释	Min / 最小值	Typ / 典型值	Max / 最大值	Unit / 单位
CLK+ to SYSREF+ timing requirement	See Figure 3 / 参见图 3				
Device clock to SYSREF+ setup time / 器件时钟至 SYSREF+建立时间	tSU_SR		117		ps
Device clock to SYSREF+ hold time / 器件时钟至 SYSREF+保持时间	tH_SR		−96		ps
SPI timing requirements	See Figure 4 / 参见图 4				
Setup time between data and SCLK rising edge / 数据与 SCLK 上升沿之间的建立时间	tDS		3		ns
Hold time between data and SCLK rising edge / 数据与 SCLK 上升沿之间的保持时间	tDH		3		ns
SCLK period / SCLK 周期	tCLK		40		ns
Setup time between CSB and SCLK / CSB 与 SCLK 之间的建立时间	tS		3		ns
Hold time between CSB and SCLK / CSB 与 SCLK 之间的保持时间	tH		3		ns
Minimum time SCLK must remain at logic high / SCLK 应处于逻辑高电平状态的最短时间	tHIGH		10		ns
Minimum time SCLK must remain at logic low / SCLK 应处于逻辑低电平状态的最短时间	tLOW		10		ns

Parameter / 参数	Symbol/Note / 符号/注释	Min / 最小值	Typ / 典型值	Max / 最大值	Unit / 单位
Time for the SDIO pin to switch from input to output relative to the SCLK falling edge (not shown in Figure 4) / 相对于 SCLK 下降沿，SDIO 引脚从输入状态切换到输出状态所需的时间(图4 未显示)	tEN_SDIO			10	ns
Time for the SDIO pin to switch from output to input relative to the SCLK rising edge (not shown in Figure 4) / 相对于 SCLK 上升沿，SDIO 引脚从输出状态切换到输入状态所需的时间(图4 未显示)	tDIS_SDIO			10	ns

时间					
相对于 SCLK 下降沿，SDIO 引脚从输入状态切换到输出状态所需的时间(图 4 未显示)	t_{EN_SDIO}		10		ns
相对于 SCLK 上升沿，SDIO 引脚从输出状态切换到输入状态所需的时间(图 4 未显示)	t_{DIS_SDIO}		10		ns

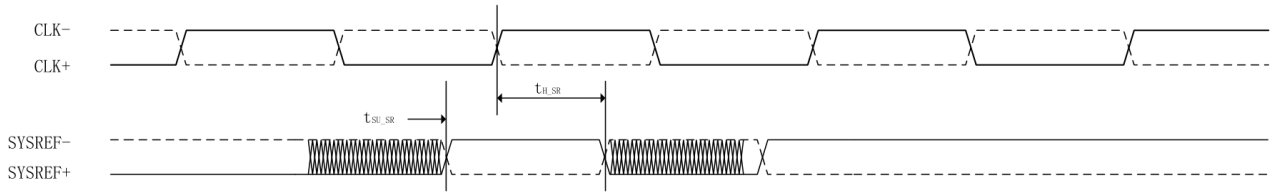


Figure 3: SYSREF± setup/hold timing

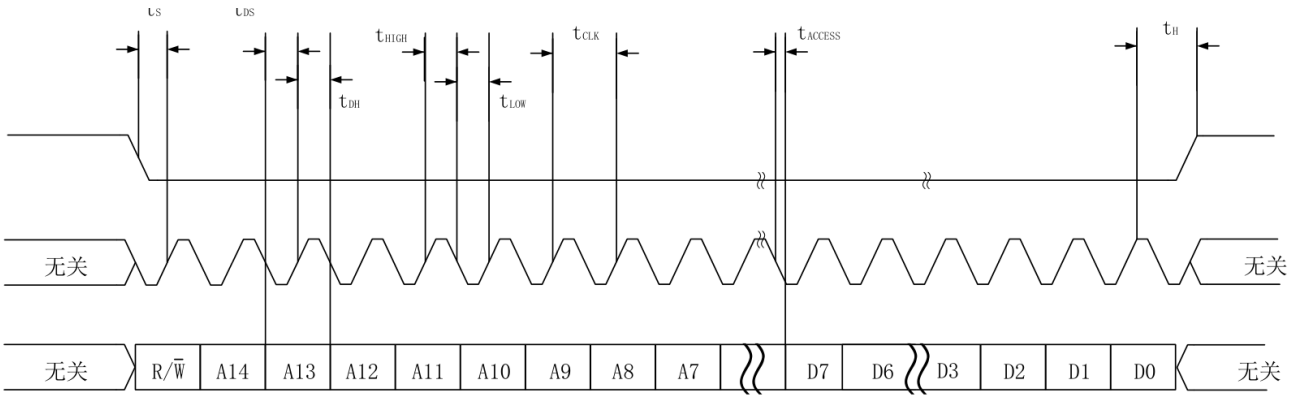


Figure 4: SPI timing

5. 产品外形图 / Package Outline

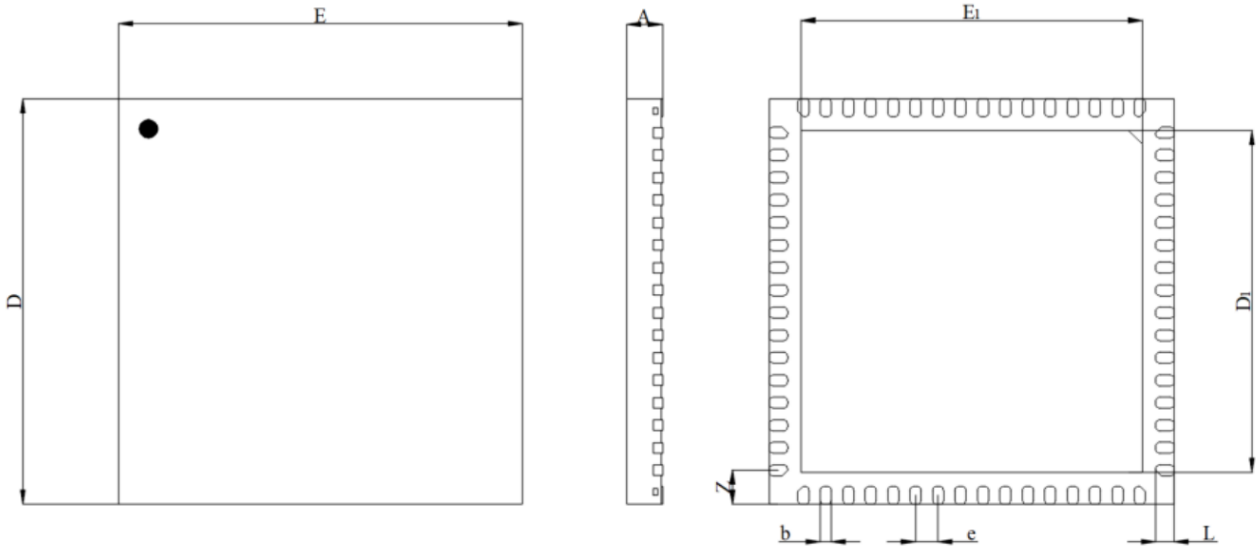


Figure 5: Package outline dimensions

Dimensions in millimeters. / 单位为毫米

Dimension / 尺寸符号	Min / 最小	Nom / 公称	Max / 最大	Dimension / 尺寸符号	Min / 最小	Nom / 公称	Max / 最大
A	0.60	0.80	1.00	D1	7.50	7.60	7.70
D	8.80	9.00 [^a]	9.20	E1	7.50	7.60 [^a]	7.70
E	8.80	9.00 [^a]	9.20	L	0.35	0.40 [^a]	0.45
b	0.20	0.25 [^a]	0.30	(Z) [^a]	—	0.75 [^a]	0.90
e	—	0.50	—				

[^a]: Design guaranteed, not tested. / 设计保证，不进行考核。 Note: see the assembly instructions for recommended pad design. / 注：推荐焊盘设计详见电装说明。

6. 引出端排列（俯视图） / Pinout (Top View)

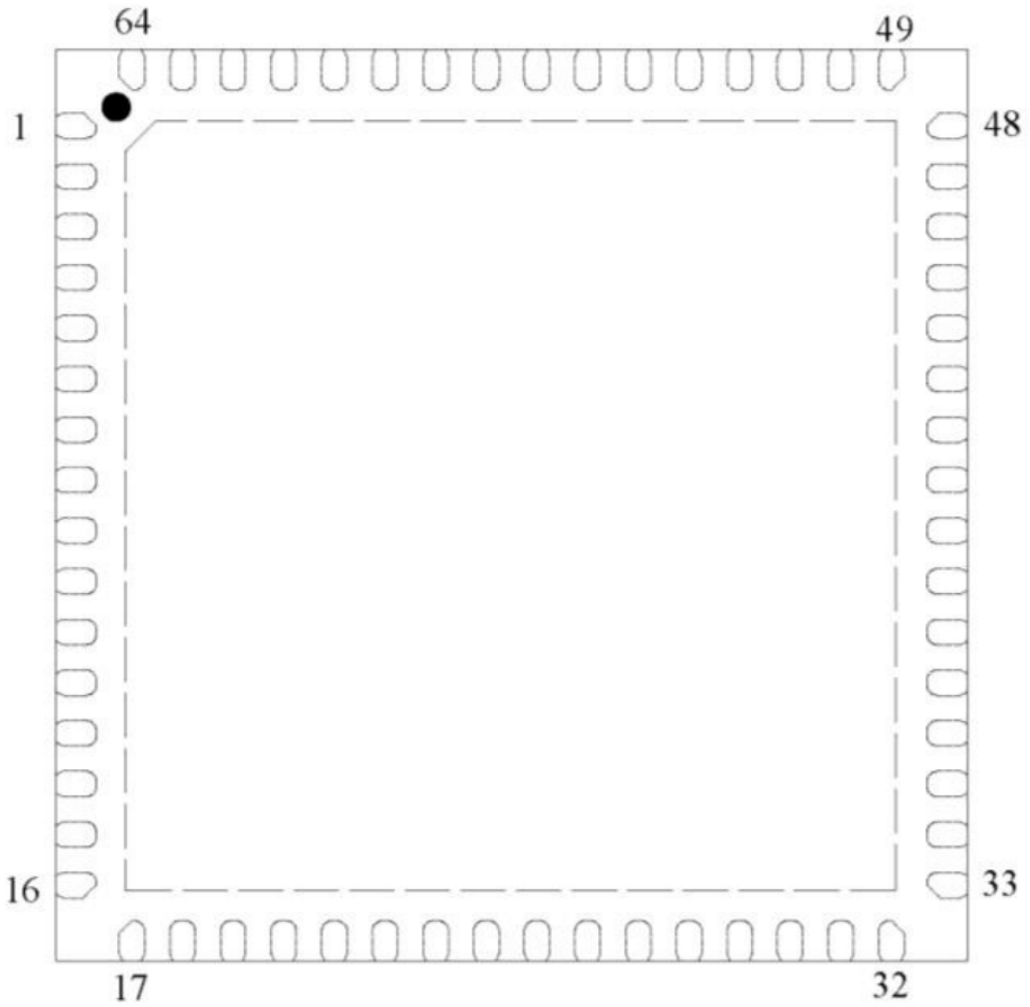


Figure 6: Pinout

7. 引出端功能符号表 / Pin Function Table

表2 引出端功能符号 / Table 2 — Pin Functions

Pin / 引出端号	Symbol / 符号	Name / 名称	I/O	Pin / 引出端号	Symbol / 符号	Name / 名称	I/O
—	EPAD	Exposed pad; must be connected to ground for normal operation. / 裸露焊盘，该焊盘必须与地相连，才能正常工作。	—	33	DGND	Digital ground / 数字地	—
1	VAVDD1	Analog supply 1 / 模拟电源 1	—	34	VDVDD	Digital supply / 数字电源	—

Pin / 引出端号	Symbol / 符号	Name / 名称	I/O	Pin / 引出端号	Symbol / 符号	Name / 名称	I/O
2	VAVDD1	Analog supply 1 / 模拟电源 1	—	35	SDIO	SPI data serial input/output / SPI 数据串行输入输出口	Input/ Output / 输入/输出
3	VAVDD2	Analog supply 2 / 模拟电源 2	—	36	SCLK	SPI serial clock / SPI 串行时钟	Input / 输入
4	VAVDD3	Analog supply 3 / 模拟电源 3	—	37	CSB	SPI chip select (active low) / SPI 芯片选择（低电平有效）	Input / 输入
5	VIN(A)−	Channel A analog input, negative / A 通道模拟输入，负端	Input / 输入	38	VSPIVDD	SPI digital supply / SPI 数字电源	—
6	VIN(A)+	Channel A analog input, positive / A 通道模拟输入，正端	Input / 输入	39	VAVDD2	Analog supply 2 / 模拟电源 2	—
7	VAVDD3	Analog supply 3 / 模拟电源 3	—	40	VAVDD2	Analog supply 2 / 模拟电源 2	—
8	VAVDD2	Analog supply 2 / 模拟电源 2	—	41	VAVDD2	Analog supply 2 / 模拟电源 2	—
9	VAVDD2	Analog supply 2 / 模拟电源 2	—	42	VAVDD3	Analog supply 3 / 模拟电源 3	—
10	VAVDD2	Analog supply 2 / 模拟电源 2	—	43	VIN(B)+	Channel B analog input, positive / B 通道模拟输入，正端	Input / 输入
11	VAVDD2	Analog supply 2 / 模拟电源 2	—	44	VIN(B)−	Channel B analog input, negative / B 通道模拟输入，负端	Input / 输入
12	V1P0	1.0 V reference voltage input / Do-not-connect. This pin can be configured via SPI as a no-connect pin or an input. When using the internal reference, do not connect this pin. When using an external reference, a 1.0 V reference input is required. / 1.0 V基准电压输入/勿连接。此引脚可通过SPI配置为不连接引脚或输入。使用内部基准电压源时，请勿连接此引脚。若使用外部基准电压源，则需要1.0 V 基准电压输入。	Input/ Output / 输入/输出	45	VAVDD3	Analog supply 3 / 模拟电源 3	—
13	VSPIVDD	SPI digital supply / SPI 数字电源	—	46	VAVDD2	Analog supply 2 / 模拟电源 2	—
14	PDWN/STBY	Power-down input (active high). Operation of this pin depends on the SPI mode and can be configured as power-down or standby. Requires an external 10 kΩ pull-down resistor. / 掉电输入(高电平有效)。此引脚的操作取决	Input / 输入	47	VAVDD1	Analog supply 1 / 模拟电源 1	—

Pin / 引出端号	Symbol / 符号	Name / 名称	I/O	Pin / 引出端号	Symbol / 符号	Name / 名称	I/O
		于SPI模式，可配置为掉电或待机。要求外接10K 下拉电阻					
15	VDVDD	Digital supply / 数字电源	—	48	VAVDD1	Analog supply 1 / 模拟电源 1	—
16	DGND	Digital ground / 数字地	—	49	VAVDD1	Analog supply 1 / 模拟电源 1	—
17	FD_A	Channel A fast-detect output / A 通道快速检测输出	Output / 输出	50	VAVDD2	Analog supply 2 / 模拟电源 2	—
18	DRGND	Digital driver ground / 数字驱动地	—	51	VAVDD2	Analog supply 2 / 模拟电源 2	—
19	VDRVDD	Digital driver supply / 数字驱动电源	—	52	VAVDD1	Analog supply 1 / 模拟电源 1	—
20	SYNCINB−	JESD204B LVDS active-low synchronization input, negative / JESD204B LVDS 低电平有效同步输入，负端	Input / 输入	53	CLK+	ADC master clock input, positive / ADC 主时钟输入，正端	Input / 输入
21	SYNCINB+	JESD204B LVDS active-low synchronization input, positive / JESD204B LVDS 低电平有效同步输入，正端	Input / 输入	54	CLK−	ADC master clock input, negative / ADC 主时钟输入，负端	Input / 输入
22	SERDOUT0−	Lane 0 data output, negative / Lane0 数据输出，负端	Output / 输出	55	VAVDD1	Analog supply 1 / 模拟电源 1	—
23	SERDOUT0+	Lane 0 data output, positive / Lane0 数据输出，正端	Output / 输出	56	AGND	SYSREF+ ground reference / SYSREF+地参考	—
24	SERDOUT1−	Lane 1 data output, negative / Lane1 数据输出，负端	Output / 输出	57	VAVDD1_SR	Synchronization circuit analog supply / 同步电路模拟电源	—
25	SERDOUT1+	Lane 1 data output, positive / Lane1 数据输出，正端	Output / 输出	58	SYSREF+	Synchronization reference clock, positive / 同步参考时钟，正端	Input / 输入
26	SERDOUT2−	Lane 2 data output, negative / Lane2 数据输出，负端	Output / 输出	59	SYSREF−	Synchronization reference clock, negative / 同步参考时钟，负端	Input / 输入
27	SERDOUT2+	Lane 2 data output, positive / Lane2 数据输出，正端	Output / 输出	60	AGND	SYSREF+ ground reference / SYSREF+地参考	—
28	SERDOUT3−	Lane 3 data output, negative / Lane3 数据输出，负端	Output / 输出	61	VAVDD1	Analog supply 1 / 模拟电源 1	—
29	SERDOUT3+	Lane 3 data output, positive / Lane3 数据输出，正端	Output / 输出	62	VAVDD2	Analog supply 2 / 模拟电源 2	—
30	VDRVDD	Digital driver supply / 数字驱动电源	—	63	VAVDD2		—

Pin / 引出端号	Symbol / 符号	Name / 名称	I/O	Pin / 引出端号	Symbol / 符号	Name / 名称	I/O
						Analog supply 2 / 模拟电源 2	
31	DRGND	Digital driver ground / 数字驱动地	—	64	VAVDD1	Analog supply 1 / 模拟电源 1	—
32	FD_B	Channel B fast-detect output / B 通道快速检测输出	Output / 输出				

8. 推荐工作条件 / Recommended Operating Conditions

English: - Operating frequency (fCLK): 300~1250MSPS - Analog supply voltage (VAVDD1): 1.25V~1.30V - Analog supply voltage (VAVDD2): 2.44V~2.56V - Analog supply voltage (VAVDD3): 3.2V~3.4V - SYSREF supply voltage (VAVDD1_SR): 1.25V~1.30V - Digital supply voltage (VDVDD): 1.25V~1.30V - Driver supply voltage (VDRVDD): 1.25V~1.30V - SPI supply voltage (VSPIVDD): 1.7V~2.0V - Input signal amplitude range (peak-to-peak) (VIN(P-P)): ≤1.4V-1.5V[a] - Operating temperature (TA): -40°C~85°C

[a] Recommended input signal amplitude range for users; the actual acceptance test condition is 1.58V. / 推荐用户使用输入信号幅度范围，实际考核测试条件为 1.58V。

中文： - 工作频率（fCLK）：300~1250MSPS - 模拟电源电压（VAVDD1）：1.25V~1.30V - 模拟电源电压（VAVDD2）：2.44V~2.56V - 模拟电源电压（VAVDD3）：3.2V~3.4V - SYSREF 电源电压（VAVDD1_SR）：1.25V~1.30V - 数字电源电压（VDVDD）：1.25V~1.30V - 驱动电源电压（VDRVDD）：1.25V~1.30V - SPI 电源电压（VSPIVDD）：1.7V~2.0V - 输入信号幅度范围（峰峰值）（VIN(P-P)）：≤1.4V-1.5V[a] - 工作温度（TA）：-40°C~85°C

中文： [a] 推荐用户使用输入信号幅度范围，实际考核测试条件为 1.58V。

9. 绝对最大额定值 / Absolute Maximum Ratings

- Voltage from pin VAVDD1 to VAGND: 1.32 V / 引脚 VAVDD1 到 VAGND 电压：1.32V
- Voltage from pin VAVDD1_SR to VAGND: 1.32 V / 引脚 VAVDD1_SR 到 VAGND 电压：1.32 V
- Voltage from pin VAVDD2 to VAGND: 2.75 V / 引脚 VAVDD2 到 VAGND 电压：2.75V
- Voltage from pin VAVDD3 to VAGND: 3.63 V / 引脚 VAVDD3 到 VAGND 电压：3.63V
- Voltage from pin VDVDD to VDGND: 1.32 V / 引脚 VDVDD 到 VDGND 电压：1.32V
- Voltage from pin VDRVDD to VDRGND: 1.32 V / 引脚 VDRVDD 到 VDRGND 电压：1.32V
- Voltage from pin VSPIVDD to VAGND: 3.63 V / 引脚 VSPIVDD 到 VAGND 电压：3.63V
- Voltage from pin VAGND to VDRGND: −0.3 V – 0.3 V / 引脚 VAGND 到 VDRGND 电压：-0.3V-0.3V
- Voltage from pin VIN(A)+ to VAGND: 3.2 V / 引脚 VIN(A)+到 VAGND 电压：3.2V
- Voltage from pin VIN(B)+ to VAGND: 3.2 V / 引脚 VIN(B)+到 VAGND 电压：3.2V
- Voltage from pins SCLK, SDIO, CSB to VAGND: −0.3 V – (VSPIVDD + 0.3 V) / 引脚 SCLK、SDIO、CSB 到 VAGND 电压：-0.3V-（VSPIVDD+0.3V）
- Voltage from pin PDWN/STBY to VAGND: −0.3 V – (VSPIVDD + 0.3 V) / 引脚 PDWN/STBY 到 VAGND 电压：-0.3V-（VSPIVDD+0.3V）
- Storage temperature (Tstg): −65 °C – 150 °C / 贮存温度（Tstg）：-65°C~150°C
- Lead soldering temperature (Th) (10 s): 260 °C / 引线耐焊接温度（Th）（10s）：260°C

10. 性能指标 / Performance Specifications

表3 性能指标 / Table 3 — Performance Specifications

English: Conditions (unless otherwise specified): VAVDD1=1.3V, VAVDD2=2.5V, VAVDD3=3.3V, VAVDD1_SR=1.3V, VDVDD=1.3V, VDRVDD=1.3V, VSPIVDD=1.8V, AGND=DGND=DRGND=0V, -40°C≤TA≤85°C.

中文： 条件（除另有规定外，VAVDD1=1.3，VAVDD2=2.5，VAVDD3=3.3V，VAVDD1_SR=1.3V，VDVDD=1.3，VDRVDD=1.3V，VSPIVDD=1.8，AGND=DGND=DRGND=0V，-40°C≤TA≤85°C）

特性 / Characteristic	符号 / Symbol	条件 / Condition	最小 / Min	典型值 / Typ	最大 / Max	单位 / Unit
分辨率 / Resolution	RES	——	14	14	14	Bits
采样率 / Sample rate	Fs	——	300	1250	1250	MSPS
通道数 / Number of channels	NCH	——	2	2	2	CH
功耗 / Power consumption	Pw	双通道 / Dual channel	—	4.1	4.8	W
微分非线性误差 / Differential nonlinearity error	EDL	——	-2.0	±0.7	2.0	LSB
积分非线性误差 / Integral nonlinearity error	EL	——	-20	±3	+20	LSB
基准输出电压 / Reference output voltage	VREF	——	950	1003	1050	mV
信噪比 / SNR	SNR	fIN=10MHz	58.0	65	—	dBFS
		fIN=450MHz	56.5	63	—	dBFS
		fIN=765MHz	55.0	61	—	dBFS
信噪失真比 / SINAD	SNDR	fIN=10MHz	57.5	64	—	dBFS
		fIN=450MHz	56.0	61	—	dBFS
		fIN=765MHz	54.5	59	—	dBFS
有效位 / ENOB	ENOB	fIN=10MHz	9.25	10.5	—	dBFS
		fIN=450MHz	9.00	9.9	—	dBFS
		fIN=765MHz	8.76	9.5	—	dBFS
无杂散动态范围 / SFDR	SFDR	fIN=10MHz	65.0	80	—	dBFS
		fIN=450MHz	60.0	70	—	dBFS
		fIN=765MHz	55.0	69	—	dBFS
二三阶谐波 / 2nd/3rd harmonics	HD2,3nd	fIN=10MHz	—	-79	-65.0	dBFS
		fIN=450MHz	—	-70	-60.0	dBFS
		fIN=765MHz	—	-67	-55.0	dBFS
JESD204B 接口速率 / JESD204B interface rate	fserdes	——	—	12.5	12.5	Gbps
逻辑输入高电平电压[a] / Logic input high voltage	VIH	——	0.8VSPIVDD	0.8VSPIVDD	—	V
	VIL	——	0	0.5	0.5	V

特性 / Characteristic	符号 / Symbol	条件 / Condition	最小 / Min	典型值 / Typ	最大 / Max	单位 / Unit
逻辑输入低电平电压 [a] / Logic input low voltage						
逻辑输出高电平电压 [a] / Logic output high voltage	VOH	——	0.8VSPIVDD	0.8VSPIVDD	—	V
逻辑输出低电平电压 [a] / Logic output low voltage	VOL	——	0	0.5	0.5	V
模拟电源 1 电流 [a] / Analog supply 1 current	IAVDD1	——	—	805	—	mA
模拟电源 2 电流 [a] / Analog supply 2 current	IAVDD2	——	—	800	—	mA
模拟电源 3 电流 [a] / Analog supply 3 current	IAVDD3	——	—	135	—	mA
同步电路电源电流 [a] / Sync circuit supply current	IAVDD1_SR	——	—	11	—	mA
数字电源电流 [a] / Digital supply current	IDVDD	——	—	260	—	mA
数字驱动电源电流 [a] / Digital driver supply current	IDRVDD	——	—	221	—	mA
SPI 数字电源电流 [a] / SPI digital supply current	ISPIVDD	——	—	2.5	—	mA

English: Note: typical values are room-temperature test data. [a] Not subject to acceptance testing; provided for user reference only.

中文： 注：典型值为常温测试数据，[a] 未纳入考核，仅供用户参考使用。

11. 主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

English: 1. FFT spectrum at analog input 10MHz. 2. FFT spectrum at analog input 450MHz. 3. FFT spectrum at analog input 765MHz. 4. Typical differential error (EDL) and linearity error (EL) curves.

中文： 1、模拟输入 10MHz 条件下 FFT 谱线。2、模拟输入 450MHz 条件下 FFT 谱线。3、模拟输入 765MHz 条件下 FFT 谱线。4、典型微分误差（EDL）和线性误差（EL）曲线。

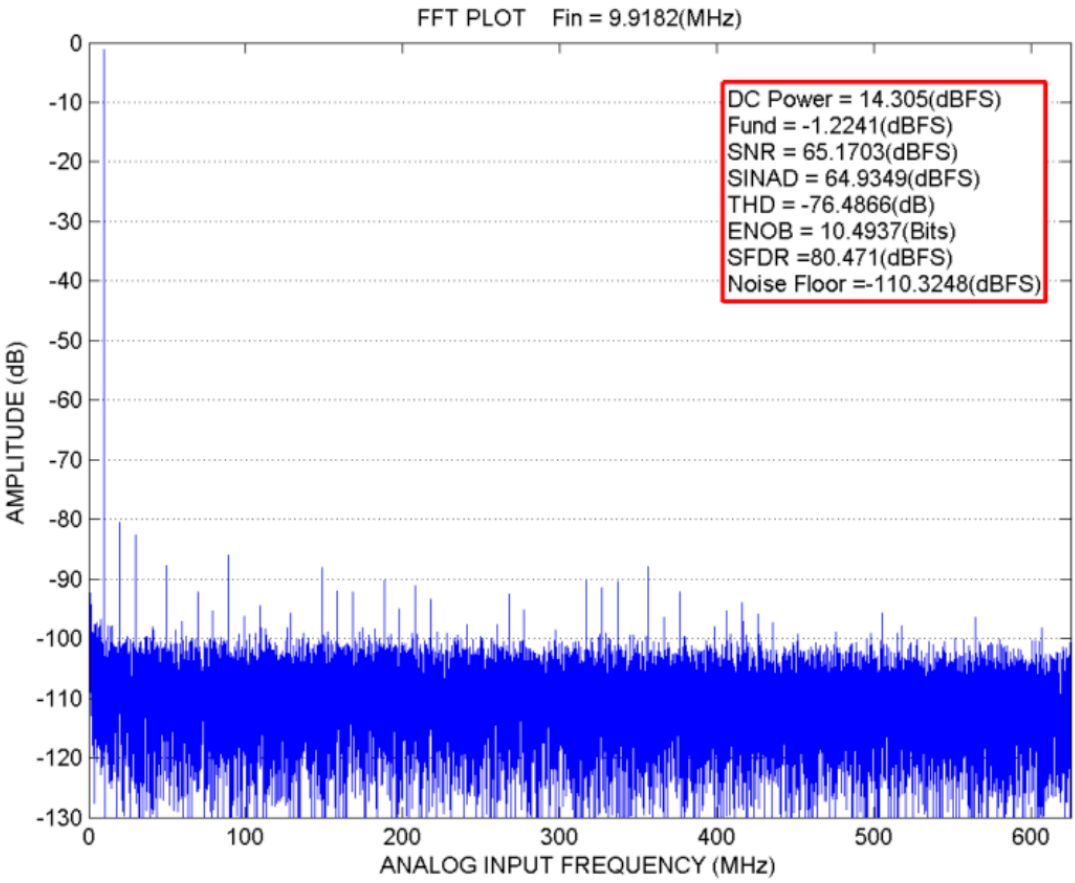


Figure 7: FFT spectrum, fCLK=1250MHz, fin=10MHz, TA=25°C

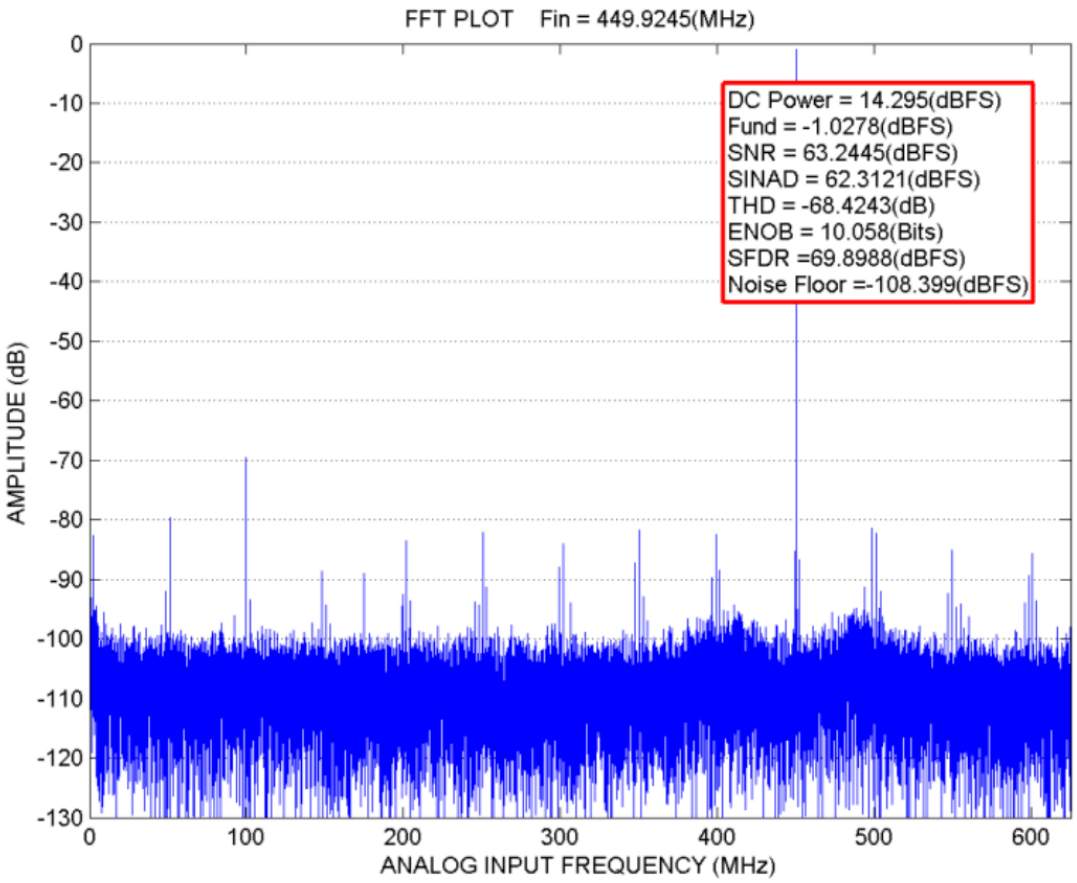


Figure 8: FFT spectrum, fCLK=1250MHz, fin=450MHz, TA=25°C

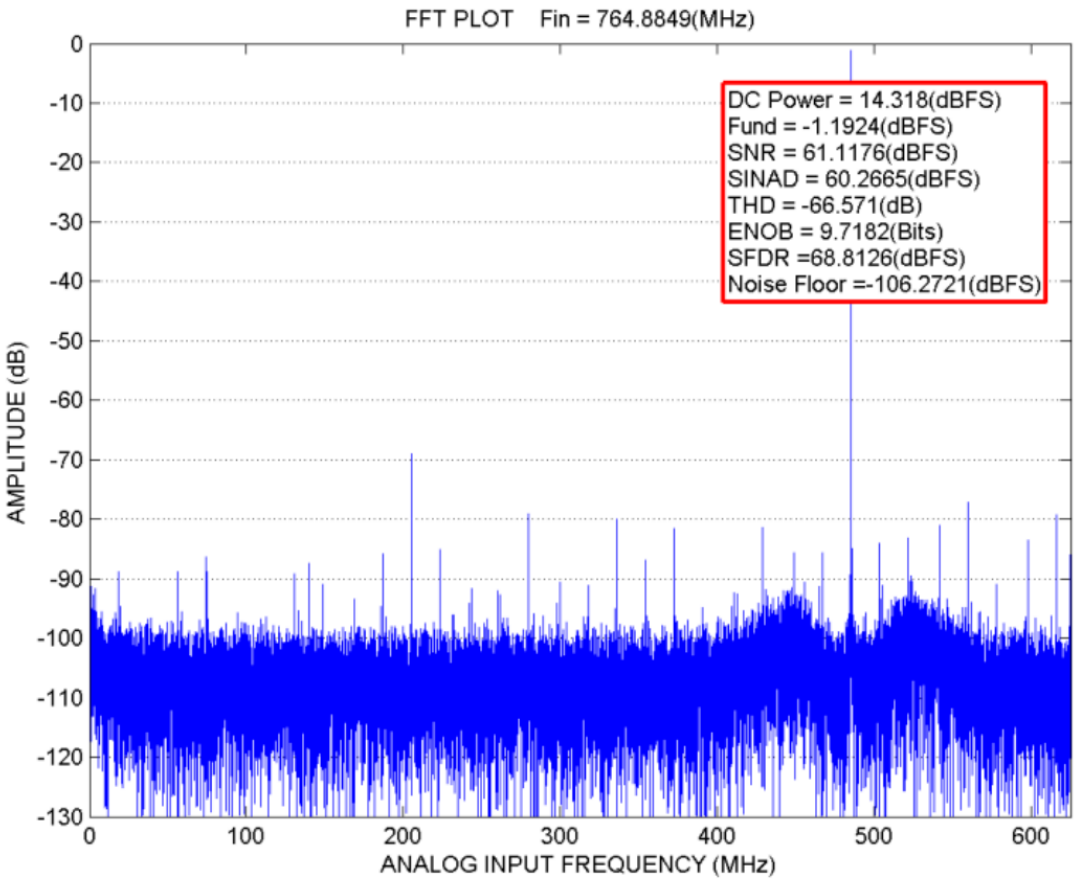


Figure 9: FFT spectrum, fCLK=1250MHz, fin=765MHz, TA=25°C

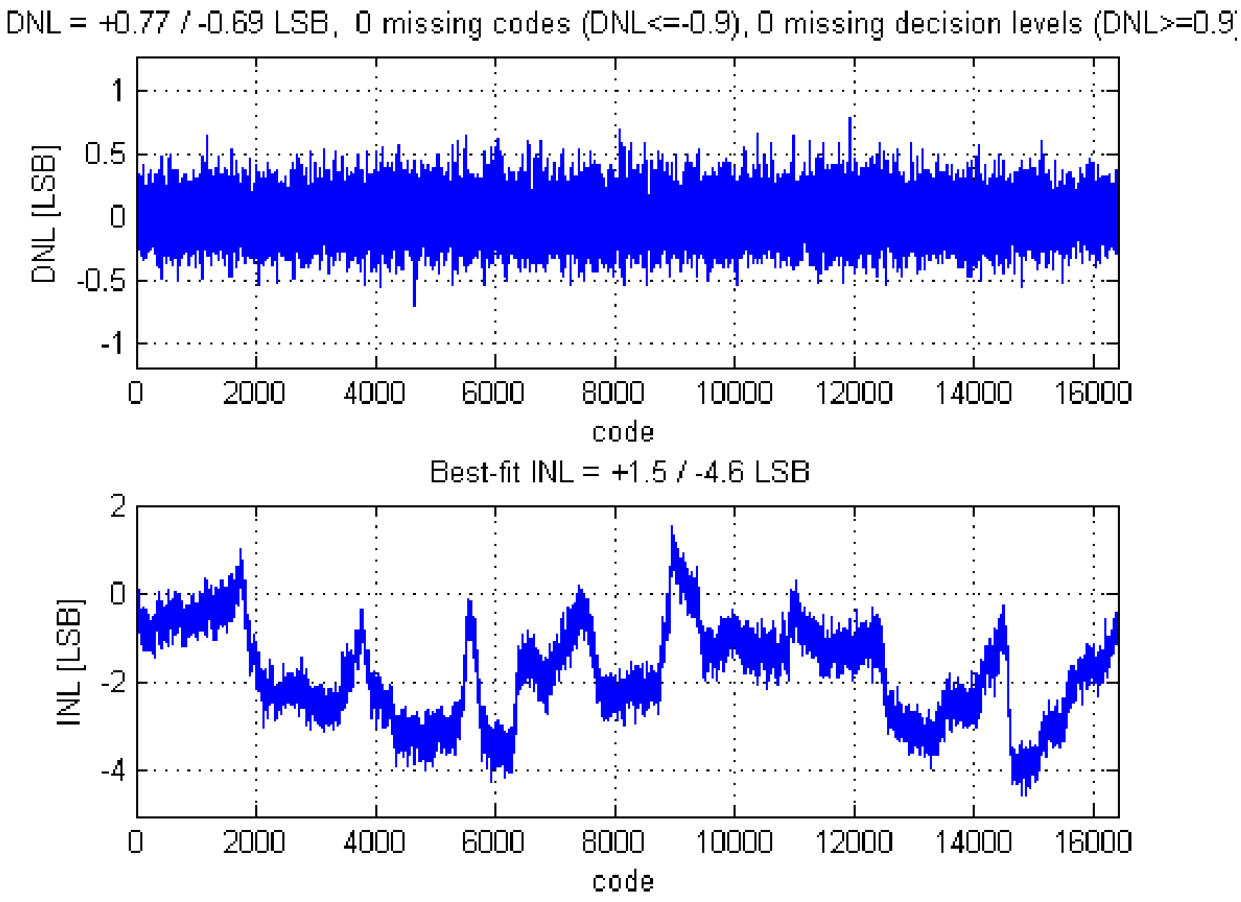


Figure 10: Differential error (EDL) and linearity error (EL) test curves

12. 典型应用线路图 / Typical Application Circuit

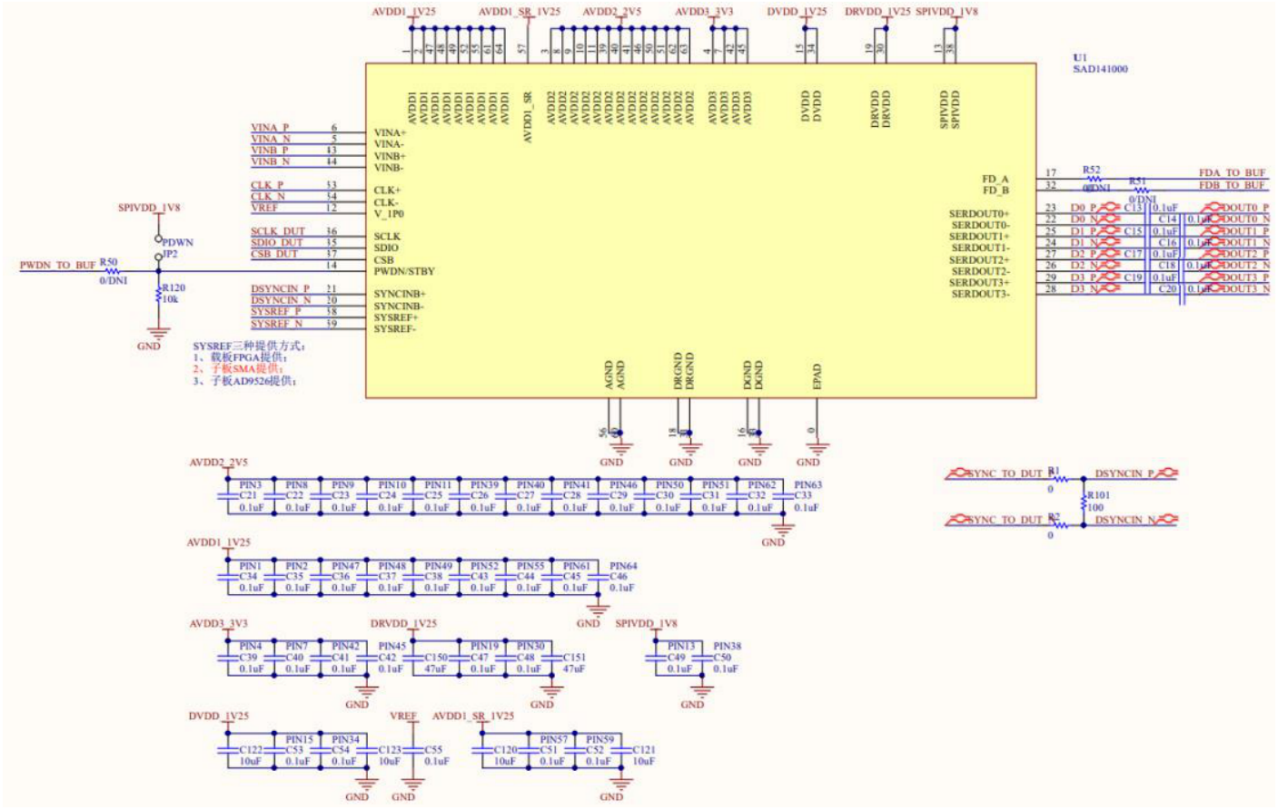


Figure 11: SXA032 peripheral circuit

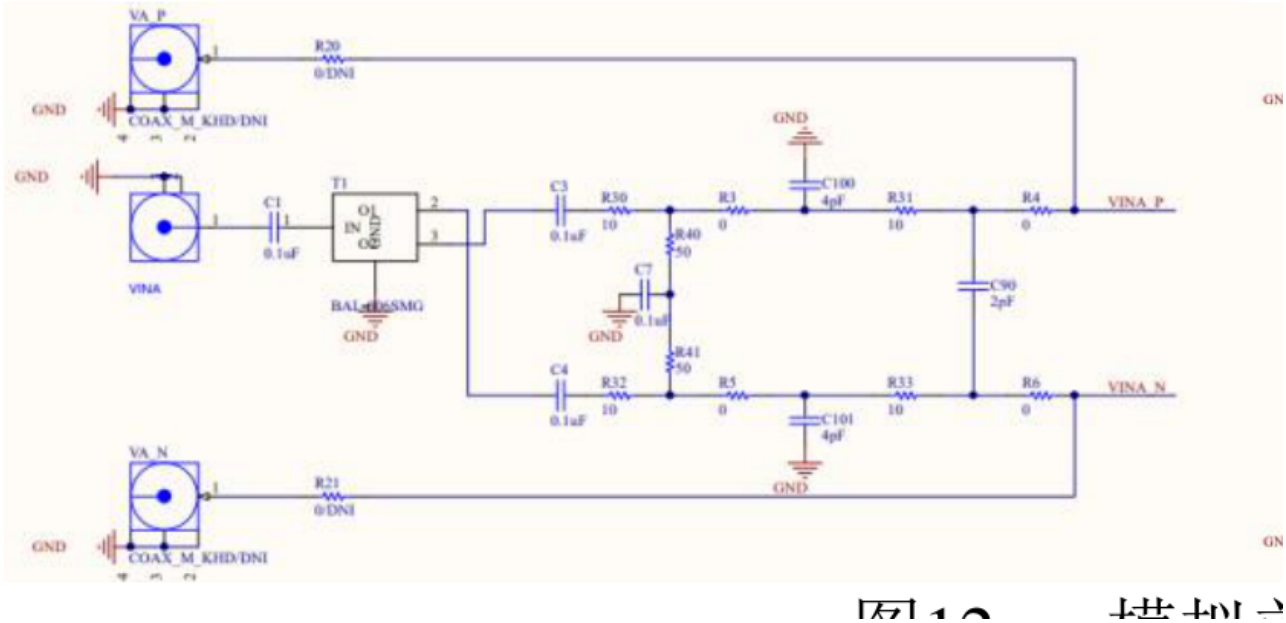


Figure 12: Analog front-end circuit

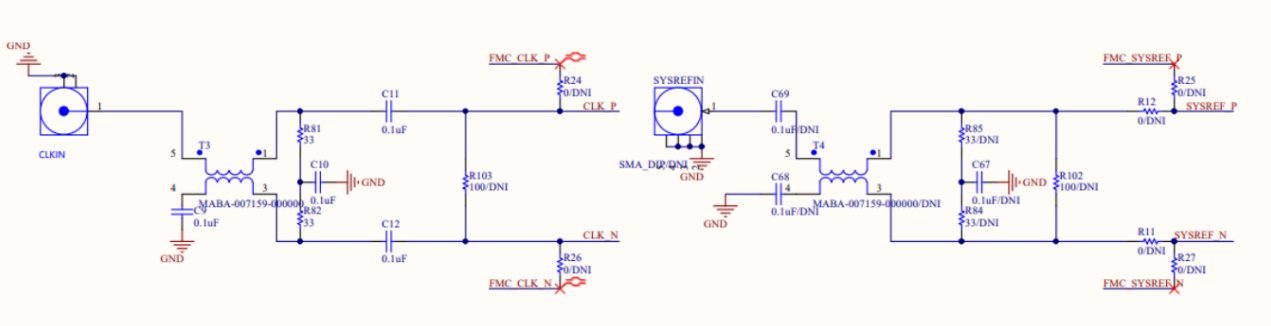


Figure 13: Clock front-end circuit

Power supply for the ADC: no power sequencing requirement; power up all supplies together. For supply filtering, refer to the figure above; each supply group requires filter capacitors. AD 供电：无供电时序要求，统一上电即可，电源滤波可参考上图，每组电源均需加滤波电容进行滤波；

ADC operating principle and modes: mainly includes the clock input serving as the ADC sampling clock; the analog signal at the analog input is AD-converted and transmitted via the 204B interface to the receiving end for digital processing, where accurate data is decoded and analyzed. ADC operating modes can be selected per the register configuration table. AD 工作原理和工作模式：主要包含时钟输入，作为ADC的采样时钟，模拟输入端的模拟信号进行AD转换，通过204B接口传输至接收端进行数字处理，解析出准确数据进行分析，AD 的工作模式可参考寄存器配置表进行选择。

13. 单元模块及工作原理 / Functional Blocks and Theory of Operation

1、模拟输入 / 13.1 Analog Input

13.1.1 Input Architecture / 1.1 输入架构

English: The SXA032 consists of a dual-channel pipelined ADC. The input buffer is designed to provide termination impedance for the analog input signal. The termination impedance can be changed via SPI to meet driver/amplifier termination requirements. The default termination is 400 Ω. The equivalent circuit of the analog input termination is shown in Figure 14. The input buffer is optimized for high linearity, low noise and low power. It provides a linear high input impedance and reduces kickback to the ADC. The buffer is optimized for high linearity, low noise and low power. The quantized outputs of each stage are combined in the digital correction logic to finally form a 14-bit conversion result. The pipelined architecture allows the first stage to process a new input sample while the other stages continue processing previous samples.

SXA032 由双通道流水线ADC组成，输入缓冲器设计用于向模拟输入信号提供端接阻抗。该端接阻抗可通过SPI改变，以满足驱动器/放大器的端接需求。默认端接值设置为400Ω。模拟输入端接的等效电路图如图14所示。输入缓冲器针对高线性度、低噪声和低功耗而优化。输入缓冲器提供线性高输入阻抗，并降低ADC的反冲。该缓冲器针对高线性度、低噪声和低功耗而优化。各级的量化输出组合在一起，在数字校正逻辑中最终形成一个14位转换结果。流水线架构允许第一级处理新的输入样本；与此同时，其它级继续处理之前的样本。

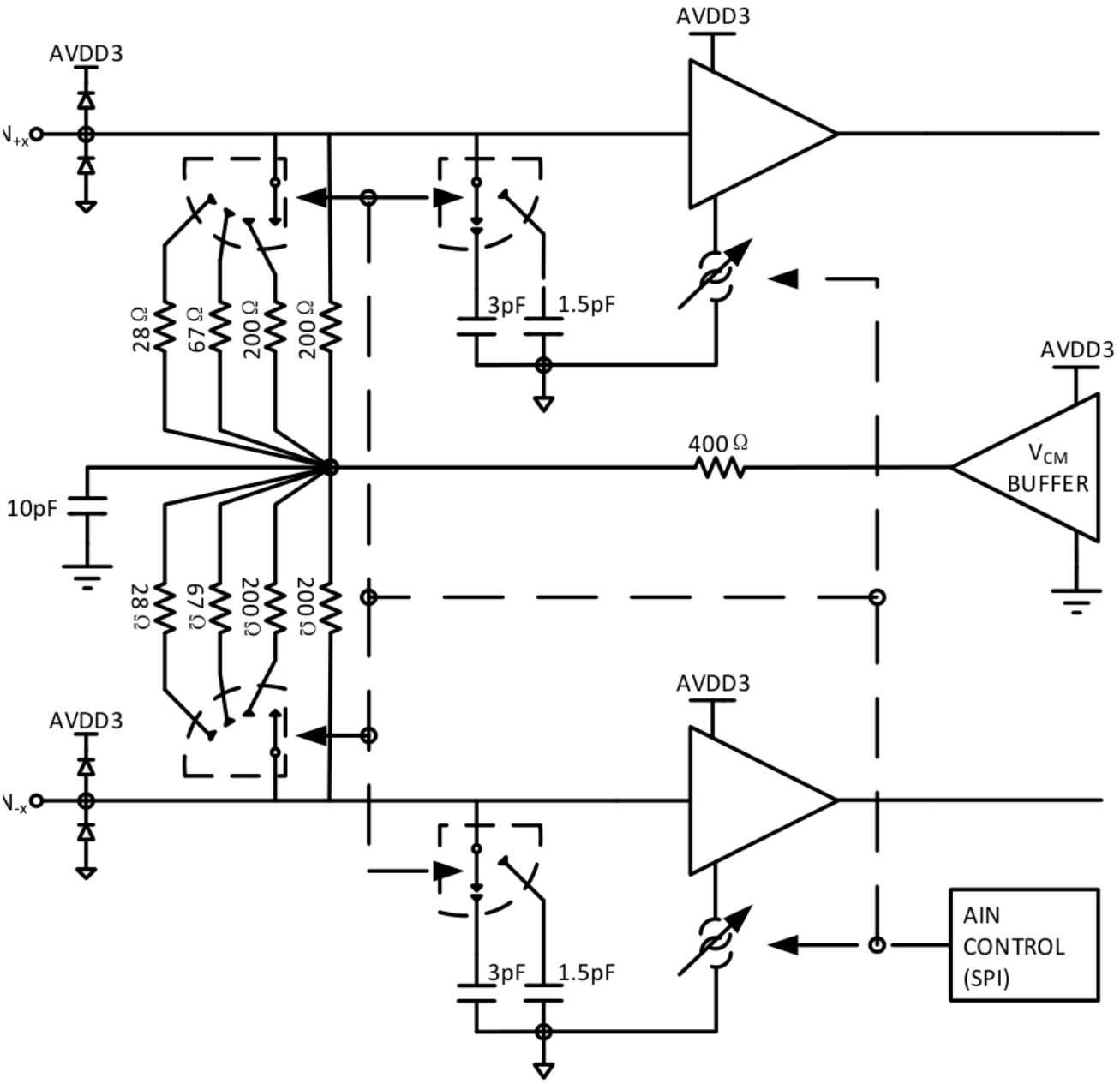


Figure 14: Analog input equivalent circuit

13.1.2 Input Amplitude / 1.2 输入幅度

English: The analog inputs of the SXA032 are differential buffers. The internal common-mode voltage of the buffer is 2.05 V. The input circuit switches between sample mode and hold mode according to the clock signal. When the input circuit switches to sample mode, the signal source must be able to charge the sampling capacitor and complete settling within half a clock period. A small resistor is placed in series with each input to help reduce peak transient current injected from the driver source output stage. For best dynamic performance, the source impedance driving VIN+x must match the source impedance driving VIN−x so that common-mode settling errors are symmetric. These errors are attenuated by the ADC's common-mode rejection. The internal reference voltage buffer forms a differential reference voltage, which in turn determines the ADC core range. In differential configuration, setting the ADC to maximum range achieves the highest SNR performance. For the SXA032, the available range is

programmable via the SPI port from 1.46 Vp-p to 1.94 Vp-p differential, with a default of 1.70 Vp-p differential.

SXA032 的模拟输入端为差分缓冲器。缓冲器的内部共模电压为2.05V。输入电路根据时钟信号在采样模式和保持模式之间切换。当输入电路切换到采样模式时，信号源必须能够对采样电容充电，并且在半个时钟周期内完成建立。每个输入端都串联一个小电阻，帮助降低从驱动源输出级注入的峰值瞬态电流。为得到最佳动态性能，必须保证驱动VIN+x的源阻抗与驱动VIN−x的源阻抗相匹配，从而保证共模建立误差是对称的。这些误差会被ADC的共模抑制削弱。内部基准电压缓冲器形成差分基准电压，进而决定ADC内核的范围。在差分配置中，将ADC 设置为最大范围可以实现最高的SNR性能。对于SXA032，可用范围可通过SPI端口在1.46Vp-p 到1.94Vp-p差分之间编程，默认值为1.70Vp-p差分。

13.1.3 Differential Input Configuration / 1.3 差分输入配置

English: There are various active or passive methods to drive the SXA032; however, driving the analog inputs differentially achieves the best performance. In applications where SNR and SFDR are critical parameters, differential transformer coupling is recommended in the input configuration (Figure 15), because the noise performance of most amplifiers is insufficient to realize the true performance of the SXA032. For higher frequencies in the second or third Nyquist zone, it is best to remove some front-end passive components (see Table 4) to ensure wideband operation.

有多种有源或无源方法可以驱动SXA032，不过，通过差分方式驱动模拟输入可实现最佳性能。在SNR和SFDR为关键参数的应用中，因为大部分放大器的噪声性能不足以实现SXA032 的真正性能，所以输入配置中建议采用差分变压器耦合(图15)。对于第二或第三奈奎斯特区中的较高频率，最好移除一些前端无源元件(见表4)，确保其以宽带工作。

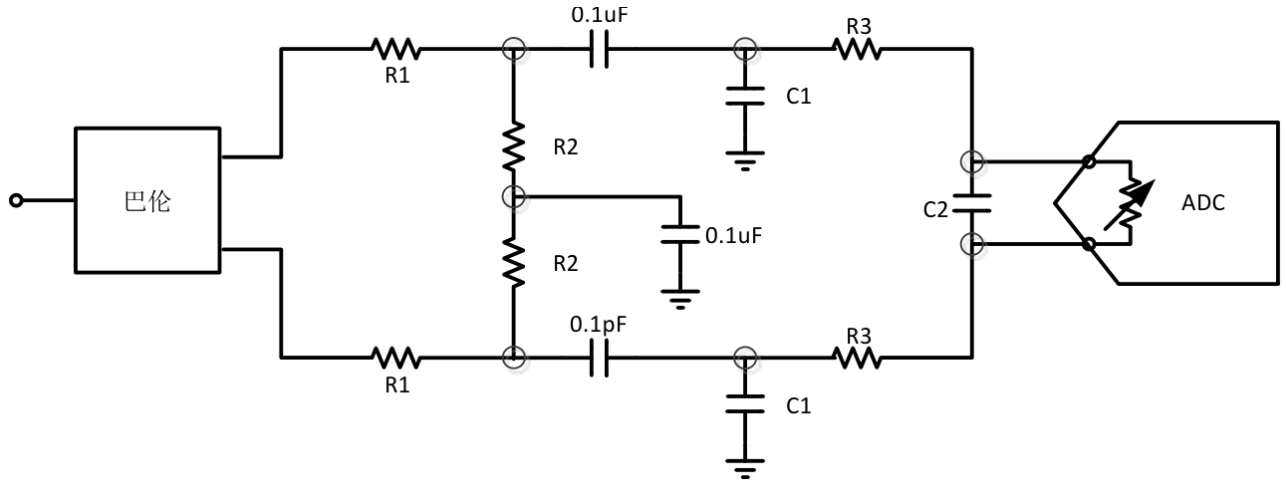


Figure 15: Differential transformer-coupled configuration

表4 前端无源元件配置 / Table 4 — Front-End Passive Component Configuration

Sample Rate / 采样率	Input Frequency Range / 输入频率范围	Transformer / 变压器	R1 (Ω)	R2 (Ω)	R3 (Ω)	C1 (pF)	C2 (pF)
1000 MSPS	DC to 500 MHz	ETC1-1-13/ BAL-0006SM	25	25	10	4	2
1000 MSPS	500 MHz to 2 GHz	BAL-0006/BAL-0006SM	25	25	0	Open	Open

13.1.4 Input Common Mode / 1.4 输入共模

English: The analog inputs of the SXA032 are internally biased to the common mode. The range of the common-mode buffer is very limited, because performance degrades significantly if the common-mode voltage drops by more than 100 mV. Therefore, in DC-coupled applications, the common-mode voltage should be set to 2.05 V ± 100 mV to ensure normal ADC operation. When operating in DC-coupled applications, the full-scale voltage setting must be 1.7 V p-p differential.

SXA032 的模拟输入内部偏置到共模。共模缓冲器的范围很有限，因为如果共模电压降低 100 mV以上，性能会大大降低。所以，在直流耦合应用中，应将共模电压设置为2.05 V±100 mV，确保ADC正常工作。若在直流耦合应用中运行，满量程电压设置必须是1.7 V p-p差分。

13.1.5 Analog Input Control and SFDR Optimization / 1.5 模拟输入控制和SFDR优化

The SXA032 provides flexible analog input control, such as input termination, buffer current and input full-scale adjustment. Register 0x018 can be used to adjust the buffer current of each channel to optimize SFDR for different input frequencies and target bandwidths. After setting the input buffer current, the current required from the AVDD3 supply changes. In some high-frequency applications, reducing the full-scale setting improves SFDR. Table 5 gives the recommended buffer current and full-scale voltage settings for different analog input frequency ranges.

SXA032 提供灵活的模拟输入控制，如输入端接、缓冲电流和输入满量程调整等。利用寄存器0x018可以调整各通道的缓冲电流，以便针对不同输入频率和目标带宽来优化SFDR。设定输入缓冲电流后，AVDD3电源需要的电流量会改,在某些高频应用中，降低满量程设置可改善 SFDR。表5给出了不同模拟输入频率范围的推荐缓冲电流和满量程电压设置。

表5 缓冲电流和满量程电压设置 / Table 5 — Buffer Current and Full-Scale Voltage Settings

| Model / 型号 | Frequency Range / 频率区间 | 0x018 | 0x019 | 0x01a | 0x11a | 0x935 | 0x025 | 0x030 | 0x016 | 0x934 | |---|---|---|---|---|---|---|---|---|---|---| | SXA032_500 | DC~250M | 0x20 (2.0X) | 0x60 | 0x0A | 0x00 | 0x04 | 0x04 (2.06V) | 0x0C | 0x0C/0x1C.. | 0x1F | | | 250M~500M | 0x70 (4.5X) | 0x60 | 0x0A | 0x00 | 0x04 | 0x04 (2.06V) | 0x0C | 0x0C/0x1C.. | 0x1F | | | 500M~1G | 0x80 (5.0X) | 0x40 | 0x08 | 0x00 | 0x00 | 0x18 (1.46V) | 0x08 | 0x0C/0x1C.. | 0x1F 或 0x00 | | | 1G~2G | 0xF0 (8.5X) | 0x40 | 0x08 | 0x00 | 0x00 | 0x18 (1.46V) | 0x08 | 0x0C/0x1C.. | 0x1F 或 0x00 | | SXA032_1000 | DC~150M | 0x10 (1.5X) | 0x50 | 0x09 | 0x00 | 0x04 | 0x18 (1.70V) | 0x0A | 0x0E/0x1E.. | 0x1F | | | DC~500M | 0x40 (3X) | 0x50 | 0x09 | 0x00 | 0x04 | 0x18 (1.70V) | 0x0A | 0x0E/0x1E.. | 0x1F | | | 500M~1G | 0xA0 (6X) | 0x60 | 0x09 | 0x20 | 0x00 | 0x18 (1.46V) | 0x08 | 0x0E/0x1E.. | 0x1F 或 0x00 | | | 1G~2G | 0xD0 (7.5X) | 0x70 | 0x09 | 0x20 | 0x00 | 0x18 (1.46V) | 0x08 | 0x0E/0x1E.. | 0x1F 或 0x00 | | SXA032_1250 | DC~625M | 0x50 (3.5X) | 0x50 | 0x09 | 0x00 | 0x04 | 0x18 (1.70V) | 0x0A | 0x0E/0x1E.. | 0x1F | | | 625M~2G | 0xA0 (6.0X) | 0x50 | 0x09 | — | 0x00 | 0x18 (1.46V) | 0x08 | 0x0E/0x1E.. | 0x1F 或 0x00 |

Note: Table 5 cell alignment follows the source PDF extraction; multi-line cells are reproduced as faithfully as possible. / 注：表5 单元格对齐按源 PDF 提取结果整理，多行单元格已尽量忠实还原。

2、基准电压源 / 13.2 Voltage Reference

English: The SXA032 integrates a stable, accurate 1.0 V voltage reference. This internal 1.0 V reference sets the full-scale input range of the ADC. The full-scale input range is adjustable via ADC function register 0x025. Figure 16 shows the control block diagram of the internal 1.0 V reference.

SXA032 内置稳定、精确的1.0 V基准电压源。该内部1.0 V基准电压源用于设置ADC的满量程输入范围。满量程输入范围可通过ADC功能寄存器0x025进行调整。图16显示了内部1.0 V基准电压源的控制框图。

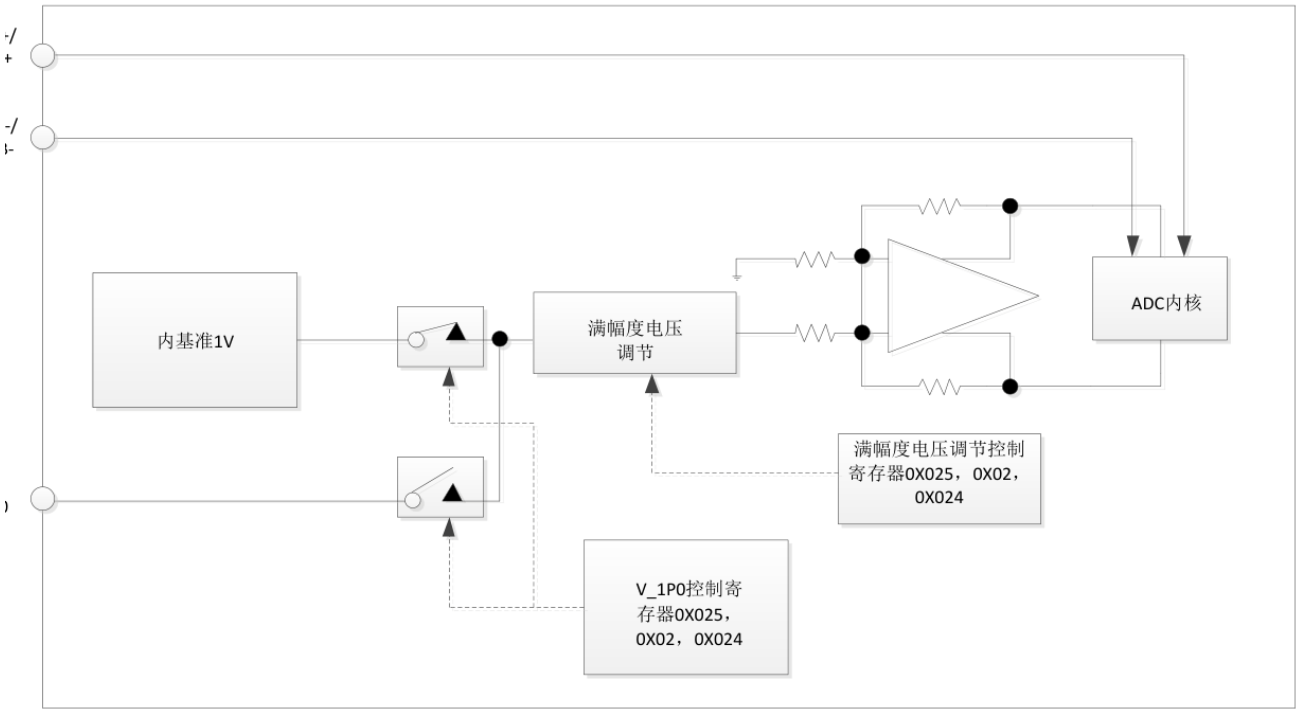


Figure 16: Reference configuration and control

English: Via SPI register 0x024, the user can select the internal 1.0 V reference or provide an external 1.0 V reference. When using an external reference, a 1.0 V reference should be provided. Full-scale adjustment is performed via SPI and is independent of the reference voltage.

通过SPI寄存器0x024，用户可以选择使用该内部1.0 V基准电压源或提供外部1.0 V基准电压源。使用外部基准电压源时，应提供1.0 V基准电压源。满量程调整利用SPI进行，与基准电压无关。

English: The external reference must be a stable 1.0 V source. Figure 17 shows how to provide an external 1.0 V reference to the SXA032. The gray area shows the part of the SXA032 that is unused because the external reference is used instead of the internal reference.

外部基准电压源必须是稳定的1.0 V基准源。图17显示如何为SXA032提供外部1.0 V基准电压。灰色区域显示SXA032中因为利用外部基准电压源而不使用内部基准。

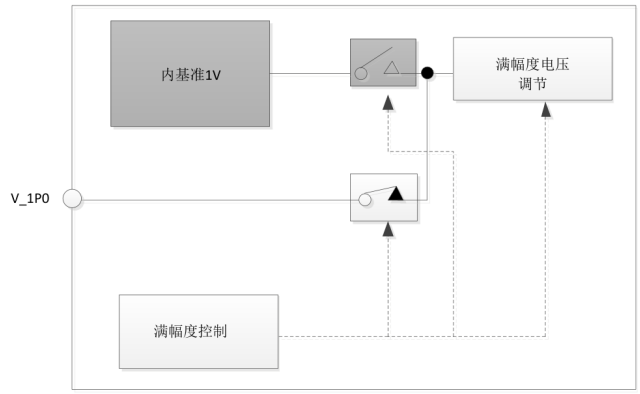


Figure 17: Using an external reference

3、时钟 / 13.3 Clock

13.3.1 Clock Input Considerations / 3.1 时钟输入考虑

English: To fully exploit the chip's performance, a differential signal should be used as the SXA032 sampling clock input (CLK+ and CLK−). Typically, a transformer or clock driver is used to AC-couple the signal to the CLK+ and CLK− pins. The CLK+ and CLK− pins are internally biased and require no additional biasing. Figure 18 shows a preferred method of providing the clock signal to the SXA032, using an RF transformer to convert the single-ended signal of a low-jitter clock source into a differential signal.

为了充分发挥芯片的性能，应利用一个差分信号作为SXA032采样时钟输入端(CLK+和 CLK−)的时钟信号。通常，应使用变压器或时钟驱动器将该信号交流耦合到CLK+引脚和CLK− 引脚。CLK+和CLK−引脚有内部偏置，无需其它偏置。图18显示了一种为SXA032提供时钟信号的首选方法，利用射频变压器，可将低抖动时钟源的单端信号转换成差分信号。

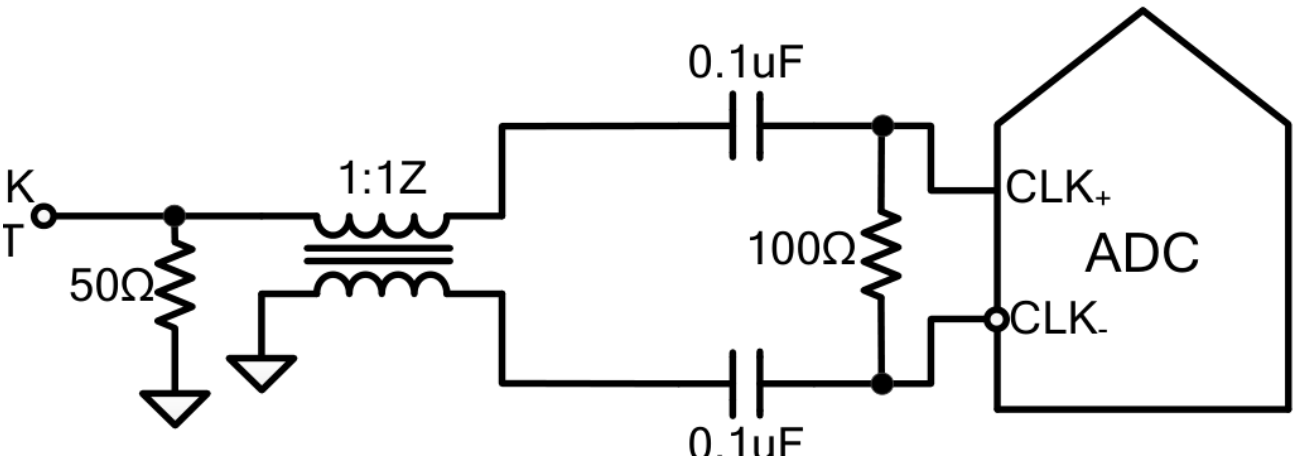


Figure 18: Transformer-coupled differential sampling clock

English: Another method is to AC-couple a differential CML or LVDS signal to the sampling clock input pins, as shown in Figure 19 and Figure 20.

另一种方法是将差分CML或LVDS信号交流耦合到采样时钟输入引脚，如图19图20所示。

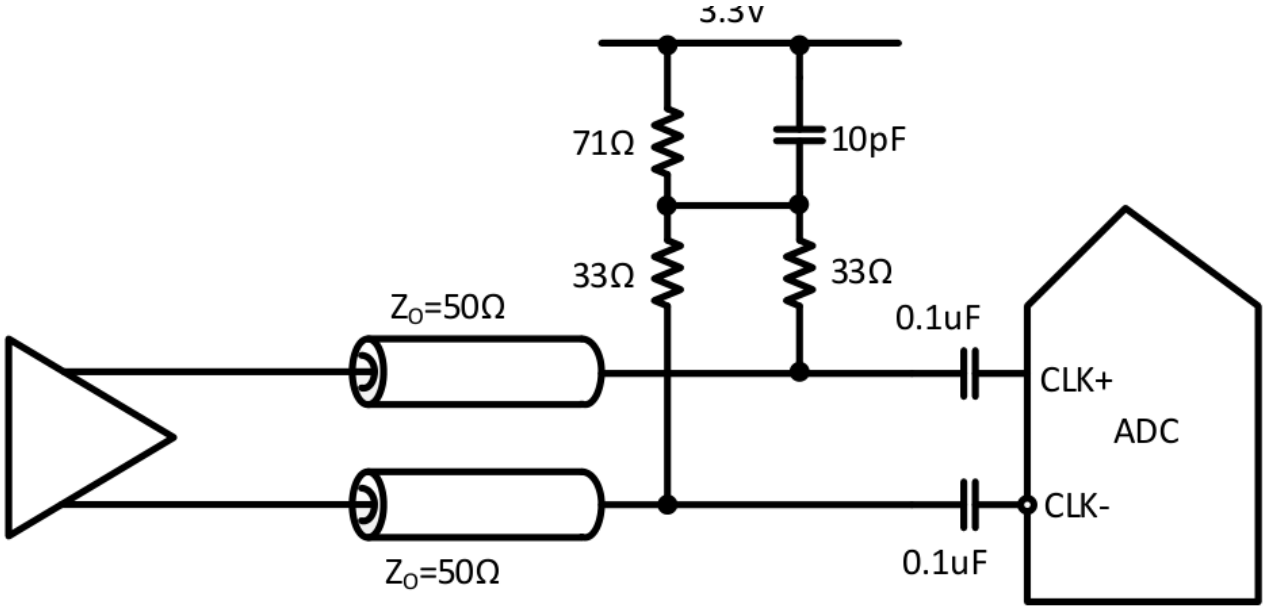


Figure 19: Differential CML sampling clock

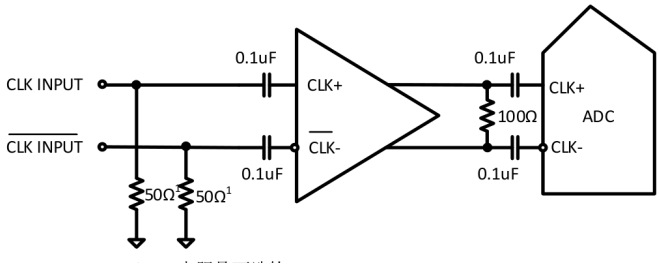


Figure 20: Differential LVDS sampling clock

13.3.2 Clock Duty Cycle Considerations / 3.2 时钟占空比考虑

English: Typical high-speed ADCs use both clock edges to generate different internal timing signals. These ADCs may therefore be sensitive to clock duty cycle. Generally, the clock duty-cycle tolerance should be 5% to maintain ADC dynamic performance. In applications where a 50% clock duty cycle cannot be guaranteed, a higher multiple-frequency clock can be provided to the device. With the internal clock divider set to 2, the SXA032 can use a 2 GHz clock. The divider output provides the internal ADC with a 50% duty-cycle, high-slew-rate clock signal.

典型的高速ADC利用两个时钟沿产生不同的内部定时信号。因此，这些ADC可能对时钟占空比很敏感。通常，为保持ADC的动态性能，时钟占空比容差应为5%。在无法保证50%时钟占空比的应用中，可以向器件提供更高的多频时钟。内部时钟分频器设为2时，SXA032可以采用 2 GHz时钟。分频器输出为内部ADC提供50%占空比、高压摆率时钟信号。

13.3.3 Input Clock Divider / 3.3 输入时钟分频器

English: The SXA032 integrates an input clock divider that can divide the Nyquist input clock by 1, 2, 4 or 8. The divide ratio is selected via register 0x10B, as shown in Figure 21. The maximum frequency of the CLK± input is 4 GHz, which is the divider limit. In applications where the clock input is a multiple of the

sampling clock, the clock divider ratio must be set carefully before applying the clock signal, to ensure current transients during device startup are controlled.

SXA032 内置一个输入时钟分频器，可对奈奎斯特输入时钟进行1、2、4和8倍分频。分频比可通过寄存器0x10B选择，如图21所示。CLK±输入的最大频率为4 GHz。这是分频器的限值。在时钟输入是采样时钟数倍的应用中，必须小心设置时钟分频器的分频比，然后施加时钟信号，确保器件启动期间的电流瞬态受控。

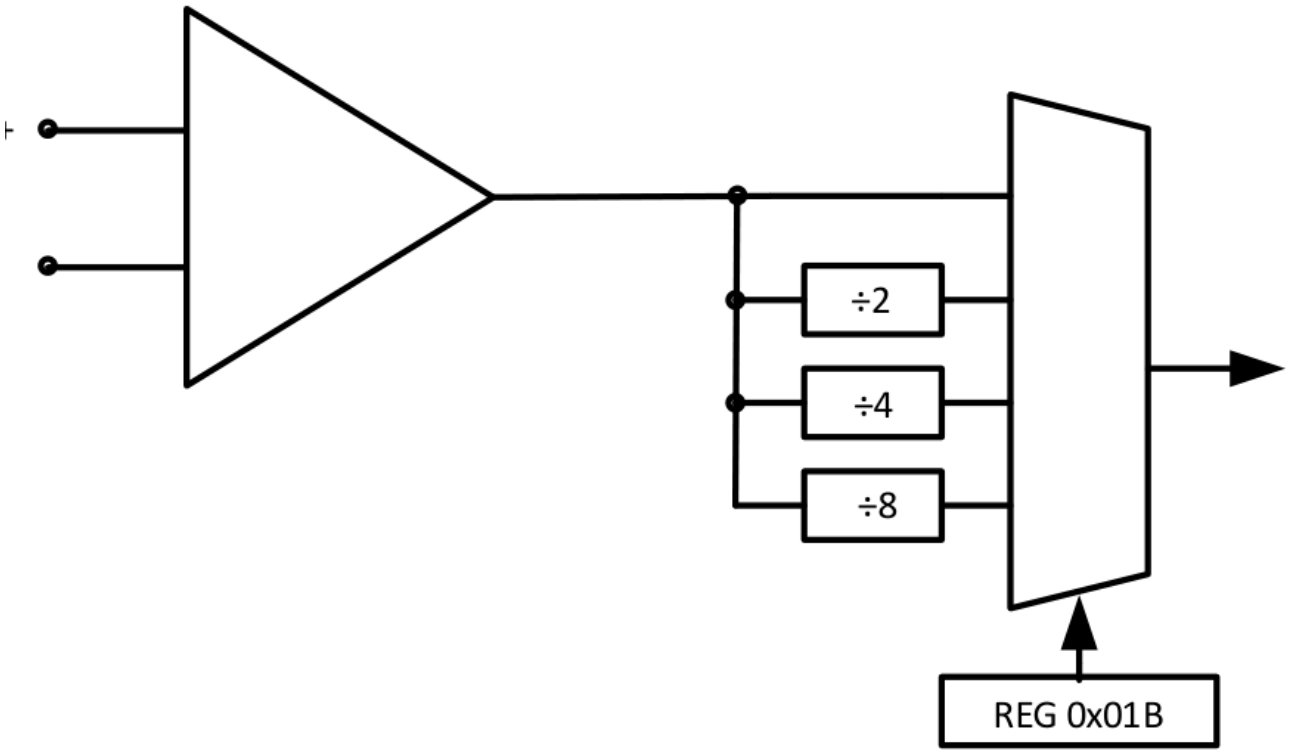


Figure 21: Clock divider circuit

English: The SXA032 clock divider can be synchronized using the external SYSREF± input signal. A valid SYSREF± resets the clock divider to a programmable state. This synchronization feature aligns the clock dividers of multiple devices, ensuring simultaneous input sampling. The recommended input clock frequency is 0.3 – 4 GHz with an amplitude of 0.6 – 1.8 Vpp.

利用外部SYSREF±输入信号可同步SXA032时钟分频器。有效SYSREF±可使时钟分频器复位至可编程状态。该同步特性可让多个器件的时钟分频器对准，从而保证同时进行输入采样。推荐输入时钟频率为0.3~4GHz，幅度0.6~1.8Vpp。

13.3.4 Clock Jitter Considerations / 3.4 时钟抖动考虑

English: High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. At a given input frequency (fA), the SNR degradation caused solely by aperture jitter (tJ) is calculated as follows:

高速、高分辨率ADC对时钟输入信号的质量非常敏感。在给定的输入频率(fA)下，仅由孔径抖动(tJ)造成的信噪比(SNR)下降计算公式如下：

English: $SNR = 20 \times \log10(2 \times \pi \times fA \times tJ)$

English: where the rms aperture jitter represents the rms of all jitter sources (including the clock input signal, analog input signal and ADC aperture jitter specification). IF undersampling applications are especially sensitive to jitter.

公式中，均方根孔径抖动表示所有抖动源(包括时钟输入信号、模拟输入信号和ADC孔径抖动规格)的均方根。中频欠采样应用对抖动尤其敏感。

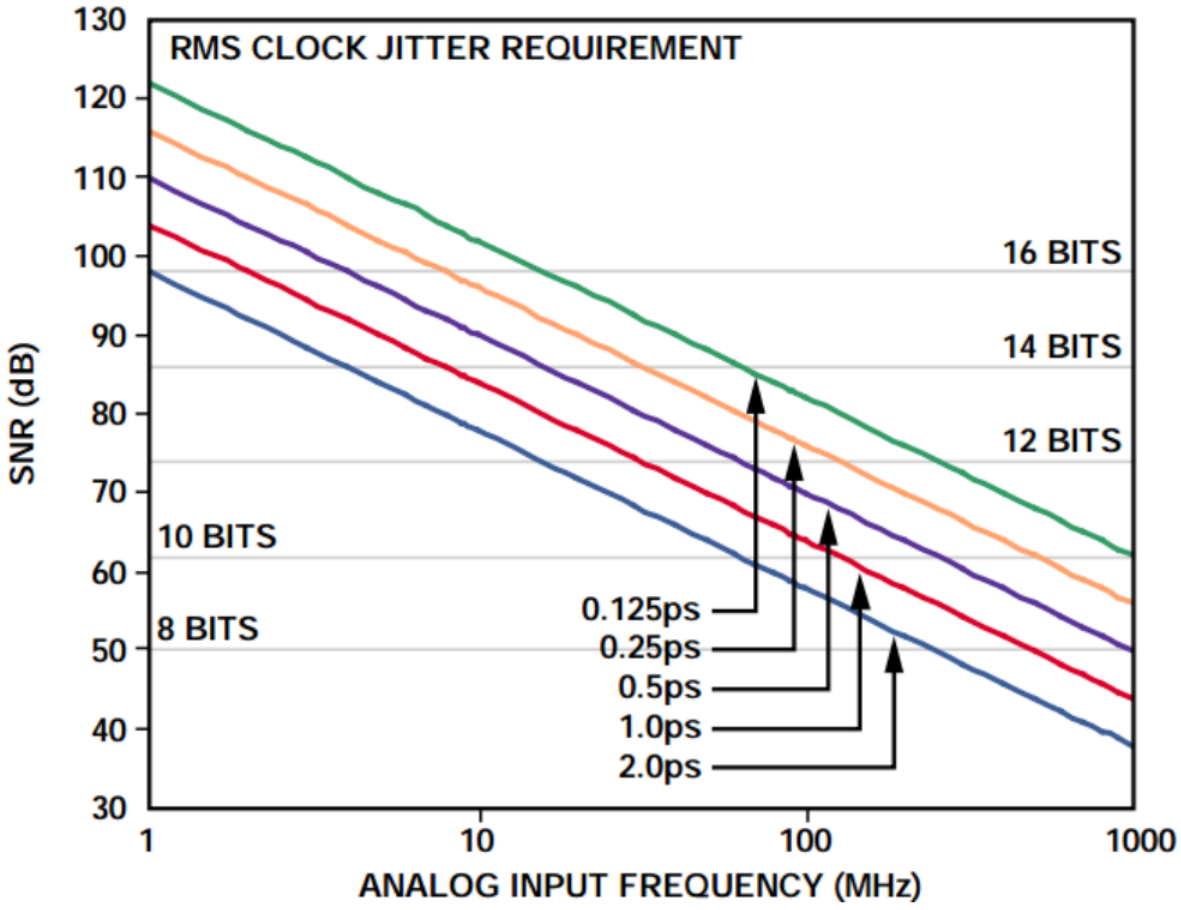


Figure 22: Ideal SNR vs. input frequency and jitter

English: When aperture jitter may affect the dynamic range of the SXA032, the clock input signal should be treated as an analog signal. Separate the clock driver supply from the ADC output driver supply to avoid mixing digital noise into the clock signal. If the clock signal comes from another type of clock source (via gating, division or other methods), the original clock should be used for retiming in the final step.

当孔径抖动可能影响SXA032的动态范围时，应将时钟输入信号视为模拟信号。将时钟驱动器电源与ADC输出驱动器电源分离，以免在时钟信号内混入数字噪声。如果时钟信号来自其它类型的时钟源(通过门控、分频或其他方法)，则需要在最后一步中利用原始时钟进行重定时。

4、掉电/待机模式 / 13.4 Power-Down/Standby Mode

English: The SXA032 has a PDWN/STBY pin that can be used to configure the device in power-down or standby mode. The default configuration is PDWN. The PDWN/STBY pin is a logic-high pin. In power-down mode, the JESD204B link is interrupted. The power-down option can also be set via register 0x03F and

register 0x040. In standby mode, the JESD204B link is not interrupted and 0 is transmitted for all converter samples. Register 0x571 bit 7 can be used to select /K/ characters for modification.

SXA032 有一个PDWN/STBY引脚，可用来将器件配置为掉电或待机模式。默认配置是 PDWN。PDWN/STBY引脚是一个逻辑高电平引脚。在掉电模式下，JESD204B链路中断。掉电选项也可通过寄存器0x03F和寄存器0x040设置。在待机模式下，JESD204B链路不中断，对所有转换器样本都传输0。这可以利用寄存器0x571的位7选择/K/字符来改变。

5、温度二极管 / 13.5 Temperature Diode

English: The SXA032 integrates a diode-based temperature sensor for measuring chip temperature. This diode outputs a voltage that serves as an ordinary temperature sensor to monitor the internal chip temperature. Via SPI, the temperature diode voltage can be output to the FD_A pin. The diode can be enabled or disabled via bit 0 of register 0x028. Register 0x028 is a local register. To enable temperature diode readout output, channel A in the device index register (0x008) must be selected. By setting register 0x040[2:0], the FD_A pin is configured to output the diode voltage. The voltage response curve of the temperature diode is shown in Figure 23.

SXA032 内置一个基于二极管的温度传感器，用于测量芯片温度。此二极管可输出一个电压，充当普通温度传感器来监控内部芯片温度。利用SPI，温度二极管电压可输出到FD_A引脚。通过寄存器0x028的位0可使能或禁用该二极管。寄存器0x028是一个本地寄存器。要使能温度二极管读数输出，必须选择器件索引寄存器(0x008)中的通道A。通过设置寄存器0x040[2:0]，配置FD_A引脚输出二极管电压。温度二极管的电压响应曲线如图23所示。

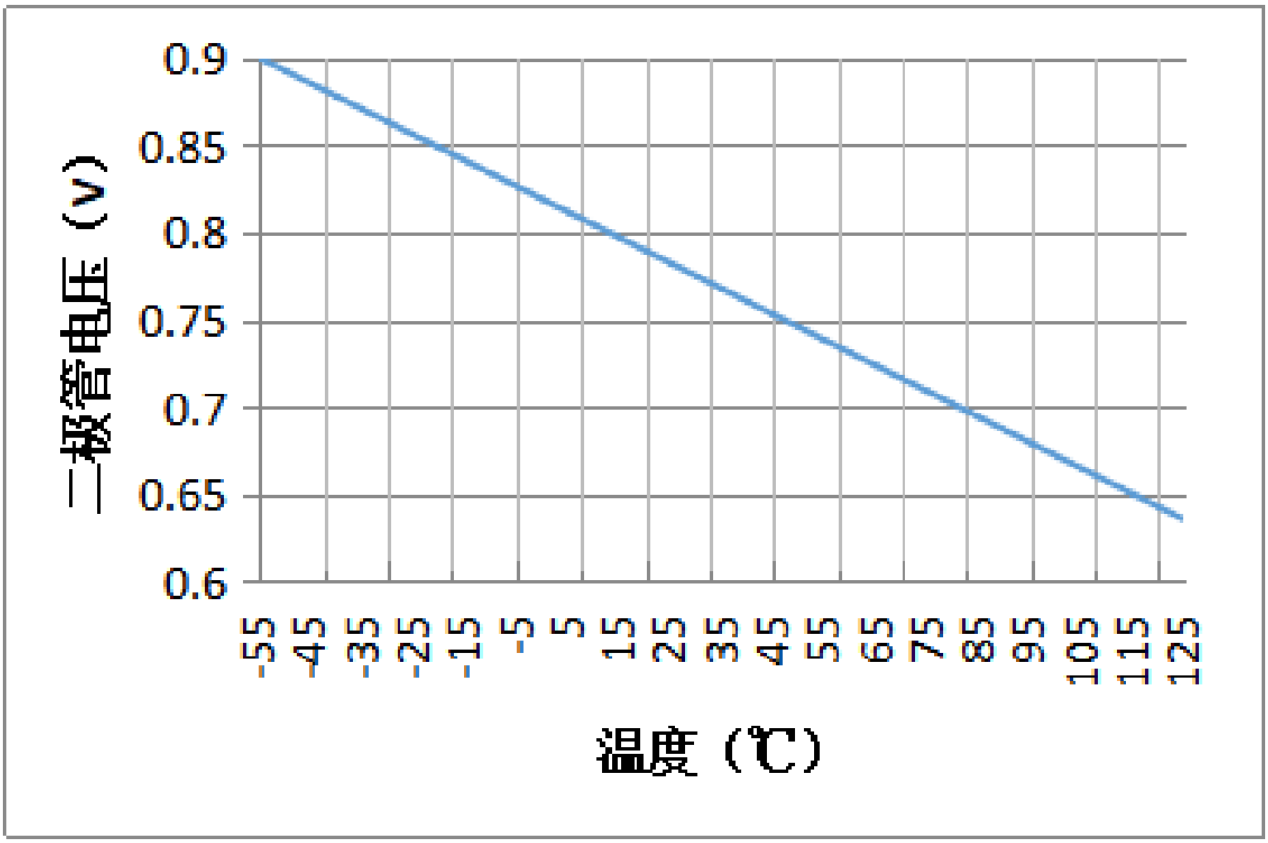


Figure 23: Temperature diode voltage vs. temperature Tj

6、温度二极管 ADC 超量程与快速检测 / 13.6 Temperature Diode ADC Overrange and Fast Detect

English: In receiver applications, a reliable mechanism is needed to determine when the converter clamps. The standard overrange bit in the JESD204B output provides limited information about the analog input state. It is therefore preferable to set a programmable threshold below full scale so that gain can be reduced before clamping occurs. In addition, because the slew rate of the input signal can be very high, the latency of this function is critical. However, high-speed high-precision pipelined converters have very large latency. The SXA032 integrates detection circuits that each channel can use to monitor thresholds and set the FD_A and FD_B pins.

在接收机应用中，需要一种可靠的机制，能够决定转换器何时发生箝位。JESD204B输出中的标准超量程位提供的模拟输入状态信息作用有限。因此，最好可以设定低于满量程的可编程阈值，以便在箝位发生前降低增益。另外，由于输入信号的压摆率可能非常高，因此该功能的延迟时间非常关键。然而，高速高精度流水线转换器有非常大的延迟。SXA032内置检测电路，可供各通道用来监控阈值并置位FD_A和FD_B引脚。

13.6.1 ADC Overrange / 6.1 ADC超量程

English: When overrange is detected at the ADC input, the ADC overrange indicator is set. The overrange indicator can be embedded in the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator is consistent with the sample latency. The SXA032 can also record the overrange condition of any of the 8 virtual converters. The overrange status of each virtual converter is recorded as a flag bit in register 0x563. The contents of register 0x563 can be cleared using register 0x562 by toggling the bit corresponding to the virtual converter to the set and reset positions.

ADC 输入端检测到超量程时，ADC超量程指示器将置位。超量程指示器可以作为一个控制位嵌入JESD204B链路中(CSB>0时)。该超量程指示器的延迟与样本延迟一致。SXA032还能记录8个虚拟转换器中任一个的超量程状况。各虚拟转换器的超量程状态记录为寄存器0x563中的一个标记位。寄存器0x563的内容可利用寄存器0x562清除，方法是将虚拟转换器对应的位切换到设置和复位位置。

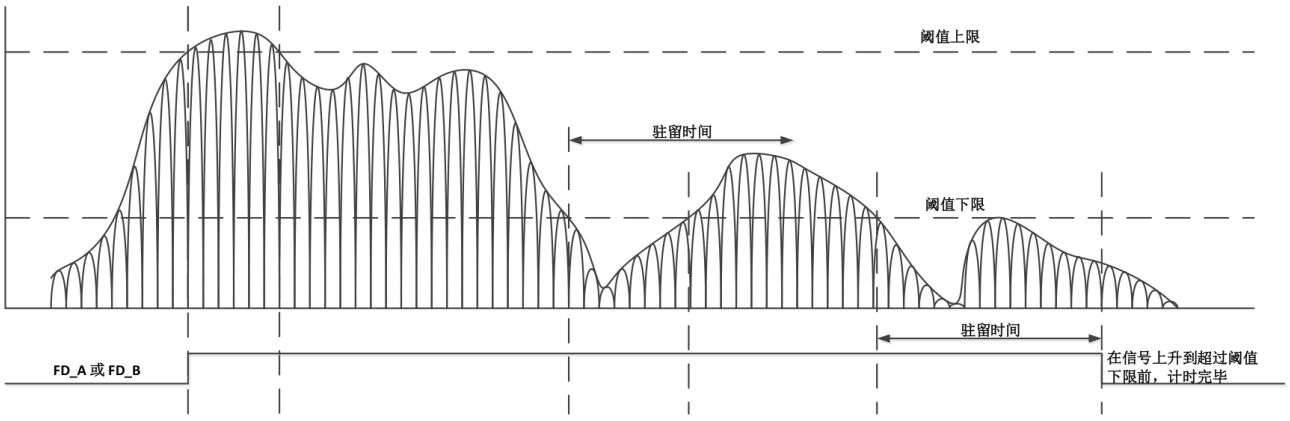


Figure 24: FD_A and FD_B threshold settings

13.6.2 Fast Threshold Detect (FD_A and FD_B) / 6.2 快速阈值检测(FD_A和FD_B)

English: The FD bit is set to 1 immediately whenever the absolute value of the input signal exceeds the programmable upper threshold. The FD bit is cleared to 0 only when the absolute value of the input signal

falls below the lower threshold and remains there longer than the programmable dwell time. This feature provides hysteresis to prevent the FD bit from toggling too frequently.

中文： 只要输入信号的绝对值超过可编程阈值上限，FD位就会立即置1。只有当输入信号的绝对值降至阈值下限以下并且持续时间超过可编程驻留时间时，FD位才会清0。该特性提供迟滞，防止FD位过于频繁地切换。

English: The upper/lower threshold registers and dwell-time register operate as shown in Figure 24. When the input signal amplitude exceeds the fast-detect upper-threshold register setting (registers 0x247 and 0x248), the FD indicator is set. The selected threshold register value is compared against the signal amplitude of the ADC output. Fast upper-threshold detection has a latency of 28 clock cycles (maximum). The approximate upper-threshold amplitude is defined by:

阈值上限和下限寄存器工作以及驻留时间寄存器的情况如图24所示。当输入信号幅度超过快速检测阈值上限寄存器(寄存器0x247和0x248)的设置值时，FD指示器置位。选定阈值寄存器的值与ADC输出的信号幅度进行比较。快速阈值上限检测具有28个时钟周期的延迟(最大值)。近似阈值上限幅度由下式定义：

Upper threshold amplitude (dBFS) = 20 log(threshold amplitude / 2^{13}) 阈值上限幅度 (dBFS) = 20 log (阈值幅度/2^{13})

English: The FD indicator is not cleared until the signal falls below the lower threshold and the dwell time has elapsed. The lower threshold is set in the fast-detect lower-threshold registers (registers 0x249 and 0x24A). The 13-bit fast-detect lower-threshold register value is compared against the signal amplitude of the ADC output. This comparison is governed by the ADC pipeline latency; comparison accuracy depends on converter resolution. The lower-threshold amplitude is defined by:

在信号降至阈值下限以下且保持时间超过设定的驻留时间之前，FD指示器不会清零。阈值下限在快速检测阈值下限寄存器(寄存器0x249和0x24A)中进行设置。13位快速检测阈值下限寄存器的值与ADC输出的信号幅度进行比较。该比较受ADC流水线延迟的控制；比较精度取决于转换器分辨率。阈值下限幅度由下式定义：

Lower threshold amplitude (dBFS) = 20 log(threshold amplitude / 2^{13}) 阈值下限幅度 (dBFS) = 20 log (阈值幅度/2^{13})

English: For example, to set an upper threshold of −6 dBFS, write 0xFFF to registers 0x247 and 0x248; to set a lower threshold of −10 dBFS, write 0xA1D to registers 0x249 and 0x24A. The dwell time can be set from 1 to 65535 sample clock cycles by writing the desired value to the fast-detect dwell-time registers (registers 0x24B and 0x24C).

例如，要设置−6 dBFS的阈值上限，应将0xFFF写入寄存器0x247和寄存器0x248；要设置−10 dBFS的阈值下限，应将0xA1D写入寄存器0x249和寄存器0x24A。驻留时间可以在1至65535个采样时钟周期范围内设置，方法是将所需值写入快速检测驻留时间寄存器(寄存器0x24B和 0x24C)。

7、数字下变频器(DDC) / 13.7 Digital Downconverter (DDC)

English: The SXA032 integrates 4 digital downconverters (DDC 0 to DDC 3) for filtering and reducing the output data rate. The digital processing section includes an NCO, half-band decimation filters, FIR filters, a gain stage and a complex-to-real conversion stage. Each processing block has control lines and can be individually enabled or disabled to provide the required processing functions. By configuring the digital downconverters, real or complex output data can be produced.

SXA032 内置4个数字下变频器(DDC 0至DDC 3)，用于滤波和降低输出数据速率。该数字处理部分包括NCO、半带抽取滤波器、FIR滤波器、增益级和复数-实数转换级。各处理模块都有控制线路，能单独使能或者禁用，以便提供所需的处理功能。通过配置数字下变频器，可以输出实数数据或复数数据。

13.7.1 DDC I/Q Input Selection / 7.1 DDC I/Q输入选择

English: The SXA032 has 2 ADC channels and 4 DDC channels. Each DDC channel has 2 input ports, which can be paired through the I/Q crossbar multiplexer to support real or complex inputs. For real signals, both DDC input ports must select the same ADC channel, e.g.: DDC input port I = ADC channel A, input port Q = ADC channel A. For complex signals, each DDC input port must select a different ADC channel, e.g.: DDC input port I = ADC channel A, input port Q = ADC channel B. The inputs of each DDC are controlled by the DDC input select registers (register 0x311, register 0x331, register 0x351 and register 0x371).

SXA032 有2个ADC通道和4个DDC通道。每个DDC通道有2个输入端口，这些端口可以配对以通过I/Q纵横式多路复用器支持实数或复数输入。对于实数信号，两个DDC输入端口必须选择同一ADC通道，例如：DDC输入端口I = ADC通道A，输入端口Q = ADC通道A。对于复数信号，各DDC输入端口必须选择不同ADC通道，例如：DDC输入端口I =ADC通道A，输入端口Q = ADC通道B。各DDC的输入由DDC输入选择寄存器(寄存器0x311、寄存器0x331、寄存器0x351 和寄存器0x371)控制。

13.7.2 DDC I/Q Output Selection / 7.2 DDC I/Q输出选择

English: Each DDC channel has 2 output ports, which can be paired to support real or complex outputs. For real output signals, only DDC output port I is used (DDC output port Q is invalid). For complex I/Q output signals, both DDC output port I and DDC output port Q are used. The I/Q outputs of each DDC channel are controlled by the DDC complex-to-real enable bit (bit 3) in the DDC control registers (register 0x310, register 0x330, register 0x350 and register 0x370).

每个DDC通道有2个输出端口，这些端口可以配对以支持实数或复数输出。对于实数输出信号，仅使用DDC输出端口I(DDC输出端口Q无效)。对于复数I/Q输出信号，DDC输出端口I和 DDC输出端口Q均要使用。各DDC通道的I/Q输出由DDC控制寄存器(寄存器0x310、寄存器 0x330、寄存器0x350和寄存器0x370)中的DDC复数转实数使能位(位3)控制。

English: The chip Q ignore bit (bit 5) in the chip application mode register (register 0x200) controls the chip output multiplexing of all DDC channels. When all DDC channels use real outputs, this bit must be set high to ignore all DDC Q output ports. When any DDC channel is set to use complex I/Q output, the user must clear this bit to use both DDC output port I and DDC output port Q.

芯片应用模式寄存器(寄存器0x200)中的芯片Q忽略位(位5)控制所有DDC通道的芯片输出复用。所有DDC通道都使用实数输出时，此位必须设置为高电平以忽略所有DDC Q输出端口。当设置任一DDC通道使用复数I/Q输出时，用户必须清除此位以便同时使用DDC输出端口I和 DDC输出端口Q。

13.7.3 DDC Overview / 7.3 DDC概述

English: The four DDC blocks extract a portion of the full digital spectrum captured by the ADC. They are designed for IF sampling or oversampled baseband radios requiring wideband input signals.

四个DDC模块用于提取ADC捕捉的全数字频谱的一部分。它们设计用于需要宽带宽输入信号的中频采样或过采样基带无线电。

Each DDC block contains 4 signal-processing stages: / 各DDC模块包含4个信号处理级：

13.7.4 Frequency Translation Stage (Optional) / 7.4 频率转换级(可选)

English: The frequency translation stage consists of a 12-bit complex NCO and a quadrature mixer, usable for frequency translation of real or complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

频率转换级由12位复数NCO和正交混频器组成，可用于实数或复数输入信号的频率转换。该级将一部分可用数字频谱下移至基带。

13.7.5 Filter Stage / 7.5 滤波级

English: After shifting to baseband, the filter stage decimates the spectrum for rate conversion using up to 4 cascaded half-band low-pass filters. Decimation reduces the output data rate and thus the output interface rate.

中文： 下移至基带后，滤波级利用最多4个相连的半带低通滤波器抽取频谱进行速率转换。抽取过程会降低输出数据速率，进而降低输出接口速率。

13.7.6 Gain Stage (Optional) / 7.6 增益级(可选)

English: Mixing a real input signal down to baseband incurs loss; the gain stage compensates by adding 0 dB or 6 dB of gain.

中文： 实数输入信号下混频至基带会有损失，增益级通过增加0 dB或6 dB的增益予以补偿。

13.7.7 Complex-to-Real Conversion Stage (Optional) / 7.7 复数至实数转换级(可选)

English: When real output is required, the complex-to-real conversion stage performs an fS/4 mixing operation and filters out the complex component of the signal through filters, converting the complex output back to real output. Figure 25 shows the detailed DDC block diagram as implemented in the SXA032.

需要实数输出时，复数至实数转换级执行fS/4混频操作，并通过滤波器滤除信号的复数成分，从而将复数输出转回实数输出。图25所示为SXA032中实现的DDC详细框图。

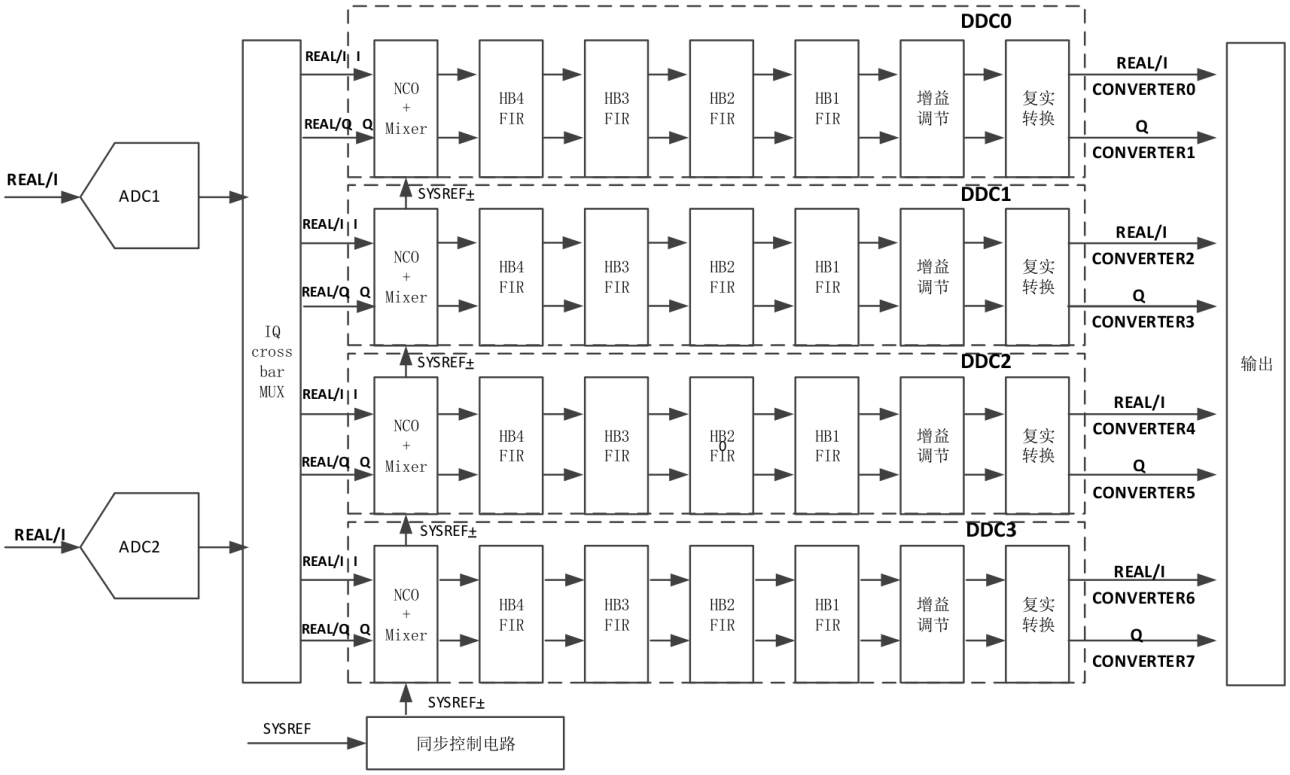


Figure 25: Detailed DDC block diagram

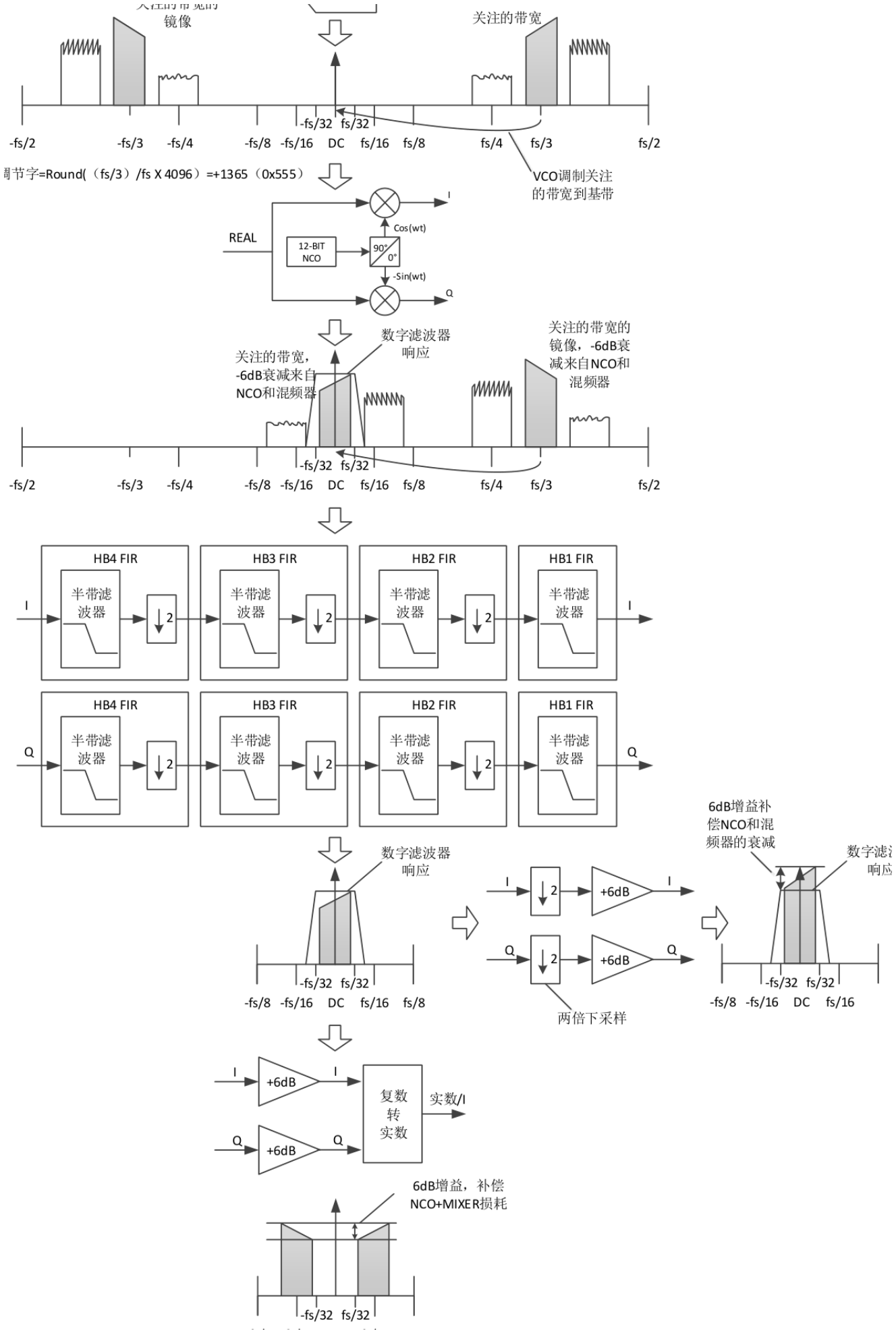

镜像
关注的带宽
-fs/32 fs/32
-fs/2 -fs/3 -fs/4 -fs/8 -fs/16 DC fs/16 fs/8 fs/4 fs/3 fs/2
VCO调制关注的带宽到基带
节字=Round(（fs/3）/fs X 4096）=+1365（0x555）
REAL
12-BIT NCO
Cos(wt)
-Sin(wt)
90°
0°
I
Q
关注的带宽，-6dB衰减来自NCO和混频器
数字滤波器响应
关注的带宽的镜像，-6dB衰减来自NCO和混频器
HB4 FIR
HB3 FIR
HB2 FIR
HB1 FIR
半带滤波器
2
6dB增益补偿NCO和混频器的衰减
+6dB
两倍下采样
复数转实数
实数/I
6dB增益，补偿NCO+MIXER损耗

Figure 26: DDC operating principle

English: The figure shows an example use of one DDC block with a real input signal and four half-band filters (HB4, HB3, HB2 and HB1). Both complex (16× decimation) and real (8× decimation) output options are shown.

显示了其中一个DDC模块的使用实例，它采用实数输入信号和四个半带滤波器(HB4、HB3、HB2和HB1)。复数(16倍抽取)和实数(8倍抽取)输出选项均有显示。

English: When DDCs have different decimation ratios, the chip decimation ratio (register 0x201) must be set to the lowest decimation ratio among all DDC blocks. In this case, samples of higher-decimation DDCs are repeated to match the chip decimation sample rate. A DDC soft reset must be performed whenever the NCO frequency is set or changed. Without a DDC soft reset, the output may have amplitude errors. Tables 6–10 show DDC samples with chip decimation ratios of 1, 2, 4, 8 and 16 respectively.

当DDC有不同的抽取比时，芯片抽取比(寄存器0x201)必须设置为所有DDC模块中最低的抽取比。这种情况下，较高抽取比DDC的样本会重复以匹配芯片抽取比样本速率。只要设置或改变NCO频率，就必须执行DDC软复位。如果不执行DDC软复位，输出可能会有幅度偏差。表6-0分别显示芯片抽取比设置为1、2、4、8和16倍时的DDC样本。

表6 DDC 样本(芯片抽取比 = 1) / Table 6 — DDC Samples (Chip Decimation Ratio = 1)

Real (I) Output (complex-to-real enabled) / 实数(I)输出(使能复数转实数)				**Complex (I/Q) Output (complex-to-real disabled) / 复数(I/Q)输出(禁用复数转实数)**			
HB1 FIR (DCM1=1)	HB2 FIR + HB1 FIR (DCM1=2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1=4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB1 FIR (DCM1=2)	HB2 FIR + HB1 FIR (DCM1=4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=16)
N	N	N	N	N	N	N	N
N+1	N	N	N	N	N	N	N
N+2	N+1	N	N	N+1	N	N	N
N+3	N+1	N	N	N+1	N	N	N
N+4	N+2	N+1	N	N+2	N+1	N	N
N+5	N+2	N+1	N	N+2	N+1	N	N
N+6	N+3	N+1	N	N+3	N+1	N	N
N+7	N+3	N+1	N	N+3	N+1	N	N
N+8	N+4	N+2	N+1	N+4	N+2	N+1	N
N+9	N+4	N+2	N+1	N+4	N+2	N+1	N
N+10	N+5	N+2	N+1	N+5	N+2	N+1	N
N+11	N+5	N+2	N+1	N+5	N+2	N+1	N
N+12	N+6	N+3	N+1	N+6	N+3	N+1	N

Real (I) Output (complex-to-real enabled) / 实数(I)输出(使能复数转实数)				Complex (I/Q) Output (complex-to-real disabled) / 复数(I/Q)输出(禁用复数转实数)			
N+13	N+6	N+3	N+1	N+6	N+3	N+1	N
N+14	N+7	N+3	N+1	N+7	N+3	N+1	N
N+15	N+7	N+3	N+1	N+7	N+3	N+1	N
N+16	N+8	N+4	N+2	N+8	N+4	N+2	N+1
N+17	N+8	N+4	N+2	N+8	N+4	N+2	N+1
N+18	N+9	N+4	N+2	N+9	N+4	N+2	N+1
N+19	N+9	N+4	N+2	N+9	N+4	N+2	N+1
N+20	N+10	N+5	N+2	N+10	N+5	N+2	N+1
N+21	N+10	N+5	N+2	N+10	N+5	N+2	N+1
N+22	N+11	N+5	N+2	N+11	N+5	N+2	N+1
N+23	N+11	N+5	N+2	N+11	N+5	N+2	N+1
N+24	N+12	N+6	N+3	N+12	N+6	N+3	N+1
N+25	N+12	N+6	N+3	N+12	N+6	N+3	N+1
N+26	N+13	N+6	N+3	N+13	N+6	N+3	N+1
N+27	N+13	N+6	N+3	N+13	N+6	N+3	N+1
N+28	N+14	N+7	N+3	N+14	N+7	N+3	N+1
N+29	N+14	N+7	N+3	N+14	N+7	N+3	N+1
N+30	N+15	N+7	N+3	N+15	N+7	N+3	N+1
N+31	N+15	N+7	N+3	N+15	N+7	N+3	N+1

1 DCM = decimation / DCM = 抽取

表7 DDC 样本(芯片抽取比 = 2) / Table 7 — DDC Samples (Chip Decimation Ratio = 2)

Real (I) Output (complex-to-real enabled) / 实数(I)输出(使能复数转实数)				Complex (I/Q) Output (complex-to-real disabled) / 复数(I/Q)输出(禁用复数转实数)			
HB2 FIR + HB1 FIR (DCM1=2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1=4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB1 FIR (DCM1=2)	HB2 FIR + HB1 FIR (DCM1=4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=16)	
N	N	N	N	N	N	N	
N+1	N	N	N+1	N	N	N	
N+2	N+1	N	N+2	N+1	N	N	
N+3	N+1	N	N+3	N+1	N	N	

Real (I) Output (complex-to-real enabled) / 实数(I)输出(使能复数转实数)			Complex (I/Q) Output (complex-to-real disabled) / 复数(I/Q)输出(禁用复数转实数)			
N+4	N+2	N+1	N+4	N+2	N+1	N
N+5	N+2	N+1	N+5	N+2	N+1	N
N+6	N+3	N+1	N+6	N+3	N+1	N
N+7	N+3	N+1	N+7	N+3	N+1	N
N+8	N+4	N+2	N+8	N+4	N+2	N+1
N+9	N+4	N+2	N+9	N+4	N+2	N+1
N+10	N+5	N+2	N+10	N+5	N+2	N+1
N+11	N+5	N+2	N+11	N+5	N+2	N+1
N+12	N+6	N+3	N+12	N+6	N+3	N+1
N+13	N+6	N+3	N+13	N+6	N+3	N+1
N+14	N+7	N+3	N+14	N+7	N+3	N+1
N+15	N+7	N+3	N+15	N+7	N+3	N+1

1 DCM = decimation / DCM = 抽取

表8 DDC 样本(芯片抽取比 = 4) / Table 8 — DDC Samples (Chip Decimation Ratio = 4)

Real (I) Output (complex-to-real enabled) / 实数(I)输出(使能复数转实数)			Complex (I/Q) Output (complex-to-real disabled) / 复数(I/Q)输出(禁用复数转实数)	
HB3 FIR + HB2 FIR + HB1 FIR (DCM1=4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB2 FIR + HB1 FIR (DCM1=4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=16)
N	N	N	N	N
N+1	N	N+1	N	N
N+2	N+1	N+2	N+1	N
N+3	N+1	N+3	N+1	N
N+4	N+2	N+4	N+2	N+1
N+5	N+2	N+5	N+2	N+1
N+6	N+3	N+6	N+3	N+1
N+7	N+3	N+7	N+3	N+1

1 DCM = decimation / DCM = 抽取

表9 DDC 样本(芯片抽取比 = 8) / Table 9 — DDC Samples (Chip Decimation Ratio = 8)

Real (I) Output (complex-to-real enabled) / 实数(I)输出(使能复数转实数)	Complex (I/Q) Output (complex-to-real disabled) / 复数(I/Q)输出(禁用复数转实数)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1=8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=16)
N	N	N
N+1	N+1	N
N+2	N+2	N+1
N+3	N+3	N+1
N+4	N+4	N+2
N+5	N+5	N+2
N+6	N+6	N+3
N+7	N+7	N+3

1 DCM = decimation / DCM = 抽取

表10 DDC 样本(芯片抽取比 = 16) / Table 10 — DDC Samples (Chip Decimation Ratio = 16)

Real (I) Output (complex-to-real enabled) / 实数(I)输出(使能复数转实数)	Complex (I/Q) Output (complex-to-real disabled) / 复数(I/Q)输出(禁用复数转实数)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM=16): N/A / 不适用	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1=16): N, N+1, N+2, N+3

1 DCM = decimation / DCM = 抽取

English: If the chip decimation ratio is set to 4× decimation, DDC 0 is set to use HB2 + HB1 filters (complex output, 4× decimation), and DDC 1 is set to use HB4 + HB3 + HB2 + HB1 filters (real output, 8× decimation), then for every DDC 0 output, the DDC 1 output data is repeated twice. The corresponding output samples are shown in Table 11.

如果芯片抽取比设置为4倍抽取，DDC 0设置为使用HB2 + HB1滤波器(复数输出4倍抽取)，DDC 1设置为使用HB4 + HB3 + HB2+ HB1滤波器(实数输出8倍抽取)，则对每一个DDC 0输出，DDC 1的输出数据都会重复两次。相应的输出样本如表11所示。

表11 DCM1 = 4、DDC0 DCM1= 4(复数)且 DDC1 DCM1 = 8(实数)时的 DDC 输出样本 / Table 11 — DDC Output Samples (DCM1 = 4, DDC0 DCM1 = 4 (complex), DDC1 DCM1 = 8 (real))

DDC Input Samples / DDC 输入样本	DDC 0 Output Port I / 输出端口 I	DDC 0 Output Port Q / 输出端口 Q	DDC 1 Output Port I / 输出端口 I	DDC 1 Output Port Q / 输出端口 Q
N				
N+1	I0[N]	Q0[N]		

DDC Input Samples / DDC 输入样本	DDC 0 Output Port I / 输出端口 I	DDC 0 Output Port Q / 输出端口 Q	DDC 1 Output Port I / 输出端口 I	DDC 1 Output Port Q / 输出端口 Q
N+2				
N+3			I1[N]	N/A / 不适用
N+4				
N+5	I0[N+1]	Q0[N+1]		
N+6				
N+7				
N+8				
N+9	I0[N+2]	Q0[N+2]		
N+10				
N+11			I1[N+1]	N/A / 不适用
N+12				
N+13	I0[N+3]	Q0[N+3]		
N+14				
N+15				

13.7.8 Frequency Translation / 7.8 频率转换

Overview / 概述

English: Frequency translation is implemented using a 12-bit complex NCO and a digital quadrature mixer. Frequency translation converts a real or complex input signal from an intermediate frequency (IF) to a baseband complex digital output (carrier = 0 Hz). The frequency translation stage of each DDC can be controlled individually, supporting four different IF modes, selectable via bits [5:4] of the DDC control registers (register 0x310, register 0x330, register 0x350 and register 0x370). The IF modes are:

频率转换是利用12位复数NCO和数字正交混频器实现的。频率转换将一个实数或复数输入信号从中频(IF)转换为基带复数数字输出(载波 = 0 Hz)。各DDC的频率转换级可以单独控制，支持四种不同的IF模式，利用DDC控制寄存器(寄存器0x310、寄存器0x330、寄存器0x350和寄存器0x370)的位[5:4]可以选择具体模式。这些IF模式如下：

- Variable IF mode / 可变IF模式
- 0 Hz IF (ZIF) mode / 0 Hz IF (ZIF)模式
- fS/4 Hz IF mode / fS/4 Hz IF模式
- Test mode / 测试模式

Variable IF mode: NCO and mixer enabled. The NCO output frequency can be used to digitally tune the IF frequency. 可变 IF 模式：NCO和混频器使能。NCO输出频率可用来对IF频率进行数字调谐。

0 Hz IF (ZIF) mode: mixer bypassed, NCO disabled. 0 Hz IF (ZIF)模式：混频器旁路，NCO禁用。

fS/4 Hz IF mode: mixer and NCO enabled in a special fS/4 mixing mode to save power. fS/4 Hz IF 模式：混频器和NCO在特殊的fS/4下混频模式中使能以节省功耗。

Test mode: forces input samples to 0.999 to positive full scale. NCO enabled. This test mode allows the NCO to directly drive the decimation filters. Figures 27 and 29 show examples of the frequency translation stage for real and complex inputs. 测试模式：迫使输入样本达到0.999至正满量程。NCO使能。该测试模式允许NCO直接驱动抽取滤波器。图27和图28显示用于实数和复数输入的频率转换级的实例。

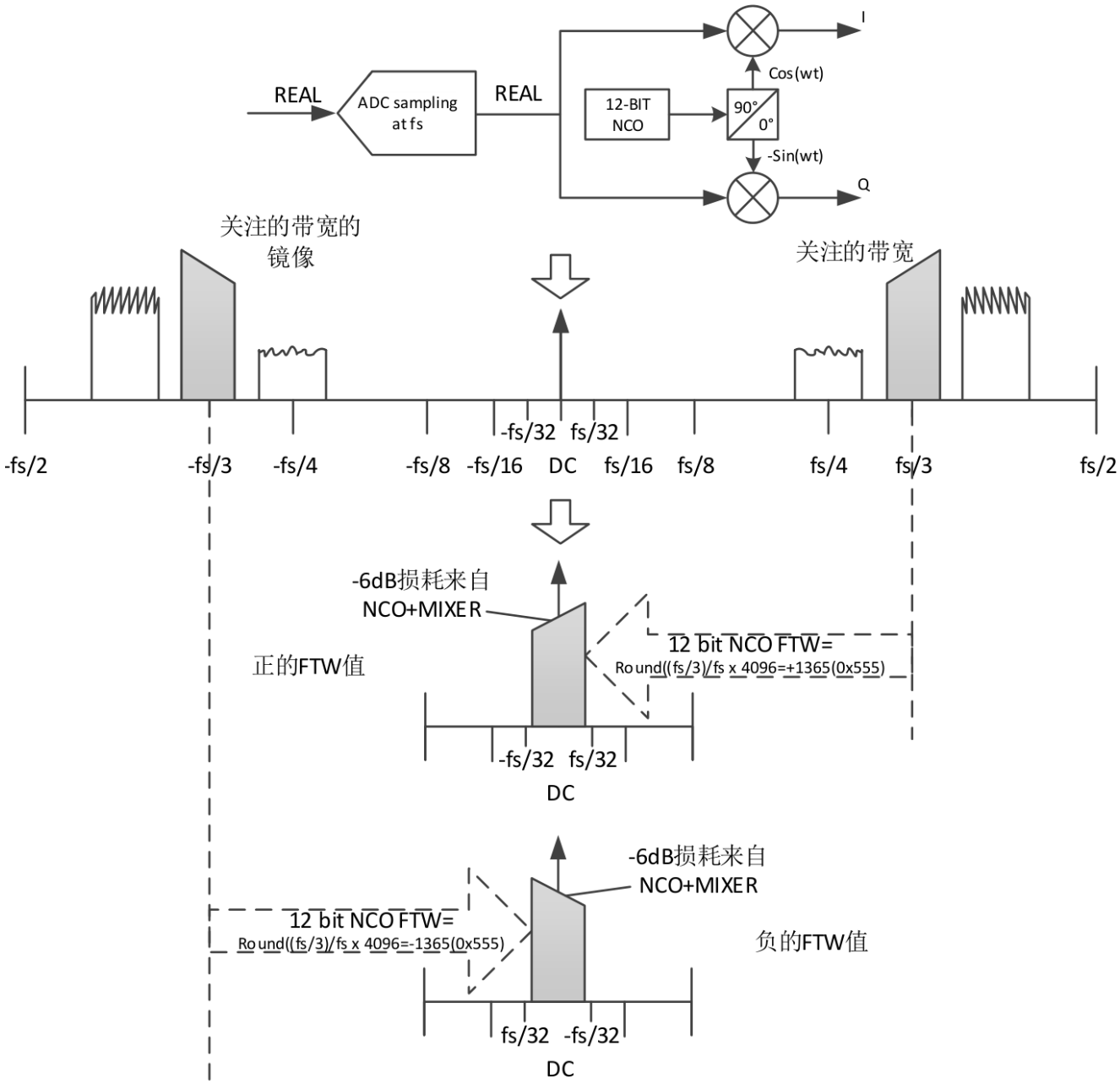


Figure 27: NCO frequency tuning word selection — real input

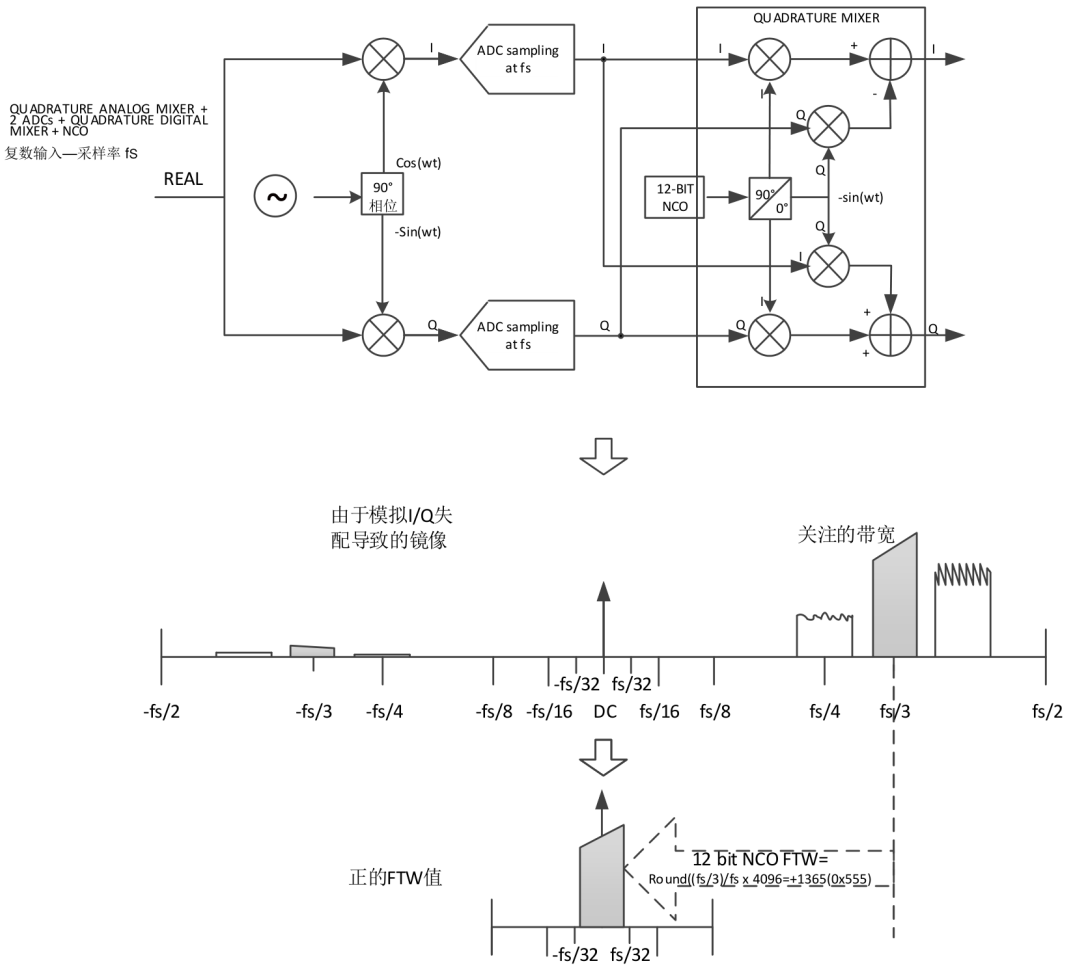


Figure 28: NCO frequency tuning word selection — complex input

DDC NCO Plus Mixer Loss and SFDR / DDC NCO 加混频器的损失和 SFDR

English: When down-mixing a real input signal to baseband, the signal suffers 6 dB of loss due to filtering of the negative image. In addition, the NCO causes 0.05 dB of loss. The total loss of a real input signal down-mixed to baseband is 6.05 dB. It is therefore recommended to enable the 6 dB additional gain in the DDC gain stage to compensate for the above loss, re-centering the signal's dynamic range in the full scale of the output bits.

将实数输入信号下混频至基带时，由于对负镜像的滤波，信号会有6 dB的损失。另外，NCO 也会造成0.05 dB的损失。下混频至基带的实数输入信号的总损失为6.05 dB。因此，建议用户使能DDC增益级中的6 dB附加增益来补偿上述损失，从而将信号的动态范围中心重新定位在输出位的满量程中。

English: When down-mixing a complex input signal to baseband, the maximum value each I/Q sample can reach after the complex mixer is 1.414 × full scale. For complex signals, to prevent I/Q samples from exceeding the range and to keep the data bit width consistent with real mixing, the mixer causes 3.06 dB of loss (0.707 × full scale). In addition, the NCO causes 0.05 dB of loss. The total loss of a complex input signal down-mixed to baseband is −3.11 dB.

将复数输入信号下混频至基带时，每个I/Q样本经过复数混频器后能达到的最大值是1.414 × 满量程。对于复数信号，为了防止I/Q样本超出量程，以及使数据位宽与实数混频一致，混频器会造成3.06 dB的损失(0.707 × 满量程)。另外，NCO也会造成0.05 dB的损失。下混频至基带的复数输入信号的总损失为−3.11 dB。

English: For all output frequencies, the SFDR of the worst-case spurious signal at the NCO output is greater than 102 dBc.

对于所有输出频率，NCO输出的最差情况杂散信号的SFDR大于102 dBc。

Numerically Controlled Oscillator / 数控振荡器

English: Each DDC of the SXA032 has a 12-bit NCO to support the frequency translation process. The NCO can adjust the input spectrum to a DC signal, which is then effectively filtered by the following filters to prevent signal aliasing. The NCO is set via the frequency tuning word (FTW) and phase offset word (POW).

SXA032 的每个DDC都有一个12位NCO，用以支持频率转换过程。NCO可将输入频谱调整为直流信号，由后面的滤波器对其进行有效滤波，防止信号混叠。NCO可通过频率调谐字(FTW) 和相位偏移字(POW)来设置。

Setting the NCO FTW and POW / 设置 NCO FTW 和 POW

English: The NCO frequency value is determined by the 12-bit two's-complement number of the input NCO FTW.

NCO频率值由输入NCO FTW的12位二进制补码数决定。

English: The following frequency words represent frequency values between −fS/2 and fS/2 (excluding fS/2):

中文： 下列频率字代表−fS/2和fS/2(不包括fS/2)之间的频率值：

- 0x800 represents a frequency of −fS/2. / 0x800代表−fS/2的频率。
- 0x000 represents DC (frequency 0 Hz). / 0x000代表DC(频率为0 Hz)。
- 0x7FF represents a frequency of +fS/2 − fS/2^{12}. / 0x7FF代表+fS/2 − fS/2^{12}的频率。

The NCO frequency tuning word is calculated as: / NCO频率调谐字可通过下式计算：

English: NCO_FTW = round(2^{12} × Mod(fc, fs) / fs)

where: / 其中：

- NCO_FTW is the 12-bit two's-complement value representing the NCO FTW. / NCO_FTW是代表NCO FTW的12位二进制补码数值。
- fS is the SXA032 sampling frequency (clock rate), in Hz. / fS是SXA032采样频率(时钟速率)，单位为Hz。
- fC is the desired carrier frequency, in Hz. / fC是所需的载波频率，单位为Hz。
- Mod() is the modulo function. For example, Mod(110, 100) = 10; for negative numbers, Mod(−32, 10) = −2. / Mod()是求余函数。例如，Mod(110,100) = 10；对于负数，Mod(−32, 10) = −2。
- round() is the rounding function. For example, round(3.6) = 4; for negative numbers, round(−3.4) = −3. / round()是四舍五入函数。例如，round(3.6) = 4；对于负数，round(−3.4)= −3。

English: Note: this formula applies to signal aliasing in the digital domain (i.e., aliasing introduced when digitizing analog signals).

中文： 注意，此公式适用于数字域中的信号混叠(即数字化模拟信号时引入的混叠)。

English: For example, if the ADC sampling frequency (fS) is 1250 MSPS and the carrier frequency (fC) is 416.667 MHz, then

例如，如果ADC采样频率(fS)为1250 MSPS且载波频率(fC)为 416.667 MHz，则

English: NCO_FTW = round(2^{12} × Mod(416.667, 1250) / 1250) = 1365

English: which is then converted to the 12-bit two's-complement representation of NCO_FTW: 0x555.

然后将其转换为NCO_FTW的12位二进制补码表示0x555。

The actual carrier frequency is calculated as: / 实际载波频率可根据下式计算：

English: fc_actual = NCO_FTW × fS / 2^{12} = 416.56 MHz

English: Each NCO uses a 12-bit POW to establish a known phase relationship between multiple SXA032 chips or between DDC channels within one SXA032. The following procedure must be followed to update the FTW and/or POW registers to ensure normal NCO operation:

每个NCO利用12位POW来建立多个SXA032芯片之间或一个SXA032内部各DDC通道之间的已知相位关系。必须按照以下程序来更新FTW和/或POW寄存器，确保NCO正常工作：

- Write the FTW registers of all DDCs. / 写入所有DDC的FTW寄存器。
- Write the POW registers of all DDCs. / 写入所有DDC的POW寄存器。
- Synchronize the NCO via SPI access to the DDC soft-reset bit, or by asserting the SYSREF± pins. / 通过SPI访问DDC软复位位，或通过置位SYSREF±引脚来同步NCO。

English: Note: after completing all write operations to the FTW or POW registers, the NCO must be synchronized via SPI or the SYSREF± pins. This synchronization is required to ensure normal NCO operation.

注意，完成对FTW或POW寄存器的所有写操作之后，必须通过SPI或SYSREF±引脚同步NCO。这种同步是确保NCO正常工作所必需。

NCO Synchronization / NCO 同步

English: Each NCO contains a separate phase accumulator word (PAW) that determines the instantaneous phase of the NCO. The initial reset value of each PAW is determined by the POW as described in the "Setting NCO_FTW and POW" section. The phase increment of each PAW is determined by the FTW.

每个NCO都含有一个单独的相位累加器字(PAW)，用于确定NCO的瞬时相位。各PAW的初始复位值由"设置NCO_FTW和POW"部分所述的POW决定。各PAW的相位递增值由FTW决定。

There are two methods to synchronize multiple PAWs within a chip: / 同步芯片内的多个PAW有两种方法：

- Using SPI. The DDC NCO soft-reset bit in the DDC synchronization control register (register 0x300 bit 4) can be used to reset all PAWs in the chip. This is done by toggling the DDC NCO soft-reset bit. This method can only synchronize DDC channels within the same SXA032 chip. 使用SPI。可以利用DDC同步控制寄存器中的DDC NCO软复位位(寄存器0x300的位4)来复位芯片中的所有PAW。这可通过切换DDC NCO软复位位来实现。这种方法只能用来同步同一SXA032芯片内的DDC通道。
- Using the SYSREF± pins. If the SYSREF± pins are enabled via the SYSREF± control registers (register 0x120 and register 0x121), and DDC synchronization is enabled via bits [1:0] of the DDC

synchronization control register (register 0x300), then any subsequent SYSREF± event resets all PAWs in the chip. This method can synchronize DDC channels both within the same SXA032 chip and across different SXA032 chips. 使用SYSREF±引脚。如果通过SYSREF±控制寄存器(寄存器0x120和寄存器0x121)使能 SYSREF±引脚，并且通过DDC同步控制寄存器(寄存器0x300)的位[1:0]使能DDC同步，则随后的任何SYSREF±事件都会复位芯片中的全部PAW。这种方法既可同步同一SXA032芯片内的DDC通道，也可同步不同SXA032芯片内的DDC通道。

Mixer / 混频器

English: The NCO is accompanied by a mixer whose operation is similar to an analog quadrature mixer. It uses the NCO frequency as the local oscillator to down-convert the input signal (real or complex). For real input signals, the mixer performs real mixer operation (using two multipliers). For complex input signals, it performs complex mixer operation (using four multipliers and two adders). The mixer adjusts its operation according to the input signal (real or complex) provided to each channel. Bit 7 of the DDC control registers (register 0x310, register 0x330, register 0x350 and register 0x370) controls the real or complex input selection of each DDC block.

NCO伴随一个混频器，其操作类似于模拟正交混频器。它将NCO频率用作本振，对输入信号(实数或复数)进行下变频。对于实数输入信号，此混频器执行实数混频器操作(利用两个乘法器)。对于复数输入信号，此混频器执行复数混频器操作(利用四个乘法器和两个加法器)。混频器根据提供给各通道的输入信号(实数或复数)调整其操作。利用DDC控制寄存器(寄存器0x310、寄存器0x330、寄存器0x350和寄存器0x370)的位7，可以控制各DDC模块的实数或复数输入选择。

DDC Configuration Examples / DDC 配置示例

Table 12 lists register settings for several DDC configuration examples. / 表12列出了多个DDC配置示例的寄存器设置。

表12 DDC 配置示例 / Table 12 — DDC Configuration Examples

Chip Application Layer / 芯片应用层	Chip Decimation Ratio / 芯片抽取比	DDC Input Type / DDC 输入类型	DDC Output Type / DDC 输出类型	Bandwidth per DDC / 每个 DDC 的带宽	Virtual Converters Required (M) / 所需的虚拟转换器数 (M)	Register Settings / 寄存器设置
1 DDC	2	Complex / 复数	Complex / 复数	77%×fS	2	寄存器0x200 = 0x01 (one DDC; select I/Q / 一个DDC；选择I/Q); 寄存器0x201 = 0x01 (chip 2× decimation / 芯片2倍抽取); 寄存器0x310 = 0x83 (complex mixer; 0 dB gain; variable IF; complex output; HB1 filter / 复数混频器；0 dB增益；可变IF；复数输出；HB1滤波器); 寄存器0x311 = 0x04 (DDC I input = ADC channel A; DDC Q input = ADC channel B / DDC I输入 = ADC通道A；DDC Q输入 = ADC通道B); 寄存器0x314, 0x315, 0x320, 0x321 = FTW and POW set per application requirements for DDC 0 / FTW 和 POW 按照应用对DDC 0的要求而设置
2 DDCs	4	Complex / 复数	Complex / 复数	38.5%×fS	4	寄存器0x200 = 0x02 (two DDCs; select I/Q / 两个DDC；选择I/Q); 寄存器0x201 = 0x02

Chip Application Layer / 芯片应用层	Chip Decimation Ratio / 芯片抽取比	DDC Input Type / DDC 输入类型	DDC Output Type / DDC 输出类型	Bandwidth per DDC / 每个 DDC 的带宽	Virtual Converters Required (M) / 所需的虚拟转换器数 (M)	Register Settings / 寄存器设置
						(chip 4× decimation / 芯片4倍抽取); 寄存器0x310, 0x330 = 0x80 (complex mixer; 0 dB gain; variable IF; complex output; HB2+HB1 filters / 复数混频器；0 dB增益；可变IF；复数输出；HB2+HB1滤波器); 寄存器0x311, 0x331 = 0x04 (DDC I input = ADC channel A; DDC Q input = ADC channel B / DDC I输入 = ADC通道A；DDC Q输入 = ADC通道B); 寄存器0x314, 0x315, 0x320, 0x321 = FTW and POW set per application requirements for DDC 0 / FTW和POW按照应用对DDC 0的要求而设置; 寄存器0x334, 0x335, 0x340, 0x341 = FTW and POW set per application requirements for DDC 1 / FTW和POW按照应用对DDC 1的要求而设置
2 DDCs	4	Complex / 复数	Real / 实数	19.25%×fS	2	寄存器0x200 = 0x22 (two DDCs; select ignore Q / 两个DDC；选择忽略Q); 寄存器0x201 = 0x02 (chip 4× decimation / 芯片4倍抽取); 寄存器0x310, 0x330 = 0x89 (complex mixer; 0 dB gain; variable IF; real output; HB3+HB2+HB1 filters / 复数混频器；0 dB增益；可变IF；实数输出；HB3+HB2+HB1滤波器); 寄存器0x311, 0x331 = 0x04 (DDC I input = ADC channel A; DDC Q input = ADC channel B / DDC I输入 = ADC通道A；DDC Q输入 = ADC通道B); 寄存器0x314, 0x315, 0x320, 0x321 = FTW and POW set per application requirements for DDC 0 / FTW和POW按照应用对DDC 0的要求而设置; 寄存器0x334, 0x335, 0x340, 0x341 = FTW and POW set per application requirements for DDC 1 / FTW和POW按照应用对DDC 1的要求而设置
2 DDCs	4	Real / 实数	Real / 实数	19.25%×fS	2	寄存器0x200 = 0x22 (two DDCs; select ignore Q / 两个DDC；选择忽略Q); 寄存器0x201 = 0x02 (chip 4× decimation / 芯片4倍抽取); 寄存器0x310, 0x330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3+HB2+HB1 filters / 实数混频器；6 dB增益；可变IF；实数输出；HB3+HB2+HB1滤波器); 寄存器0x311 = 0x00 (DDC0 I input = ADC channel A; DDC0 Q input = ADC channel A / DDC0 I输入 = ADC通道A；DDC0 Q输入 = ADC通道A); 寄存器0x331 = 0x05 (DDC1 I input = ADC channel B; DDC1 Q input = ADC channel B / DDC1 I输入 = ADC通道B；DDC1 Q输入 = ADC通道B); 寄存器0x314, 0x315, 0x320, 0x321 = FTW and POW set per application requirements for DDC 0 / FTW和POW按照应用对DDC 0的要

Chip Application Layer / 芯片应用层	Chip Decimation Ratio / 芯片抽取比	DDC Input Type / DDC 输入类型	DDC Output Type / DDC 输出类型	Bandwidth per DDC / 每个 DDC 的带宽	Virtual Converters Required (M) / 所需的虚拟转换器数 (M)	Register Settings / 寄存器设置
						求而设置; 寄存器0x334, 0x335, 0x340, 0x341 = FTW and POW set per application requirements for DDC 1 / FTW和POW按照应用对DDC 1的要求而设置
2 DDCs	4	Real / 实数	Complex / 复数	38.5%×fS	4	寄存器0x201 = 0x02 (chip 4× decimation / 芯片4倍抽取); 寄存器0x310, 0x330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2+HB1 filters / 实数混频器；6 dB增益；可变IF；复数输出；HB2+HB1滤波器); 寄存器0x311 = 0x00 (DDC 0 I input = ADC channel A; DDC 0 Q input = ADC channel A / DDC 0 I输入 = ADC通道A；DDC 0 Q输入 = ADC通道A); 寄存器0x331 = 0x05 (DDC1 I input = ADC channel B; DDC1 Q input = ADC channel B / DDC1 I输入 = ADC通道B；DDC1 Q输入 = ADC通道B); 寄存器0x314, 0x315, 0x320, 0x321 = FTW and POW set per application requirements for DDC 0 / FTW和POW按照应用对DDC 0的要求而设置; 寄存器0x334, 0x335, 0x340, 0x341 = FTW and POW set per application requirements for DDC 1 / FTW和POW按照应用对DDC 1的要求而设置
4 DDCs	8	Real / 实数	Complex / 复数	19.25%×fS	8	寄存器0x200 = 0x03 (four DDCs; select I/Q / 四个DDC；选择I/Q); 寄存器0x201 = 0x03 (chip 8× decimation / 芯片8倍抽取); 寄存器0x310, 0x330, 0x350, 0x370 = 0x41 (real mixer; 6 dB gain; variable IF; complex output; HB3+HB2+HB1 filters / 实数混频器；6 dB增益；可变IF；复数输出；HB3+HB2+HB1滤波器); 寄存器0x311 = 0x00 (DDC 0 I input = ADC channel A; DDC 0 Q input = ADC channel A); 寄存器0x331 = 0x00 (DDC 1 I input = ADC channel A; DDC 1 Q input = ADC channel A); 寄存器0x351 = 0x05 (DDC 2 I input = ADC channel B; DDC 2 Q input = ADC channel B); 寄存器0x371 = 0x05 (DDC 3 I input = ADC channel B; DDC 3 Q input = ADC channel B); FTW/POW registers for DDC 0–DDC 3 set per application / FTW 和 POW 按照应用对各 DDC 的要求而设置
4 DDCs	16	Real / 实数	Complex / 复数	9.625%×fS	8	寄存器0x200 = 0x03 (four DDCs; select I/Q / 四个DDC；选择I/Q); 寄存器0x201 = 0x04 (chip 16× decimation / 芯片16倍抽取); 寄存器0x310, 0x330, 0x350, 0x370 = 0x42 (real mixer; 6 dB gain; variable IF; complex output; HB4+HB3+HB2+HB1 filters / 实数混频器；6 dB增益；可变IF；复数输出；

Chip Application Layer / 芯片应用层	Chip Decimation Ratio / 芯片抽取比	DDC Input Type / DDC 输入类型	DDC Output Type / DDC 输出类型	Bandwidth per DDC / 每个 DDC 的带宽	Virtual Converters Required (M) / 所需的虚拟转换器数 (M)	Register Settings / 寄存器设置
						HB4+HB3+HB2+HB1滤波器); 寄存器0x311 = 0x00 (DDC 0 I/Q inputs = ADC channel A); 寄存器0x331 = 0x00 (DDC 1 I/Q inputs = ADC channel A); 寄存器0x351 = 0x05 (DDC 2 I/Q inputs = ADC channel B); 寄存器0x371 = 0x05 (DDC 3 I/Q inputs = ADC channel B); FTW/POW registers for DDC 0–DDC 3 set per application / FTW和POW按照应用对各 DDC 的要求而设置

Notes / 备注： 1. fS = ADC sample rate. The listed bandwidths are for < −0.001 dB passband ripple and > 100 dB stopband alias rejection. / fs = ADC 采样速率。所列带宽为<−0.001 dB 的通带纹波和>100 dB 的阻带混叠抑制。 2. After completing all write operations to the FTW or POW registers, the NCO must be synchronized via SPI or the SYSREF± pins. This synchronization is required to ensure normal NCO operation. / 完成对 FTW 或 POW 寄存器的所有写操作之后，必须通过 SPI 或 SYSREF±引脚同步 NCO。这是确保 NCO 正常工作所必需的。

8、JESD204B 接口 / 13.8 JESD204B Interface

13.8.1 JESD204B Interface Introduction / 8.1 JESD204B接口简介

English: The SXA032 digital output is designed per JEDEC standard JESD204B ("serial interface for data converters"). JESD204B is the protocol by which the SXA032 connects to digital processing devices via a serial interface (lane rates up to 10 Gbps). Advantages of the JESD204B interface over LVDS include: less board space required for data-interface routing, and smaller packages for converters and logic devices.

SXA032 数字输出根据JEDEC标准JESD204B("数据转换器串行接口")进行设计。JESD204B 是SXA032通过串行接口(通道速率高达10 Gbps)连接数字处理设备的协议。JESD204B接口相对于LVDS的优势包括：数据接口布线所需电路板空间更少，以及转换器和逻辑器件的封装更小。

13.8.2 JESD204B Overview / 8.2 JESD204B概述

English: The JESD204B data transmit block combines parallel data from the ADC into data frames, and outputs serial data using 8B/10B encoding with optional data scrambling. During initial link establishment, special control characters support lane synchronization; synchronization thereafter is maintained by additional control characters embedded in the data stream. A JESD204B receiver is required to complete the serial link. For details of the JESD204B interface, refer to the JESD204B standard.

JESD204B 数据发送模块可将来自ADC的并行数据组合成数据帧，并使用8B/10B编码以及可选数据加扰技术，输出串行数据。在链路初始建立过程中，使用特殊控制字符来支持通道同步；此后的同步靠数据流中嵌入的附加控制字符来维持。完成串行链路需要JESD204B接收机。有关JESD204B接口的详细信息，请参见JESD204B标准。

English: The SXA032 JESD204B data transmit block can map up to 2 real ADCs or 8 virtual converters (when DDCs are enabled) through the link. The link can be configured to use 1, 2 or 4 JESD204B lanes. The JESD204B specification references several parameters to define the link; these parameters must match between the JESD204B transmitter and receiver. A JESD204B link is described by the following parameters:

SXA032 JESD204B数据发送模块通过链路最多可映射2个实际ADC或8个虚拟转换器(DDC 使能时)。可以配置链路以使用1个、2个或4个JESD204B通道。JESD204B规范引用多个参数来定义链路，JESD204B发射机和JESD204B接收机的这些参数必须匹配。JESD204B链路可通过下列参数描述：

- L = number of data lanes per converter (data lanes per link) (SXA032 values: 1, 2 or 4) / L =数据通路数/转换器(数据通路数/链路)(SXA032的值为1、2或4)
- M = number of converters per converter (virtual converters per link) (SXA032 values: 1, 2, 4 or 8) / M = 转换器数/转换器(虚拟转换器数/链路)(SXA032的值为1、2、4或8)
- F = number of octets per frame (SXA032 values: 1, 2, 4, 8 or 16) / F = 8位字数/帧(SXA032的值为1、2、4、8或16)
- N′ = number of bits per sample (JESD204B word size) (SXA032 values: 8 or 16) / N′ = 每个样本的位数(JESD204B字大小)(SXA032的值为8或16)
- N = converter resolution (SXA032 values: 7 to 16) / N = 转换器分辨率(SXA032的值为7至16)
- CS = number of control bits per sample (SXA032 values: 0, 1, 2 or 3) / CS = 控制位数/样本(SXA032的值为0、1、2或3)
- K = number of frames per multiframe (SXA032 values: 4, 8, 12, 16, 20, 24, 28 or 32) / K = 每个多帧的帧数(SXA032的值为4、8、12、16、20、24、28或32)
- S = number of samples transmitted per single converter per frame period (automatically set from L, M, F and N′) / S = 传送的样本数/单个转换器/帧周期(值根据L、M、F和N′自动设置)
- HD = high-density mode (automatically set from L, M, F and N′) / HD = 高密度模式(根据L、M、F和N′自动设置)
- CF = number of control words per frame clock period per converter (value 0) / CF = 控制字数/帧时钟周期/转换器(值为0)

English: Figure 29 shows a simplified block diagram of the SXA032 JESD204B link. The default configuration uses two converters and four data lanes. Converter A data is output to SERDOUT0± and/or SERDOUT1±; converter B data is output to SERDOUT2± and/or SERDOUT3±. The SXA032 supports other configurations, such as combining the outputs of both converters into a single lane, or changing the mapping of the A and B digital output paths. These modes are set via the quick-configuration registers in the SPI register map, with additional customization options.

图29显示SXA032 JESD204B链路的简化框图。默认配置为使用两个转换器和四个数据通路。转换器A的数据输出至SERDOUT0±和/或SERDOUT1±，转换器B的数据输出至SERDOUT2± 和/或SERDOUT3±。SXA032支持其它配置，如将两个转换器的输出组合成单通道，或改变A和 B数字输出路径的映射。这些模式可通过SPI寄存器映射中的快速配置寄存器进行设置，并且提供额外的自定义选项。

English: By default, each SXA032 converter's 14-bit converter word is split into two 8-bit words (data bits are 8 bits). The first 8-bit word includes bit 13 (MSB) through bit 6. The second 8-bit word includes bits 5 through 0 plus 2 tail bits. The tail bits can be configured as 0 or a pseudorandom number sequence, or replaced by control bits indicating overrange, SYSREF± or fast-detect output. The resulting two 8-bit words can be scrambled. Scrambling is optional but recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing polynomial-based

algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

默认情况下，每个SXA032转换器的14位转换器字都被分为两个8位字(数据位为8位)。第一个8位字包括位13 (MSB)到位6。第二个8位字包括位5至位0以及2个结束位。结束位可以配置为 0或伪随机数序列，还可以用指示超量程、SYSREF±或快速检测输出的控制位来取代结束位。可对生成的两个8位字进行加扰。加扰为可选项，但建议利用它来在传输相似的数字数据模式时避免频谱尖峰。加扰器采用自同步、基于多项式的算法，由方程$1 + x^{14} + x^{15}$定义。接收机中的解扰器是加扰器多项式的自同步版本。

English: The two 8-bit words then pass through the 8B/10B encoder. The 8B/10B encoder encodes 8 data bits (one 8-bit word) into a 10-bit symbol. Figure 30 shows how 14-bit data is taken from the ADC, how tail bits are added, how the two 8-bit words are scrambled, and how the 8-bit words are encoded into two 10-bit symbols.

之后，这两个8位字通过8B/10B编码器进行编码。8B/10B编码器将8个数据位(1个8位字)编码为一个10位的符号。图30显示14位的数据是如何从ADC中取出、结束位如何添加、两个8位字如何加扰，以及8位字如何被编码为两个10位符号。

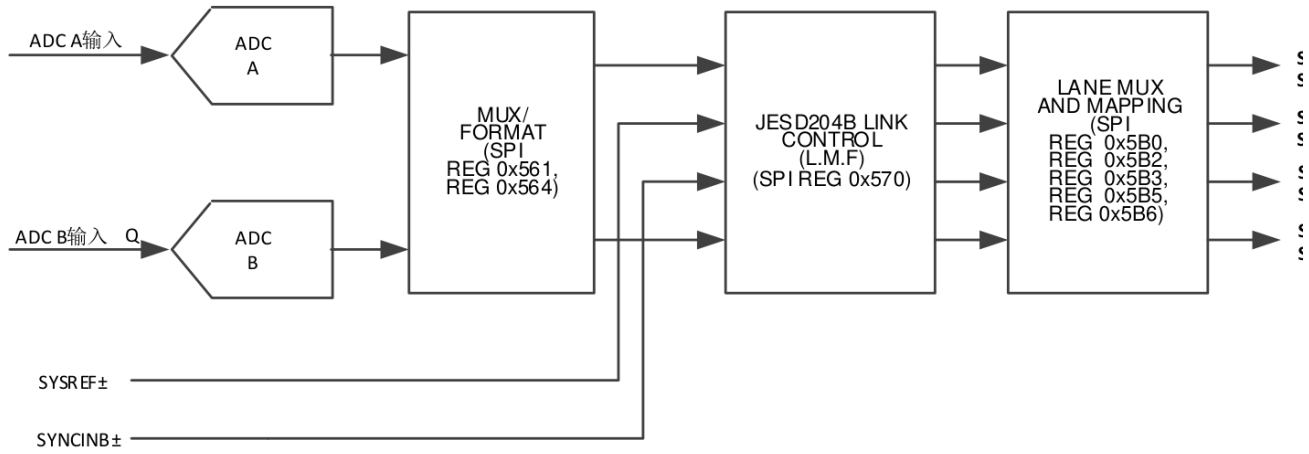


Figure 29: Simplified transmit-link diagram, full-bandwidth mode

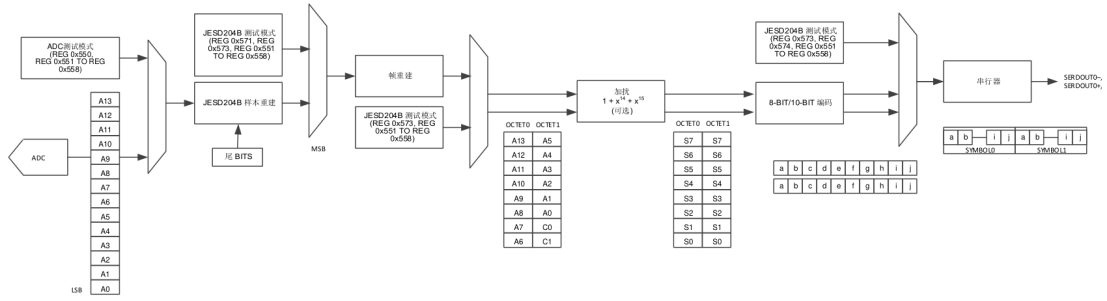


Figure 30: ADC output data path

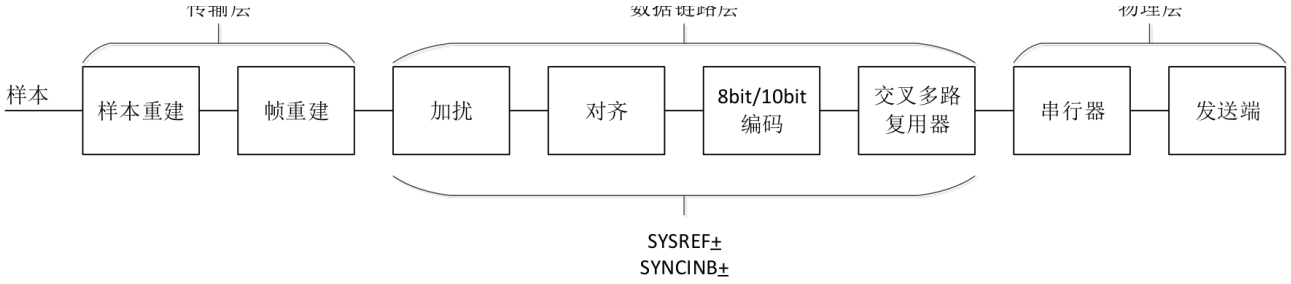


Figure 31: Data flow

13.8.3 Functional Overview / 8.3 功能概述

English: The block diagram in Figure 31 shows the JESD204B hardware data flow from sample input to physical output. Following the OSI (Open Source Initiative) model widely used to describe abstraction layers of communications systems, this processing can be divided into multiple layers: transport layer, data link layer and physical layer (serializer and output drivers).

图31中的框图显示了从样本输入到物理输出的JESD204B硬件数据流。依据广泛用于描述通信系统抽象层的OSI(开放源码促进会)模型，该处理可以分为多层：传输层、数据链路层和物理层(串行器和输出驱动器)。

13.8.4 Transport Layer / 8.4 传输层

English: The transport layer packs data (including samples and optional control bits) into JESD204B frames for mapping into 8-bit words. These 8-bit words are sent to the data link layer. Transport-layer mapping is governed by rules derived from the link parameters. Tail bits are added as needed to fill gaps. The number of tail bits in a sample (JESD204B word) is determined by:

传输层负责将数据(包括样本和可选的控制位)包装为JESD204B帧以便映射为8位字。这些8 位字被发送到数据链路层。传输层匹配由链路参数所产生的规则控制。根据需要添加结束位以填补空隙。可以利用下式来确定样本(JESD204B字)中的结束位数：

$$T = N' - N - CS$$

13.8.5 Data Link Layer / 8.5 数据链路层

English: The data link layer handles the low-level functions of data transfer through the link, including scrambling data (optional), inserting control characters to support multi-chip synchronization/lane alignment/monitoring, and encoding 8-bit words into 10-bit symbols. The data link layer also sends the initial lane alignment sequence (ILAS), which contains link configuration data used by the receiver to verify transport-layer settings.

数据链路层负责通过链路传送数据的低层功能，包括加扰数据(可选)、插入控制字符以支持多芯片同步/通道对齐/监控，以及将8位字编码为10位符号。数据链路层还负责发送初始通道对齐序列(ILAS)，其中包含链路配置数据，接收机利用这些数据验证传输层的设置。

13.8.6 Physical Layer / 8.6 物理层

English: The physical layer consists of high-speed circuits clocked at the serial clock rate. In this layer, parallel data is converted into high-speed differential serial data on 1, 2 or 4 lanes.

中文： 物理层由时钟频率为串行时钟速率的高速电路组成。在该层中，并行数据转换为1、2或4 通道的高速差分串行数据。

13.8.7 JESD204B Link Establishment / 8.7 JESD204B链路建立

English: The SXA032 JESD204B transmitter (Tx) interface operates in Subclass 1 per JEDEC Standard 204B. The link establishment process consists of the following steps: code group synchronization and SYNCINB±, initial lane alignment sequence (ILAS), and user data and error correction.

SXA032 JESD204B发射机(Tx)接口按照JEDEC标准204B的规定，以子类1工作。链路建立过程分为以下几步：代码组同步和SYNCINB±、初始通道对齐序列(ILAS)以及用户数据和错误校正。

13.8.8 Code Group Synchronization (CGS) and SYNCINB± / 8.8 代码组同步(CGS)和SYNCINB±

English: CGS is the process by which the JESD204B receiver finds the 10-bit symbol boundaries in the data stream. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must use clock and data recovery (CDR) techniques to locate /K28.5/ characters in the input data stream.

CGS是JESD204B接收机找到数据流中10位符号间界限的过程。在CGS阶段，JESD204B传送模块传送/K28.5/字符。接收机必须使用时钟和数据恢复(CDR)技术，在输入数据流中定位 /K28.5/字符。

English: The receiver drives the SYNCINB± pin of the SXA032 low to issue a synchronization request. The JESD204B Tx then begins transmitting /K/ characters. Once the receiver is synchronized, it waits until the receiver has correctly received at least 4 consecutive /K/ symbols, then deasserts SYNCINB±. The SXA032 then transmits an ILAS at the next local multiframe clock (LMFC) boundary.

接收机将SXA032的SYNCINB±引脚置位低电平，发出一个同步请求。然后，JESD204B Tx 开始发送/K/字符。一旦接收机已同步，它便等待接收机至少正确接收4个连续的/K/符号，然后解除置位SYNCINB±。SXA032接着在下一本地多帧时钟(LMFC)边界发送一个ILAS。

English: SYNCINB± pin operation can also be controlled by SPI. By default, the SYNCINB± signal is a differential LVDS-mode signal, but it can also be driven single-ended.

SYNCINB±引脚操作也可以由SPI控制。默认情况下，SYNCINB±信号是一个差分LVDS模式信号，但也可以单端驱动。

13.8.9 Initial Lane Alignment Sequence (ILAS) / 8.9 初始通道对齐序列(ILAS)

English: The CGS phase is followed by the ILAS phase, which begins at the next LMFC boundary. The ILAS consists of 4 multiframes, with /R/ characters marking the start and /A/ characters marking the end. The ILAS starts by transmitting /R/ characters, then transmits one multiframe of 0-to-255 ramp data. Link configuration data is transmitted in the second multiframe, starting from the third character. The second character is a /Q/ character confirming that link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

CGS阶段之后是ILAS阶段，它在下一LMFC边界开始。ILAS由4个多帧组成，/R/字符表示开始，/A/字符表示结束。ILAS从发送/R/字符开始，然后发送一个多帧的0至255斜坡数据。在第二个多帧发送链路配置数据，从第三个字符开始。第二个字符是/Q/字符，用以确认随后是链路配置数据。所有未定义数据时隙都用斜坡数据填充。ILAS序列从不加扰。

The ILAS sequence structure is shown in Figure 32. The 4 multiframes include: / ILAS序列结构如图32所示。4个多帧包括：

- Multiframe 1, starting with /R/ characters (/K28.0/) and ending with /A/ characters (/K28.3/). / 多帧1，以/R/字符(/K28.0/)开始，以/A/字符(/K28.3/)结束。
- Multiframe 2, starting with /R/ characters, followed by a /Q/ (/K28.4/) character, then 14 octets of link configuration parameters, ending with /A/ characters. Many parameter values are expressed as –1. / 多帧2，以/R/字符开始，接着是/Q/ (/K28.4/)字符，然后是14个配置8位字的链路配置参数，最后以/A/字符结束。许多参数值用–1表示。
- Multiframe 3, starting with /R/ characters (/K28.0/) and ending with /A/ characters (/K28.3/). / 多帧3，以/R/字符(/K28.0/)开始，以/A/字符(/K28.3/)结束。
- Multiframe 4, starting with /R/ characters (/K28.0/) and ending with /A/ characters (/K28.3/). / 多帧4，以/R/字符(/K28.0/)开始，以/A/字符(/K28.3/)结束。

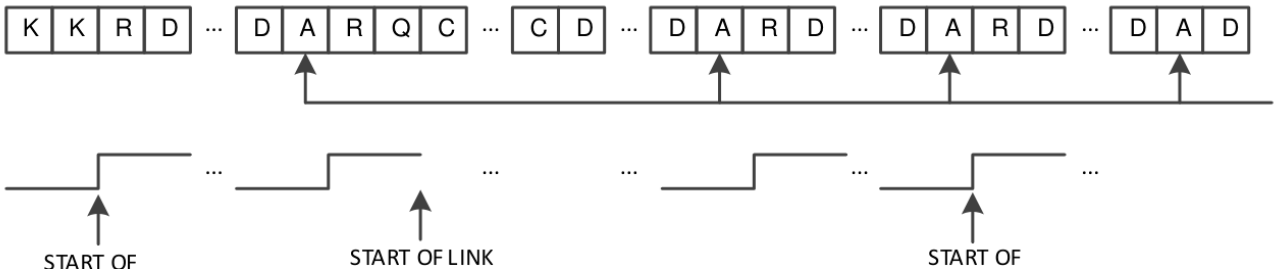


Figure 32: Initial lane alignment sequence

13.8.10 User Data and Error Detection / 8.10 用户数据和错误检测

English: User data is transmitted after the initial lane alignment sequence. Generally, all data within a frame is treated as user data. However, to monitor frame clock and multiframe clock synchronization, there is a mechanism to replace characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions differ for scrambled and unscrambled data. Scrambling is enabled by default but can be disabled via SPI.

完成初始通道对齐序列之后便发送用户数据。一般而言，在一帧以内，所有数据都被视为用户数据。然而，为了监控帧时钟和多帧时钟同步，当数据符合某些条件时，有一个机制来将字符替换为/F/或/A/对齐字符。对于未加扰和加扰的数据，这些条件是不同的。默认使能加扰操作，但可以通过SPI禁用。

English: For scrambled data, any 0xFC character at the end of a frame is replaced with /F/, and any 0xFD character at the end of a multiframe is replaced with /A/. The JESD204B receiver (Rx) checks the received data stream for /F/ and /A/ characters, verifying they appear only at expected positions. If unexpected /F/ or /A/ characters are found, the receiver handles it with dynamic alignment processing, or asserts the SYNCINB± signal for more than four frames to initiate resynchronization. For unscrambled data, if the last characters of two consecutive frames are identical, the second character is replaced with /F/ (if it is at the end of a frame) or /A/ (if it is at the end of a multiframe). Alignment character insertion can be modified via SPI. Frame alignment character insertion (FACI) is enabled by default.

对于加扰的数据，帧末尾的任何0xFC字符都用/F/替换，多帧末尾的任何0xFD字符都用/A/ 替换。JESD204B接收机(Rx)检查接收数据流中有无/F/和/A/字符，验证其仅出现在预期的位置。如果发现意外的/F/或/A/字符，接收机将利用动态对齐处理这种情况，或置位SYNCINB±信号四帧以上以启动重新同步。对于未加扰的数据，如果两个

连续帧的最后字符相同，则第二个字符将被替换为/F/(若它位于一个帧的末尾)或/A/(若它位于一个多帧的末尾)。对齐字符的插入可通过SPI修改。帧对齐字符插入(FACI)默认使能。

13.8.11 8B/10B Encoder / 8.11 8B/10B编码器

The 8B/10B encoder converts 8-bit words into 10-bit symbols and inserts control characters into the stream when needed. The control characters used by JESD204B are shown in Table 13. 8B/10B encoding ensures DC balance of the signal by using an equal number of 1s and 0s across multiple symbols.

8B/10B编码器将8位字转换为10位符号，并在需要时将控制字符插入流中。JESD204B使用的控制字符如表12所示。8B/10B编码通过在多个符号上使用相同数量的1和0来确保信号达到直流平衡。

English: 8B/10B interface options are controllable via SPI, including bypass and inversion. These options serve as troubleshooting tools for digital front-end (DFE) verification.

8B/10B接口的选项可通过SPI控制，包括旁路和反转。这些选项用作数字前端(DFE)验证的故障排除工具。

表13 JESD204B 使用的 ASXA032 控制字符 / Table 13 — SXA032 Control Characters Used by JESD204B

Abbreviation / 缩写	Control Symbol / 控制符号	8-Bit Value / 8位值	10-Bit Value, RD = −1 / 10位值，RD = −1	10-Bit Value, RD = +1 / 10位值，RD = +1	Description / 说明
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Multiframe start / 多帧开始
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment / 通道对齐
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Link configuration data start / 链路配置数据开始
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group sync / 组同步
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment / 帧对齐

9、数字输出、时序和控制 / 13.9 Digital Output, Timing and Control

English: The SXA032 physical layer consists of drivers specified by JEDEC Standard 204B (July 2011). The differential digital outputs are powered up by default. Each driver uses a 100 Ω dynamic internal termination resistor to reduce reflections. Placing a 100 Ω differential termination resistor at each receiver input achieves a nominal 300 mV p-p receiver swing. Single-ended 50 Ω termination resistors can also be used. With single-ended termination, the termination voltage is DRVDD/2; in addition, 0.1 µF AC-coupling capacitors can be used for termination to any single-ended voltage.

SXA032 物理层由JEDEC标准204B(2011年7月)所规定的驱动器组成。差分数字输出默认上电。每个驱动器利用100Ω的动态内部端接电阻来降低反射干扰。在每个接收机的输入端放置一个100Ω差分端接电阻，可实现标称300 mV p-p的接收机摆幅。也可使用单端50Ω端接电阻。使用单端端接电阻时，端接电压DRVDD/2，此外，还可使用0.1µF交流耦合电容以便端接至任意单端电压。

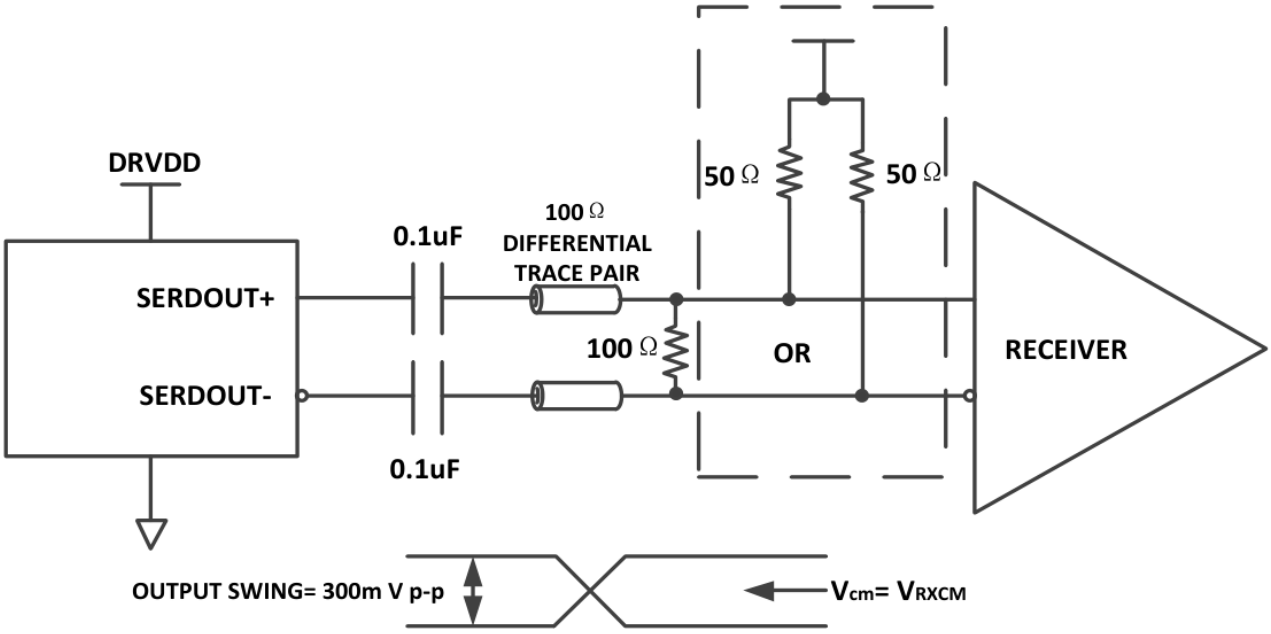


Figure 33: AC-coupled digital output termination example

English: The SXA032 digital outputs can interface with custom ASICs and FPGA receivers for excellent switching performance in high-noise environments. A single point-to-point network topology is recommended, with a single 100 Ω differential termination resistor placed as close as possible to the receiver input. The common-mode voltage of the digital outputs is automatically biased to half of the 1.2 V DRVDD supply (VCM = 0.6 V). Figure 34 shows the output DC-coupled to receiver logic.

SXA032 数字输出可与定制的ASIC和FPGA接收机接口，从而在高噪声环境中实现出色的开关性能。推荐使用单一点到点网络拓扑结构，并将单个100Ω差分端接电阻尽可能靠近接收机输入端放置。数字输出的共模电压自动偏置到1.2 V DRVDD电源的一半(VCM= 0.6 V)。图34显示输出直流耦合到接收机逻辑。

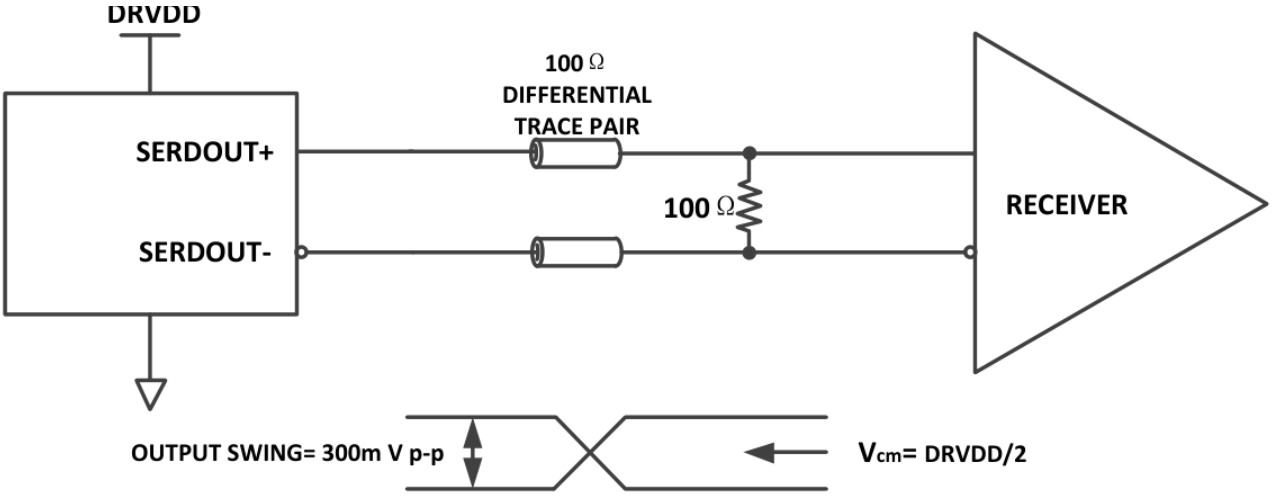


Figure 34: DC-coupled digital output termination example

English: If there is no far-end receiver termination resistor, or if differential trace routing is poor, timing errors may result. To avoid timing errors, trace lengths should not exceed 6 inches, and differential output traces should be routed as close to each other as possible with equal lengths.

中文： 如果没有远端接收机端接电阻，或者差分走线布线不佳，可能会导致时序错误。为避免产生时序错误，建议走线长度不要超过6英寸，差分输出走线应尽可能彼此靠近且长度相等。

13.9.1 De-emphasis / 9.1 去加重

English: When interconnect insertion loss does not meet the JESD204B specification, de-emphasis can be used to meet the receiver eye-diagram mask. The de-emphasis feature should only be used when the receiver cannot recover the clock due to excessive insertion loss. Generally, this feature is disabled to save power. Enabling and setting an excessively high de-emphasis value on a short link may cause receiver eye-diagram failure. De-emphasis settings should be used with caution because they increase electromagnetic interference (EMI).

当互连插入损耗不符合JESD204B规范时，利用去加重可以符合接收机眼图眼罩。只能在接收机因为插入损耗过大而无法恢复时钟时使用去加重特性。一般情况下，该特性禁用以节省功耗。此外，对一个短链路使能并设置过高的去加重值，可能导致接收机眼图失效。去加重设置应慎重使用，因为它会增加电磁干扰(EMI)。

13.9.2 Phase-Locked Loop / 9.2 锁相环

English: The phase-locked loop (PLL) generates the serializer clock, which operates at the JESD204B lane rate. PLL lock status can be checked via the PLL lock status bit (register 0x56F bit 7). This read-only bit tells the user whether PLL lock has been achieved for a given setting. The JESD204B lane rate control (register 0x56E bit 4) setting must correspond to the lane rate.

锁相环(PLL)用于产生串行器时钟，它以JESD204B通道速率工作。PLL锁定的状态可通过 PLL锁定状态位(寄存器0x56F的位7)来检查。此只读位告知用户特定设置是否实现了PLL锁定。JESD204B通道速率控制(寄存器0x56E的位4)的设置必须与通道速率对应。

13.9.3 JESD204B Tx Converter Mapping / 9.3 JESD204B Tx转换器映射

English: To support different chip operating modes, the SXA032 design treats each sample stream (real or I/Q) as coming from a different virtual converter. I/Q samples are always mapped in pairs, with I samples mapped to the first virtual converter and Q samples mapped to the second virtual converter. With this transport-layer mapping, the number of virtual converters is the same in the following cases:

为了支持不同的芯片工作模式，SXA032设计将每个样本流(实数或I/Q)视为来自不同的虚拟转换器。I/Q样本始终成对映射，I样本映射到第一个虚拟转换器，Q样本映射到第二个虚拟转换器。采用这种传输层映射，以下各种情况下的虚拟转换器数量相同：

- Using a single real converter and one digital downconverter block to produce I/Q output; / 使用单个实数转换器和一个数字下变频器模块来产生I/Q输出；
- Or using one analog downconverter and two real converters to produce I/Q output. / 或使用一个模拟下变频器和两个实数转换器来产生I/Q输出。

English: Figure 35 shows the I/Q transport-layer mapping block diagram for both cases above.

中文： 图35显示了上述两种情况下I/Q传输层映射的框图。

English: The SXA032 JESD204B Tx block supports up to 4 DDC blocks. Each DDC block outputs either two sample streams (I/Q) of complex data components (real + imaginary), or one sample stream of real (I)

data. Depending on the DDC configuration, the JESD204B interface can use up to 8 virtual converters. Figure 36 shows the virtual converters and their relationship to DDC outputs when using complex output. Table 14 gives the virtual converter mapping for various chip operating modes when lane mapping is disabled.

SXA032 的JESD204B Tx模块最多支持4个DDC模块。每个DDC模块要么输出复数数据分量 (实部+虚部)的两个样本流(I/Q)，要么输出实数(I)数据的一个样本流。根据DDC配置，JESD204B 接口最多可以使用8个虚拟转换器。图36显示了虚拟转换器及使用复数输出时其与DDC输出的关系。表14给出了通道映射禁用时各种芯片工作模式的虚拟转换器映射。

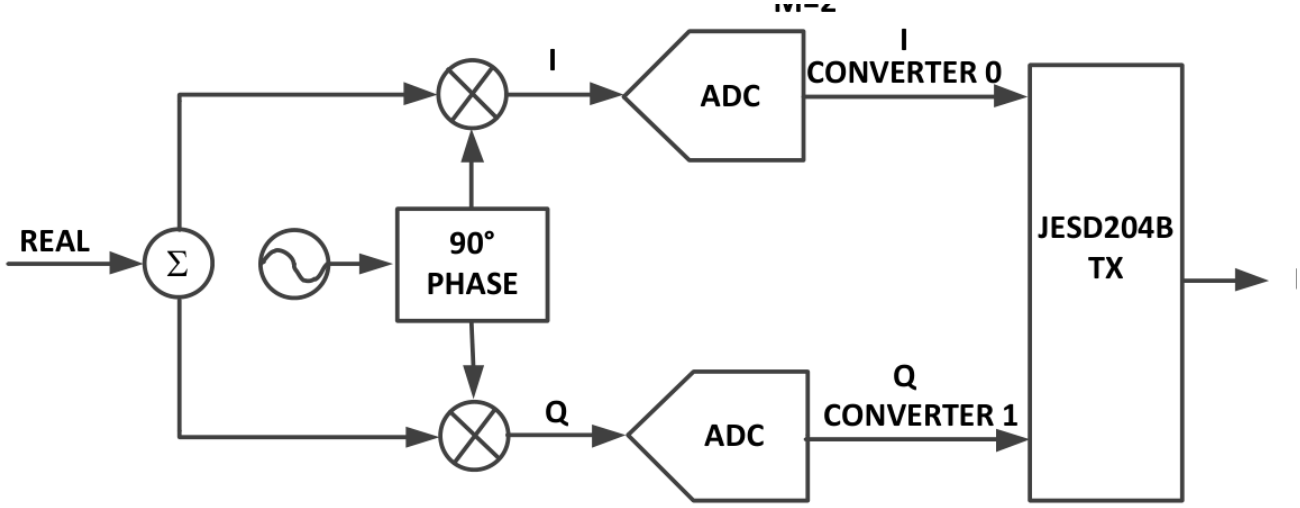


Figure 35: I/Q transport-layer mapping

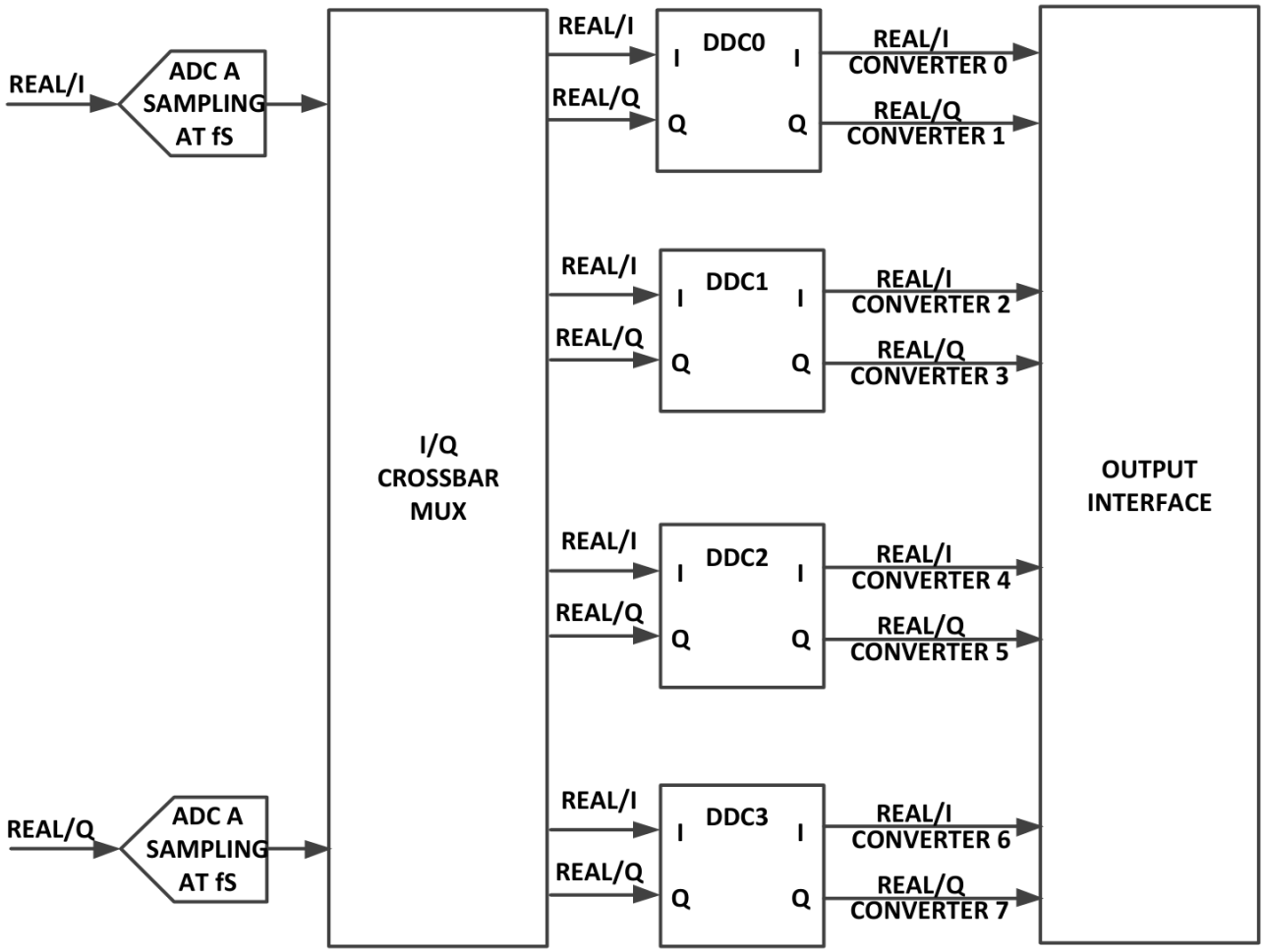


Figure 36: DDC to virtual converter mapping

表14 虚拟转换器映射 / Table 14 — Virtual Converter Mapping

Supported Virtual Converters / 支持的虚拟转换器数	Chip Mode (0x200[1:0]) / 模式	Chip Q Ignore (0x200, Bit 5) / 芯片 Q 忽略(0x200, Bit 5)	Virtual Converter Mapping: 0 / 虚拟转换器映射	1	2	3	4	5	6	7
1–2	Full-bandwidth mode (0x0) / 全带宽模式(0x0)	Real or complex (0x0) / 实数或复数(0x0)	ADC A sample / ADC A 样本	ADC B sample / ADC B 样本	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用		
1	1 DDC mode (0x1) / 1 个 DDC 模式 (0x1)	Real (I only) (0x1) / 实数（仅 I）(0x1)	DDC0 I sample / DDC0 I 样本	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用		
2	1 DDC mode (0x1) / 1 个 DDC 模式(0x1)	Complex (I/Q) (0x0) / 复数 (I/Q)(0x0)	DDC0 I sample / DDC0 I 样本	DDC0 Q sample / DDC0 Q 样本	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	
2	2 DDC modes (0x2) / 2 个 DDC 模式(0x2)	Real (I only) (0x1) / 实数（仅 I）(0x1)	DDC0 I sample / DDC0 I 样本	DDC1 I sample / DDC1 I 样本	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	
4	2 DDC modes (0x2) / 2 个 DDC 模式(0x2)	Complex (I/Q) (0x0) / 复数 (I/Q)(0x0)	DDC0 I sample / DDC0 I 样本	DDC0 Q sample / DDC0 Q 样本	DDC1 I sample / DDC1 I 样本	DDC1 Q sample / DDC1 Q 样本	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	
4	4 DDC modes (0x3) / 4 个 DDC 模式(0x3)	Real (I only) (0x1) / 实数（仅 I）(0x1)	DDC0 I sample / DDC0 I 样本	DDC1 I sample / DDC1 I 样本	DDC2 I sample / DDC2 I 样本	DDC3 I sample / DDC3 I 样本	Unused / 未用	Unused / 未用	Unused / 未用	Unused / 未用	
8	4 DDC modes (0x3) / 4 个 DDC 模式(0x3)	Complex (I/Q) (0x0) / 复数 (I/Q)(0x0)	DDC0 I sample / DDC0 I 样本	DDC0 Q sample / DDC0 Q 样本	DDC1 I sample / DDC1 I 样本	DDC1 Q sample / DDC1

Q 样本 | DDC2 I sample / DDC2 I 样本 | DDC2 Q sample / DDC2 Q 样本 | DDC3 I sample / DDC3 I 样本 | DDC3 Q sample / DDC3 Q 样本 |

13.9.4 Configuring the JESD204B Link / 9.4 配置JESD204B链路

The SXA032 has one JESD204B link. The JESD204B link is easily set up via the JESD204B quick-configuration register (register 0x570). The serial outputs (SERDOUT0± to SERDOUT3±) are part of one JESD204B link. The basic parameters determining the link setup include:

SXA032 有一个JESD204B链路。通过JESD04B快速配置寄存器(寄存器0x570)很容易设置 JESD204B链路。串行输出(SERDOUT0±至SERDOUT3±)是一个JESD204B链路的一部分。决定链路设置的基本参数包括：

- Number of data lanes per link (L) / 每链路的数据通路数(L)
- Number of converters per link (M) / 每链路的转换器数(M)
- Number of octets per frame (F) / 每帧的8位字数(F)

English: If internal DDCs are used for on-chip digital processing, M represents the number of virtual converters. The virtual converter mapping is shown in Figure 36.

如果内部DDC用于片内数字处理，则M代表虚拟转换器的数量。虚拟转换器映射设置如图 36所示。

English: The JESD204B specification supports a maximum lane rate of 12.5 Gbps. The lane line rate relates to the JESD204B parameters as:

JESD204B 规范支持的最大通道速率为12.5 Gbps。通路线速率与JESD204B参数有如下关系：

English: $\text{LaneLineRate} = M \times N' \times (10/8) \times fOUT / L$

where: / 其中：

English: $fOUT = fADC_CLOCK / DecimationRatio$

English: The decimation ratio (DCM) is the parameter written to register 0x201. The output can be configured with the following steps:

抽取比(DCM)是写入寄存器0x201的参数。可以使用下面的步骤来配置输出：

1. Turn off the link. / 关断链路。
2. Select the quick-configuration option. / 选择快速配置选项。
3. Configure the detailed options. / 配置详细选项。
4. Set the output lane mapping (optional). / 设置输出通道映射(可选)。
5. Set other driver configuration options (optional). / 设置其他驱动器配置选项(可选)。
6. Power up the link. / 链路上电。

English: If the calculated lane line rate is below 6.25 Gbps, select the low-line-rate option, i.e., write 0x10 to register 0x56E. Tables 15 and 16 show the supported JESD204B output configurations for $N' = 16$ and $N' = 8$ given the number of virtual converters. The serial line rate for a given configuration must be within the supported range of 3.125 Gbps to 12.5 Gbps.

如果计算的通道线速率低于6.25 Gbps，应选择低线速率选项，也就是将值0x10写入寄存器 0x56E。表15和表16显示了给定虚拟转换器数量时N′ = 16和N′ = 8支持的JESD204B输出配置。必须确保给定配置的串行线速率在支持的范围3.125 Gbps至12.5 Gbps以内。

表15 N′=16 对应的 JESD204B 输出配置 / Table 15 — JESD204B Output Configurations for N′ = 16

Supported Virtual Converters (M) / 支持的虚拟转换器数(同 M 值)	JESD204B Quick Config (0x570) / JESD204B 快速配置 (0x570)	JESD204B Serial Line Rate / JESD204B 串行线速率	L	M	F	S	HD	N	N′	CS	K
1	0x01	20 × fout	1	1	2	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	Valid K divisible by 4 only / 仅支持能被 4 整除的有效 K 值
	0x40	10 × fout	2	1	1	1	1	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x41	10 × fout	2	1	2	2	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x80	5 × fout	4	1	1	2	1	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x81	5 × fout	4	1	2	4	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
2	0x0A	40 × fout	1	2	4	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x49	20 × fout	2	2	2	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x88	10 × fout	4	2	1	1	1	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x89	10 × fout	4	2	2	2	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
4	0x13	80 × fout	1	4	8	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x52	40 × fout	2	4	4	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x91	20 × fout	4	4	2	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	

Supported Virtual Converters (M) / 支持的虚拟转换器数(同 M 值)	JESD204B Quick Config (0x570) / JESD204B 快速配置 (0x570)	JESD204B Serial Line Rate / JESD204B 串行线速率	L	M	F	S	HD	N	N′	CS	K
8	0x1C	160 × fout	1	8	16	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x5B	80 × fout	2	8	8	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	
	0x9A	40 × fout	4	8	4	1	0	8 to 16 / 8 至 16	16	0 to 3 / 0 至3	

Notes / 备注： 1. fOUT = output sample rate = ADC sample rate / chip decimation ratio. The JESD204B serial line rate must be ⩾ 3125 Mbps and ⩽ 12,500 Mbps; when the serial line rate is ⩽ 12.5 Gbps and ⩾ 6.25 Gbps, the low-line-rate mode must be disabled (set bit 4 of 0x56E to 0x0). When the serial line rate is < 6.25 Gbps and ⩾ 3.125 Gbps, the low-line-rate mode must be enabled (set bit 4 of 0x56E to 0x1). fOUT = 输出采样速率 = ADC 采样速率/芯片抽取比。JESD204B 串行线速率必须≥3125 Mbps 且≤12,500 Mbps；当串行线速率≤12.5 Gbps 且≥ 6.25 Gbps 时，必须禁用低线速率模式(将 0x56E 的位 4 设为 0x0)。当串行线速率<6.25 Gbps 且≥3.125 Gbps，必须使能低线速率模式(将 0x56E 的位 4 设为 0x1)。 2. See the "JESD204B Overview" section for the JESD204B transport-layer description. / JESD204B 传输层说明参见"JESD204B 概述"部分。 3. For F = 1, K = 20, 24, 28 and 32. For F = 2, K = 12, 16, 20, 24, 28 and 32. For F = 4, K = 8, 12, 16, 20, 24, 28 and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28 and 32. 对于 F = 1，K = 20、24、28 和 32。对于 F = 2，K = 12、16、20、24、28 和 32。对于 F = 4，K = 8、12、16、20、24、28 和 32。对于 F = 8 和 F = 16，K = 4、8、12、16、20、24、28 和 32。

表16 N′=8 对应的 JESD204B 输出配置 / Table 16 — JESD204B Output Configurations for N′ = 8

Supported Virtual Converters (M) / 支持的虚拟转换器数(同 M 值)	JESD204B Quick Config (0x570) / JESD204B 快速配置 (0x570)	JESD204B Serial Line Rate / JESD204B 串行线速率	L	M	F	S	HD	N	N′	CS	K
1	0x00	10 × fout	1	1	1	1	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	Valid K divisible by 4 only / 仅支持能被 4 整除的有效 K 值
	0x01	10 × fout	1	1	2	2	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x40	5 × fout	2	1	1	2	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x41	5 × fout	2	1	2	4	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x42	5 × fout	2	1	4	8	0		8		

Supported Virtual Converters (M) / 支持的虚拟转换器数(同 M 值)	JESD204B Quick Config (0x570) / JESD204B 快速配置 (0x570)	JESD204B Serial Line Rate / JESD204B 串行线速率	L	M	F	S	HD	N	N′	CS	K
								7 to 8 / 7 至8		0 to 1 / 0 至1	
	0x80	2.5 × fout	4	1	1	4	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x81	2.5 × fout	4	1	2	8	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
2	0x09	20 × fout	1	2	2	1	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x48	10 × fout	2	2	1	1	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x49	10 × fout	2	2	2	2	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x88	5 × fout	4	2	1	2	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x89	5 × fout	4	2	2	4	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	
	0x8A	5 × fout	4	2	4	8	0	7 to 8 / 7 至8	8	0 to 1 / 0 至1	

Notes / 备注： 1. fOUT = output sample rate = ADC sample rate / chip decimation ratio. The JESD204B serial line rate must be ≥ 3125 Mbps and ≤ 12,500 Mbps; when the serial line rate is ≤ 12.5 Gbps and ≥ 6.25 Gbps, the low-line-rate mode must be disabled (set bit 4 of register 0x56E to 0x0). When the serial line rate is < 6.25 Gbps and ≥ 3.125 Gbps, the low-line-rate mode must be enabled (set bit 4 of register 0x56E to 0x1). fOUT = 输出采样速率 = ADC 采样速率/芯片抽取比。JESD204B 串行线速率必须≥3125 Mbps 且≤12,500 Mbps；当串行线速率≤12.5 Gbps 且≥ 6.25 Gbps 时，必须禁用低线速率模式(将寄存器 0x56E 的位 4 设为 0x0)。当串行线速率<6.25 Gbps 且≥3.125 Gbps，必须使能低线速率模式(将寄存器 0x56E 的位 4 设为 0x1)。 2. See the "JESD204B Overview" section for the JESD204B transport-layer description. / JESD204B 传输层说明参见"JESD204B 概述"部分。 3. For F = 1, K = 20, 24, 28 and 32. For F = 2, K = 12, 16, 20, 24, 28 and 32. For F = 4, K = 8, 12, 16, 20, 24, 28 and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28 and 32. 对于 F = 1，K = 20、24、28 和 32。对于 F = 2，K = 12、16、20、24、28 和 32。对于 F = 4，K = 8、12、16、20、24、28 和 32。对于 F = 8 和 F = 16，K = 4、8、12、16、20、24、28 和 32。

English: For which JESD204B transport-layer settings are valid for a given chip mode, see the following two examples: "Example 1: Full-Bandwidth Mode" and "Example 2: ADC with DDC Option (2 ADCs plus 4 DDCs)".

关于哪些JESD204B传输层设置对给定的芯片模式有效，请参见以下两个例子："示例1：全带宽模式"和"示例2：带DDC选项的ADC(2个ADC加4个DDC)"。

Example 1: Full-Bandwidth Mode / 示例1：全带宽模式

English: Chip application mode = full-bandwidth mode (see Figure 37).

中文： 芯片应用模式 = 全带宽模式(参见图37)。

- 2 14-bit converters operating at 1000 MSPS / 2个14位转换器以1000 MSPS速率工作
- Full-bandwidth application-layer mode / 全带宽应用层模式
- No decimation / 无抽取

JESD204B output configuration: / JESD204B输出配置：

- 2 virtual converters required / 需要2个虚拟转换器
- Output sample rate (fOUT) = 1000/1 = 1000 MSPS / 输出采样速率(fOUT) = 1000/1 = 1000 MSPS

Supported JESD204B output configurations include: / JESD204B支持的输出配置包括：

- N′ = 16 bits / N′ = 16位
- N = 14 bits / N = 14位
- L = 4, M = 2, F = 1, or L = 4, M = 2, F = 2 (quick config = 0x80 or 0x81) / L = 4、M = 2、F = 1，或L = 4、M = 2、F = 2(快速配置= 0x80或0x81)
- CS = 0 to 2 / CS = 0至2
- K = 32 / K = 32
- Output serial line rate = 10 Gbps per lane, low-line-rate mode disabled / 输出串行线速率 = 每通道10 Gbps，禁用低线速率模式

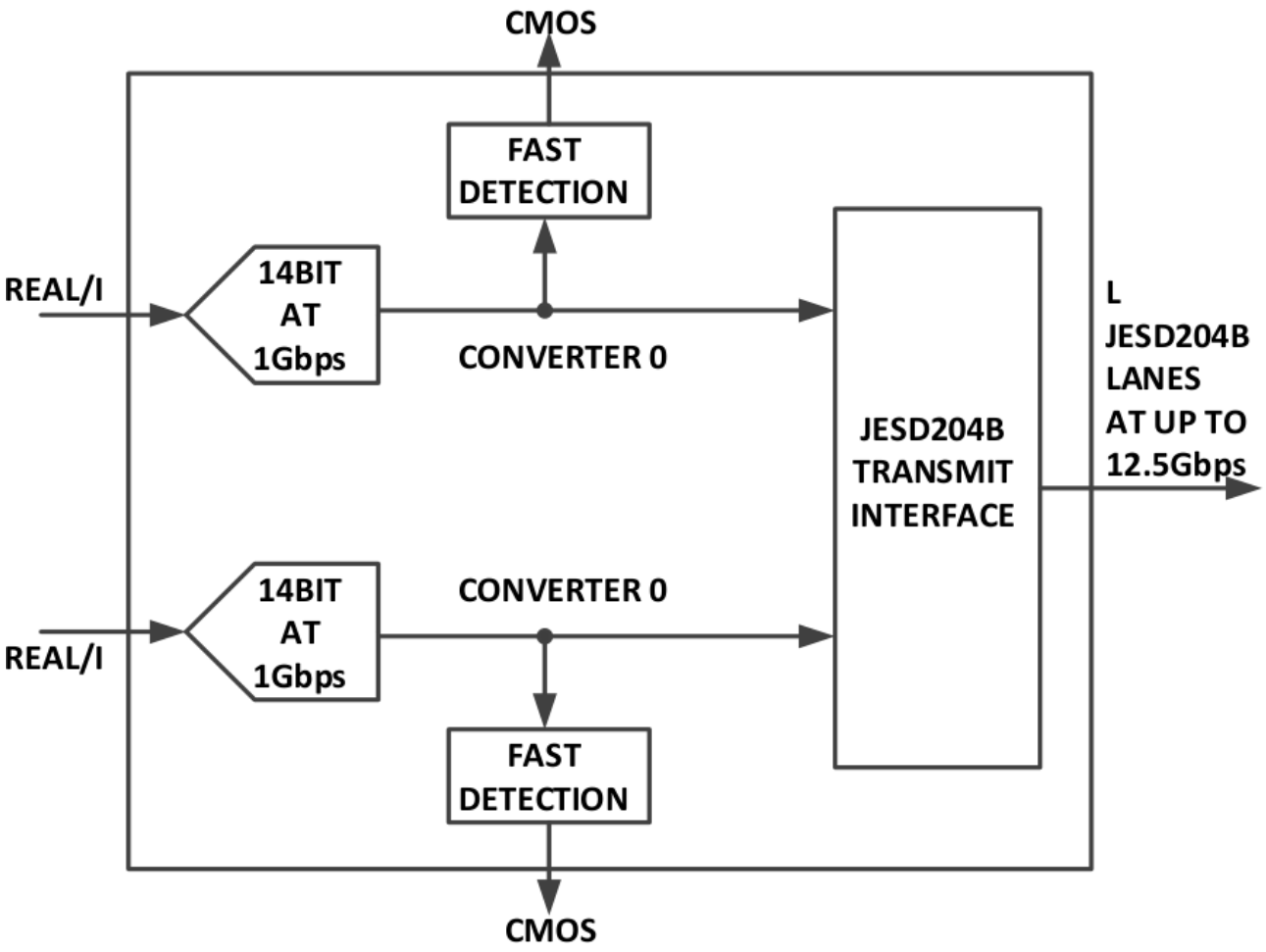


Figure 37: Full-bandwidth mode

Example 2: ADC with DDC Option (2 ADCs plus 4 DDCs) / 示例2：带DDC选项的ADC(2个ADC加4个DDC)

English: Chip application mode = 4-DDC mode (see Figure 38).

芯片应用模式 = 4 DDC模式。(参见图38)。

- 2 14-bit converters operating at 1 MSPS / 2个14位转换器以1 MSPS速率工作
- 4-DDC application-layer mode, complex output (I/Q) / 4个DDC应用层模式，复数输出(I/Q)
- Chip decimation ratio = 16 / 芯片抽取比 = 16
- DDC decimation ratio = 16 / DDC抽取比 = 16

JESD204B output configuration: / JESD204B输出配置：

- 8 virtual converters required / 需要8个虚拟转换器
- Output sample rate (fOUT) = 1000/16 = 62.5 MSPS / 输出采样速率(fOUT) = 1000/16 = 62.5 MSPS

Supported JESD204B output configurations: / JESD204B支持的输出配置：

- N′ = 16 bits / N′ = 16位
- N = 14 bits / N = 14位
- L = 1, M = 8, F = 16, or L = 2, M = 8, F = 8 (quick config = 0x1C or 0x5B) / L = 1、M = 8、F = 16，或L = 2、M = 8、F = 8(快速配置= 0x1C或0x5B)
- CS = 0 to 1 / CS = 0至1

- K = 32 / K = 32
- Output serial line rate = 10 Gbps per lane (L = 1) or 5 Gbps per lane (L = 2). For L = 1, disable low-line-rate mode. For L = 2, enable low-line-rate mode. / 输出串行线速率 = 每通道10 Gbps (L = 1)或每通道5 Gbps (L = 2)。对于L = 1，禁用低线速率模式。对于L = 2，使能低线速率模式。

English: Example 2 demonstrates the digital and lane configuration flexibility of the SXA032. The sample rate is 1 GSPS, but depending on the I/O speed capability of the receiving device, the outputs are combined into one or two lanes.

示例2显示了SXA032数字和通道配置的灵活性。采样速率为1 GSPS，但根据接收器件的I/O 速度能力，输出都合并到一个或两个通道中。

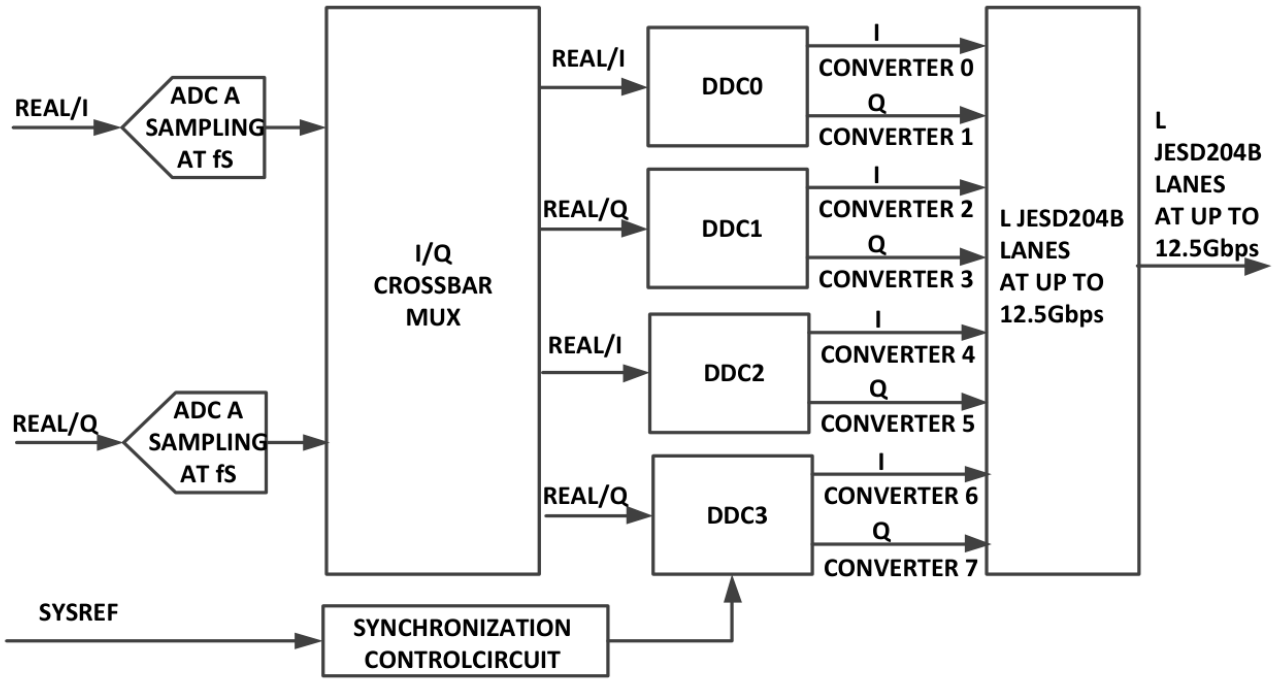


Figure 38: 2 ADCs plus 4 DDCs mode

14. 寄存器 / Registers

English: All address locations not included in Table 17 are currently not supported by this device and should not be written.

中文： 此器件目前不支持表17中未包括的所有地址位置，不应写入这些位置。

表17 存储器映射寄存器 / Table 17 — Memory-Mapped Registers

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
0x000	INTERFACE_CONFIG_A		LSB first: 0 = MSB, 1 =		0	0		LSB first: MSB, 1 =

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		Soft reset (self-clearing) / 软复位(自清零)	LSB / LSB 优先: 0 = MSB, 1 = LSB	Address ascending / 地址上升			Address ascending / 地址上升	LSB 优先 MSB, 1 =
0x001	INTERFACE_CONFIG_B	Single instruction / 单指令	0	0	0	0	0	Data pat reset (se clearing) 据路径软 (自清零)
0x002	DEVICE_CONFIG (local / 局部)	0	0	0	0	0	0	00 = nor operatio = 正常工 = standb = 待机; 1 power-d 11 = 掉电
0x003	CHIP_TYPE	0011 = high-speed ADC / 0011 = 高速 ADC						
0x004	CHIP_ID (low byte / 低字节)	1	1	0	0	1	0	0
0x005	CHIP_ID (high byte / 高字节)	0	0	0	0	0	0	0
0x006	CHIP_GRADE	1100 = 1250 MSPS; 1010 = 1000 MSPS; 1000 = 820 MSPS; 0101 = 500 MSPS				X	X	X
0x008	Device index	0	0	0	0	0	0	Channel
0x00A	Scratch pad	0	0	0	0	0	0	0
0x00B	SPI revision	0	0	0	0	0	0	0
0x00C	Vendor ID (low byte / 低字节)	0	1	0	1	0	1	1
0x00D	Vendor ID (high byte / 高字节)	0	0	0	0	0	0	1
0x015	Analog Input (local / 局部)	0	0	0	0	0	0	0
0x016								

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
	Input termination (local / 局部)	Analog input differential termination / 模拟输入差分端接: 0000 = 400 Ω; 0001 = 200 Ω; 0010 = 100 Ω; 0110 = 50 Ω				1110 = SXA032-1250 and SXA032-1000; 1100 = SXA032-820 and SXA032-500		
0x934	Input capacitance (local / 局部)	0	0	0	0x1F = 3 pF to GND (default); 0x00 = 1.5 pF to GND / 0x1F = 3 pF to GND (默认); 0x00 = 1.5 pF to GND			
0x018	input buffer current control (local / 局部)	0000 = 1.0× buffer current (default / 默认); 0001 = 1.5×; 0010 = 2.0×; 0011 = 2.5×; 0100 = 3.0×; 0101 = 3.5×; …; 1111 = 8.5× buffer current / 缓冲电流				0	0	0
0x019	input buffer Control 1 (local / 局部)	0100 = setting 1 (default for SXA032-820); 0101 = setting 2 (default for SXA032-1250 and SXA032-1000); 0110 = setting 3 (default for SXA032-500); 0111 = setting 4 / 设置				0	0	0
0x01A	input buffer Control 2 (local / 局部)	0	0	0	0	1000 = setting 1; 1001 = setting 2 (default for SXA032-1250, SXA032-1000 and SXA032-820); 1010 = setting		

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
						3 (default for SXA032-500) / 设置		
0x11A	input buffer Control 3 (local / 局部)	0	0	High-frequency setting: 0 = off (default), 1 = on / 高频设置: 0 = off (默认), 1 = on	0	0	0	0
0x935	input buffer Control 4 (local / 局部)	0	0	0	0	0	Low-frequency setting: 0 = off, 1 = on (default) / 低频设置: 0 = off, 1 = on (默认)	0
0x024	V_1P0 control	0	0	0	0	0	0	0
0x025	Input fullscale range (local / 局部)	0	0	0	0	Full-scale adjust / 满量程调整: 0000 = 1.94 V; 1000 = 1.46 V; 1001 = 1.58 V; 1010 = 1.70 V; 1011 = 1.82 V		
0x028	Temperature diode	0	0	0	0	0	0	0
0x030	input fullscale control (local / 局部)	0	0	0	Full-scale control / 满量程控制: 10 = 1.82 to 1.94 V;		0	0

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
					11 = 1.46 to 1.70 V			
0x03F	PDWN/STBY pin control (local / 局部)	0 = PDWN/STBY enabled; 1 = disabled / 0 = PDWN/STBY 使能; 1 = 禁用	0	0	0	0	0	0
0x040	Chip pin control	PDWN/STBY function: 00 = power-down, 01 = standby, 10 = disabled / PDWN/STBY 功能: 00 = 掉电, 01 = 待机, 10 = 禁用		Fast detect B (FD_B): 000 = FD_B output; 001 = JESD204B LMFC output; 010 = JESD204B internal SYNC~ output; 111 = disabled / 快速检测 B (FD_B): 000 = 快速检测 B 输出; 001 = JESD204B LMFC 输出; 010 = JESD204B 内部 SYNC~ 输出; 111 = 禁用			Fast detect A (FD_A): 000 = FD_A output; 001 = JESD204B LMFC output; 010 = JESD204B internal SYNC~ output; 011 = temperature diode; 111 = disabled / 快速检测 A (FD_A): 000 = 快速检测 A 输出; 001 = JESD204B LMFC 输出; 010 = JESD204B 内部 SYNC~ 输出; 011 = 温度二极管; 111 = 禁用	
0x10B	Clock divider	0	0	0	0	0	000 = divide by 1; 001 = divide by 2; 011 = divide by 4; 111 = divide by 8 / 000 = 1 分频; 001 = 2 分频; 011 = 4 分频; 111 = 8 分频	
0x10C	Clock divider phase (local / 局部)	0	0	0	Independent control of channel A and B clock divider phase shift / 独立控			

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
					制通道 A 和通道 B 时钟分频器相位偏移: 0000 = 0 input clock cycle delay; 0001 = ½ input clock cycle delay; 0010 = 1 input clock cycle delay; 0011 = 1½ input clock cycle delays; 0100 = 2 input clock cycle delays; 0101 = 2½ input clock cycle delays; …; 1111 = 7½ input clock cycle delays / 0000 = 0 输入时钟周期延迟; 0001 = ½输入时钟周期延迟; 0010 = 1 输入时钟周期延迟; 0011 = 1½输入时钟周期延迟; 0100 = 2 输入时钟周期延迟; 0101 = 2½输入时钟周期延迟; …; 1111 = 7½输入时钟周期延迟			
0x10D	Clock divider and SYSREF control	Clock divider auto phase adjust: 0 = disabled, 1 = enabled / 时钟分频器自动相位调节: 0 = disabled, 1 = enabled	Clock divider negative skew window / 时钟分频器负 skew 窗口: 00 = no negative skew; 01 = 1 device clock of negative skew; 10 = 2		Clock divider positive skew window / 时钟分频器正 skew 窗口: 00 = no positive skew; 01 = 1 device clock of positive skew; 10 = 2 device clocks		0x00	Clock div must be

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
			device clocks of negative skew; 11 = 3 device clocks of negative skew		of positive skew; 11 = 3 device clocks of positive skew			
0x117	Clock delay Control	0	0	0	0	0	0	0
0x118	Clock fine delay (local / 局部)	Clock fine delay adjust register [7:0], two's complement, 1.7 ps step / 时钟精细延迟调节寄存器[7:0]，补码调节，调节步长 1.7ps: ⩽ −88 = −151.7 ps; −87 = −150 ps; …; 0 = 0 ps; …; ⩾ +87 = +150 ps						
0x11C	Clock status	0	0	0	0	0	0	0
0x120	SYSREF± Control 1	0	SYSREF± flag reset: 0 = normal operation, 1 = flag hold reset; bit status / SYSREF± 标志复位: 0 = 正常工作, 1 = 标志保持复位; 位状态	0	SYSREF± transition select: 0 = low-to-high, 1 = high-to-low / SYSREF± 跃迁选择: 0 = 低至高, 1 = 高至低	CLK± edge select: 0 = rising, 1 = falling / CLK± 边沿选择: 0 = 上升, 1 = 下降	SYSREF± mode select: 00 = disabled; 01 = continuous; 10 = N-shot / SYSREF± 模式选择: 00 = 禁用; 01 = 连续; 10 = N 次	

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
0x121	SYSREF± Control 2	SYSREF N-shot ignore counter select / SYSREF N-次忽略计数器选择: 0000 = next SYSREF± only; 0001 = ignore first SYSREF± transition; 0010 = ignore first two SYSREF± transitions; …; 1111 = ignore first 16 SYSREF± transitions / 0000 = 仅下一 SYSREF±; 0001 = 忽略第一次 SYSREF± 跃迁; 0010 = 忽略前两次 SYSREF± 跃迁; ⋯; 1111 = 忽略前 16 次 SYSREF± 跃迁						
0x123	SYSREF± timestamp delay	SYSREF± timestamp delay, bits [6:0] / SYSREF± 时间戳延迟: 0x00 = no delay; 0x01 = 1 clock delay; …; 0x7F = 127 clocks delay						
0x128	SYSREF± Status 1	SYSREF± hold status, register 0x128[7:4], refer to Table 29 / SYSREF±hold status, Register 0x128[7:4], refer to 表 29				SYSREF± setup status, register 0x128[3:0], refer to Table 29 / SYSREF± setup status, Register 0x128[3:0], refer to 表 29		
0x129	SYSREF± and clock divider status	Clock divider phase captured at SYSREF± / 捕						

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		捉到 SYSREF± 时的时钟分频器相位: 0000 = in phase; 0001 = SYSREF± delayed ½ cycle relative to clock; 0010 = SYSREF± delayed 1 cycle relative to clock; 0011 = 1½ input clock cycle delay; 0100 = 2 input clock cycle delay; 0101 = 2½ input clock cycle delay; …; 1111 = 7½ input clock cycle delay / 0000 = 同相; 0001 = SYSREF±相对于时钟延迟½周期; 0010 = SYSREF±相对于时钟延迟 1 周期; 0011 = 1½输入时钟周期延迟; 0100 = 2 输入时钟周期延迟; 0101 = 2½输入时钟周期延迟; …; 1111 = 7½输入时钟周期延迟						
0x12A	SYSREF± counter	SYSREF counter, increments bits [7:0] when SYSREF± is captured / SYSREF 计数器，捕捉到 SYSREF± 时位[7:0]递增						
0x1FF	Chip sync mode	Synchronization mode / Synchronization mode: 00 =						

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		normal; 01 = timestamp						
0x200	Chip application mode	0	0	Chip Q ignore: 0 = normal (I/Q), 1 = ignore (I only) / 芯片 Q 忽略: 0 = 正常 (I/Q), 1 = 忽略 (仅 I)	0	0	0	Chip operatin mode / 芯 作模式: 0 full-bandwid mode / 全 模式; 01 = DDC 0 enabled DDC 0 开 10 = DDC and DDC enabled DDC 0 和 1 开启; 1 DDC 0, D DDC 2 ar DDC 3 enabled DDC 0、 1、DDC DDC 3 开
0x201	Chip decimation ratio	0	0	0	0	0	Chip decimation ratio select / 芯片抽取比选择: 000 = full sample rate (decimation = 1) / 全采样速率 (抽取比= 1); 001 = 2× decimation / 2 倍抽取; 010 = 4× decimation / 4 倍抽取; 011 = 8× decimation / 8 倍抽取; 100 = 16× decimation / 16 倍抽取	
0x228	Customer offset	Offset adjust in LSBs, from +127 to −128 (two's						

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		complement) / 失调调整以 LSB 为单位，从+127 到−128(二进制补码格式)						
0x245	Fast detect (FD) control (local / 局部)	0	0	0	0	Force FD_A/ FD_B pins: 0 = normal operation, 1 = force pins / 强制 FD_A / FD_B 引脚: 0 = 正常工作; 1 = 强制引脚	Force FD_A/ FD_B pin value; if pin is forced true, FD pin outputs this value / 强制 FD_A/FD_B 引脚数值；若强制引脚为真值，则 FD 引脚输出该数值	
0x247	FD upper threshold LSB (local / 局部)	Fast detect upper threshold, bits [7:0] / 快速检测阈值上限，位 [7:0]						
0x248	FD upper threshold MSB (local / 局部)	0	0	0	0	Fast detect upper threshold, bits [12:8] / 快速检测阈值上限，位 [12:8]		
0x249	FD lower threshold LSB (local / 局部)	Fast detect lower threshold, bits [7:0] / 快速检测阈值下限，位 [7:0]						
0x24A	FD lower threshold MSB (local / 局部)	Fast detect lower threshold, bits [12:8] / 快速检测阈值下限，位 [12:8]						
0x24B	FD dwell time LSB (local / 局部)	Fast detect dwell time, bits [7:0] / 快速检测驻留时间，位 [7:0]						
0x24C	FD dwell time MSB (local / 局部)	Fast detect dwell time, bits						

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		[15:8] / 快速检测驻留时间，位 [15:8]						
0x26F	Signal monitor synchronization control	Synchronization mode / Synchronization mode: 00 = disabled; 01 = continuous; 11 = one shot / 同步模式: 00 = disabled; 01 = continuous; 11 = one shot						
0x270	Signal monitor control (local / 局部)	Peak detector: 0 = disabled, 1 = enabled / Peak detector: 0 = disabled, 1 = enabled						
0x271	Signal Monitor Period Register 0 (local / 局部)	Signal monitor period, bits [7:0] / Signal monitor period, Bits[7:0]						
0x272	Signal Monitor Period Register 1 (local / 局部)	Signal monitor period, bits [15:8] / Signal monitor period, Bits[15:8]						
0x273	Signal Monitor Period Register 2 (local / 局部)	Signal monitor period, bits [23:16] / Signal monitor period, Bits[23:16]						
0x274								

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
	Signal monitor result control (local / 局部)	Result update: 1 = update results (self-clearing) / Result update: 1 = update results (自清零)	Result selection: 0 = reserved, 1 = peak detector / Result selection: 0 = reserved, 1 = peak detector					
0x275	Signal Monitor Result Register 0 (local / 局部)	Signal monitor result, bits [7:0] / Signal monitor result, Bits[7:0]. When register 0x0274[0] = 1, result bits [19:7] = peak detector absolute value [12:0]; result bits [6:0] = 0.						
0x276	Signal Monitor Result Register 1 (local / 局部)	Signal monitor result, bits [15:8] / Signal monitor result, Bits[15:8]						
0x277	Signal Monitor Result Register 1 (local)	Signal monitor result, bits [19:16] / Signal monitor result, Bits[19:16]						
0x278	Signal monitor period counter result (local / 局部)	Period count result, bits [7:0] / Period count result, Bits[7:0]						
0x279	Signal monitor SPORT over JESD204B control (local / 局部)	0	0	0	0	0	0	00 = disa 11 = ena 00 = disa 11 = ena
0x27A	SPORT over JESD204B input selection (local / 局部)	0	0	0	0	0	0	Peak detector disabled enabled

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
								Peak Detector disabled enabled
0x300	DDC synch control	DDC NCO soft reset: 0 = normal operation, 1 = reset / DDC NCO 软复位: 0 = 正常工作, 1 = 复位	Sync mode (triggered by SYSREF±) / 同步模式(由 SYSREF± 触发): 00 = disabled / 禁用; 01 = continuous / 连续; 11 = one shot / 1 次					
0x310	DDC 0 control	Mixer select: 0 = real mixer, 1 = complex mixer / 混频器选择: 0 = 实数混频器, 1 = 复数混频器	Gain select: 0 = 0 dB gain, 1 = 6 dB gain / 增益选择: 0 = 0 dB 增益, 1 = 6 dB 增益	IF mode / IF(中频)模式: 00 = variable IF mode (mixer and NCO enabled) / 可变 IF 模式(混频器和 NCO 使能); 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) / 0 Hz IF 模式(混频器旁路，NCO 禁用); 10 = fS/4 Hz IF mode (fS/4 mixing mode) / fS/4 Hz IF 模式(fS/4 下混频模式); 11 = test mode (mixer input forced to +fS, NCO enabled) /		Complex-to-real enable: 0 = disabled, 1 = enabled / 复数转实数使能: 0 = 禁用, 1 = 使能	0	(Comple real disabled = 2× decimati 00 = 4× decimati 01 = 8× decimati 10 = 16× decimati (复数转实 用): 11 = 抽取; 00 抽取; 01 抽取; 10 倍抽取; (comple real enab 11 = 1× decimati 00 = 2× decimati 01 = 4× decimati 10 = 8× decimati (复数转实 能): 11 = 抽取; 00 抽取; 01 抽取; 10 抽取

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
				测试模式(混频器输入强制为 +fS，NCO 使能)				
0x311	DDC 0 input selection	0	0	0	0	0	Q input select: 0 = channel A, 1 = channel B / Q 输入选择: 0 = 通道 A, 1 = 通道 B	0
0x314	DDC 0 frequency LSB	DDC 0 NCO frequency value, bits [7:0] (two's complement) / DDC 0 NCO 频率值，位7:0						
0x315	DDC 0 frequency MSB	X	X	X	X	DDC 0 NCO frequency value, bits [11:8] (two's complement) / DDC 0 NCO 频率值，位11:8		
0x320	DDC 0 phase LSB	DDC 0 NCO phase value, bits [7:0] (two's complement) / DDC 0 NCO 相位值，位7:0						
0x321	DDC 0 phase MSB	X	X	X	X	DDC 0 NCO phase value, bits [11:8] (two's complement) / DDC 0 NCO 相位值，位11:8		
0x327	DDC 0 output test mode selection	0	0	0	0	0	Q output test mode: 0 = disabled, 1 = enabled (channel B) / Q 输出测试模式: 0 = 禁用, 1 = 使能通道 B	0
0x330	DDC 1 control							

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		Same bit definitions as DDC 0 control (0x310), except IF mode bit 10 = fADC/4 Hz IF mode (fADC/4 mixing mode) / 与 DDC 0 控制(0x310)位定义相同，IF 模式 10 = fADC/4 Hz IF 模式(fADC/4 下混频模式)除外						
0x331	DDC 1 input selection	0	0	0	0	0	Q input select: 0 = channel A, 1 = channel B / Q 输入选择	0
0x334	DDC 1 frequency LSB	DDC 1 NCO frequency value, bits [7:0] (two's complement) / DDC 1 NCO 频率值，位7:0						
0x335	DDC 1 frequency MSB	X	X	X	X	DDC 1 NCO frequency value, bits [11:8] (two's complement) / DDC 1 NCO 频率值，位11:8		
0x340	DDC 1 phase LSB	DDC 1 NCO phase value, bits [7:0] (two's complement) / DDC 1 NCO 相位值，位7:0						
0x341	DDC 1 phase MSB	X	X	X	X	DDC 1 NCO phase value, bits [11:8] (two's complement) / DDC 1 NCO 相位值，位11:8		
0x347	DDC 1 output test mode selection	0	0	0	0	0	Q output test mode: 0 =	0

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
							disabled, 1 = enabled (channel B) / Q 输出测试模式	
0x350	DDC 2 control	Same bit definitions as DDC 0 control (0x310), except IF mode bit 10 = fADC/4 Hz IF mode (fADC/4 mixing mode) / 与 DDC 0 控制 (0x310)位定义相同，IF 模式 10 = fADC/4 Hz IF 模式(fADC/4 下混频模式)除外						
0x351	DDC 2 input selection	0	0	0	0	0	Q input select: 0 = channel A, 1 = channel B / Q 输入选择	0
0x354	DDC 2 frequency LSB	DDC 2 NCO frequency value, bits [7:0] (two's complement) / DDC 2 NCO 频率值，位7:0						
0x355	DDC 2 frequency MSB	X	X	X	X	DDC 2 NCO frequency value, bits [11:8] (two's complement) / DDC 2 NCO 频率值，位11:8		
0x360	DDC 2 phase LSB	DDC 2 NCO phase value, bits [7:0] (two's complement) / DDC 2 NCO 相位值，位7:0						
0x361	DDC 2 phase MSB	X	X	X	X	DDC 2 NCO phase value, bits [11:8] (two's complement) /		

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
						DDC 2 NCO 相位值，位11:8		
0x367	DDC 2 output test mode selection	0	0	0	0	0	Q output test mode: 0 = disabled, 1 = enabled (channel B) / Q 输出测试模式	0
0x370	DDC 3 control	Same bit definitions as DDC 0 control (0x310), except IF mode bit 10 = fADC/4 Hz IF mode (fADC/4 mixing mode) / 与 DDC 0 控制(0x310)位定义相同，IF 模式 10 = fADC/4 Hz IF 模式(fADC/4 下混频模式)除外						
0x371	DDC 3 input selection	0	0	0	0	0	Q input select: 0 = channel A, 1 = channel B / Q 输入选择	0
0x374	DDC 3 frequency LSB	DDC 3 NCO frequency value, bits [7:0] (two's complement) / DDC 3 NCO 频率值，位7:0						
0x375	DDC 3 frequency MSB	X	X	X	X	DDC 3 NCO frequency value, bits [11:8] (two's complement) / DDC 3 NCO 频率值，位11:8		
0x380	DDC 3 phase LSB	DDC 3 NCO phase value, bits [7:0] (two's complement) / DDC 3 NCO 相位值，位7:0						

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
0x381	DDC 3 phase MSB	X	X	X	X	DDC 3 NCO phase value, bits [11:8] (two's complement) / DDC 3 NCO 相位值，位11:8		
0x387	DDC 3 output test mode selection	0	0	0	0	0	Q output test mode: 0 = disabled, 1 = enabled (channel B) / Q 输出测试模式	0
0x550	ADC test modes (local / 局部)	User mode select: 0 = continuous repeat, 1 = single pattern / 用户模式选择: 0 = 连续重复, 1 = 单一模式	0	Generate reset PN long sequence: 0 = PN long sequence enabled, 1 = PN long sequence reset / 产生复位 PN 长序列: 0 = PN 长序列使能, 1 = PN 长序列复位	Generate reset PN short sequence: 0 = PN short sequence enabled, 1 = PN short sequence reset / 产生复位 PN 短序列: 0 = PN 短序列使能, 1 = PN 短序列复位	Test mode select / 测试模式选择: 0000 = off, normal mode / 关，正常模式; 0001 = mid-level short code / 中间电平短码; 0010 = positive full scale / 正满量程; 0011 = negative full scale / 负满量程; 0100 = alternating checkerboard / 交替棋盘形式; 0101 = PN long sequence / PN 长序列; 0110 = PN short sequence / PN 短序列; 0111 = 1/0 word alternate / 1/0 字交替; 1000 = user test mode (uses bit [7] of register 0x0550 and user mode 1, 2, 3, 4 registers) / 用户测试模式(使用寄存器 0x0550 的位[7]和用户模式 1、		

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
						2、3、4 寄存器); 1111 = ramp output / 斜坡输出		
0x551	User Pattern 1 LSB	0	0	0	0	0	0	0
0x552	User Pattern 1 MSB	0	0	0	0	0	0	0
0x553	User Pattern 2 LSB	0	0	0	0	0	0	0
0x554	User Pattern 2 MSB	0	0	0	0	0	0	0
0x555	User Pattern 3 LSB	0	0	0	0	0	0	0
0x556	User Pattern 3 MSB	0	0	0	0	0	0	0
0x557	User Pattern 4 LSB	0	0	0	0	0	0	0
0x558	User Pattern 4 MSB	0	0	0	0	0	0	0

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
0x559	Output Mode Control 1	0	Converter control bit 1 select / 转换器控制位 1 选择: 000 = tied low (1'b0) / 接低电平 (1'b0); 001 = overrange bit / 超量程位; 011 = fast detect (FD) bit / 快速检测 (FD)位; 101 = SYSREF±. Used only when CS (register 0x58F) = 2 or 3 / 仅当 CS(寄存器 0x58F)= 2 或 3 时使用			0	Converter control bit 0 select / 转换器控制位 0 选择: 000 = tied low (1'b0) / 接低电平(1'b0); 001 = overrange bit / 超量程位; 011 = fast detect (FD) bit / 快速检测 (FD)位; 101 = SYSREF±. Used only when CS (register 0x58F) = 3 / 仅当 CS(寄存器 0x58F)= 3 时使用	
0x55A	Output Mode Control 2	0	0	0	0	0	Converter control bit 2 select / 转换器控制位 2 选择: 000 = tied low (1'b0) / 接低电平(1'b0); 001 = overrange bit / 超量程位; 011 = fast detect (FD) bit / 快速检测 (FD)位; 101 = SYSREF±. Used when CS (register 0x58F) = 1, 2 or 3 / 当 CS(寄存器 0x58F)= 1、2 或 3 时使用	
0x561	Output mode	0	0	0	0	0	Sample invert: 0 = normal, 1 =	Data forr select / 数

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
							sample inverted / 样本反转: 0 = 正常, 1 = 样本反转	格式选择 offset bi 偏移二进 01 = two complen 二进制补
0x562	Output overrange (OR) clear	Virtual converter 7 OR: 0 = OR bit enabled, 1 = OR bit cleared / 虚拟转换器 7 OR: 0 = OR 位使能, 1 = OR 位清零	Virtual converter 6 OR: 0 = OR bit enabled, 1 = OR bit cleared / 虚拟转换器 6 OR	Virtual converter 5 OR: 0 = OR bit enabled, 1 = OR bit cleared / 虚拟转换器 5 OR	Virtual converter 4 OR: 0 = OR bit enabled, 1 = OR bit cleared / 虚拟转换器 4 OR	Virtual converter 3 OR: 0 = OR bit enabled, 1 = OR bit cleared / 虚拟转换器 3 OR	Virtual converter 2 OR: 0 = OR bit enabled, 1 = OR bit cleared / 虚拟转换器 2 OR	Virtual converte OR: 0 = C enabled, OR bit cleared / 转换器 1
0x563	Output OR status	Virtual converter 7 OR: 0 = no OR, 1 = OR occurred / 虚拟转换器 7 OR: 0 = 无 OR, 1 = OR 出现	Virtual converter 6 OR: 0 = no OR, 1 = OR occurred / 虚拟转换器 6 OR	Virtual converter 5 OR: 0 = no OR, 1 = OR occurred / 虚拟转换器 5 OR	Virtual converter 4 OR: 0 = no OR, 1 = OR occurred / 虚拟转换器 4 OR	Virtual converter 3 OR: 0 = no OR, 1 = OR occurred / 虚拟转换器 3 OR	Virtual converter 2 OR: 0 = no OR, 1 = OR occurred / 虚拟转换器 2 OR	Virtual converte OR: 0 = n 1 = OR occurred 拟转换器
0x564	Output channel select	0000000						
0x56E	JESD204B lane rate control	0 = serial lane rate ⩾ 6.25 Gbps and ⩽ 12.5 Gbps; 1 = serial lane rate ⩾ 3.125 Gbps and ⩽ 6.25 Gbps / 0 = 串行通道速率 ⩾6.25 Gbps 且⩽12.5 Gbps; 1 = 串行通道速率必须大于 ⩾3.125 Gbps 且 ⩽6.25 Gbps						

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
0x56F	JESD204B PLL lock status	PLL lock: 0 = not locked, 1 = locked / PLL 锁定: 0 = 未锁定, 1 = 已锁定	0000000					
0x570	JESD204B quick configuration	JESD204B quick configuration / JESD204B 快速配置: L = number of lanes = 2^(register 0x570 bits [7:6]) / L = 通道数 = 2^寄存器 0x570 的位[7:6]; M = number of converters = 2^(register 0x570 bits [5:3]) / M = 转换器数 = 2^寄存器 0x570 的位[5:3]; F = octets per frame = 2^(register 0x570 bits [2:0]) / F = 8 位字数/帧 = 2^寄存器 0x570 的位[2:0]						
0x571	JESD204B Link Mode Control 1	Standby mode: 0 = all converters output 0, 1 = CGS (/K28.5/) / 待机模式: 0 = 所有转换器输出 0, 1 = CGS (/K28.5/)	Tail bit (t) PN: 0 = disabled, 1 = enabled / 结束位(t) PN: 0 = 禁用, 1 = 使能	Long transport layer test: 0 = disabled, 1 = enabled / 长传输层测试: 0 = 禁用, 1 = 使能	Lane sync: 0 = disabled FACI use / K28.7/, 1 = enabled FACI use /K28.3/ and /K28.7/ / 通道同步: 0 = 禁用 FACI 使用 /K28.7/, 1 = 使能 FACI 使用 /K28.3/ 和 /K28.7/	ILAS sequence mode / ILAS 序列模式: 00 = ILAS disabled / ILAS 禁用; 01 = ILAS enabled / ILAS 使能; 11 = ILAS always on, test mode / ILAS 始终开启，测试模式		FACI: 0 = enabled, disabled FACI: 0 = 1 = 禁用
0x572	JESD204B Link Mode Control 2	SYNCINB± pin control: 00 = normal, 10 = ignore SYNCINB± (force CGS), 11 = ignore		SYNCINB± pin invert: 0 = active low, 1 = active high / SYNCINB±	SYNCINB± pin type: 0 = differential, 1 = CMOS / SYNCINB± 引脚类型: 0 = 差分, 1 = CMOS	0	8B/10B bypass: 0 = normal, 1 = bypass / 8B/10B 旁路: 0 = 正常, 1 = 旁路	8B/10B b inversion normal, inverted abcdefgh symbol / 10B 位反

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		SYNCINB± (force ILAS/user data) / SYNCINB±引脚控制: 00 = 正常, 10 = 忽略 SYNCINB± (强制 CGS), 11 = 忽略 SYNCINB± (强制 ILAS/用户数据)		引脚反转: 0 = 低电平有效, 1 = 高电平有效				= 正常, 1 转 abcde 符号
0x573	JESD204B Link Mode Control 3	CHKSUM mode / CHKSUM 模式: 00 = sum of all 8-bit link configuration registers / 所有 8 位链路配置寄存器之和; 01 = sum of each link configuration field / 各链路配置域之和; 10 = checksum set to 0 / 校验和设为 0		Test injection point / 测试注入点: 00 = N′ sample input / N′样本输入; 01 = 10-bit data at 8B/10B output (for PHY test) / 8B/10B 输出时的 10 位数据(用于 PHY 测试); 10 = 8-bit data at scrambler input / 加扰输入时的 8 位数据		JESD204B test mode / JESD204B 测试模式: 0000 = normal operation (test mode disabled) / 正常工作(测试模式禁用); 0001 = alternating checkerboard / 交替棋盘形式; 0010 = 1/0 word alternate / 1/0 字交替; 0011 = 31-bit PN sequence — $X^{31} + X^{28} + 1$ / 31 位 PN 序列—X31+ X28+ 1; 0100 = 23-bit PN sequence — $X^{23} + X^{18} + 1$ / 23 位 PN 序列—X23+ X18+ 1; 0101 = 15-bit PN sequence — $X^{15} + X^{14} + 1$ / 15 位 PN 序列—X15+ X14+ 1; 0110 = 9-bit PN sequence — $X^{9} + X^{5} + 1$ / 9 位 PN 序列—X9+ X5+ 1; 0111 = 7-bit PN sequence — $X^{7} + X^{6} + 1$ / 7 位	

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
						PN 序列—X7+ X6+ 1; 1000 = ramp output / 斜坡输出; 1110 = continuous/ repeat user test / 连续/重复用户测试; 1111 = single user test / 单用户测试		
0x574	JESD204B Link Mode Control 4	Transmit ILAS at the first LMFC after SYNCINB± deassertion / SYNCINB±解除置位后的第一个 LMFC 时发送 ILAS: 0001 = at the second LMFC after SYNCINB± deassertion / SYNCINB±解除置位后的第二个 LMFC 时发送 ILAS; …; 1111 = at the 16th LMFC after SYNCINB± deassertion / SYNCINB±解除置位后的第 16 个 LMFC 时发送 ILAS				0	Link layer test mode / 链路层测试模式: 000 = normal operation (link layer test mode disabled) / 正常工作(链路层测试模式禁用); 001 = continuous sequence of / D21.5/ characters / / D21.5/字符的连续序列; 100 = modified RPAT test sequence / 修改的 RPAT 测试序列; 101 = JSPAT test sequence / JSPAT 测试序列; 110 = JTSPAT test sequence / JTSPAT 测试序列	
0x578	JESD204B LMFC offset	0	0	0	LMFC phase offset [4:0] / LMFC 相位偏移值[4:0]			
0x580	JESD204B DID config	JESD204B Tx DID value [7:0] / JESD204B Tx DID 值[7:0]						
0x581	JESD204B BID config	0	0	0	0			

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
						JESD204B Tx BID value, bits [3:0] / JESD204B Tx BID 值，位[3:0]		
0x583	JESD204B LID Config 0	0	0	0	0	Lane 0 LID value, bits [4:0] / Lane 0 LID value, Bits[4:0]		
0x585	JESD204B LID Config 1	0	0	0	0	Lane 1 LID value, bits [4:0] / Lane 1 LID value, Bits[4:0]		
0x587	JESD204B LID Config 2	0	0	0	0	Lane 2 LID value, bits [4:0] / Lane 2 LID value, Bits[4:0]		
0x589	JESD204B LID Config 3	0	0	0	0	Lane 3 LID value, bits [4:0] / Lane 3 LID value, Bits[4:0]		
0x58B	JESD204B parameters SCR/L	JESD204B scrambling (SCR): 0 = disabled, 1 = enabled / JESD204B 加扰 (SCR): 0 = 禁用, 1 = 使能	0	0	0	0	0	JESD204 number lanes (L) 1 lane, 0 lanes, 11 lanes / JESD204 道数(L): 0 通道, 01 = 道, 11 = 4
0x58C	JESD204B F config	Number of octets per frame, F = register 0x58C[7:0] + 1 / Number of octets per frame, F = Register 0x58C[7:0] + 1						
0x58D	JESD204B K config	Frames per multiframe, K =						

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		register 0x58D[4:0] + 1. Only values with (F × K) mod 4 = 0 are supported / 每个多帧的帧数，K = 寄存器 0x58D[4:0] + 1。仅支持(F × K) mod 4 = 0 的值						
0x58E	JESD204B M config	Number of converters per link [7:0] / 每链路的转换器数 [7:0]: 0x00 = link connected to 1 virtual converter (M = 1) / 链路连接到 1 个虚拟转换器(M = 1); 0x01 = link connected to 2 virtual converters (M = 2) / 链路连接到 2 个虚拟转换器(M = 2); 0x03 = link connected to 4 virtual converters (M = 4) / 链路连接到 4 个虚拟转换器(M = 4); 0x07 = link connected to 8 virtual converters (M = 8) / 链路连接到 8 个虚拟转换器(M = 8)						
0x58F	JESD204B CS/N config	Control bits per frame (CS) / 每帧的控制位数 (CS): 00 = no control bits (CS = 0) / 无控制位 (CS = 0); 01 = 1 control bit (CS = 1), control bit 2 only / 1 控制位		0	ADC converter resolution (N) / ADC 转换器分辨率(N): 0x0D = 14-bit resolution / 14 位分辨率; 0x0F = 16-bit			

Addr (Hex) / 寄存器地址(十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		(CS = 1)，仅控制位 2; 10 = 2 control bits (CS = 2), control bits 2 and 1 only / 2 控制位(CS = 2)，仅控制位 2 和 1; 11 = 3 control bits (CS = 3), all control bits (2, 1, 0) / 3 控制位(CS = 3)，所有控制位(2、1、0)			resolution / 16 位分辨率			
0x590	JESD204B N′ config	Subclass support (subclass V) / 子类支持(子类 V): 000 = subclass 0 (no deterministic latency) / 子类 0(无确定性延迟); 001 = subclass 1 / 子类 1			0	ADC bits per sample (N′) / ADC 每样本的位数(N′): 0x7 = 8 bits / 8 位; 0xF = 16 bits / 16 位		
0x591	JESD204B S config	0	0	1	Samples per converter per frame (S) / 每个转换器帧的样本数(S): S = register 0x591[4:0] + 1 / S 值 = 寄存器 0x591[4:0] + 1			
0x592	JESD204B HD and CF config	HD value: 0 = disabled, 1 = enabled / HD 值: 0 = 禁用, 1 = 使能	0	0	Control words per frame clock period per link (CF) / 每链路上每个帧时钟周期的控制字(CF): CF = bits [4:0] of register 0x592 / CF 值 = 寄存器 0x592 的位 [4:0]			
0x5A0	JESD204B CHKSUM 0							

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
		CHKSUM value of SERDOUT0±, bits [7:0] / SERDOUT0±的 CHKSUM 值，位 [7:0]						
0x5A2	JESD204B CHKSUM 1	CHKSUM value of SERDOUT1±, bits [7:0] / SERDOUT1±的 CHKSUM 值，位 [7:0]						
0x5A4	JESD204B CHKSUM 2	CHKSUM value of SERDOUT2±, bits [7:0] / SERDOUT2±的 CHKSUM 值，位 [7:0]						
0x5A6	JESD204B CHKSUM 3	CHKSUM value of SERDOUT3±, bits [7:0] / SERDOUT3±的 CHKSUM 值，位 [7:0]						
0x5B0	JESD204B lane powerdown	1	SERDOUT3±: 0 = on, 1 = off / SERDOUT3±: 0 = 开, 1 = 关	1	SERDOUT2±: 0 = on, 1 = off / SERDOUT2±: 0 = 开, 1 = 关	1	SERDOUT1±: 0 = on, 1 = off / SERDOUT1±: 0 = 开, 1 = 关	1
0x5B2	JESD204B lane SERDOUT0± assign	X	X	X	X	X	SERDOUT0± lane assignment / SERDOUT0±通道分配: 000 = logical lane 0 / 逻辑通道 0; 001 = logical lane 1 / 逻辑通道 1; 010 = logical lane 2 / 逻辑通道 2; 011 = logical lane 3 / 逻辑通道 3	
0x5B3	JESD204B lane SERDOUT1± assign	X	X	X	X	X	SERDOUT1± lane assignment / SERDOUT1±通道分配: 000 =	

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
							logical lane 0 / 逻辑通道 0; 001 = logical lane 1 / 逻辑通道 1; 010 = logical lane 2 / 逻辑通道 2; 011 = logical lane 3 / 逻辑通道 3	
0x5B5	JESD204B lane SERDOUT2± assign	X	X	X	X	X	SERDOUT2± lane assignment / SERDOUT2±通道分配: 000 = logical lane 0 / 逻辑通道 0; 001 = logical lane 1 / 逻辑通道 1; 010 = logical lane 2 / 逻辑通道 2; 011 = logical lane 3 / 逻辑通道 3	
0x5B6	JESD204B lane SERDOUT3± assign	X	X	X	X	X	SERDOUT3± lane assignment / SERDOUT3±通道分配: 000 = logical lane 0 / 逻辑通道 0; 001 = logical lane 1 / 逻辑通道 1; 010 = logical lane 2 / 逻辑通道 2; 011 = logical lane 3 / 逻辑通道 3	
0x5BF	JESD serializer drive adjust	0	0	0	0	Swing / 摆幅: 0000 = 237.5 mV; 0001 = 250 mV; 0010 = 262.5 mV; 0011 = 275 mV; 0100 = 287.5 mV; 0101 = 300 mV (default / 默认); 0110 = 312.5 mV; 0111 = 325 mV; 1000 =		

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
						337.5 mV; 1001 = 350 mV; 1010 = 362.5 mV; 1011 = 375 mV; 1100 = 387.5 mV; 1101 = 400 mV; 1110 = 412.5 mV; 1111 = 425 mV		
0x5C1	Deemphasis select	0	SERDOUT3±: 0 = disabled, 1 = enabled / SERDOUT3±: 0 = 禁用, 1 = 使能	0	SERDOUT2±: 0 = disabled, 1 = enabled / SERDOUT2±: 0 = 禁用, 1 = 使能	0	SERDOUT1±: 0 = disabled, 1 = enabled / SERDOUT1±: 0 = 禁用, 1 = 使能	0
0x5C2	Deemphasis setting for SERDOUT0±	0	0	0	0	SERDOUT0± de-emphasis setting / SERDOUT0±去加重设置: 0000 = 0 dB; 0001 = 0.3 dB; 0010 = 0.8 dB; 0011 = 1.4 dB; 0100 = 2.2 dB; 0101 = 3.0 dB; 0110 = 4.0 dB; 0111 = 5.0 dB		
0x5C3	Deemphasis setting for SERDOUT1	0	0	0	0	SERDOUT1 de-emphasis setting / SERDOUT1 去加重设置: 0000 = 0 dB; 0001 = 0.3 dB; 0010 = 0.8 dB; 0011 = 1.4 dB; 0100 = 2.2 dB; 0101 = 3.0 dB; 0110 = 4.0 dB; 0111 = 5.0 dB		
0x5C4	Deemphasis setting for SERDOUT2	0	0	0	0	SERDOUT2 de-emphasis setting / SERDOUT2 去加重设置: 0000 = 0 dB; 0001 = 0.3 dB; 0010 = 0.8 dB; 0011 =		

Addr (Hex) / 寄存器地址 (十六进制)	Register Name / 寄存器名	Bit 7 (MSB) / 位 7	Bit 6 / 位6	Bit 5 / 位5	Bit 4 / 位4	Bit 3 / 位3	Bit 2 / 位2	Bit 1 / 位
						1.4 dB; 0100 = 2.2 dB; 0101 = 3.0 dB; 0110 = 4.0 dB; 0111 = 5.0 dB		
0x5C5	Deemphasis setting for SERDOUT3	0	0	0	0	SERDOUT3 de-emphasis setting / SERDOUT3 去加重设置: 0000 = 0 dB; 0001 = 0.3 dB; 0010 = 0.8 dB; 0011 = 1.4 dB; 0100 = 2.2 dB; 0101 = 3.0 dB; 0110 = 4.0 dB; 0111 = 5.0 dB		

15. 电源地间保护 / Power-to-Ground Protection

English: To improve the device's ESD immunity, ESD protection loops exist between the internal supply pins of the device. The forward conduction voltage drop of each ESD protection device is approximately 0.7 V. During power-up and normal use, prolonged forward conduction of these ESD protection devices should be avoided. The Diode cell is a series connection of one or more parallel forward/reverse diode cells; PC1 is the low-voltage PowerClamp protection cell and PC2 is the high-voltage PowerClamp protection cell.

为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.7V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通，其中 Diode 单元为一个或多个正反二极管并联单元的串联，PC1 为低压 PowerClamp 保护单元，PC2 为高压 PowerClamp 保护单元。

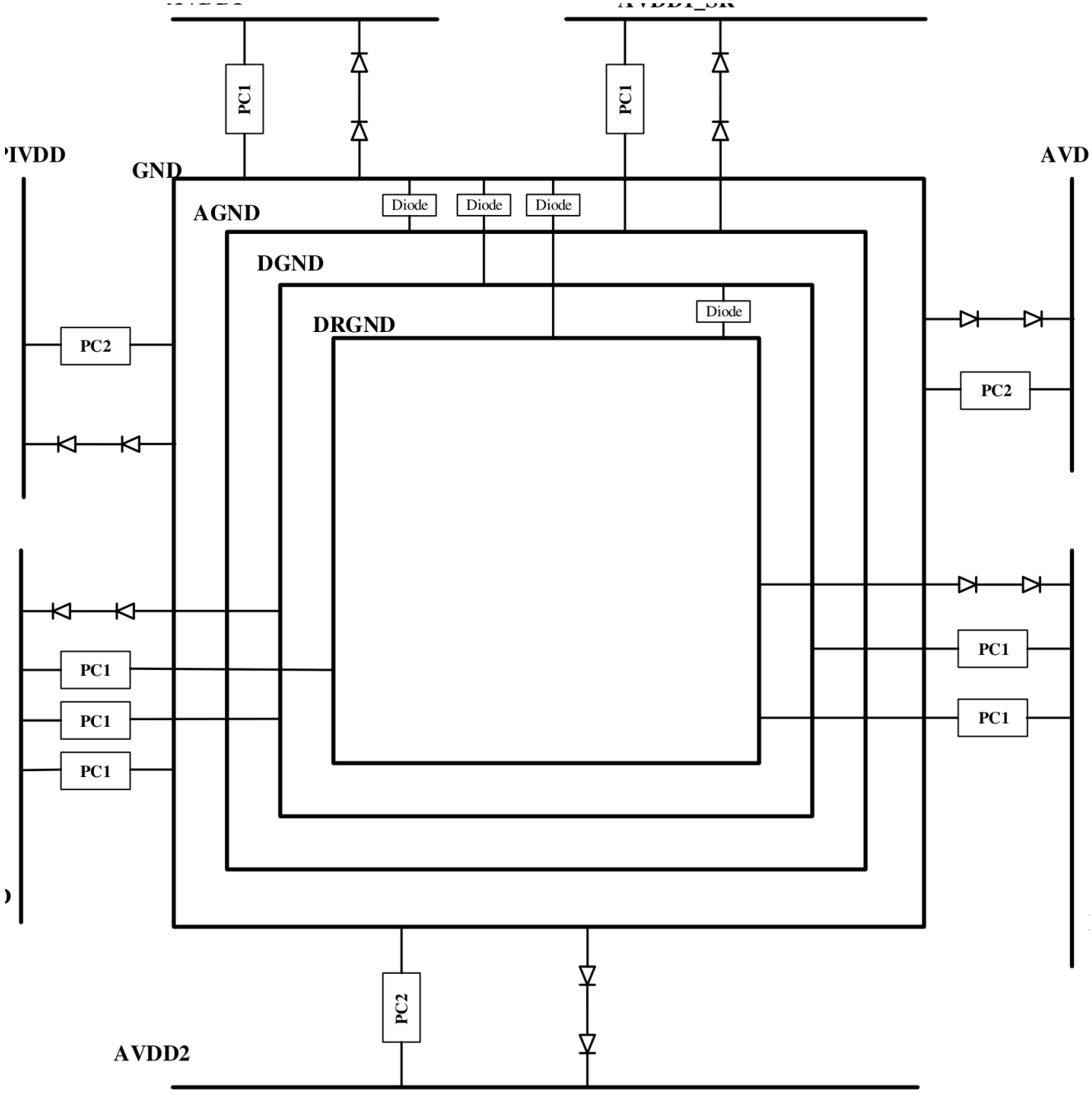


Figure 39: Internal ESD protection circuit between supplies

16. 注意事项 / Notes

1、产品安装注意事项 / 16.1 Product Installation Notes

1. The application PCB is required to have a complete, clean ground. / 要求应用对象电路板有一个完整干净的地。
2. The application board is required to be a multi-layer board with an independent ground plane. / 要求应用对象为多层布线板且内含独立的地层。
3. The digital ground and analog ground of the application board should be separated as much as possible; do not route digital lines next to analog lines or under the ADC. / 要求应用对象电路板的数字地和模拟地尽量分离，不要将数字线布于模拟线旁边或于 ADC 底下。

4. Supplies must be connected with high-quality ceramic bypass capacitors, placed as close as possible to the pins; connections between pins and bypass capacitors should be as short and wide as possible. / 电源要接高质量的陶瓷旁路电容，且旁路电容要尽量靠近管脚，连接管脚和旁路电容的连线越短越宽越好。

2、产品使用注意事项 / 16.2 Product Usage Notes

1. Differential inputs should be routed close together and parallel to each other. / 差分输入应尽量靠近且相互平行。
2. Input connections should be as short as possible to minimize parasitic capacitance and noise pickup. / 输入连线应尽量短以最小化寄生电容和噪声引入。
3. Pay attention to ambient temperature in actual use, and ensure heat dissipation. For better heat dissipation and electrical performance, the die attach pad of the chip should be soldered to a large ground area of the PCB to maximize the thermal performance of the package. / 建议实际使用时关注环境温度，并注意散热。为了更好的散热并获得更好的电性能，芯片的底板应焊接到 PCB 板的一个大的地端，从而最大限度发挥封装的热性能。
4. The chip ground should be connected to the PCB ground plane through as many vias and as much area as possible. / 芯片的地应该通过尽量多的渠道和足够多的面积与 PCB 板的地层相连。
5. For the relationship between output data, output clock and analog input, see the timing diagram section. / 输出数据和输出时钟和模拟输入关系看时序图说明部分。
6. No power-up sequencing; power-up settling time is less than 10 ms. Unused input/output pins should be left floating; the thermal pad must be grounded; the lid has no potential requirement. / 无上电顺序，上电建立时间小于 10ms。未使用输入输出引脚悬空处理，热层需要接地，盖板无电位要求。
7. After power-up, it is recommended to first reset the circuit (write 0x81 to register 0x000) before use. / 推荐上电后首先对电路进行复位（寄存器 0x000 打 0x81），再进行使用。

3、产品防护注意事项 / 16.3 Product Protection Notes

1. Electrostatic charge easily accumulates on the human body and test equipment and may discharge without being noticed. Although this product has dedicated ESD protection circuits, permanent device damage may occur under high-energy electrostatic discharge. Appropriate ESD precautions are therefore recommended to avoid degraded device performance or loss of functionality. Electrostatic discharge sensitivity rating: Class IB (up to 500 V). / 静电电荷很容易在人体和测试设备上累积，并可能在没有察觉的情况下放电。尽管本产品具有专用 ESD 保护电路，但在遇到高能量静电放电时，可能会发生永久性器件损坏。因此，建议采取适当的 ESD 防范措施，以避免器件性能下降或功能丧失。静电放电敏感度等级：IB 级（达到 500V）。
2. Exceeding absolute maximum ratings may cause permanent damage to the device. These are ratings only and do not indicate that the device can operate normally under these conditions or any other conditions beyond those shown in this product manual. Operating at absolute maximum ratings for extended periods affects device reliability. / 超出绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。长期在绝对最大额定值条件下工作会影响器件的可靠性。

4、电装说明 / 16.4 Assembly Instructions

1. This product has moisture sensitivity level MSL3. After removing the product from the moisture-barrier bag, the allowable floor life before reflow after dry storage or baking is: ⩽ 30 °C / 60 RH%, 168 h. / 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出，进行干燥储存或烘干后到回流焊所暴露在外部环境的允许时间为：≤30°C/60RH%，168h 车间寿命；
2. Before assembly, if the product has not been stored dry, bake at 125 °C for 8 h to remove internal moisture (note: after baking, the environment is extremely dry and static is easily generated; take ESD precautions). / 产品在组装之前，若未干燥保存，需要在 125°C条件下烘烤 8h，以去除内部湿气（注：产品烘烤后，环境特别干燥，极易产生静电，要注意 ESD 保护）。
3. Leaded reflow soldering (Sn63Pb37) is recommended for board-level assembly, with a recommended peak temperature range of 210 °C – 230 °C; the maximum peak temperature should not exceed 245 °C; time within ±5 °C of peak temperature ⩽ 20 s; time above liquidus 60 – 90 s; ramp-up rate ⩽ 3 °C/s; ramp-down rate ⩽ 6 °C/s. / 板级组装建议采用有铅回流焊（Sn63Pb37），推荐峰值温度范围 210°C~230°C，最大峰值温度不建议超过 245°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s。升温速率≤3°C/s，降温速率≤6°C/s。
4. For lead-free reflow soldering (SAC305), the recommended peak temperature range is 230 °C – 245 °C; the maximum peak temperature should not exceed 260 °C; time within ±5 °C of peak temperature ⩽ 20 s; time above liquidus 60 – 90 s; ramp-up rate ⩽ 3 °C/s; ramp-down rate ⩽ 6 °C/s. / 若采用无铅回流焊（SAC305），推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s。升温速率≤3°C/s，降温速率≤6°C/s。
5. If a mixed board-level assembly process requires higher temperatures, ensure the device body temperature does not exceed 260 °C. (The device body temperature is measured at the top surface of the device during reflow.) / 若混合板级组装工艺需要温度升高，应保证器件本体温度最高不超过 260°C。（器件本体温度测量点位于回流焊时器件上表面）
6. The solderable plating on the product terminals is NiPdAu, with a gold layer thickness of 0.08 μm ± 0.03 μm; gold content is far below 3%, so no gold embrittlement occurs and tinning is not required. / 本产品焊接端镀层材料为镍钯金，金层厚度 0.08μm±0.03μm，金含量远小于 3%，不会出现金脆"现象，因此不需要搪锡。
7. If the user requires forced tinning, perform it per the national aerospace industry standard QJ3267-2006 "Technical requirements for tinning of electronic components". Note: the device must be dry before tinning; tinning equipment set temperature must not exceed 300 °C; pad tinning/de-tinning time must not exceed 10 s; cumulative tinning/de-tinning time for the four side terminal edges must not exceed 40 s; tinning no more than once. / 若用户有强制搪锡需求，按《国家航天行业标准 QJ3267-2006 电子元器件搪锡工艺技术要求》标准进行搪锡。应注意搪锡前器件处于干燥状态，搪锡设备的设置温度不超过 300°C，焊盘上锡及去锡时间不超过 10 秒，底面四边引出端上锡及去锡时间累计不超过 40 秒，搪锡次数不超过 1 次。
8. The side pads of this product are bare copper and do not wet during soldering; no touch-up soldering/fillet is required on the sides. / 本产品侧面焊盘为裸铜，不具备焊接润湿性，侧面不要求补焊爬锡。

5、使用散热建议 / 16.5 Heatsink Recommendations

1. Users are advised to enhance heat dissipation during use, e.g., covering the circuit case with thermal grease and a metal heatsink (which may be shared with surrounding devices); add a fan

structure if possible, as shown in Figure 40. / 建议用户使用过程中加强散热，例如电路上壳覆盖散热硅脂与金属散热片（可与周围器件共用），有条件可增加风扇结构，如图 40 所示；

2. For PCB layout design, it is recommended to divide the package thermal pad into a 4- or 9-grid pattern according to size to improve solder coverage, as shown in Figure 41. / PCB 版图设计推荐封装热沉根据大小划分为 4、9 宫格形式，提升焊接覆盖面，如图 41 所示。



Figure 40: Recommended heatsink design

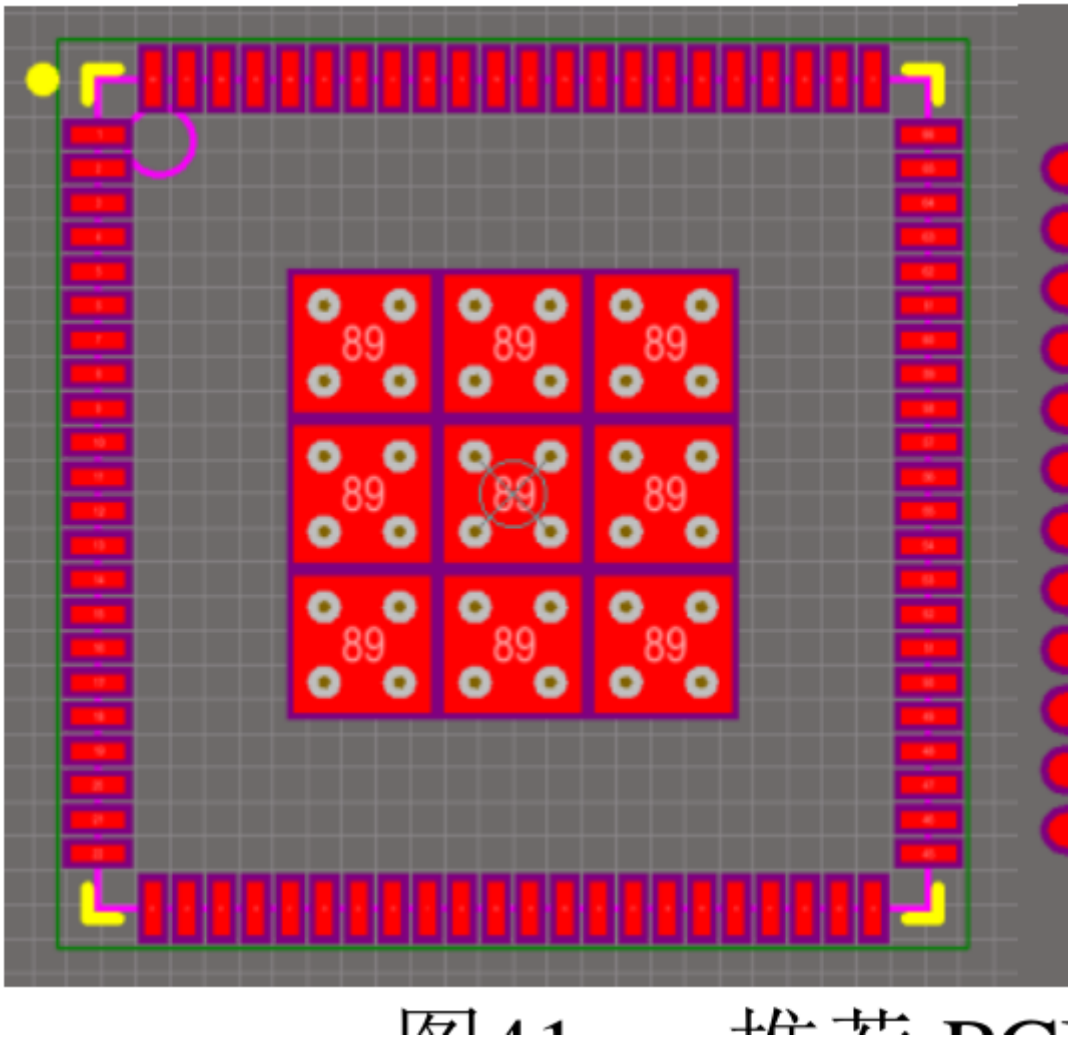


Figure 41: Recommended PCB thermal pad design

6、热阻 / 16.6 Thermal Resistance

表18 热阻 / Table 18 — Thermal Resistance

Item / 项目	Measured Value / 实测值	Standard and Method / 依据标准及方法
Rthja (junction-to-ambient thermal resistance) / Rthja（结到环境的热阻）	33.41 K/W	JESD51-2: natural-convection thermal test environment requirements and test methods for integrated circuits / JESD51-2 集成电路自然对流热测试环境要求及测试方法
Rthjt (junction-to-top thermal resistance) / Rthjt(结到器件顶面的热阻)	3.244 K/W	JESD51-14: one-dimensional heat-flow-path dual-interface separation method / JESD51-14 一维传热路径双界面分离法
Rthj-bottom (junction-to-bottom thermal resistance) / Rthj-bottom（结到器件底面的热阻）	1.964 K/W	JESD51-14: inflection-point theory for internal device structure delayering / JESD51-14 拐点理论器件内部结构分层得到

17. 常见故障及处理办法 / Troubleshooting

1. No signal output: check that supply voltages, input signal and clock are loaded correctly. / 无信号输出：检查电源电压、输入信号、时钟是否正确加载。
2. Overflow signal: check that the reference is working normally and the input signal amplitude is correct. / 出现溢出信号：检查基准是否正常工作，输入信号幅度是否正确。
3. Unstable device operation: check the power supplies to ensure stable supply voltage. / 器件工作不稳定：检查电源，保证电源电压稳定。

18. 联系方式 / Contact Information

English: - Felix (Flip) Lai, CEO - Email: felix@shenxinic.com - Phone: +852 51367095 - Website: shenxinic.com

中文： - Felix (Flip) Lai，CEO - 邮箱：felix@shenxinic.com - 电话：+852 51367095 - 官网：shenxinic.com

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19. 附加说明 / Additional Notes

1. This manual was first issued on July 22, 2026. / 本说明书首次发布日期：2026 年 7 月 22 日。
2. Product status: ☑ Production (this product model is currently in production; formal product available) / 本产品状态：☑ 生产（该产品型号目前已在生产，可以提供正式产品）；☐ Pre-release (this product model is not yet in formal production; samples available) / ☐预发布（该产品型号尚未投入正式生产，可以提供样品）
3. Comparison with the international reference product / 替代国外产品情况说明：

1）绝对最大额定值对比 / 1) Absolute Maximum Ratings Comparison

附表1 绝对最大额定值对比 / Appendix Table 1. Absolute Maximum Ratings Comparison

参数 / Parameter	SXA032	国外产品 / International Product (AD9680)	比对结果 / Comparison Result
引脚 VAVDD1 到 VAGND 电压 / Voltage from pin VAVDD1 to VAGND	1.32V	1.32V	一致 / Consistent
引脚 VAVDD1_SR 到 VAGND 电压 / Voltage from pin VAVDD1_SR to VAGND	1.32 V	1.32 V	一致 / Consistent
引脚 VAVDD2 到 VAGND 电压 / Voltage from pin VAVDD2 to VAGND	2.75V	2.75V	一致 / Consistent
引脚 VAVDD3 到 VAGND 电压 / Voltage from pin VAVDD3 to VAGND	3.63V	3.63V	一致 / Consistent
引脚 VDVDD 到 VDGND 电压 / Voltage from pin VDVDD to VDGND	1.32V	1.32V	一致 / Consistent
引脚 VDRVDD 到 VDRGND 电压 / Voltage from pin VDRVDD to VDRGND	1.32V	1.32V	一致 / Consistent
	3.63V	3.63V	一致 / Consistent

参数 / Parameter	SXA032	国外产品 / International Product (AD9680)	比对结果 / Comparison Result
引脚 VSPIVDD 到 VAGND 电压 / Voltage from pin VSPIVDD to VAGND			
引脚 VAGND 到 VDRGND 电压 / Voltage from pin VAGND to VDRGND	-0.3V-0.3V	-0.3V-0.3V	一致 / Consistent
引脚 VIN(A)+到 VAGND 电压 / Voltage from pin VIN(A)+ to VAGND	3.2V	3.2V	一致 / Consistent

2）推荐工作条件对比 / 2) Recommended Operating Conditions Comparison

附表2 推荐工作条件对比 / Appendix Table 2. Recommended Operating Conditions Comparison

参数 / Parameter	SXA032	国外产品 / International Product (AD9680)	比对结果 / Comparison Result
工作频率（fCLK）/ Operating frequency (fCLK)	≤1250MSPS	≤1250MSPS	一致 / Consistent
模拟电源电压（VAVDD1）/ Analog supply voltage (VAVDD1)	1.25V~1.30V	1.22~1.28V	不一致 / Not consistent
模拟电源电压（VAVDD2）/ Analog supply voltage (VAVDD2)	2.44~2.56V	2.44~2.56V	一致 / Consistent
模拟电源电压（VAVDD3）/ Analog supply voltage (VAVDD3)	3.2~3.4V	3.2~3.4V	一致 / Consistent
SYSREF 电源电压（VAVDD1_SR）/ SYSREF supply voltage (VAVDD1_SR)	1.25V~1.30V	1.22~1.28V	不一致 / Not consistent
数字电源电压（VDVDD）/ Digital supply voltage (VDVDD)	1.25V~1.30V	1.22~1.28V	不一致 / Not consistent
驱动电源电压（VDRVDD）/ Driver supply voltage (VDRVDD)	1.25V~1.30V	1.22~1.28V	不一致 / Not consistent
SPI 电源电压（VSPIVDD）/ SPI supply voltage (VSPIVDD)	规范 1.7~2.0V，实际摸底 1.8~3.3V / Specified 1.7~2.0V; verified in practice 1.8~3.3V	1.8~3.3V	一致 / Consistent
输入信号幅度范围（峰峰值）（VIN(P-P)）/ Input signal amplitude range (peak-to-peak) (VIN(P-P))	1.58V	1.58V	一致 / Consistent
工作温度（TA）/ Operating temperature (TA)	-40°C~85°C	-40°C~85°C	一致 / Consistent

3）性能指标对比 / 3) Performance Specifications Comparison

附表3 性能指标对比 / Appendix Table 3. Performance Specifications Comparison

English: Conditions (unless otherwise specified): VAVDD1=1.30V, VAVDD2=2.5V, VAVDD3=3.3V, VAVDD1_SR=1.30V, VDVDD=1.30V, VDRVDD=1.30V, VSPIVDD=1.8V, AGND=DGND=DRGND=0V, -40°C≤TA≤85°C.

中文： 条件（除另有规定外，VAVDD1=1.30V，VAVDD2=2.5V，VAVDD3=3.3V，VAVDD1_SR=1.30V，VDVDD=1.30V，VDRVDD=1.30V，VSPIVDD=1.8V，AGND=DGND=DRGND=0V，-40°C≤TA≤85°C）

特性 / Characteristic	条件 / Condition	SXA032 最小 / Min	SXA032 典型值 / Typ	SXA032 最大 / Max	国外产品最小 / Int'l Min	国外产品典型值 / Int'l Typ	国外产品最大 / Int'l Max	单位 / Unit	对比结果 / Comparison
分辨率 / Resolution	——	14	14	14	14	14	14	Bits	一致 / Consistent
采样率 / Sample rate	——	1250	1250	1250	1250	1250	1250	MSPS	一致 / Consistent
通道数 / Number of channels	——	2	2	2	2	2	2	CH	一致 / Consistent
功耗 / Power consumption	——	—	4.1	4.8	—	3.7	—	W	相当 / Comparable
微分非线性误差 / Differential nonlinearity error	——	-2.0	±0.7	2.0	-0.8	—	0.8	LSB	相当 / Comparable
积分非线性误差 / Integral nonlinearity error	——	-20	±3	+20	-6	—	6	LSB	相当 / Comparable
基准输出电压 / Reference output voltage	——	950	1003	1050	—	1000	—	mV	相当 / Comparable
信噪比 / SNR	fIN=10MHz	58.0	65	—	—	63.6	—	dBFS	相当 / Comparable
	fIN=450MHz	56.5	63	—	—	62.2	—	dBFS	相当 / Comparable
	fIN=765MHz	55.0	61	—	—	61.1	—	dBFS	相当 / Comparable
信噪失真比 / SINAD	fIN=10MHz	57.5	64	—	—	63.5	—	dBFS	相当 / Comparable
	fIN=450MHz	56.0	61	—	—	61.8	—	dBFS	相当 / Comparable
	fIN=765MHz	54.5	59	—	—	60.8	—	dBFS	相当 / Comparable
有效位 / ENOB	fIN=10MHz	9.25	10.5	—	—	10.3	—	dBFS	相当 / Comparable
	fIN=450MHz	9.00	9.9	—	—	10.0	—	dBFS	相当 / Comparable
	fIN=765MHz	8.76	9.5	—	—	9.8	—	dBFS	相当 / Comparable
无杂散动态范围 / SFDR	fIN=10MHz	65.0	80	—	—	84	—	dBFS	相当 / Comparable
	fIN=450MHz	60.0	70	—	—	78	—	dBFS	稍低 / Slightly lower

特性 / Characteristic	条件 / Condition	SXA032 最小 / Min	SXA032 典型值 / Typ	SXA032 最大 / Max	国外产品最小 / Int'l Min	国外产品典型值 / Int'l Typ	国外产品最大 / Int'l Max	单位 / Unit	对比结果 / Comparison
	fIN=765MHz	55.0	69	—	—	77	—	dBFS	稍低 / Slightly lower
二三阶谐波 / 2nd/3rd harmonics	fIN=10MHz	—	-79	-65.0	—	-84	—	dBFS	相当 / Comparable
	fIN=450MHz	—	-70	-60.0	—	-76	—	dBFS	稍低 / Slightly lower
	fIN=765MHz	—	-67	-55.0	—	-77	—	dBFS	稍低 / Slightly lower
JESD204B 接口速率 / JESD204B interface rate	——	—	12.5	12.5	3.125	12.5	12.5	Gbps	一致 / Consistent
逻辑输入高电平电压 / Logic input high voltage	——	0.8VSPIVDD	0.8VSPIVDD	—	—	—	—	V	一致 / Consistent
逻辑输入低电平电压 / Logic input low voltage	——	0	0.5	0.5	0	—	0.5	V	一致 / Consistent
逻辑输出高电平电压 / Logic output high voltage	——	0.8VSPIVDD	0.8VSPIVDD	—	—	—	—	V	一致 / Consistent
逻辑输出低电平电压 / Logic output low voltage	——	0	0.5	0.5	0	—	0.5	V	一致 / Consistent
模拟电源 1 电流 / Analog supply 1 current	——	—	805	—	—	785	880	mA	相当 / Comparable
模拟电源 2 电流 / Analog supply 2 current	——	—	800	—	—	675	780	mA	相当 / Comparable
模拟电源 3 电流 / Analog supply 3 current	——	—	135	—	—	125	142	mA	相当 / Comparable
同步电路电源电流 / Sync circuit supply current	——	—	11	—	—	17	20	mA	相当 / Comparable
数字电源电流 / Digital supply current	——	—	260	—	—	250	325	mA	相当 / Comparable
数字驱动电源电流 / Digital driver supply current	——	—	221	—	—	220	300	mA	相当 / Comparable
	——	—	2.5	—	—	5	6	mA	相当 / Comparable

特性 / Characteristic	条件 / Condition	SXA032 最小 / Min	SXA032 典型值 / Typ	SXA032 最大 / Max	国外产品最小 / Int'l Min	国外产品典型值 / Int'l Typ	国外产品最大 / Int'l Max	单位 / Unit	对比结果 / Comparison
SPI 数字电源电流 / SPI digital supply current									

English: Note: In Appendix Table 3, the typical values of the domestic product are room-temperature measured values, and the typical values of the international product are the values in its product datasheet.

中文： 注：附表 3 中，国内产品典型值为常温实测值，国外产品典型值为其产品手册值。

4）寄存器对比 / 4) Register Comparison

English: The registers show no differences from the international product.

中文： 寄存器与国外产品无差异。

5）其它指标对比 / 5) Other Parameter Comparison

附表4 其它指标对比 / Appendix Table 4. Other Parameter Comparison

参数 / Parameter	SXA032	国外产品 / International Product (AD9680)	比对结果 / Comparison Result
封装形式 / Package	QFN64	LFCSP64	相同 / Same
质量等级 / Quality grade	企标 / Enterprise standard	工业级 / Industrial grade	有差异 / Different
尺寸 / Dimensions	9mm9mm0.75mm	9mm9mm0.75mm	相同 / Same
替代建议 / Cross-reference recommendation	☐直接替代 / ☐Direct replacement ☐有效替代 / ☐Effective alternative ☑功能替代 / ☑Functional alternative		

End of document / 文档结束