SXA036

Quad 14-Bit, 125 MSPS A/D Converter

四通道 14 位 125MSPS A/D 转换器

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXA036 Quad-Channel 14-Bit 125 MSPS A/D Converter — Datasheet & User Manual

SXA036 型四通道 14 位 125MSPS A/D 转换器 — 产品说明书、使用手册

深信科技 / Shenzhen Shenxin Technology Co., Ltd.

Version / 版本：V1.20260727

Table of Contents / 目录

- Product Applications and Scope / 产品用途及应用范围
- Standard / 标准
- Features / 产品特点
- Product Description / 产品描述
- Package Outline and Physical Photo / 产品外形图和实物图片
- Pin Arrangement (Top View) / 引出端排列（俯视图）
- Pin Function Symbol Table / 引出端功能符号表
- Absolute Maximum Ratings / 绝对最大额定值
- Recommended Operating Conditions / 推荐工作条件
- Performance Specifications / 性能指标
- Typical Characteristic Curves (Electrical Test Curves) / 主要特性曲线图（电特性测试图）
- Typical Application Circuit / 典型应用线路图
- Functional Modules and Operating Principles / 单元模块及工作原理
- Registers / 寄存器
- Power-to-Ground Protection / 电源地间保护
- Notes / 注意事项
- Common Faults and Remedies / 常见故障及处理办法
- Contact Information / 联系方式
- Additional Notes / 附加说明

Revision History / 版本修订记录

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20260 727	2026.07.27	——	首次发布 / First release	

Product Applications and Scope / 产品用途及应用范围

Medical imaging; high-speed imaging; radio receivers; portable measurement equipment.

医疗成像；高速成像；无线电接受机；便携式测量设备。

Standard / 标准

Detailed specification and approval number: Q/GC 0207-2026, "Detailed Specification for SXA036 Type 14-Bit 125MSPS A/D Converter, Semiconductor Integrated Circuit". Quality grade: enterprise standard.

详细规范及确认号：Q/GC 0207-2026《半导体集成电路 SXA036 型 14 位 125MSPS A/D 转换器详细规范》。质量等级：企标。

Features / 产品特点

特性 / Feature	规格 / Specification
模拟电源电压 / Analog Supply Voltage	1.8V
数字电源电压 / Digital Supply Voltage	1.8V
接口电源电压 / Interface Supply Voltage	1.8V
分辨率 / Resolution	14bit
转换速率 / Conversion Rate	125MSPS
信噪比 / SNR	≥75.9dBFS
无杂散动态范围 / SFDR	≥89dBFS
微分线性误差 / DNL	±0.3LSB
积分线性误差 / INL	±2.0LSB
功耗 / Power Consumption	≤150mW/每通道 (per channel)
模拟输入范围 / Analog Input Range	2VPP～2.6VPP
电路接口 / Interface	LVDS
ESD 等级 / ESD Rating	1C 级，HBM 模型，1000V (Class 1C, HBM model, 1000V)
产品重量 / Product Weight	0.20g±0.04g
湿敏等级和封装形式 / Moisture Sensitivity Level and Package	MSL3，QFN48

Product Description / 产品描述

This product is a 4-channel, 14-bit, 125 MSPS analog-to-digital converter (ADC) developed and designed specifically for low power, small size, and design flexibility. The maximum conversion rate of this product reaches 125 MSPS, featuring excellent dynamic performance and ultra-low power consumption, suitable for a wide range of application scenarios.

The ADC operates from a 1.8 V single supply with an LVPECL/CMOS/LVDS-compatible sampling clock signal. No external reference source or drivers are required.

Each internal channel can be independently shut down; with all channels disabled, typical power consumption is less than 14 mW. The ADC integrates multiple functions, including programmable clock output, data alignment, and digital test pattern generation. Available digital test patterns include: built-in fixed test patterns and pseudo-random test patterns, and user-defined test patterns via the serial port interface (SPI) are also supported.

This product is offered in a 48-pin plastic quad flat no-lead package (QFN48). The rated operating temperature range of the ADC is −40°C to +85°C.

The functional block diagram of this product is shown in Figure 1.

本产品是一款 4 通道，14 位，125 MSPS 采样率的模数转换器(Analog-to-Digital Converter，ADC)，专门针对低功耗、小尺寸和使用灵活性进行开发设计。该产品转换速率最高可达到 125 MSPS，具有优异的动态性能和超低功耗特性，适用多种应用场景。

该 ADC 采用 1.8 V 单电源供电和 LVPECL /CMOS/LVDS 兼容型采样时钟信号。无需外部基准电压源和驱动器即可满足需求。

支持独立关闭内部各通道功能；禁用全部通道后，典型功耗小于 14mW。该 ADC 内置多种功能，包括可编程时钟输出、数据对齐、生成数字测试码等。可获得的数字测试码包括：内置固定测试码和伪随机测试码，也支持用户通过串行端口接口(SPI)自定义测试码的方式。

本产品采用 48 引脚塑料四边无引线扁平封装（QFN48），该 ADC 额定工作范围为：-40°C 到+85°C

该产品功能框图如图 1 所示。

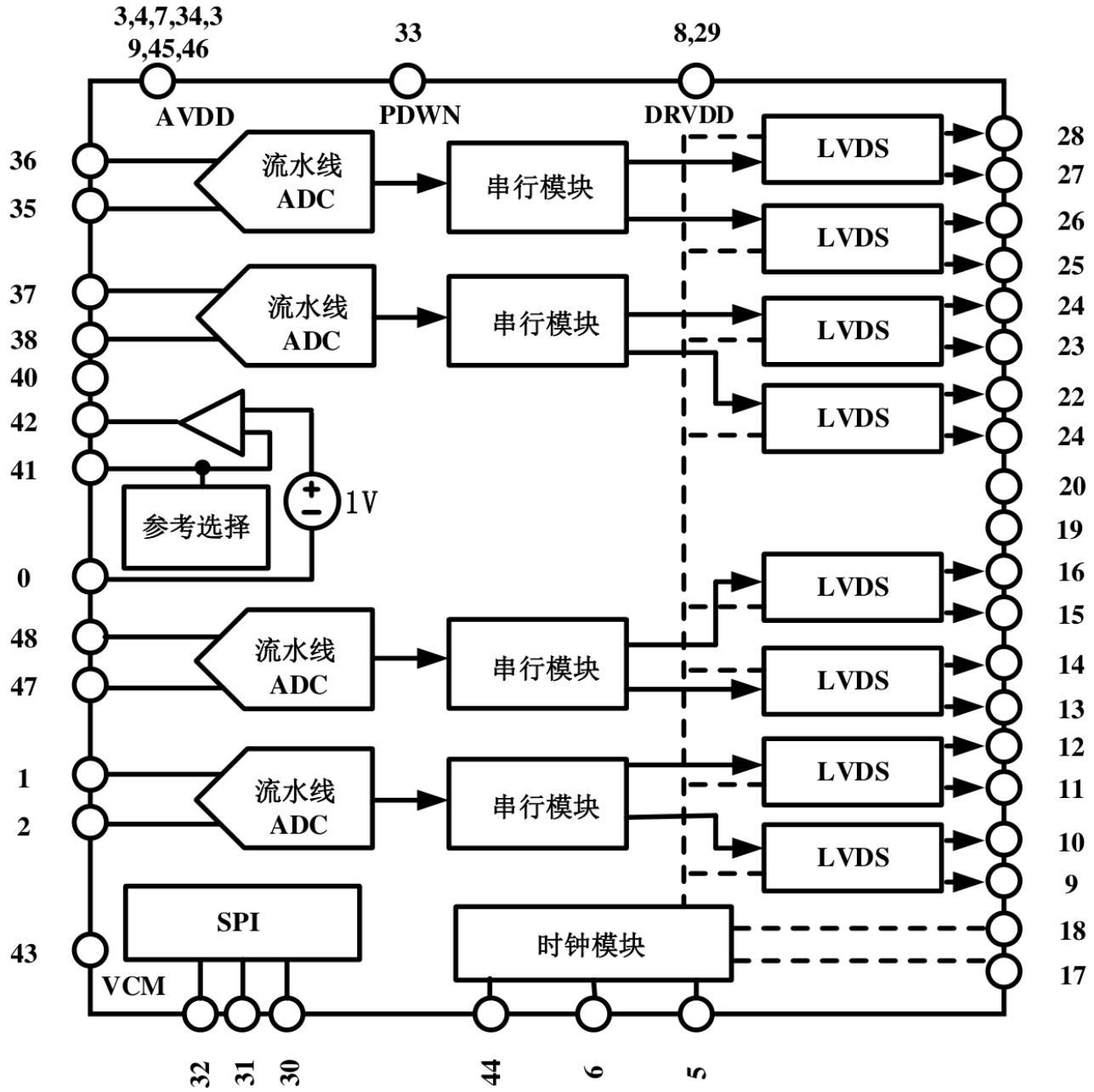


Figure 1: SXA036 Functional Block Diagram

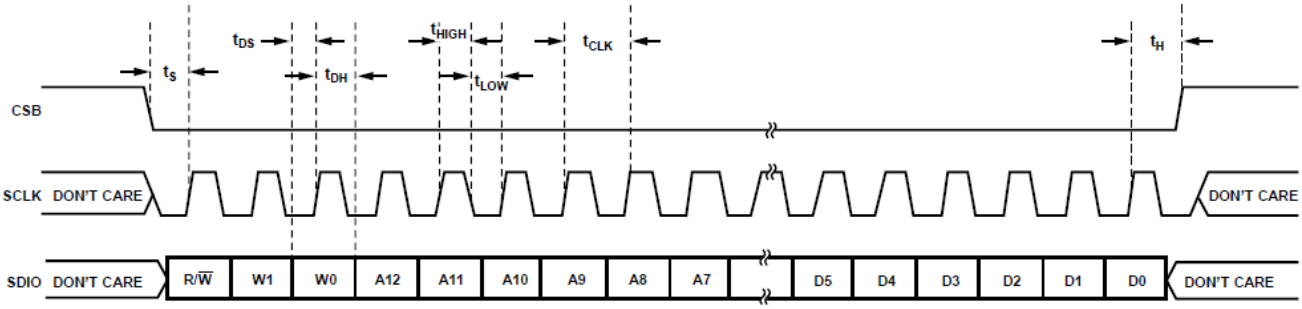


Figure 2: SPI Timing

Package Outline and Physical Photo / 产品外形图和实物图片

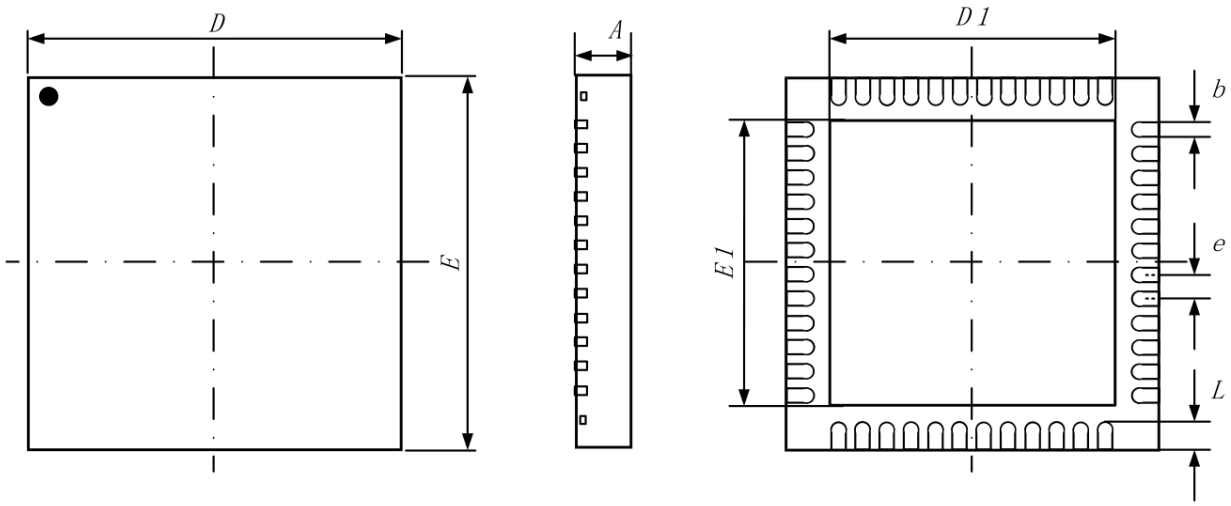


Figure 3: Product Outline Dimension Drawing

单位为毫米 / Units in mm

尺寸符号 / Dimension	最小 / Min	公称 / Nominal	最大 / Max	尺寸符号 / Dimension	最小 / Min	公称 / Nominal	最大 / Max
A	0.70	0.75	0.80	D	6.90	7.00	7.10
b	0.18	0.25	0.30	D1	5.50	5.60	5.70
e	—	0.50	—	E	6.90	7.00	7.10
L	0.35	0.40	0.45	E1	5.50	5.60	5.70

注 / Note:

The nominal values above are the actual nominal values of the package; users are recommended to refer to these dimensions for design and use. For recommended pad design, see the assembly instructions.

外壳实际公称值，推荐用户参考该尺寸设计使用；推荐焊盘设计详见电装说明。

Pin Arrangement (Top View) / 引出端排列（俯视图）

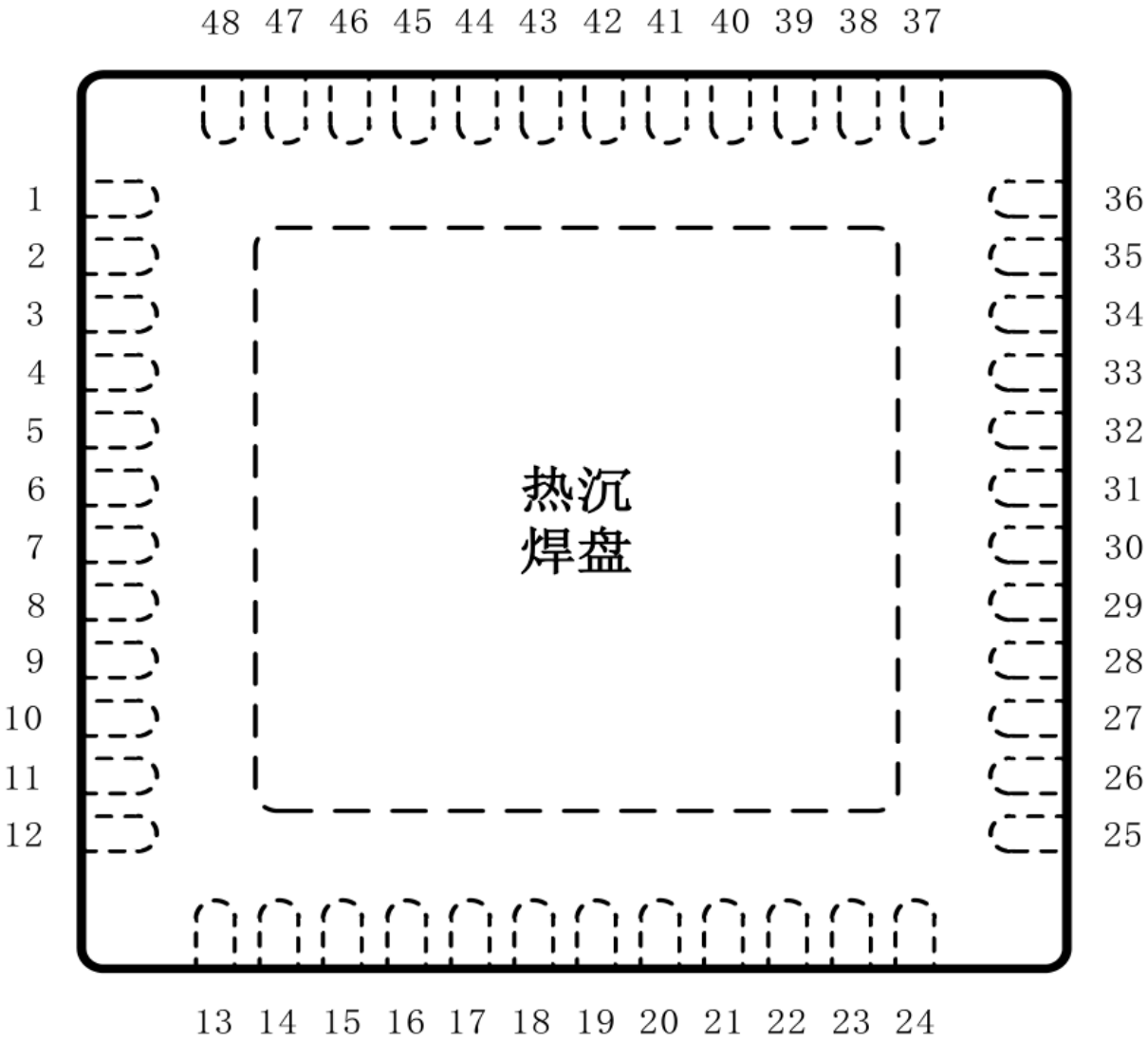


Figure 4: Pin Arrangement

Pin Function Symbol Table / 引出端功能符号表

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q
0	AGND	模拟地 / Analog Ground	/	25	D1A-	A 通道数字输出（-）/ Channel A Digital Output (−)	O
1	VIND+	ADC D 通道模拟输入(+) / ADC Channel D Analog Input (+)	I	26	D1A+	A 通道数字输出（+）/ Channel A Digital Output (+)	O
2	VIND-	ADC D 通道模拟输入(-) / ADC Channel D Analog Input (−)	I	27	D0A-	A 通道数字输出（-）/ Channel A Digital Output (−)	O

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q
3	AVDD	1.8V 模拟电源引脚 / 1.8V Analog Supply Pin	/	28	D0A+	A 通道数字输出（+）/ Channel A Digital Output (+)	O
4	AVDD	1.8V 模拟电源引脚 / 1.8V Analog Supply Pin	/	29	DRVDD	数字输出驱动器电源 / Digital Output Driver Supply	/
5	CLK-	差分时钟(-) / Differential Clock (−)	I	30	SCLK/DTP	SPI 时钟输入/数字测试码 / SPI Clock Input / Digital Test Pattern	I
6	CLK+	差分时钟(+) / Differential Clock (+)	I	31	SDIO/OLM	SPI 数据输入和输出 / SPI Data Input and Output	I
7	AVDD	1.8V 模拟电源引脚 / 1.8V Analog Supply Pin	/	32	CSB	SPI 片选信号 / SPI Chip Select	I
8	DRVDD	数字输出驱动器电源 / Digital Output Driver Supply	/	33	PDWN	数字输入(高电平=关断；低电平=工作) / Digital Input (High = Power-down; Low = Normal operation)	I
9	D1D-	D 通道数字输出（-）/ Channel D Digital Output (−)	O	34	AVDD	1.8V 模拟电源引脚 / 1.8V Analog Supply Pin	/
10	D1D+	D 通道数字输出（+）/ Channel D Digital Output (+)	O	35	VINA-	ADC A 通道模拟输入(-) / ADC Channel A Analog Input (−)	I
11	D0D-	D 通道数字输出（-）/ Channel D Digital Output (−)	O	36	VINA+	ADC A 通道模拟输入(+) / ADC Channel A Analog Input (+)	I
12	D0D+	D 通道数字输出（+）/ Channel D Digital Output (+)	O	37	VINB+	ADC B 通道模拟输入(+) / ADC Channel B Analog Input (+)	I
13	D1C-	C 通道数字输出（-）/ Channel C Digital Output (−)	O	38	VINB-	ADC B 通道模拟输入(-) / ADC Channel B Analog Input (−)	I
14	D1C+	C 通道数字输出（+）/ Channel C Digital Output (+)	O	39	AVDD	1.8V 模拟电源引脚 / 1.8V Analog Supply Pin	/
15	D0C-	C 通道数字输出（-）/ Channel C Digital Output (−)	O	40	RBIAS	设置模拟电流偏置 / Sets Analog Current Bias	I
16	D0C+	C 通道数字输出（+）/ Channel C Digital Output (+)	O	41	SENSE	基准电压模式选择 / Reference Voltage Mode Select	I
17	DCO-	数据时钟输出（-）/ Data Clock Output (−)	O	42	VREF	基准电压输入和输出引脚 / Reference Voltage Input/Output Pin	O
18	DCO+	数据时钟输出（+）/ Data Clock Output (+)	O	43	VCM	模拟输入共模电压 / Analog Input Common-Mode Voltage	O
19	FCO-	帧时钟输出（-）/ Frame Clock Output (−)	O	44	SYNC	数字输入，时钟分频器的 SYNC 输入 / Digital Input, Clock Divider SYNC Input	I
20	FCO+		O	45	AVDD	1.8V 模拟电源引脚 / 1.8V Analog Supply Pin	/

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/Q
		帧时钟输出（+）/ Frame Clock Output (+)					
21	D1B-	B 通道数字输出（-）/ Channel B Digital Output (−)	O	46	AVDD	1.8V 模拟电源引脚 / 1.8V Analog Supply Pin	/
22	D1B+	B 通道数字输出（+）/ Channel B Digital Output (+)	O	47	VINC-	ADC C 通道模拟输入(-) / ADC Channel C Analog Input (−)	I
23	D0B-	B 通道数字输出（-）/ Channel B Digital Output (−)	O	48	VINC+	ADC C 通道模拟输入(+) / ADC Channel C Analog Input (+)	I
24	D0B+	B 通道数字输出（+）/ Channel B Digital Output (+)	O				

Absolute Maximum Ratings / 绝对最大额定值

- 模拟电源电压（VDDA）/ Analog supply voltage (VDDA): 2V
- 数字电源电压（VDDD）/ Digital supply voltage (VDDD): 2V
- 贮存温度（Tstg）/ Storage temperature (Tstg): -65°C~150°C
- 结温（TJ）/ Junction temperature (TJ): 150°C

Recommended Operating Conditions / 推荐工作条件

- 工作频率（fCLK）/ Operating frequency (fCLK): 20MHz~125MHz
- 模拟电源电压（VDDA）/ Analog supply voltage (VDDA): 1.75V~1.9V
- 数字电源电压（VDDD）/ Digital supply voltage (VDDD): 1.75V~1.9V
- 输入信号幅度范围（峰峰值）/ Input signal amplitude range (peak-to-peak): ≤2V
- 模拟输入共模电压 / Analog input common-mode voltage: 0.8V~1.0V
- 工作环境温度（TA）/ Operating ambient temperature (TA): -40°C~85°C

Performance Specifications / 性能指标

条件（除另有规定外，VPP=2.0V，VAVDD=VDRVDD=1.8V，AGND=0V，Fs=125MSPS，-40°C≤TA≤85°C。）/ Conditions (unless otherwise specified, VPP=2.0V, VAVDD=VDRVDD=1.8V, AGND=0V, Fs=125MSPS, −40°C≤TA≤85°C.)

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小 / Min	典型值 / Typ	最大 / Max	单位 / Unit
分辨率 / Resolution	RES			14		bits
通道数 / Number of Channels	N			4		—
失调误差 / Offset Error	Eo		-0.9	-0.26	+0.3	%FSR

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小 / Min	典型值 / Typ	最大 / Max	单位 / Unit
增益误差 / Gain Error	Eg		-14	-4	+5	%FSR
微分线性误差 / Differential Nonlinearity	EDL	fIN=10MHz	-0.99	±0.3	+1.5	LSB
积分非线性误差 / Integral Nonlinearity	EIL	fIN=10MHz	-10	±2	+10	LSB
内部基准电压源 / Internal Reference Voltage	VREF		0.95	1	1.05	V
模拟输入共模电压范围 / Analog Input Common-Mode Voltage Range	VCM		0.8	0.9	1	V
功耗 / Power Consumption	PW	四通道 / Four channels	—	600	750	mW
转换率 / Conversion Rate	SR		20a		125a	MSPS
信噪比 / Signal-to-Noise Ratio	SNR	-1dBFS，fIN=10MHz	69	75.9	—	dBFS
信噪失真比 / Signal-to-Noise and Distortion Ratio	SINAD	-1dBFS，fIN=10MHz	68	75.5	—	dBFS
有效位 / Effective Number of Bits	ENOB	-1dBFS，fIN=10MHz	11	12.1	—	bits
无杂散动态范围 / Spurious-Free Dynamic Range	SFDR	-1dBFS，fIN=10MHz	82	89	—	dBFS
逻辑输入高电平（SCLK、SDIO、CSB）/ Logic Input High Level (SCLK, SDIO, CSB)	VIH		1.2		1.8	V
逻辑输入低电平（SCLK、SDIO、CSB）/ Logic Input Low Level (SCLK, SDIO, CSB)	VIL		0		0.75	V

a: This operating rate is the maximum/minimum rate only when the divider function is not enabled; if the divider is enabled, multiply by the corresponding division factor. For example, with an 8× divider, the maximum input clock is 1GSPS.

该工作速率仅为不启用分频器功能时的最高/最低速率，若启用分频器，则乘以相应的分频数，例如 8 分频最高输入时钟为 1GSPS。

注 / Note: 典型值为常温测试数据 / Typical values are room-temperature test data.

Typical Characteristic Curves (Electrical Test Curves) / 主要特性曲线图（电特性测试图）

1. Spectrum plot under fs=125MSPS, fIN=10MHz conditions

1、fs=125MSPS，fIN=10MHz 条件下频谱图

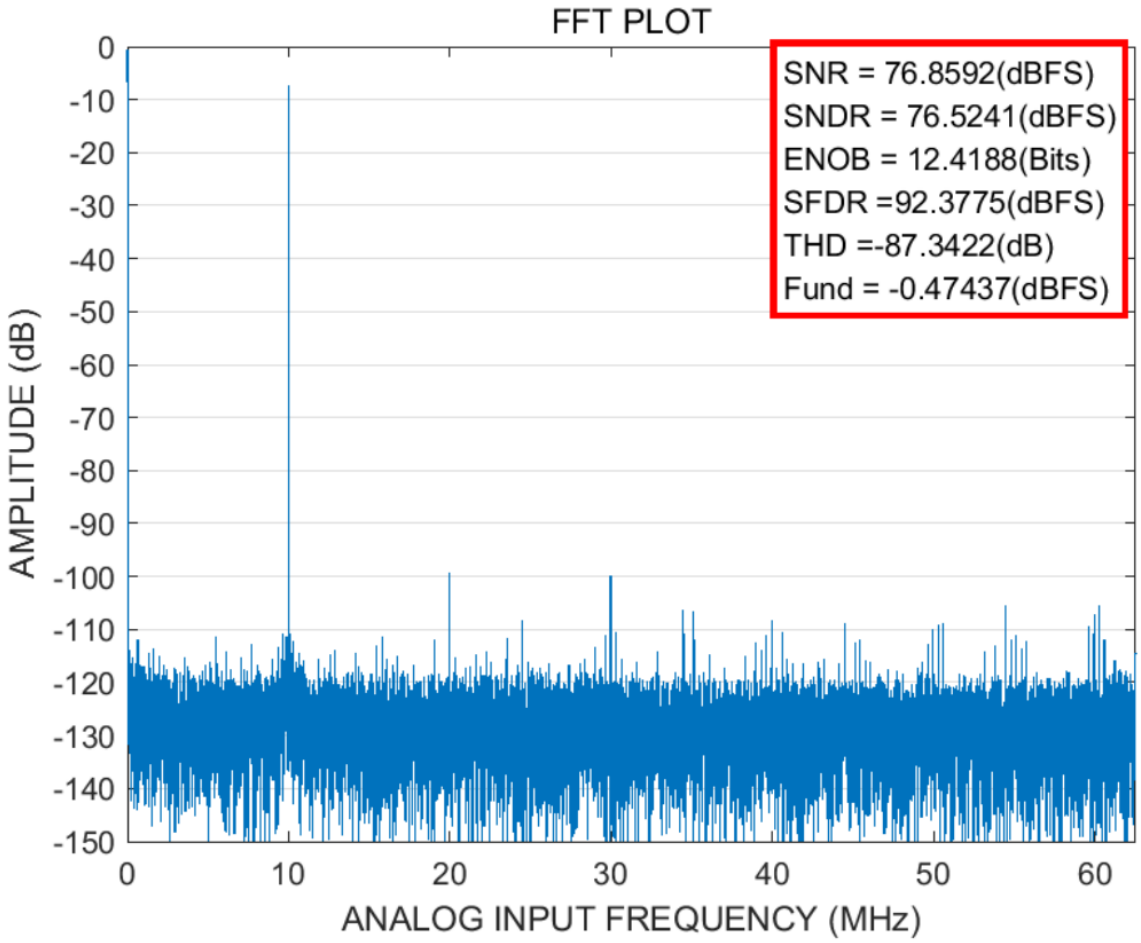


Figure 5: Single-Tone 32K (fIN=10MHz, fS=125MSPS), TA=25°C

2. Spectrum plot under fs=125MSPS, fIN=70MHz conditions

2、fs=125MSPS，fIN=70MHz 条件下频谱图

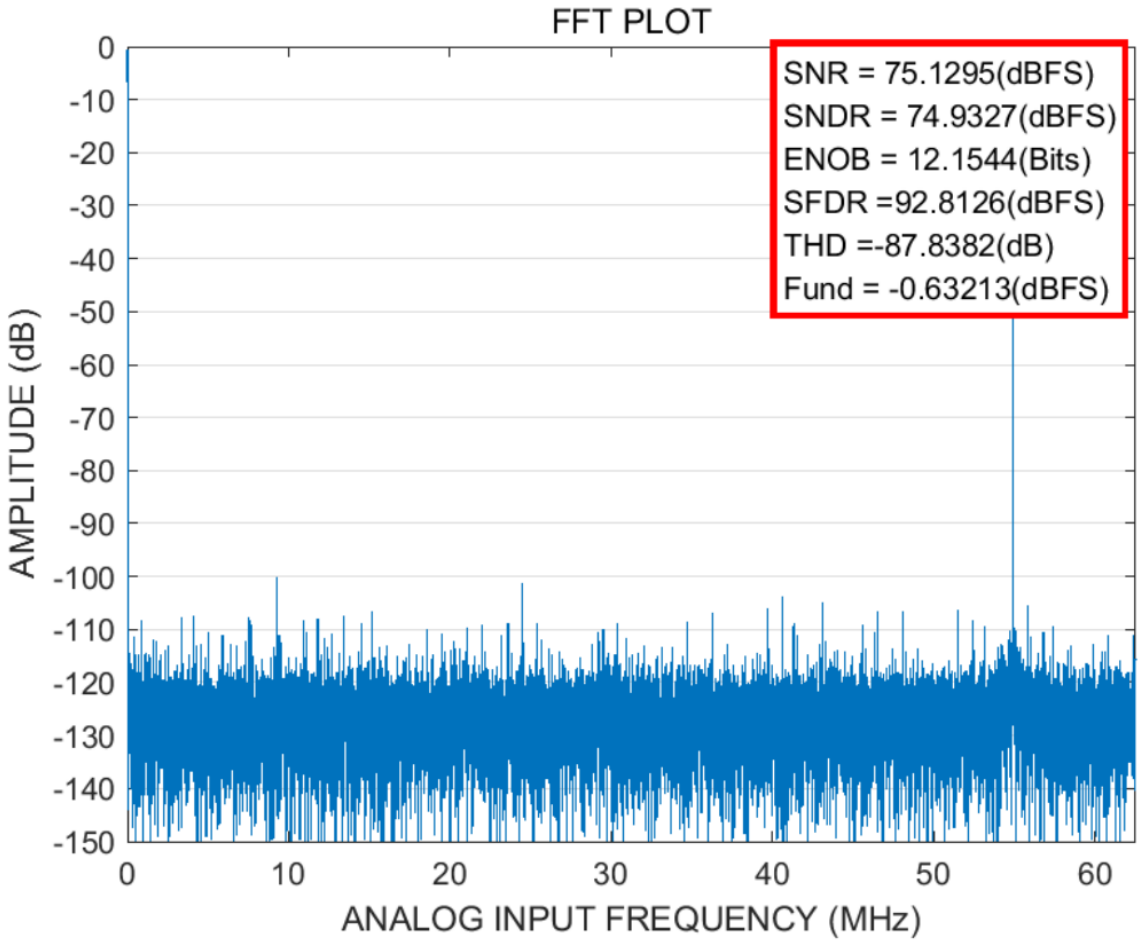


Figure 6: Single-Tone 32K (fIN=70MHz, fS=125MSPS), TA=25°C

3. Spectrum plot under fs=125MSPS, fIN=125MHz conditions

3、fs=125MSPS，fIN=125MHz 条件下频谱图

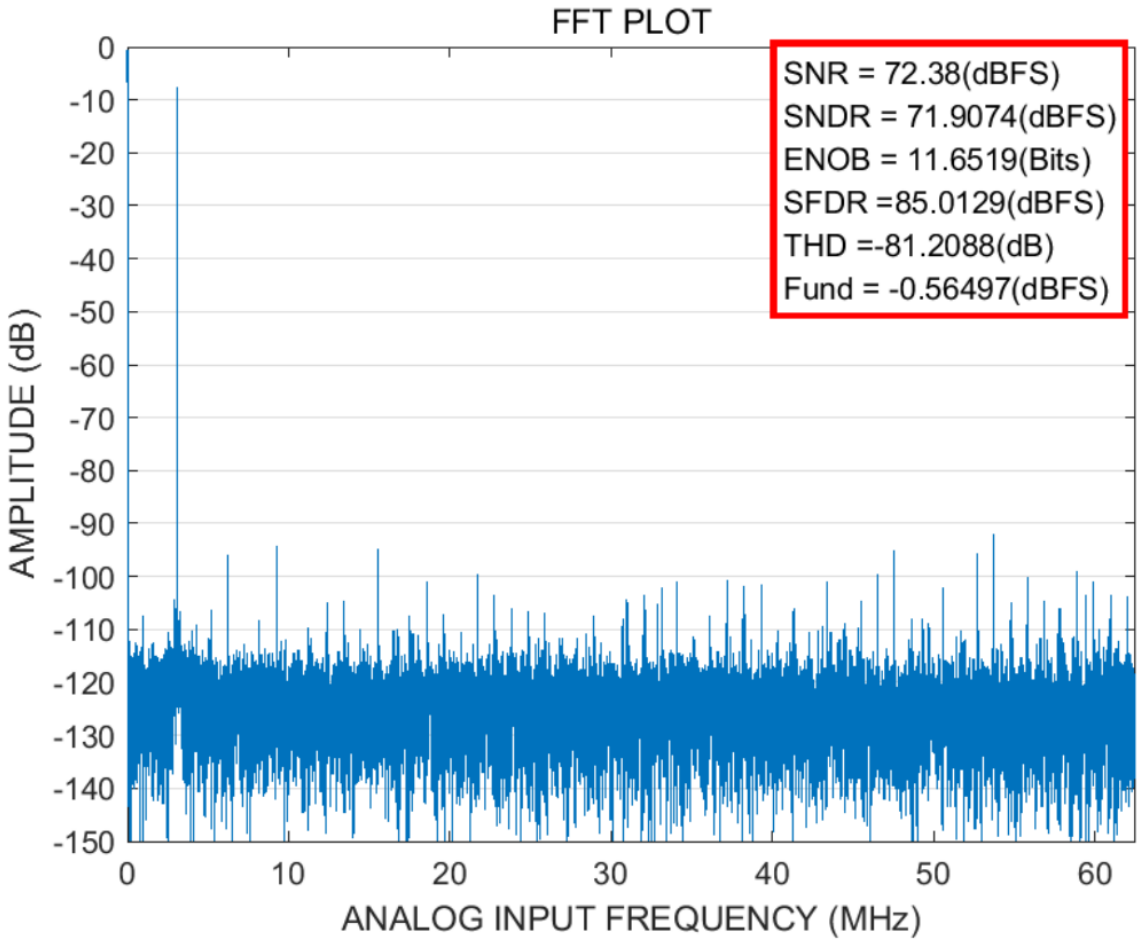


Figure 7: Single-Tone 32K (fIN=128MHz, fS=125MSPS), TA=25°C

4. Spectrum plot under fs=125MSPS, fIN=200MHz conditions

4、fs=125MSPS，fIN=200MHz 条件下频谱图

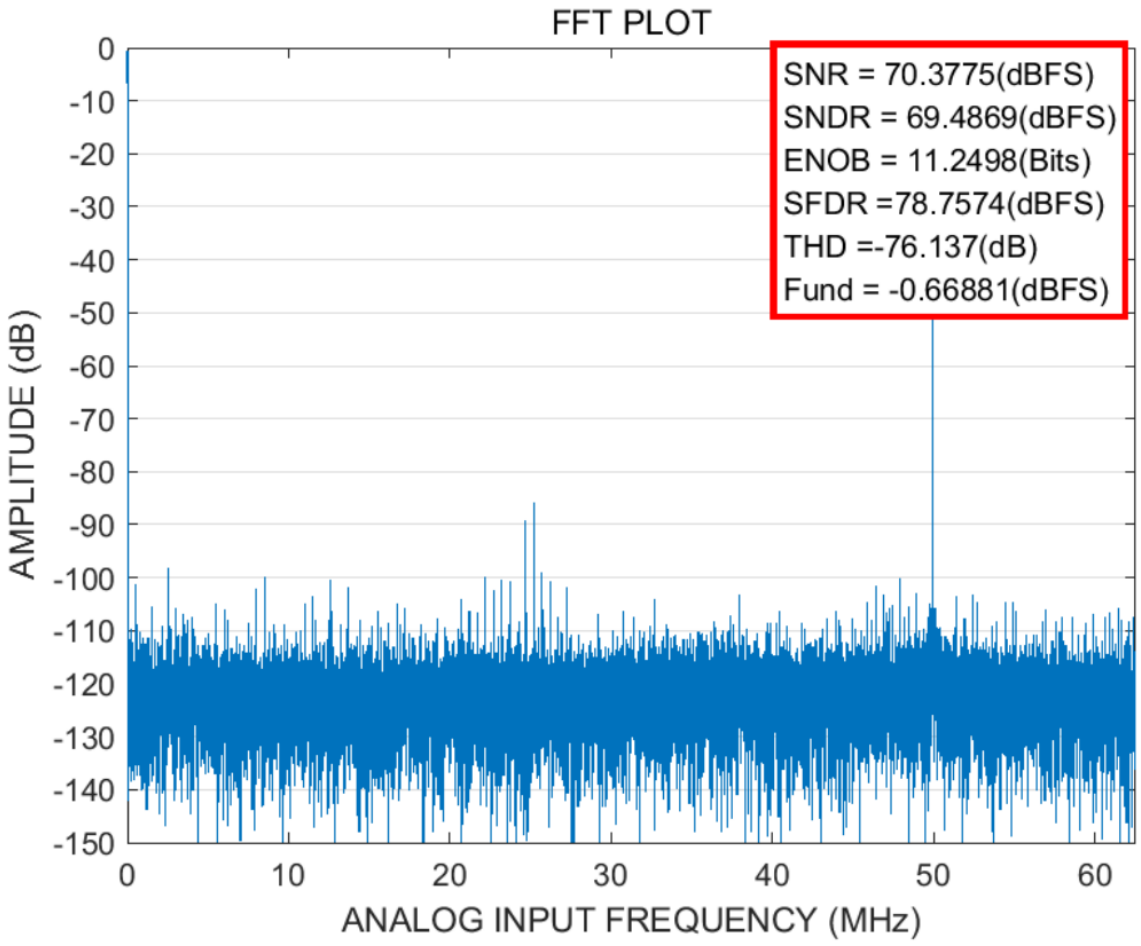


Figure 8: Single-Tone 32K (fIN=200MHz, fS=125MSPS), TA=25°C

5. Differential nonlinearity error and integral nonlinearity error plot

5、微分非线性误差和积分非线性误差图

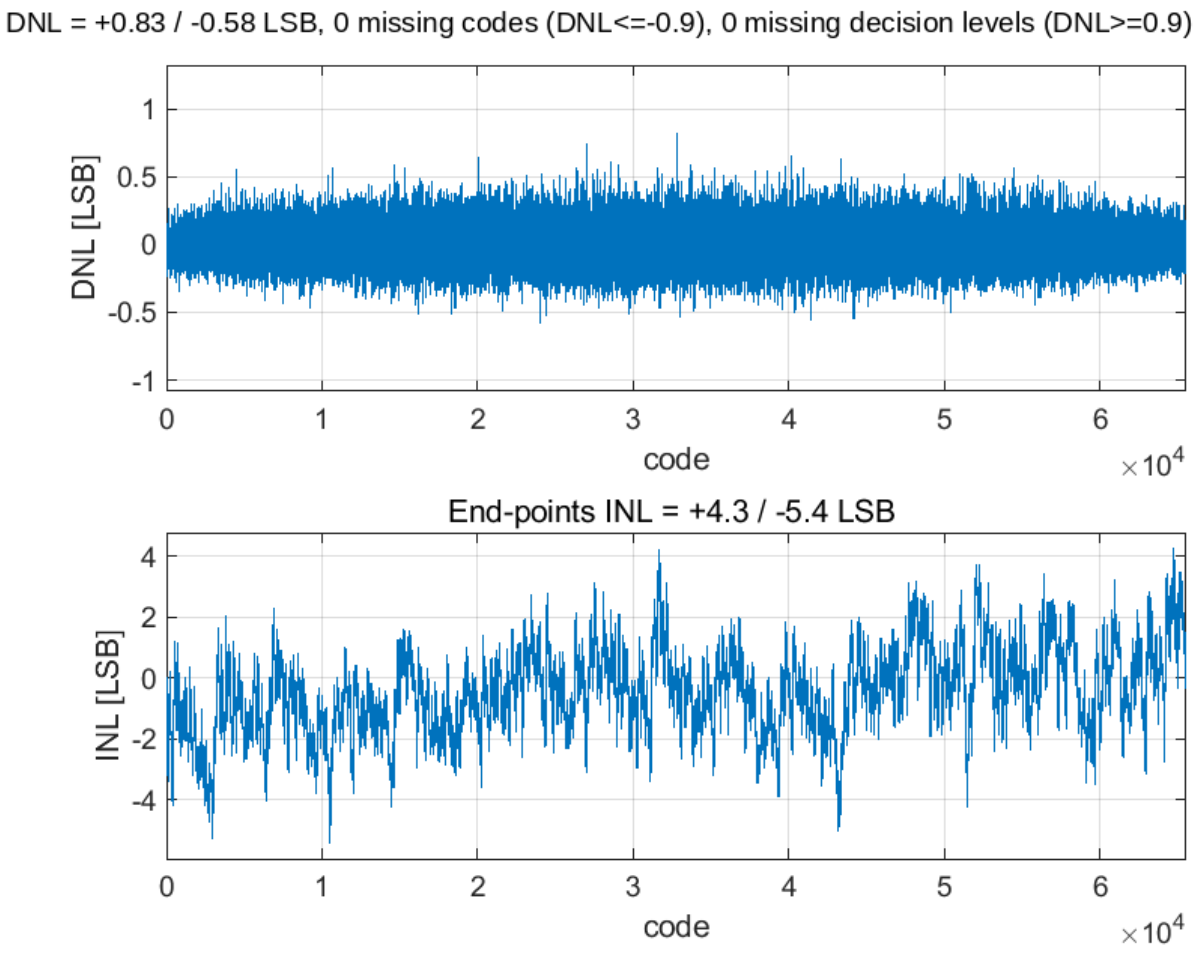


Figure 9: DNL/INL (fIN=10MHz, fS=125MSPS), TA=25°C

Typical Application Circuit / 典型应用线路图

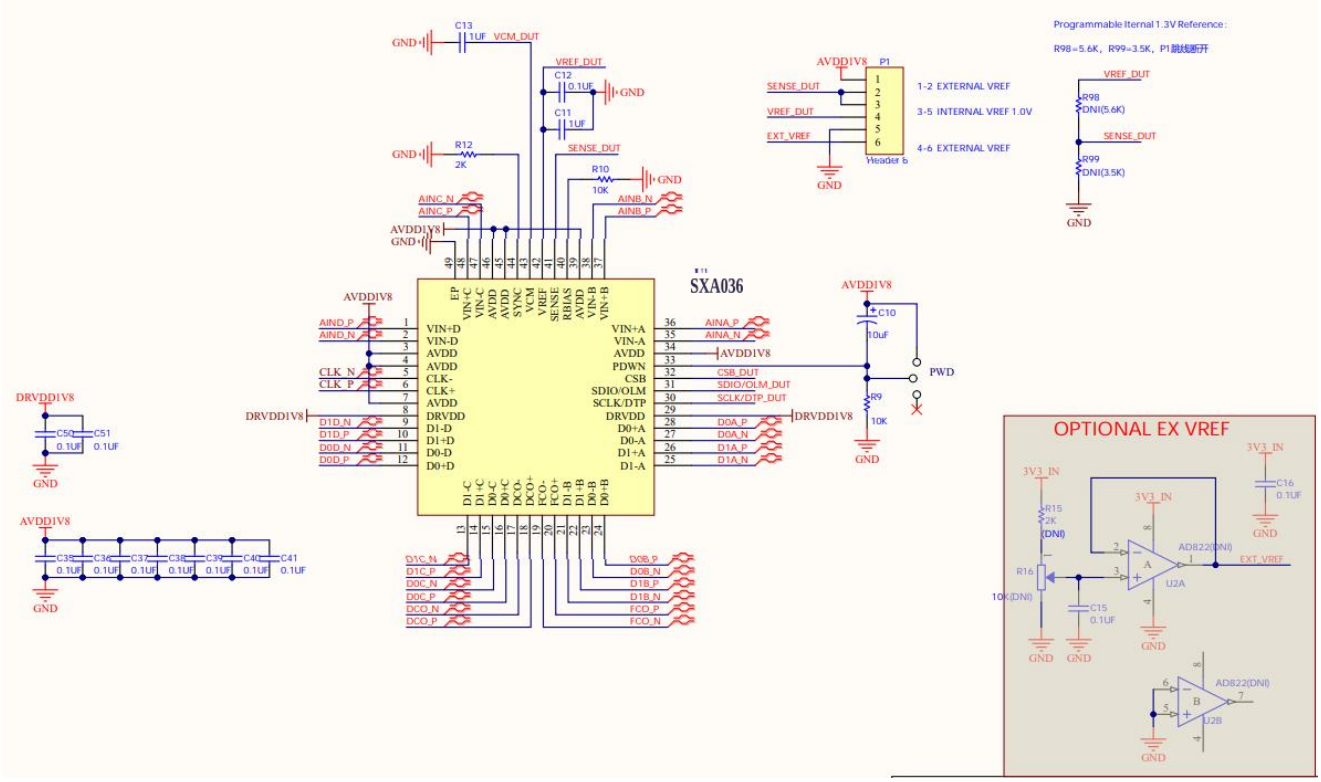


Figure 10: Typical Application Circuit

Functional Modules and Operating Principles / 单元模块及工作原理

1. Theory Overview / 原理概述

The core of this product uses a multi-stage pipelined ADC architecture, with each stage providing one redundant bit to eliminate the offset error of the coarse-quantization comparators. The pipelined quantization structure of each stage is reconstructed in the digital domain by a shift adder to form a 14-bit conversion result. The serializer transmits this conversion result in a fourteen-bit output format.

Except for the last stage, each stage of the pipeline consists of a low-resolution Flash ADC, a connected switched-capacitor DAC, and an inter-stage residue amplifier (e.g., a multiplying digital-to-analog converter [MDAC]). The residue amplifier amplifies the difference between the reconstructed DAC output and the Flash input for the next stage of the pipeline. To aid digital correction of Flash errors, each stage is set with one bit of redundancy. The last stage consists only of a Flash ADC.

本产品内核使用多级流水线型 ADC 架构，各级提供一位冗余位消除粗量化比较器的失调误差。各级流水线量化结构在数字域由移位加法器重构形成 14 位转换结果。串化器以十四位输出格式发送该转换结果。

除最后一级以外，流水线的每一级都由一个低分辨率 Flash 型 ADC、与之相连的一个开关电容 DAC 和一个级间余量放大器(例如乘法数模转换器[MDAC])组成。余量放大器放大重构 DAC 输出与 Flash 型输入之差，以便提供给流水线的下一级。为了帮助对 Flash 误差进行数字校正，每一级设定了一位的冗余量。最后一级仅由一个 Flash 型 ADC 组成。

2. Analog Input / 模拟输入

The analog input of this product is a differential switched-capacitor circuit designed to handle differential input signals. This circuit supports a wide common-mode range while maintaining excellent performance. Signal-dependent errors are minimized and optimal performance is achieved when the input common-mode voltage is at the mid-supply voltage.

本产品的模拟输入端为一个差分开关电容电路，设计用于处理差分输入信号。该电路支持宽共模范围，同时能保持出色的性能。当输入共模电压为中间电源电压时，信号相关误差最小，并且能实现最佳性能。

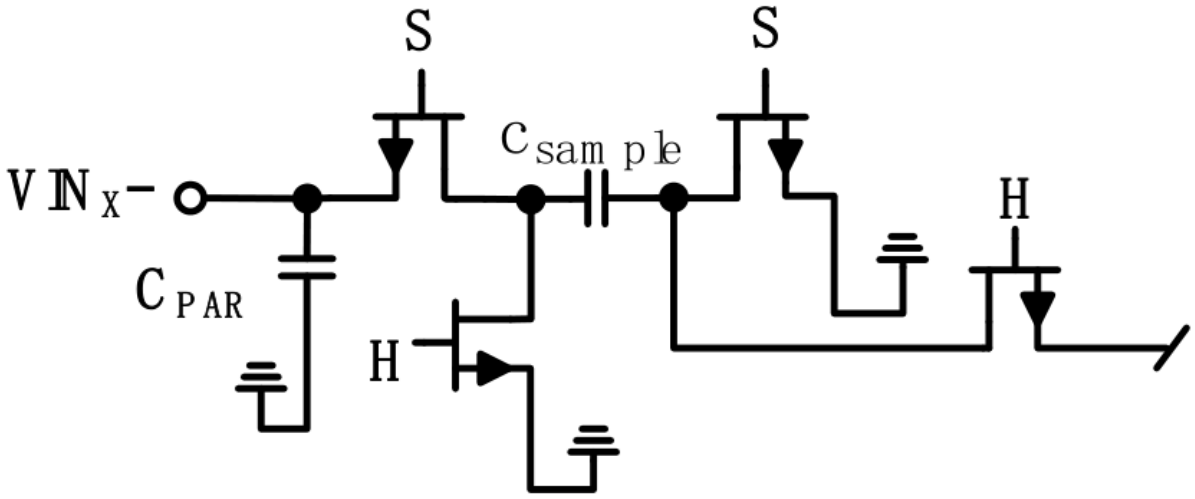


Figure 11: Analog Input Equivalent Circuit

3. Input Common-Mode Level / 输入共模电平

The analog input of this product has no internal DC bias; in AC-coupled applications, the user must provide an external bias. For optimal dynamic performance, the user must configure the device so that the input common-mode level VCM = AVDD/2.

This product provides an on-chip reference voltage through the VCM pin; the VCM pin must be bypassed to ground with a 0.1F capacitor .

In a differential configuration, setting the device input to the maximum range achieves the highest signal-to-noise ratio (SNR) performance. For this product, the input range depends on the reference voltage; exceeding the input range will sharply degrade performance.

本产品的模拟输入端无内部直流偏置，在交流耦合应用中，用户必须提供外部偏置。为了获得最佳的动态性能，用户必须对器件进行配置，使输入共模电平 VCM=AVDD/2。

本产品通过引脚 VCM 提供片内基准电压，必须使用一个 0.1F 电容将 VCM 引脚旁路到地。

在差分配置中，将器件输入设置为最大范围可以实现最高的信噪比(SNR)性能，对于本产品输入范围取决于基准电压，超过输入范围性能将急剧恶化。

4. Differential Input Configuration / 差分输入配置

There are various active and passive ways to effectively drive this product; driving differentially suppresses even-order harmonics to achieve optimal performance.

In baseband applications, driving this product with a differential balun configuration provides excellent performance and a flexible interface for the ADC (refer to Figure 11).

In applications where SNR is a critical parameter, because the noise performance of most amplifiers is insufficient to meet the true performance of this product, the input configuration requires differential transformer coupling (refer to Figure 12).

The value of capacitor C1 in the above two applications must be selected to match the input spectrum; it is recommended to reduce this capacitance or remove it when converting high-frequency analog input signals.

Single-ended input drive of this product is not recommended.

有多种有源和无源方式可以有效驱动本产品，通过差分方式驱动可以抑制偶次谐波从未获得最佳性能。

在基带应用中，利用差分巴伦配置驱动本产品能够为 ADC 提供出色的性能和灵活接口（参考图 11）。

在 SNR 为关键参数的应用中，因为绝大部分放大器的噪声性能不足以满足本产品的真实性能，所以输入配置要求采用差分变压器耦合(参考图 12)。

以上两种应用中的电容 C1 的选值需要和输入频谱配合选择，建议转换高频模拟输入信号时减小该电容容值或者移除该电容。

不建议单端输入方式驱动本产品。

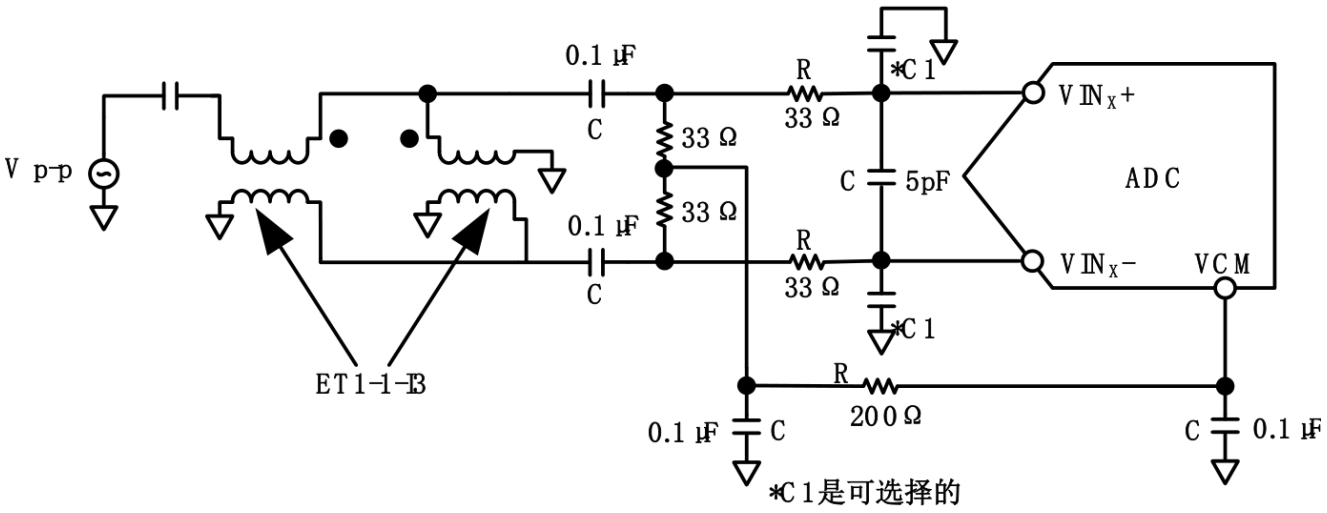


Figure 12: Differential Dual-Balun Configuration

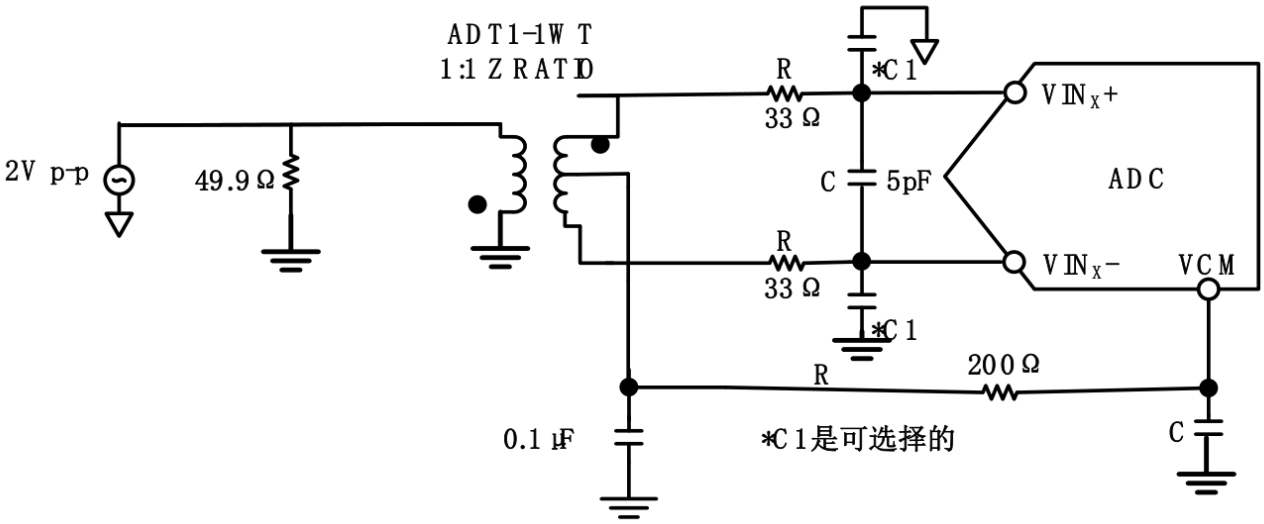


Figure 13: Differential Transformer Coupling

5. Reference Voltage / 基准电压

This product has a built-in stable, accurate reference voltage source. VREF can be configured using the internal 1.0 V reference, an externally applied 1.0 V to 1.3 V reference, or an external resistor divider acting on the internal reference, to generate a user-selectable reference voltage. See the "Internal Reference Voltage Connection" section and the "External Reference Voltage" section for a description of reference source modes. The VREF pin should be bypassed to ground through the parallel combination of an external low equivalent series resistance (ESR) 1.0μF capacitor and a low ESR 0.1μF ceramic capacitor.

The built-in comparator of this product can detect the voltage on the SENSE pin, thereby configuring the reference voltage into one of three possible modes. If the SENSE pin is grounded, the reference voltage amplifier switch is connected to the internal resistor divider (see Figure 13), thus setting the VREF pin voltage V to 1.0 V. If the SENSE pin is connected to an external resistor divider (see Figure 14), VREF is defined as:

VREF = 0.5 x (1 + R2/R1)

where 7 kΩ ⩽ (R1 + R2) ⩽ 10 kΩ

本产品内置稳定、精确的基准电压源。VREF 可以利用内部 1.0 V 基准电压、外部施加的 1.0 V 至 1.3 V 基准电压或作用于内部基准电压的外部电阻分压器来配置，产生用户可选的基准电压。基准电压源模式说明参见"内部基准电压连接"部分和"外部基准电压"部分。VREF 引脚应通过外部一个低等效串联电阻(ESR)1.0μF 电容和一个低 ESR 0.1μF 陶瓷电容的并联旁路至地。

本产品的内置比较器可检测出 SENSE 引脚的电压，从而将基准电压配置成三种可能的模式之一。如果 SENSE 引脚接地，则基准电压放大器开关与内部电阻分压器相连(见图 13)，因而将 VREF 引脚电压 V 设为 1.0 V。如果 SENSE 引脚连接到外部电阻分压器(见图 14)，则 VREF 定义为：

VREF=0.5 x (1 + R2/R1)

其中，7 kΩ ⩽ (R1 + R2) ⩽ 10 kΩ

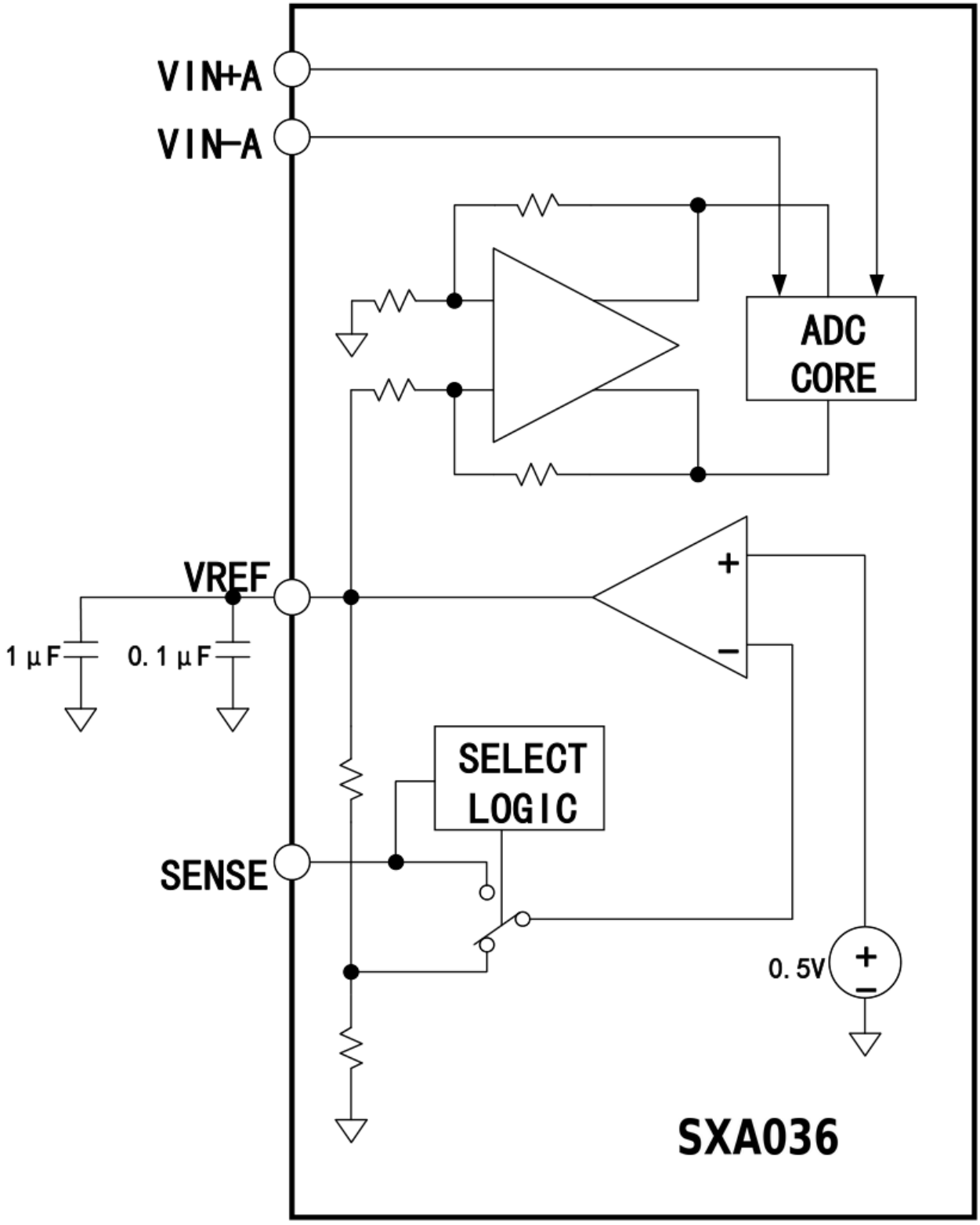


Figure 14: 1.0V Reference Voltage Configuration

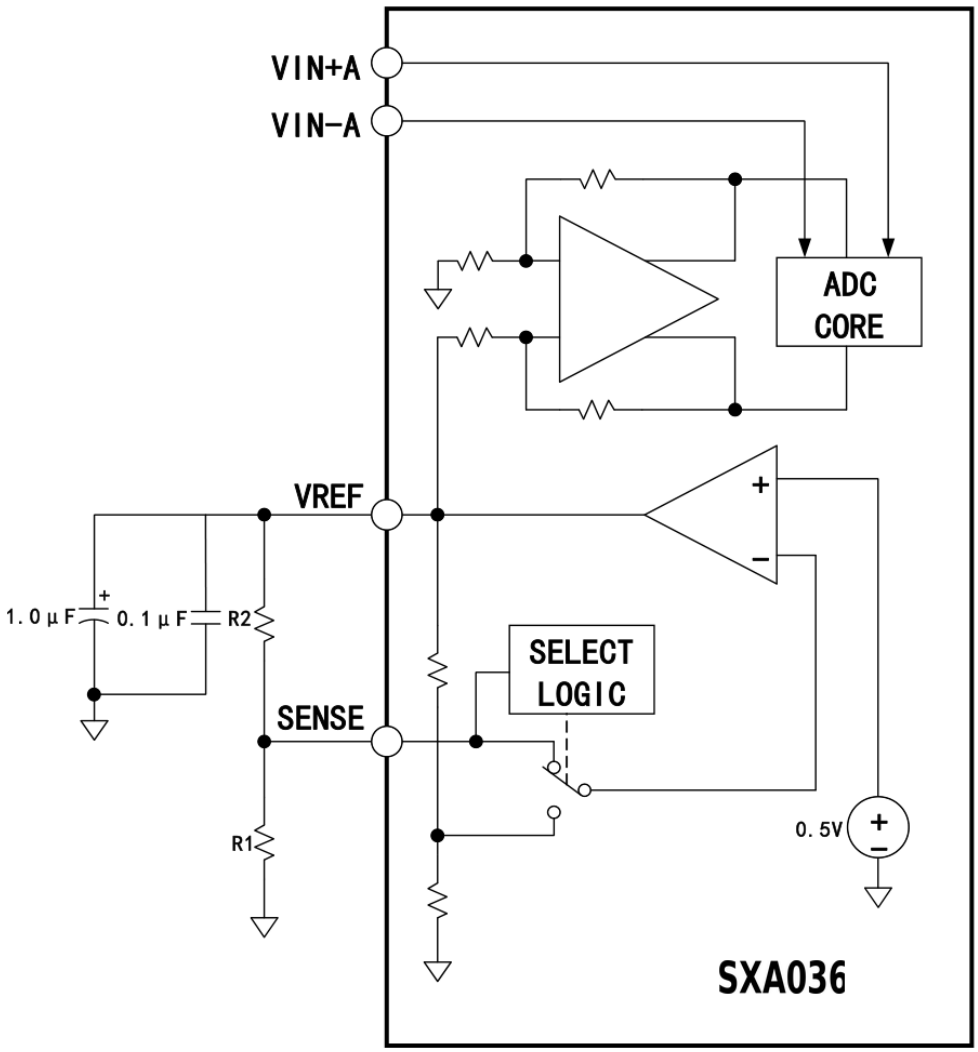


Figure 15: External Reference Voltage Configuration

If the internal reference voltage of this product is used to drive multiple converters to improve gain matching, the load of the other converters on the reference voltage must be considered. Figure 15 and Figure 16 show how the load affects the internal reference voltage.

如需利用本产品的内部基准电压来驱动多个转换器，从而提高增益的匹配度，则必须考虑到其它转换器对基准电压的负载。图 15 和图 16 显示负载如何影响内部基准电压。

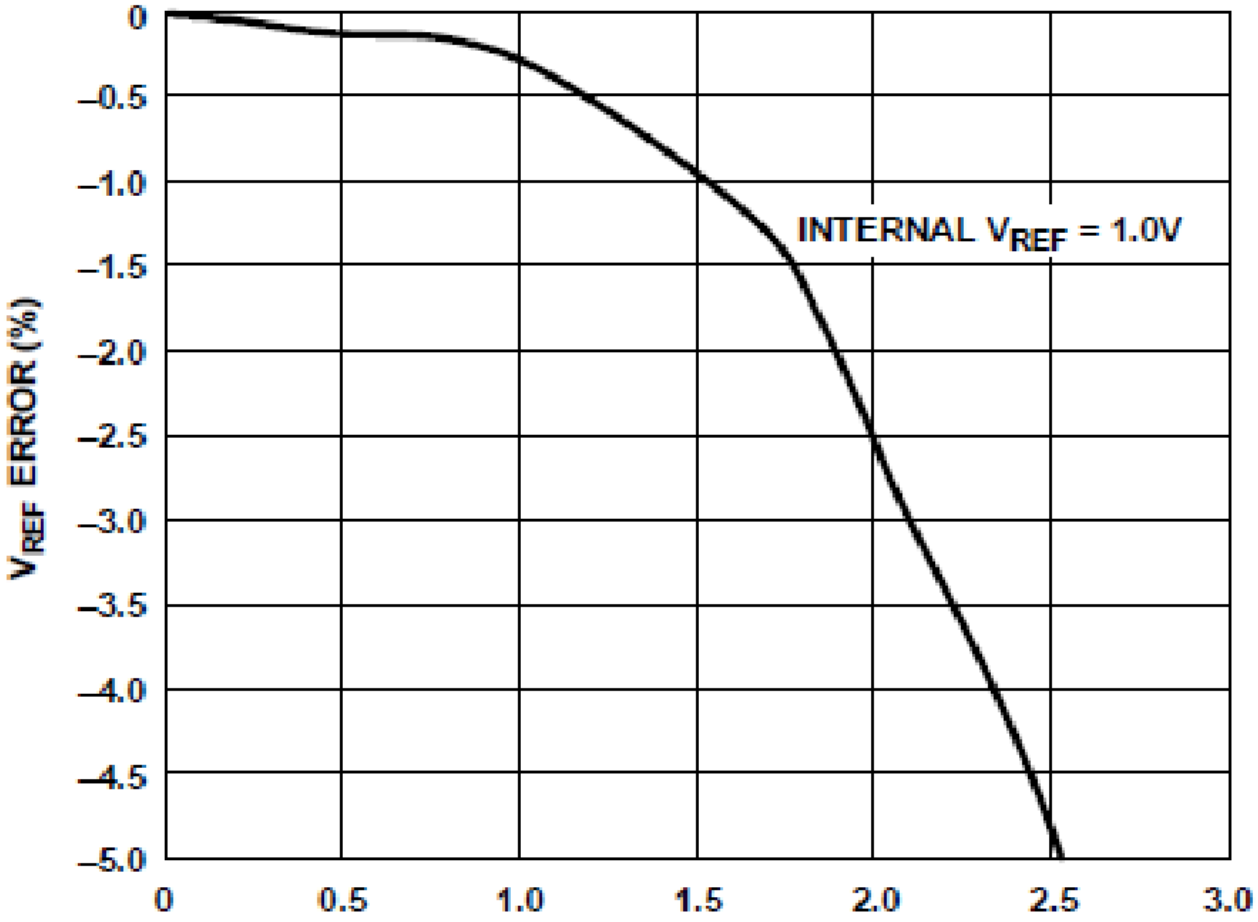


Figure 16: VREF Error (Internal VREF = 1.0 V) vs. Load Current

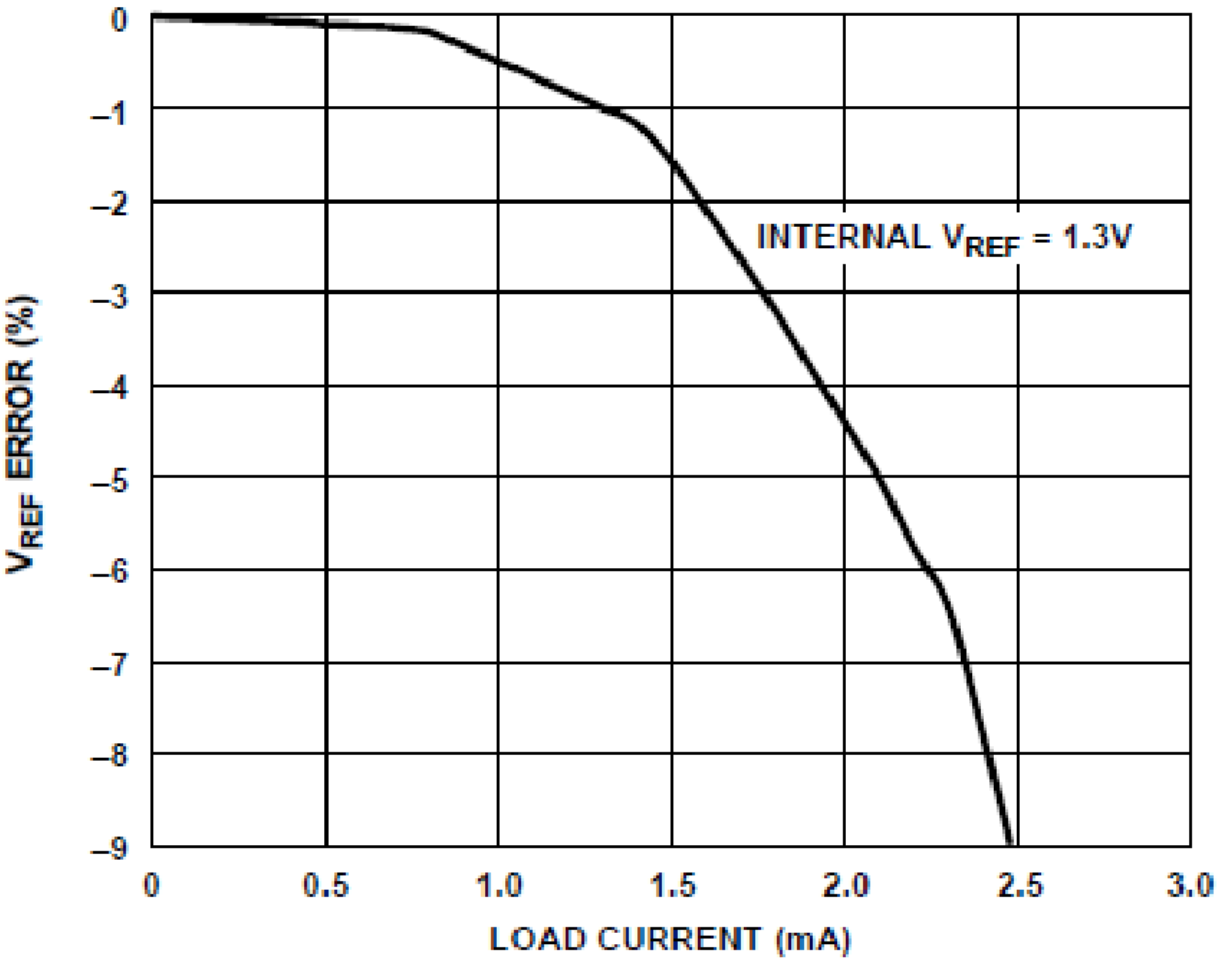


Figure 17: VREF Error (Internal VREF = 1.3 V) vs. Load Current

6. External Reference Voltage / 外部基准电压

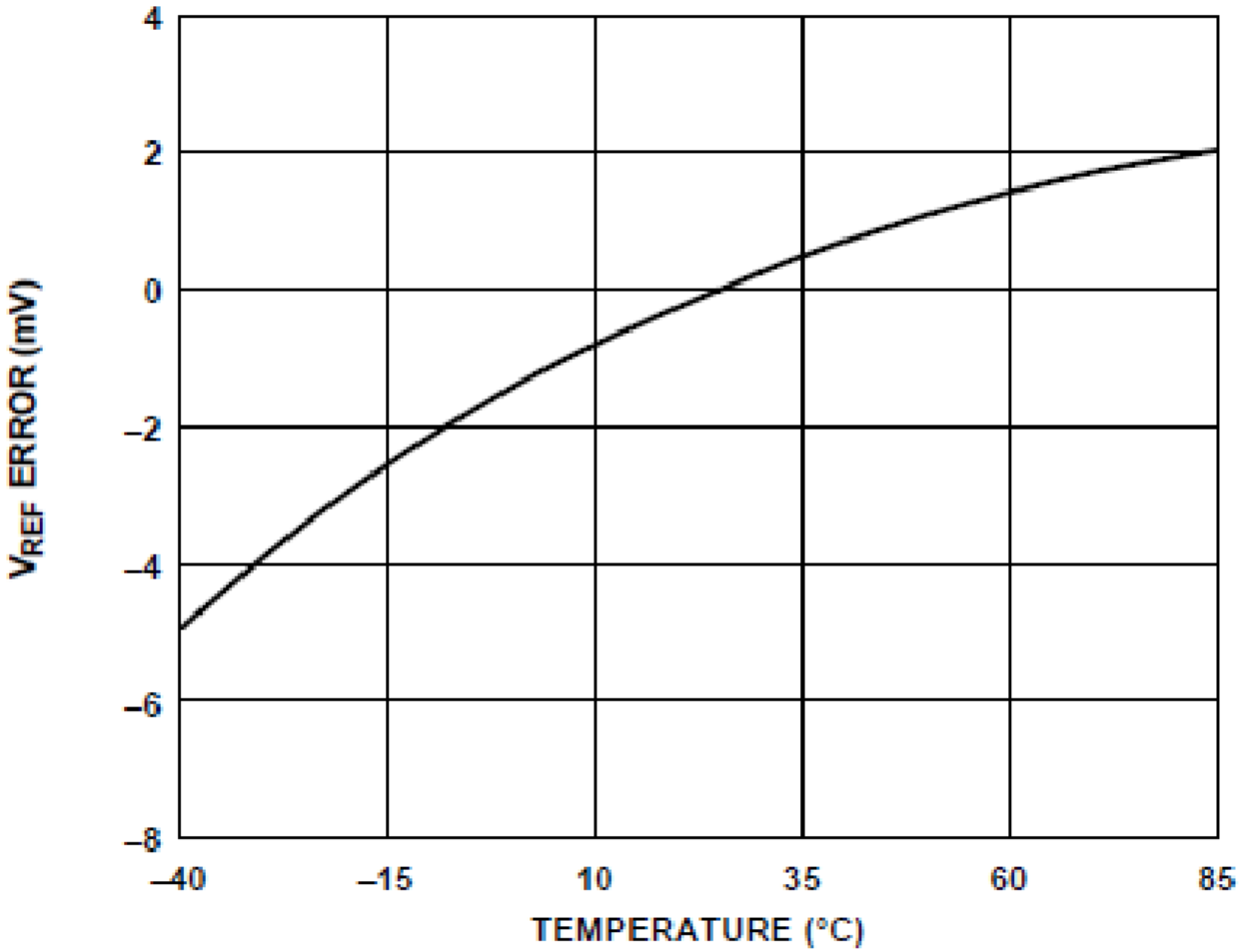


Figure 18: VREF Error vs. Temperature (VREF = 1.0 V Typical Drift)

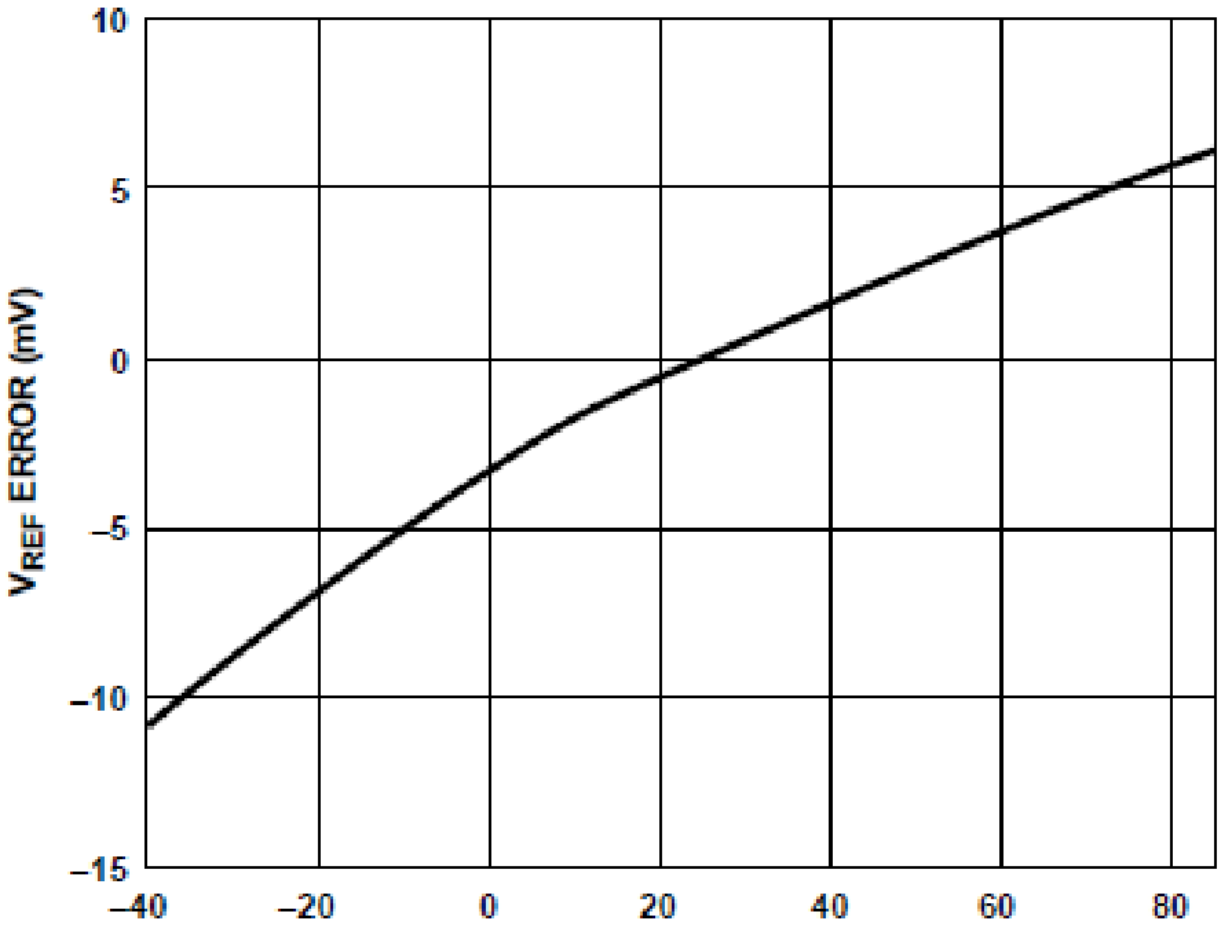


Figure 19: VREF Error vs. Temperature (VREF = 1.3 V Typical Drift)

An external reference voltage must be used to further improve ADC gain accuracy and thermal drift characteristics. Figure 17 and Figure 18 show the typical drift characteristics of the internal reference voltage source in 1.0 V mode and 1.3 V mode, respectively. Connecting the SENSE pin to AVDD disables the internal reference voltage source, allowing the use of an external reference voltage source. The load of the internal reference buffer on the external reference source is equivalent to a 7.5 kΩ load. The internal buffer generates the positive and negative full-scale reference voltages for the ADC core. Leaving the SENSE pin floating is not recommended.

必须采用外部基准电压才可能进一步提高 ADC 增益精度、改善热漂移特性。图 17 和图 18 显示内部基准电压源分别在 1.0 V 模式和 1.3 V 模式下的典型漂移特性。将 SENSE 引脚与 AVDD 相连时，可以禁用内部基准电压源，从而允许使用外部基准电压源。内部基准电压缓冲器对外部基准电压源的负载相当于 7.5 kΩ 负载。内部缓冲器为 ADC 内核生成正、负满量程基准电压。不建议悬空 SENSE 引脚。

7. Clock Input Considerations / 时钟输入考虑

To fully exploit the performance of the chip, a differential signal should be used as the sampling clock input (CLK+ and CLK−) of this product. This signal is typically AC-coupled into the CLK+ and CLK− pins using a transformer or capacitors. These two pins are internally biased, so no external bias is required.

为了充分发挥芯片的性能，应利用一个差分信号作为本产品采样时钟输入端(CLK+和 CLK−)的时钟信号。该信号通常使用变压器或电容器交流耦合到 CLK+和 CLK−引脚内。这两个引脚有内部偏置，无需外部偏置。

8. Clock Input / 时钟输入

This product has a flexible clock input structure. CMOS, LVDS, LVPECL, or sine-wave signals can all serve as its clock input signal. Regardless of which signal is used, clock source jitter must be taken into account (see the jitter considerations section). A low-jitter clock source's single-ended signal can be converted to a differential signal using an RF transformer or RF balun. For clock frequencies from 125 MHz to 1 GHz, the RF balun configuration is recommended; for clock frequencies from 40 MHz to 200 MHz, the RF transformer configuration is recommended. Schottky diodes connected across the transformer/balun secondary winding can limit the clock signal fed into this product to approximately 0.8V peak-to-peak differential (see Figure 19 and Figure 20).

This both prevents large-voltage-swing clock feedthrough to other parts of this product and preserves the fast rise and fall times of the signal, which is important for achieving low-jitter performance. However, when the frequency exceeds 500 MHz, diode capacitance will have an effect. Appropriate signal-limiting diodes must be carefully selected.

本产品具有灵活的时钟输入结构。CMOS、LVDS、LVPECL 或正弦波信号均可作为其时钟输入信号。无论采用哪种信号，都必须考虑到时钟源抖动(见抖动考虑部分说明)。利用射频变压器或射频巴伦，可将低抖动时钟源的单端信号转换成差分信号。对于 125 MHz 至 1 GHz 的时钟频率，建议采用射频巴伦配置；对于 40 MHz 至 200 MHz 的时钟频率，建议采用射频变压器配置。跨接在变压器/巴伦次级绕组上的肖特基二极管可以将输入到本产品中的时钟信号限制为约差分 0.8V 峰峰值(见图 19 和图 20)。

这样，既可以防止时钟的大电压摆幅馈通至本产品的其它部分，还可以保留信号的快速上升和下降时间，这一点对实现低抖动性能来说非常重要。但是，当频率高于 500 MHz 时，二极管电容会产生影响。必须小心选择适当的信号限幅二极管。

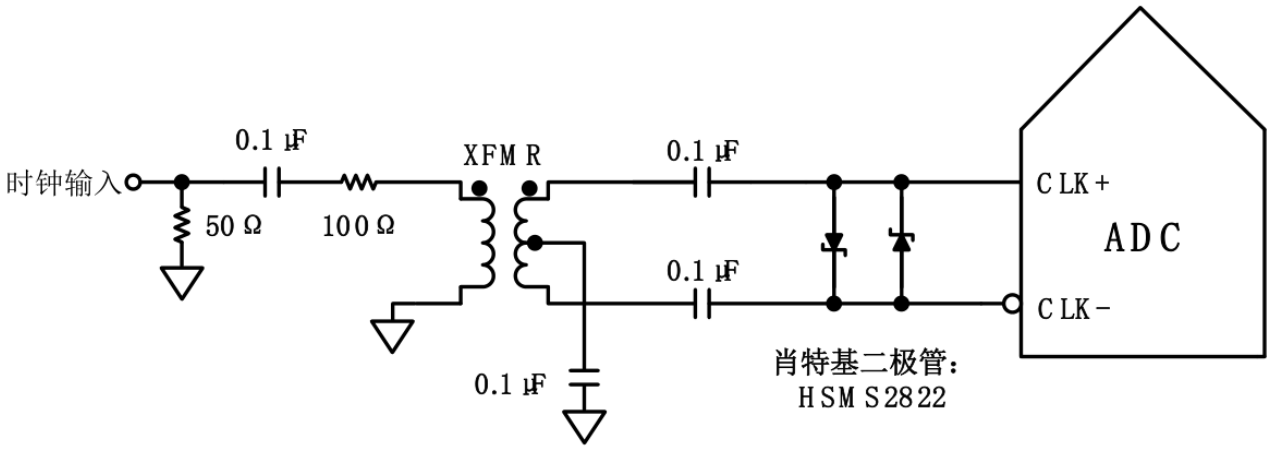


Figure 20: Transformer-Coupled Differential Clock (Frequencies up to 200 MHz)

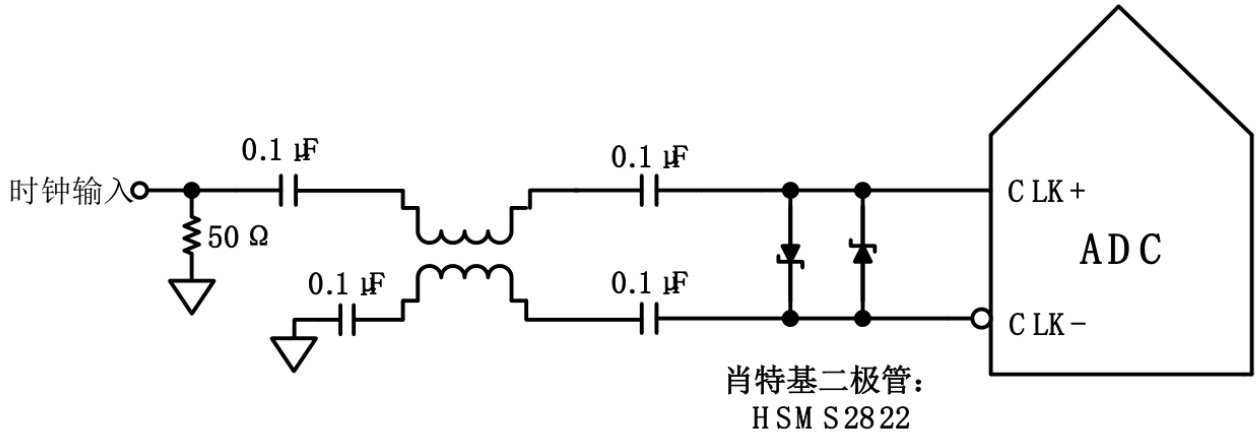


Figure 21: Balun-Coupled Differential Clock (Frequencies up to 1 GHz)

If no low-jitter clock source is available, another approach is to AC-couple a differential PECL signal and transmit it to the sampling clock input pins (as shown in Figure 21). AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

如果没有低抖动的时钟源，那么，另一种方法是对差分 PECL 信号进行交流耦合，并传输至采样时钟输入引脚(如图 21 所示)。AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 时钟驱动器具有出色的抖动性能。

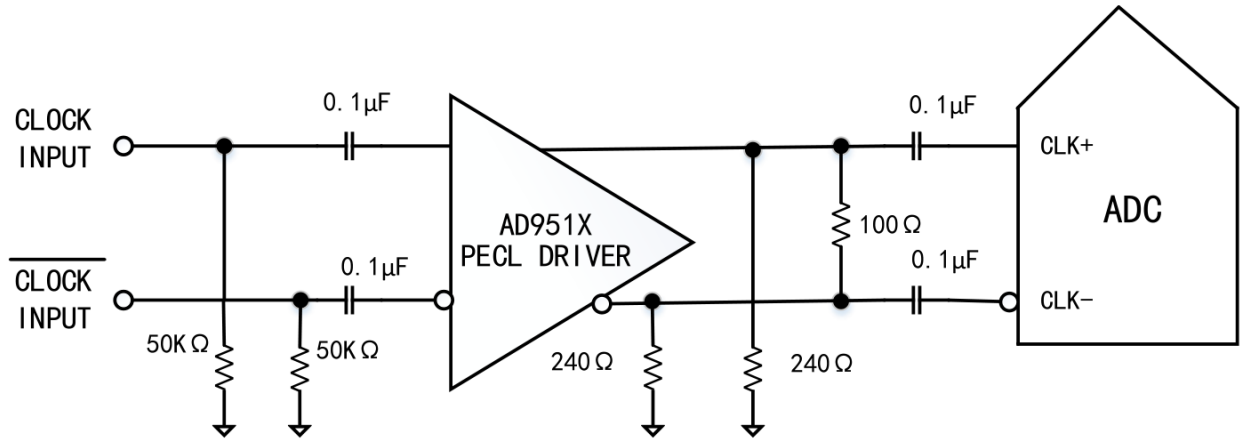


Figure 22: Differential PECL Sampling Clock (Frequencies up to 1 GHz)

Another approach is to AC-couple a differential LVDS signal to the sampling clock input pins (as shown in Figure 22). AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 clock drivers offer excellent jitter performance.

另一种方法是将差分 LVDS 信号交流耦合至采样时钟输入引脚(如图 22 所示)。AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517 时钟驱动器具有出色的抖动性能。

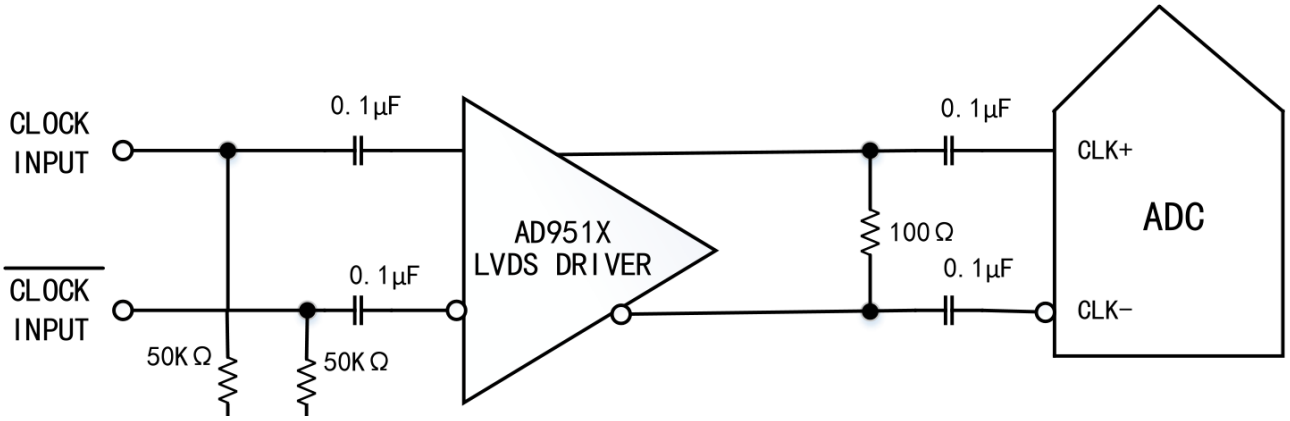


Figure 23: Single-Ended 1.8 V CMOS Input Clock (Frequencies up to 200 MHz)

9. Input Clock Divider / 输入时钟分频器

This product has a built-in input clock divider that can divide the input clock by an integer factor of 1 to 8. The clock divider of this product can be synchronized using the external SYNC input signal. By writing to bits 0 and 1 of register 0x109, the clock divider can be set to resynchronize after each SYNC signal or only after the first SYNC signal. A valid SYNC resets the divider to its initial state. This synchronization feature allows the clock dividers of multiple devices to be aligned, ensuring simultaneous input sampling.

本产品内置一个输入时钟分频器，可对输入时钟进行 1 至 8 整数倍分频。利用外部 SYNC 输入信号，可同步本产品时钟分频器。通过对寄存器 0x109 的位 0 和位 1 进行写操作，可以设置每次收到 SYNC 信号或者仅第一次收到 SYNC 信号后对时钟分频器再同步。有效 SYNC 可使分频器复位至初始状态。该同步特性可让多个器件的时钟分频器对准，从而保证同时进行输入采样。

10. Clock Duty Cycle / 时钟占空比

Typical high-speed ADCs use both clock edges to generate different internal timing signals, so they are very sensitive to clock duty cycle. Generally, to maintain ADC dynamic performance, the clock duty cycle tolerance should be ±5%.

This product has a built-in duty cycle stabilizer (DCS) that retimes the non-sampling edge (falling edge) and provides an internal clock signal with a nominal 50% duty cycle. When the clock input duty cycle deviates from the nominal 50% duty cycle by more than the ±5% rating, this feature minimizes performance degradation. Enabling the DCS function significantly improves noise and distortion performance for clock input duty cycles of 30% to 45% and 55% to 70%.

Jitter on the input rising edge remains a concern and cannot be easily reduced with the internal stabilization circuit. In applications with dynamically changing clock rates, the time constant associated with this loop must be considered. A wait of 1.5 µs to 5 µs is required before the DCS loop relocks to the input signal.

典型的高速 ADC 利用两个时钟边沿产生不同的内部定时信号，因此，它对时钟占空比非常敏感。通常，为保持 ADC 的动态性能，时钟占空比容差应为±5%。

本产品内置一个占空比稳定器(DCS)，可对非采样边沿(下降沿)进行重新定时，并提供标称占空比为 50%的内部时钟信号。当时钟输入占空比偏离标称 50%占空比的幅度大于±5%额定值时，该特性可最大程度减少性能的下降。使能 DCS 功能可显著改善 30%至 45%和 55%至 70%的时钟输入占空比的噪声和失真性能。

输入上升沿的抖动依然值得关注，且无法借助内部稳定电路来轻易减少这种抖动。在时钟速率动态改变的应用中，必须考虑与该环路相关的时间常量。在 DCS 环路重新锁定输入信号前，都需要等待 1.5 µs 至 5 µs 的时间。

11. Jitter Considerations / 抖动考虑

High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. Intermediate-frequency undersampling applications are especially sensitive to jitter (see Figure 23).

高速、高分辨率 ADC 对时钟输入信号的质量非常敏感。中频欠采样应用对抖动尤其敏感(见图 23)。

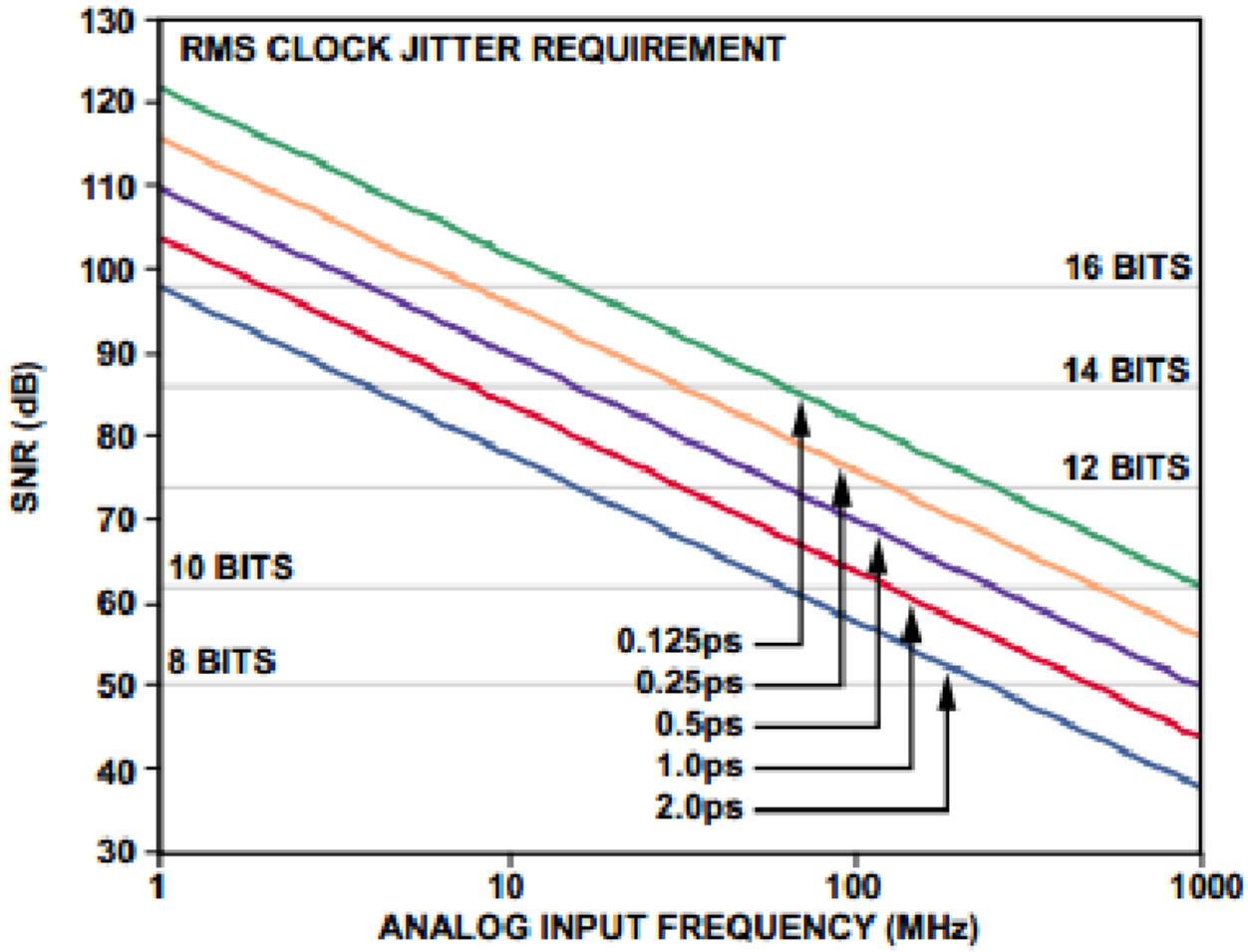


Figure 24: Ideal SNR vs. Analog Input Frequency and Jitter

When aperture jitter may affect the dynamic range of this product, the clock input signal should be treated as an analog signal. The clock driver supply should be separated from the ADC output driver supply to avoid mixing digital noise into the clock signal. A low-jitter crystal-controlled oscillator provides the best clock source. If the clock signal comes from another type of clock source (via gating, division, or other methods), the original clock should be used for retiming in the final step.

当孔径抖动可能影响本产品的动态范围时，应将时钟输入信号视为模拟信号。将时钟驱动器电源与 ADC 输出驱动器电源分离，以免在时钟信号内混入数字噪声。低抖动的晶体控制振荡器可提供最佳时钟源。如果时钟信号来自其它类型的时钟源(通过门控、分频或其它方法)，则需要在最后一步中利用原始时钟进行重定时。

12. Power Consumption and Power-Saving Modes / 功耗和省电模式

As shown in Figure 24, the power consumption of this product is proportional to its sampling rate. This product can be placed into power-saving mode through the SPI port or by setting the PDWN pin high. In power-saving mode, the typical power consumption of the ADC is 2 mW. In power-saving mode, the output drivers are in a high-impedance state. Setting the PDWN pin low returns this product to normal operating mode. Note that PDWN is referenced to the data output driver supply voltage (DRVDD) and must not exceed that supply voltage.

In power-saving mode, low power consumption is achieved by turning off the reference voltage source, reference voltage buffer, bias network, and clock. When entering power-saving mode, the internal capacitors discharge; when returning to normal operating mode, the internal capacitors must be recharged. Therefore, the wake-up time depends on the time spent in power-saving mode; the shorter the time in power-saving mode, the shorter the corresponding wake-up time. When using the SPI port interface, the user can place the ADC in power-saving mode or standby mode. For shorter wake-up times, standby mode can be used, in which the internal reference voltage circuit remains powered. For more information on using these features, see the "Memory Map" section.

如图 24 所示，本产品的功耗与其采样速率成比例关系。通过 SPI 端口或将 PDWN 引脚置位高电平，可使本产品进入省电模式。在省电模式下，ADC 的典型功耗为 2 mW。省电模式下，输出驱动器处于高阻抗状态。将 PDWN 引脚置位低电平时，本产品返回正常工作模式。注意，PDWN 以数据输出驱动器电源电压(DRVDD)为基准，且不得高于该电源电压。

在省电模式下，通过关闭基准电压源、基准电压缓冲器、偏置网络以及时钟，可实现低功耗。进入省电模式时，内部电容放电；返回正常工作模式时，内部电容必须重新充电。因此，唤醒时间与处于省电模式的时间有关；处于省电模式的时间越短，则相应的唤醒时间越短。使用 SPI 端口接口时，用户可将 ADC 置于省电模式或待机模式。如需较短的唤醒时间，可以使用待机模式，该模式下内部基准电压电路处于通电状态。有关使用这些功能的更多信息，请参见"存储器映射"部分。

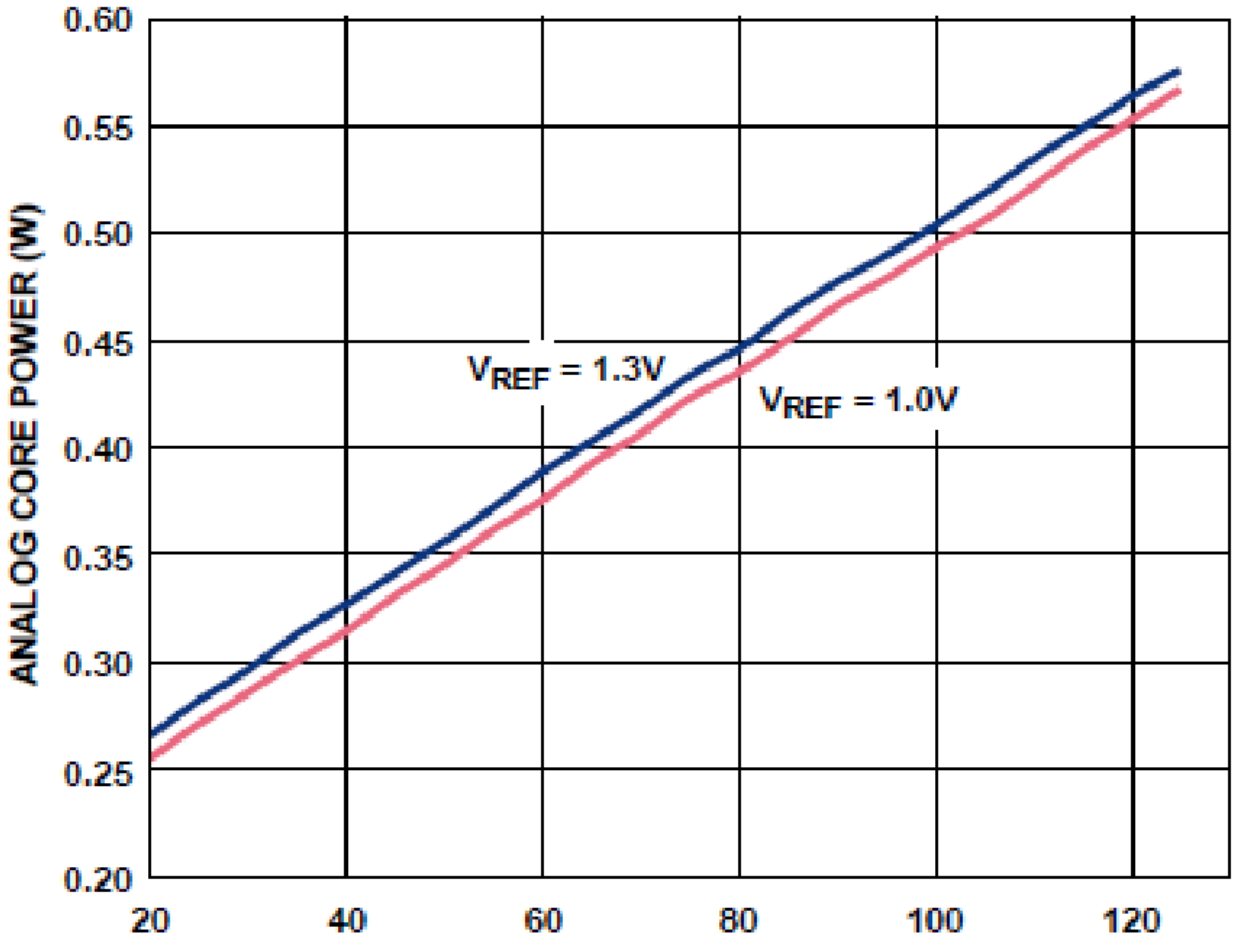


Figure 25: Total Power Consumption vs. fSAMPLE

13. Digital Outputs / 数字输出

The digital outputs of this product use the ANSI-644 LVDS standard, with an output current of 3.5 mA and a 100 Ω termination resistor load, yielding a 350 mV swing. In the default mode, the output timing relationship is shown in Figure 25.

本产品数字输出采用 ANSI-644 LVDS 标准，输出电流为 3.5mA，负载 100 欧姆的端电阻，摆幅 350mV。默认模式下，输出的时序关系如图 25 所示。

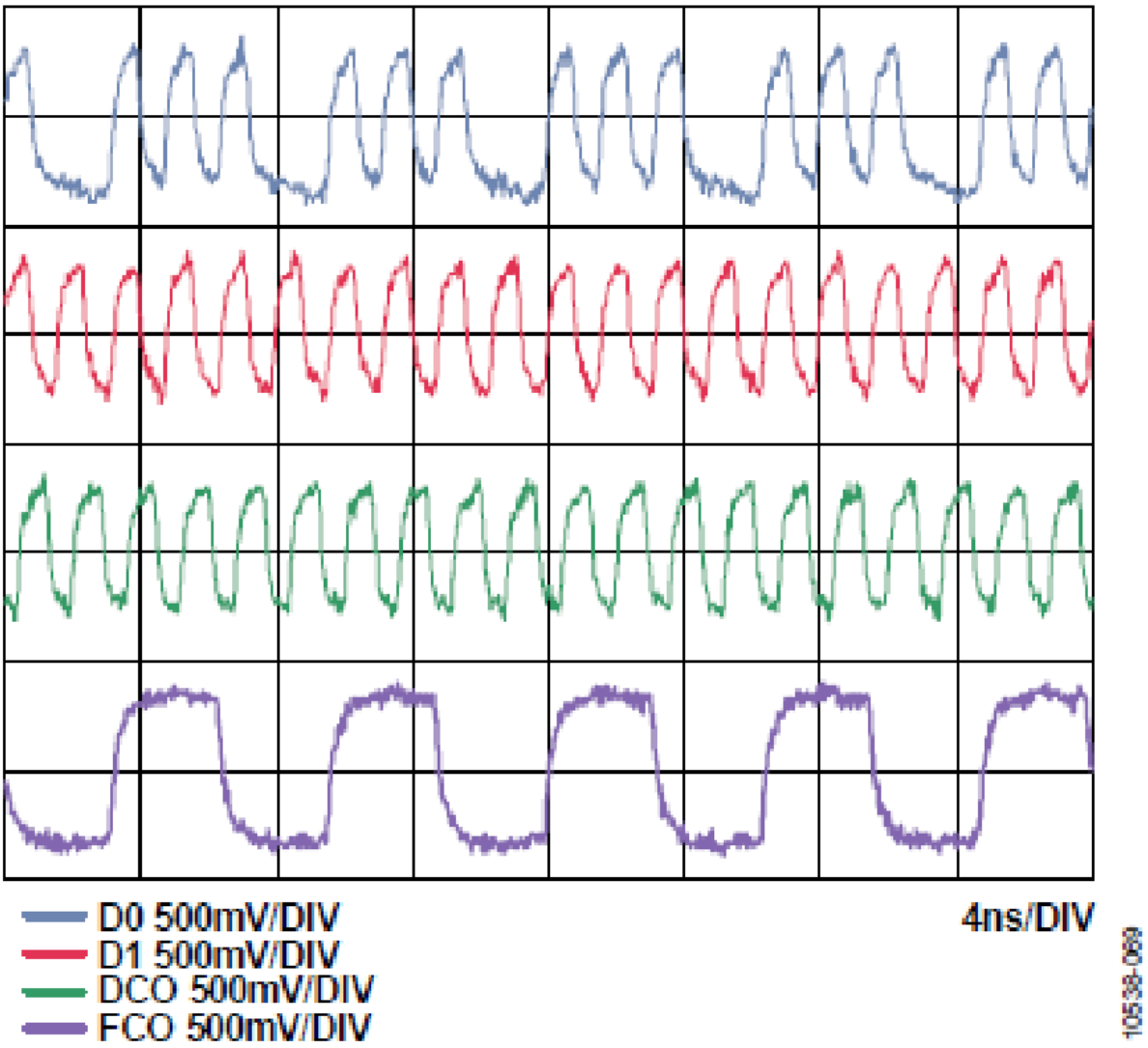


Figure 26: LVDS Output Timing Example

Registers / 寄存器

The SPI of this product is a three-wire control interface; the SPI timing control diagram is shown in Figure 2.

After power-up, first complete the register reset operation, and configure register address 0x100.

本产品 SPI 为三线控制，SPI 的时序控制图如图 2 所示。

上电后，请先完成寄存器复位操作，并配置寄存器地址 0x100。

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
芯片配置寄存器 / Chip Configuration Registers											
0x00	SPI 端口配置 / SPI Port Configuration	0=SDO 有效 / 0=SDO active	LSB 优先 / LSB first	软复位 / Soft reset	1=16 位地址 / 1=16-bit address	1=16 位地址 / 1=16-bit address	软复位 / Soft reset	LSB 优先 / LSB first	0=SDO 有效 / 0=SDO active	0x18	半字节之间是镜像关系，使得 LSB 优先或 MSB 优先模式寄存器均能正确记录数据。ADC 的默认值为 16 位模式。/ The nibbles are mirrored so that registers are correctly written in either LSB-first or MSB-first mode. The ADC default is 16-bit mode.
0x01	芯片 ID（全局）/ Chip ID (Global)	8 位芯片 ID，位[7:0]：0xB5 = 四通道、14 位、125 MSPS 串行 LVDS / 8-bit chip ID, bits[7:0]: 0xB5 = quad-channel, 14-bit, 125 MSPS serial LVDS								0xB5	唯一芯片 ID，用来区分器件；只读。/ Unique chip ID used to distinguish the device; read-only.
0x02	芯片等级（全局）/ Chip	禁用 / Disabled	速度等级 ID[6:4]：110 = 125			禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled		唯一速度等级 ID，用来区分器件等级；只读。/

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
	Grade (Global)		MSPS / Speed grade ID[6:4]: 110 = 125 MSPS								Unique speed grade ID used to distinguish the device grade; read-only.
器件索引和传送寄存器 / Device Index and Transfer Registers											
0x05	器件索引 / Device Index	禁用 / Disabled	禁用 / Disabled	时钟通道 DCO / Clock channel DCO	时钟通道 FCO / Clock channel FCO	时钟通道 D / Clock channel D	时钟通道 C / Clock channel C	时钟通道 B / Clock channel B	时钟通道 A / Clock channel A	0x3F	设置这些位以决定片内哪个器件接收下一个写命令。默认为片内所有器件。/ Set these bits to determine which on-chip device receives the next write command. Default is all on-chip devices.
0xFF	传输 / Transfer	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	启动覆盖 / Initiate override	0x00	设置采样速率覆盖。/ Sets the sample rate override.
全局 ADC 功能寄存器 / Global ADC											

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
Function Registers											
0x08	功耗模式（全局）/ Power Modes (Global)	禁用 / Disabled	禁用 / Disabled	外部掉电引脚功能：0=完全掉电，1=待机 / External power-down pin function: 0=full power-down, 1=standby	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	功耗模式：00=芯片运行；01=完全掉电；10=待机；11=复位 / Power modes: 00=chip run; 01=full power-down; 10=standby; 11=reset		0x00	决定芯片的一般工作模式。/ Determines the general operating mode of the chip.
0x09	时钟（全局）/ Clock (Global)	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	占空比稳定：0=开，1=关 / Duty cycle stabilizer: 0=on, 1=off	0x01	打开或关闭占空比稳定器。/ Turns the duty cycle stabilizer on or off.
0x0B	时钟分频（全局）/ Clock Divide (Global)	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	时钟分频比[2:0]：000=1 分频；001=2 分频；010=3 分频；011=4 分频；100=5 分频；101=6 分频；110=7 分频；111=8 分频 / Clock divide ratio[2:0]: 000=÷1; 001=÷2; 010=÷3; 011=÷4; 100=÷5;			0x00	

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
							101=÷6; 110=÷7; 111=÷8				
0x0C	禁用 / Disable	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	斩波模式：0=关，1=开 / Chopper mode: 0=off, 1=on	0x00	使能/禁用斩波模式。/ Enables/ disables chopper mode.
0x0D	测试模式（局部，PN 序列复位除外）/ Test Modes (Local, except PN sequence reset)	用户输入测试模式：00=单一；01=交替；10=单一一次；11=交替一次（仅影响用户输入测试模式，位[3:0]=1000）/ User input test mode: 00=single; 01=alternate; 10=single once; 11=alternate once (affects only user input test mode, bits[3:0]=1000)		产生复位 PN 长序列 / Generate reset PN long sequence	产生复位 PN 短序列 / Generate reset PN short sequence	输出测试模式[3:0]（局部）：0000=关（默认）；0001=中间电平短序列；0010=正 FS；0011=负 FS；0100=交替棋盘形式；0101=PN 23 序列；0110=PN 9 序列；0111=1/0 字反转；1000=用户输入；1001=1/0 位反转；1010=1×同步；1011=1 位高电平；1100=混合位频率 / Output test mode[3:0] (local): 0000=off (default); 0001=midscale short sequence; 0010=positive FS; 0011=negative FS; 0100=alternating checkerboard; 0101=PN 23 sequence; 0110=PN 9 sequence; 0111=1/0 word toggle; 1000=user input; 1001=1/0 bit toggle; 1010=1×sync; 1011=1-bit high; 1100=mixed bit frequency				0x00	置 1 时，测试数据将取代正常数据被置于输出引脚上。/ When set to 1, test data replaces normal data on the output pins.
0x10	失调调整（局部）/ Offset Adjust (Local)	8 位器件失调调整，位[7:0]（局部）：失调调整以 LSB 为单位，从 +127 到−128（二进制补码格式）/ 8-								0x00	器件失调调整。/ Device offset adjustment.

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
		bit device offset adjust, bits[7:0] (local): offset adjust in LSBs, from +127 to −128 (two's complement format)									
0x14	输出模式 / Output Mode	禁用 / Disabled	LVDS-ANSI/ LVDS-IEEE 选项：0=LVDS-ANSI；1=LVDS-IEEE / LVDS-ANSI/ LVDS-IEEE option: 0=LVDS-ANSI; 1=LVDS-IEEE	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	输出反向（局部）/ Output invert (local)	禁用 / Disabled	输出格式：0=偏移二进制；1=二进制补码（全局）/ Output format: 0=offset binary; 1=two's complement (global)	0x01	配置输出和数据格式。/ Configures the output and data format.
0x15	输出调整 / Output Adjust	禁用 / Disabled	禁用 / Disabled	输出驱动器端接[1:0]：00=无；01=200 Ω；10=100 Ω；11=100 Ω / Output driver termination[1:0]: 00=none; 01=200 Ω; 10=100 Ω; 11=100 Ω		禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	输出驱动：0=1×驱动；1=2×驱动 / Output drive: 0=1× drive; 1=2× drive	0x00	决定 LVDS 或其它输出属性。/ Determines LVDS or other output attributes.
0x16	输出相位 / Output Phase	禁用 / Disabled	输入时钟相位调整							0x03	在利用全局时钟分频的器件上，

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
			[6:4]（值为相位延迟的输入时钟周期数）/ Input clock phase adjust[6:4] (value is the number of input clock cycles of phase delay)			输出时钟相位调整[3:0]（0000 至 1011）/ Output clock phase adjust[3:0] (0000 to 1011)					决定使用分频器输出的哪个相位提供输出时钟。内部锁存不受影响。/ On devices using the global clock divider, determines which phase of the divider output provides the output clock. Internal latching is unaffected.
0x18	VREF	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	VREF 调节数字方案[2:0]：000=1.0 V p-p (1.3 V p-p)；001=1.14 V p-p (1.48 V p-p)；010=1.33 V p-p (1.73 V p-p)；011=1.6 V p-p (2.08 V p-p)；100=2.0 V p-p (2.6 V p-p) / VREF adjust digital scheme[2:0]: 000=1.0 V p-p (1.3 V p-p); 001=1.14 V p-p (1.48 V p-p); 010=1.33 V p-p (1.73 V p-p); 011=1.6 V p-p (2.08 V p-p); 100=2.0 V p-p (2.6 V p-p)			0x04	选择内部 VREF。显示值针对 VREF = 1.0 V (1.3 V)。/ Selects the internal VREF. Displayed values are for VREF = 1.0 V (1.3 V).

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
0x19	USER_PATT1_LSB（全局）/ USER_PATT1_LSB (Global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	用户定义的测试码 1 LSB。/ User-defined test pattern 1 LSB.
0x1A	USER_PATT1_MSB（全局）/ USER_PATT1_MSB (Global)	B15	B14	B13	B12	B11	B10	B9	B0 / [requires manual verification: source extraction shows B0 here, likely an extraction error for B8]	0x00	用户定义的测试码 1 MSB。/ User-defined test pattern 1 MSB.
0x1B	USER_PATT2_LSB（全局）/ USER_PATT2_LSB (Global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	用户定义的测试码 2 LSB。/ User-defined test pattern 2 LSB.
0x1C	USER_PATT2_MSB（全局）/ USER_PATT2_MSB (Global)	B15	B14	B13	B12	B11	B10	B9	B0 / [requires manual verification: source extraction shows B0 here, likely an extraction error for B8]	0x00	用户定义的测试码 2 MSB。/ User-defined test pattern 2 MSB.
0x21	串行输出数据控制（全局）/		SDR/DDR	单通道/双通道、逐位/逐字节[6:4]：000=SDR		禁用 / Disabled	选择 2×帧 / Select 2× frame	串行输出位数：		0x30	串行流控制。默认为 MSB 优先、

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
	Serial Output Data Control (Global)	LVDS 输出 LSB 优先 / LVDS output LSB first		双通道、逐位；001=SDR 双通道、逐字节；010=DDR 双通道、逐位；011=DDR 双通道、逐字节；100=DDR 单通道、逐字 / Single/dual channel, bit-wise/ byte-wise[6:4]: 000=SDR dual-channel, bit-wise; 001=SDR dual-channel, byte-wise; 010=DDR dual-channel, bit-wise; 011=DDR dual-channel, byte-wise; 100=DDR single-channel, word-wise				00=16 位 / Serial output bits: 00=16 bits			原有位流。/ Serial stream control. Defaults to MSB-first, original bit stream.
0x22	串行通道状态（局部）/ Serial Channel Status (Local)	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	通道输出复位 / Channel output reset	通道掉电 / Channel power-down	0x00	用来关断转换器的各个部分。/ Used to power down portions of the converter.
0x100	采样速率覆盖 / Sample Rate Override	禁用 / Disabled	Always write =1	Always write =01	禁用 / Disabled	采样速率：000=20 MSPS；001=40 MSPS；010=50 MSPS；011=65 MSPS；100=80 MSPS；101=105 MSPS；110=125 MSPS / Sample rate: 000=20 MSPS; 001=40 MSPS; 010=50 MSPS; 011=65 MSPS; 100=80 MSPS; 101=105 MSPS; 110=125 MSPS				0x00	需要上电配置寄存器 50（需要传输寄存器，0xFF）。/ Requires power-up configuration of register 50 (requires the transfer register, 0xFF).
0x101		禁用 / Disabled		禁用 / Disabled		禁用 / Disabled	禁用 / Disabled			0x00	

地址（十六进制）/ Address (Hex)	参数名称 / Parameter Name	位7 (MSB) / Bit7 (MSB)	位6 / Bit6	位5 / Bit5	位4 / Bit4	位3 / Bit3	位2 / Bit2	位1 / Bit1	位0 (LSB) / Bit0 (LSB)	默认值（十六进制）/ Default (Hex)	注释 / Notes
	用户 I/O 控制 2 / User I/O Control 2		禁用 / Disabled		禁用 / Disabled			禁用 / Disabled	SDIO 下拉 / SDIO pull-down		禁用 SDIO 下拉电阻。/ Disables the SDIO pull-down resistor.
0x102	用户 I/O 控制 3 / User I/O Control 3	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	VCM 掉电 / VCM power-down	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	0x00	VCM 控制。/ VCM control.
0x106	比较器阈值算法 / Comparator Threshold Algorithm	保留 / Reserved								0x00	00=关闭；01=打开第 1 级；10=打开第 2 级；11=打开第 1/2 级 / 00=off; 01=enable stage 1; 10=enable stage 2; 11=enable stages 1/2
0x109	同步 / Sync	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	禁用 / Disabled	仅与下一同步脉冲同步 / Sync only to next sync pulse	使能同步 / Enable sync	0x00	

Power-to-Ground Protection / 电源地间保护

To improve the device's anti-static capability, the following ESD protection loops exist between the power pins inside the device. The forward conduction voltage drop of each ESD protection device is approximately 0.35 V; during power-up and normal use, prolonged forward conduction of these ESD protection devices should be avoided.

为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.35V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。



Figure 27: Internal Power-Supply ESD Protection Circuit

Notes / 注意事项

1. Product Installation Notes / 产品安装注意事项

1) Pay attention to the device orientation during soldering to avoid soldering it incorrectly. 2) Instruments and meters used for debugging the circuit must have good common grounding. The PCB design must maintain good grounding and power supply decoupling. 3) Take care not to reverse the power supply or short the input/output terminals to the power supply, which can easily damage the circuit.

1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2. Product Usage Notes / 产品使用注意事项

1) Differential inputs should be kept as close together and as parallel as possible. 2) Input traces should be kept as short as possible to minimize parasitic capacitance and noise pickup. 3) For better heat dissipation and better electrical performance, the die pad of the chip should be soldered to a large ground on the PCB, maximizing the thermal performance of the package. 4) It is important that the chip ground be connected to the PCB ground plane through as many channels and as much area as possible. 5) After power-up, it is recommended to first reset the circuit before use. 6) When connecting power to this product, it is recommended to use two independent 1.8 V supplies: one supply for the analog output (AVDD) and another supply for the digital output (DRVDD and DVDD). Designers may use multiple different decoupling capacitors suitable for high and low frequencies. Decoupling capacitors should be placed close to the printed circuit board (PCB) entry point and close to the device pins, with trace lengths as short as possible. This product requires only one PCB ground plane. Reasonable decoupling and clever

partitioning of the PCB analog, digital, and clock sections can easily achieve optimal performance. 7) At power-up, this product enters the initial phase, and the internal state machine sets the biases and registers so that the device operates normally. During initialization, this product requires a stable clock. If the ADC clock source is absent or unstable during ADC power-up, the state machine will be interrupted, causing the ADC to power up into an unknown state. To correct this state, the initial sequence must be re-invoked after the ADC clock stabilizes. This can be accomplished by initiating a digital reset through register 0x08. In the default configuration (internal VREF, AC-coupled input), VREF and VCM are provided by the ADC itself, so a sufficiently stable clock is available at power-up. When VREF and/or VCM are provided by external sources, they must also be stable at power-up; otherwise, a sequential digital reset through register 0x08 is required. The pseudo-code sequence for the digital reset is shown below: SPI_Write (0x08, 0x03); # Digital Reset SPI_Write (0x08, 0x00); # Normal Operation 8) For optimal electrical and thermal performance, the exposed pad on the bottom of the ADC must be connected to analog ground (AGND). The continuous copper plane exposed (without solder mask) on the PCB must match the exposed pad (pin 0) of this product. The copper plane must have multiple vias to obtain the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. Insulating ring oxide should be used to fill or plug these vias. To maximize coverage and connection between the ADC and the PCB, a silkscreen layer should be overlaid on the PCB to divide the continuous plane on the PCB into multiple equal sections. This prevents solder buildup during reflow and provides multiple connection points between the ADC and the PCB. A continuous, undivided plane guarantees only one connection point between the ADC and the PCB. A PCB layout example can be found on the evaluation board. 9) VCM decouples the VCM pin to ground with a 0.1 µF capacitor. 10) The VREF pin should be decoupled to ground through the parallel combination of an external low ESR 0.1 µF ceramic capacitor and a low ESR 1.0 µF capacitor. 11) When the converter needs to deliver its full dynamic performance, the SPI port should be disabled. Typically, the SCLK, CSB, and SDIO signals are asynchronous to the ADC clock, so noise in these signals degrades converter performance. If other devices use the on-board SPI bus, a buffer may need to be connected between the bus and this product to prevent these signals from changing at the converter's input pins during critical sampling periods. 12) Affected by process or environmental variations, comparator thresholds may fluctuate; it is recommended to enable the comparator threshold correction function during use. The SPI pseudo-code sequence is shown below: SPI_Write (0x106, 0x03);

1) 差分输入应尽量靠近且相互平行。 2) 输入连线应尽量短以最小化寄生电容和噪声引入。 3) 为了更好的散热并获得更好的电性能，芯片的底板应焊接到 PCB 板的一个大的地端，从而最大限度发挥封装的热性能。 4) 很重要的是，芯片的地应该通过尽量多的渠道和足够多的面积与 PCB 板的地层相连。 5) 推荐上电后首先对电路进行复位，再进行使用 6) 当连接电源至本产品时，建议使用两个独立的 1.8 V 电源： 一个电源用于模拟输出(AVDD)，另一个电源用于数字输出(DRVDD 和 DVDD)。设计人员可以使用多个不同的去耦电容以适用于高频和低频。去耦电容应放置在接近印刷电路板(PCB)入口点和接近器件引脚的位置，并尽可能缩短走线长度。本产品仅需要一个 PCB 接地层。对 PCB 模拟、数字和时钟模块进行合理去耦和巧妙分隔，可以轻松获得最佳性能。 7) 上电时，本产品进入初始相位，内部状态机设置偏置和寄存器，以便器件能正常工作。在初始化过程中，本产品需要稳定的时钟。若 ADC 时钟源不存在，或在 ADC 上电期间不稳定，则会打断状态机，进而导致 ADC 上电至未知状态。要校正这一状态，必须在 ADC 时钟稳定后重新调用初始序列。可通过寄存器 0x08 发起数字复位来完成该操作。在默认配置中(内部 VREF，交流耦合输入)，VREF 和 VCM 由 ADC 自身提供，因此上电时具有足够稳定的时钟。当 VREF 和/或 VCM 由外部源提供时，它们在上电时也必须是稳定的；否则，需要通过寄存器 0x08 进行序列数字复位。数字复位的伪代码序列如下所示：SPI_Write (0x08, 0x03); # Digital Reset SPI_Write (0x08, 0x00); # Normal Operation 8) 为获得最佳的电气性能和热性能，必须将 ADC 底部的裸露焊盘连接至模拟地(AGND)。PCB 上裸露(无阻焊膜)的连续铜平面必须与本产品的裸露焊盘(引脚 0)匹配。铜平面上必须有多个通孔，获得尽可能低的热阻路径以通过 PCB 底部进行散热。应采用绝缘环氧化物来填充或堵塞这些通孔。为了最

大化地实现 ADC 与 PCB 之间的覆盖与连接，应在 PCB 上覆盖一个丝印层，以便将 PCB 上的连续平面划分为多个均等的部分。这样，在回流焊过程中，便可防止焊料堆积并在 ADC 与 PCB 之间提供多个连接点。而一个连续的、无分割的平面则仅可保证在 ADC 与 PCB 之间有一个连接点。PCB 布局范例可以参考评估板。 9) VCM 利用一个 0.1 μF 电容将 VCM 引脚去耦至地。 10) VREF 引脚应通过外部一个低 ESR 0.1 μF 陶瓷电容和一个低 ESR 1.0 μF 电容的并联去耦至地。 11) 当需要转换器充分发挥其全部动态性能时，应禁用 SPI 端口。通常 SCLK 信号、CSB 信号和 SDIO 信号与 ADC 时钟是异步的，因此，这些信号中的噪声会降低转换器性能。如果其它器件使用板上 SPI 总线，则可能需要在该总线与本产品之间连接缓冲器，以防止这些信号在关键的采样周期内，在转换器的输入引脚端发生变化。 12) 受工艺或环境变化等影响，比较器阈值会出现波动，建议使用时打开比较器阈值矫正功能。SPI 伪代码序列如下所示：SPI_Write (0x106, 0x03);

3. Product Protection Notes / 产品防护注意事项

1) All pins of this circuit are designed with ESD protection structures; however, large-energy electrical pulses may still damage the circuit, so ESD protection should be observed during testing, handling, and storage. 2) Exceeding the absolute maximum ratings may cause permanent damage to the device. These are ratings only and do not indicate that the device can operate normally under these conditions or under any other conditions exceeding those shown in this product manual. 3) Under conditions protected from direct rain and snow, product packaging boxes can be transported by safe means of transport. But they must not be stacked together with acidic, alkaline, or other corrosive objects. Packaging should be secure and existing means of transport can be used. 4) The storage environment for packaged products should meet the Class I warehouse conditions specified in Section 8.1 of Q/W 657A (temperature: 15°C~25°C, humidity: 25%~65%), with no acids, alkalis, or other corrosive gases nearby, good ventilation, and appropriate anti-static measures.

1) 该电路所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 2) 超出绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。 3) 在避免雨、雪直接影响的条件下，装有产品的包装箱可以用安全的运输工具运输。但不能和带有酸性、碱性和其它腐蚀性物体堆放在一起。包装应是安全的，可以采用现有的运输工具。 4) 包装好的产品贮存环境应满足 Q/W 657A 第 8.1 规定的 I 类库房条件要求（温度：15°C~25°C，湿度：25%~65%），周围没有酸、碱或其它腐蚀性气体，通风良好，且具备相应防静电措施。

4. Assembly Instructions / 电装说明

1) The moisture sensitivity level of this product is MSL3. The allowable time exposed to the ambient environment after removing the product from the moisture-proof bag, after dry storage or baking, and before reflow soldering is: ≤30°C/60RH%, 168h; 2) If device storage conditions cannot be controlled or traced, strictly perform baking at 125°C for 8h before assembly; 3) If the assembly environment temperature and humidity cannot be guaranteed at ≤30°C/60RH%, complete soldering within 12h after baking; 4) After baking, the product is highly susceptible to static electricity; all operations must observe ESD protection; 5) For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C~235°C, the maximum peak temperature should not exceed 235°C, dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60~90s, ramp-up rate 2~4°C/s, cool-down rate 2~6°C/s; 6) For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C~245°C, the maximum peak temperature should not exceed 260°C, dwell time within ±5°C of peak temperature ≤20s, time above liquidus 60~90s, ramp-up rate 2~4°C/s, cool-down rate 2~6°C/s; 7) If a mixed assembly process requires elevated

temperature, ensure the device body temperature does not exceed 260°C (the device body temperature measurement point is on the top surface of the device during reflow); 8) The solder terminal plating of this product is NiPdAu.

1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； 3) 若电装环境温湿度无法保证≤30°C/60RH%，请在烘烤后 12h 内完成焊接； 4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）； ⑧ 本产品焊接端镀层为镍钯金。

5. Thermal Resistance / 热阻

表1 封装热阻 / Table 1: Package Thermal Resistance

项目 / Item	实测值 / Measured Value	依据标准及方法 / Reference Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)	31.05 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2 natural convection thermal test environmental requirements and test method for integrated circuits
Rthjt（结到器件顶面的热阻）/ Rthjt (junction-to-device-top thermal resistance)	3.298 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14 one-dimensional heat transfer path dual-interface separation method
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-device-bottom thermal resistance)	2.775 K/W	JESD51-14 拐点理论器件内部结构分层得到 / JESD51-14 inflection point theory, obtained by layering the internal device structure

Common Faults and Remedies / 常见故障及处理办法

1. No signal output: check that the supply voltage, input signal, and clock are correctly applied. 2. Device not functioning properly: identify the device operating mode and confirm the configuration is correct. 3. Device operating unstably: check the power supply to ensure the supply voltage is stable.

1、 无信号输出：检查电源电压、输入信号、时钟是否正确加载。 2、 器件功能不正常：明确器件工作模式，确认配置是否正确。 3、 器件工作不稳定：检查电源，保证电源电压稳定。

Contact Information / 联系方式

深信科技 / Shenzhen Shenxin Technology Co., Ltd.

Felix (Flip) Lai, CEO

邮箱 / Email: felix@shenxinic.com

电话 / Tel: +852 51367095

官网 / Website: shenxinic.com

Additional Notes / 附加说明

1. First release date of this manual: July 2026. 2. Product status: ☑ Production (this product model is currently in production and formal products can be supplied); ☐ Pre-release (this product model is not yet in formal production; samples can be provided). 3. Model suffix difference description (for series products, describe model suffix differences as in the example below; add this section when needed): No suffix. 4. Description of alternative to foreign products:

1. 本说明书首次发布日期：2026 年 7 月。 2. 本产品状态：☑ 生产 （该产品型号目前已在生产，可以提供正式产品）；☐预发布（该产品型号尚未投入正式生产，可以提供样品） 3. 型号后缀差异性说明（系列化产品需对型号后缀说明如下示例，需要时增加此部分）：无后缀。 4. 替代国外产品情况说明：

1) 绝对最大额定值对比 / Absolute Maximum Ratings Comparison

附表1 绝对最大额定值对比 / Appendix Table 1: Absolute Maximum Ratings Comparison

参数 / Parameter	SXA036 规范要求 / SXA036 Specification	国外产品手册 / Foreign Product Datasheet	比对结果 / Comparison Result
模拟电源电压（VAVDD）/ Analog supply voltage (VAVDD)	2V	2V	一致 / Consistent
数字电源电压（VDRVDD）/ Digital supply voltage (VDRVDD)	2V	2V	一致 / Consistent
贮存温度（Tstg）/ Storage temperature (Tstg)	-65°C~150°C	-65°C~150°C	一致 / Consistent
结温（TJ）/ Junction temperature (TJ)	150°C	150°C	一致 / Consistent

2) 推荐工作条件对比 / Recommended Operating Conditions Comparison

附表2 推荐工作条件对比 / Appendix Table 2: Recommended Operating Conditions Comparison

参数 / Parameter	SXA036 规范要求 / SXA036 Specification	国外产品手册 / Foreign Product Datasheet	比对结果 / Comparison Result
工作频率（fCLK）/ Operating frequency (fCLK)	20MHz~125MHz	20MHz~125MHz	一致 / Consistent
模拟电源电压（VAVDD）/ Analog supply voltage (VAVDD)	1.75V~1.9V	1.75V~1.9V	一致 / Consistent
数字电源电压（VDRVDD）/ Digital supply voltage (VDRVDD)	1.75V~1.9V	1.75V~1.9V	一致 / Consistent
输入信号幅度范围（峰峰值）/ Input signal amplitude range (peak-to-peak)	≤2V	≤2V	一致 / Consistent
工作环境温度（TA）/ Operating ambient temperature (TA)	-40°C~85°C	-40°C~85°C	一致 / Consistent

3) 其它指标对比 / Other Specifications Comparison

附表3 其它指标对比 / Appendix Table 3: Other Specifications Comparison

参数 / Parameter	SXA036	国外产品 / Foreign Product	比对结果 / Comparison Result
封装形式 / Package	QFN48	QFN48	一致 / Consistent
质量等级 / Quality Grade	企标 / Enterprise standard	工业级 / Industrial grade	有差异 / Different
尺寸 / Dimensions	7mm×7mm×0.75mm	7mm×7mm×0.75mm	一致 / Consistent
替代建议 / Replacement Recommendation	□直接替代 □有效替代 ☑功能替代 / ☐ Direct replacement ☐ Effective alternative ☑ Functional alternative		

End of datasheet. / 本说明书结束。