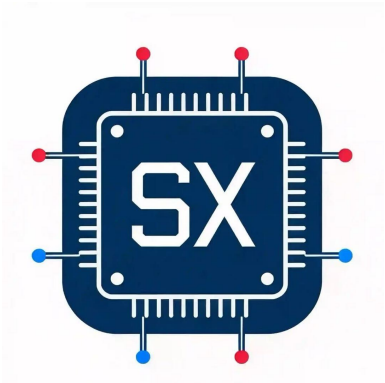


SXD005

Dual-Channel 16-Bit, 1 GSPS D/A Converter

双通道 16 位 1GSPS D/A 转换器

16-bit | 2 channels | 1 GSPS | LQFP100 | Parallel CMOS

16位 | 双通道 | 1GSPS | LQFP100 | 并行CMOS

对标 / Cross Reference: AD9779 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

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SXD005 型双通道 16 位 1GSPS D/A 转换器产品说明书、使用手册

SXD005 Dual-Channel 16-Bit 1GSPS D/A Converter — Product Specification & User Manual

深信科技 / Shenzhen Shenxin Technology Co., Ltd. 版本 / Revision: V1.20260721 对标 / Cross Reference: AD9779 — pin-to-pin compatible alternative

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原目录未列「3、时钟输入」，正文实际含该节且其后各节序号顺延（正文：1 原理概述、2 模拟输入、3 时钟输入、4 三线式接口……11 DAC 采样时钟源）；本底稿正文按正文序号编排，目录此处仍按原件目录保留。 The original contents list omits "3. Clock Input", while the body contains that section and all following section numbers are shifted by one (body: 1 Principle Overview, 2 Analog Input, 3 Clock Input, 4 Three-Wire Interface … 11 DAC Sample Clock Source). The body of this draft follows the body's numbering; the contents above are kept as in the original.

版本修订记录 / Revision History

版本号 / Version	发布日期 / Date	更改章节 / Changed Section	更改说明 / Description	备注 / Note
V1.20260721	2026.07.21	——	——	首次发布 / Initial release

产品用途及应用范围 / Applications

- 无线基础设施：W-CDMA、GSM、CDMA2000、TD-SCDMA、WiMax、LTE
- Wireless infrastructure: W-CDMA, GSM, CDMA2000, TD-SCDMA, WiMax, LTE
- 数字高/低中频功能
- Digital high/low-IF function
- 内部数字上变频功能
- Internal digital upconversion function
- 发射分集
- Transmit diversity
- 宽带通信：LMDS、MMDS、点对点通信
- Broadband communications: LMDS, MMDS, point-to-point communication

标准 / Standards

- 详细规范及确认号：Q/GC 0211-2026《半导体集成电路 SXD005 型双通道 16 位 1GSPS D/A 转换器详细规范》
- Detailed specification and approval number: Q/GC 0211-2026, "Detailed Specification for Semiconductor Integrated Circuit SXD005 Dual-Channel 16-Bit 1GSPS D/A Converter"
- 质量等级：企标
- Quality grade: Enterprise standard

产品特点 / Features

- 模拟电源电压：3.3V / Analog supply voltage: 3.3 V
- 数字电源电压：1.8V / Digital supply voltage: 1.8 V
- 分辨率：16bit / Resolution: 16 bits
- 转换速率：1000MSPS / Conversion rate: 1000 MSPS
- SFDR：87.90dBFS@4 倍内插，fDAC=800MSPS，fOUT=70MHz（典型值）/ SFDR: 87.90 dBFS at 4x interpolation, fDAC = 800 MSPS, fOUT = 70 MHz (typical)
- IMD：82.69dBFS@4 倍内插，fDAC=800MSPS，fOUT1=100MHz，fOUT2=99MHz（典型值）/ IMD: 82.69 dBFS at 4x interpolation, fDAC = 800 MSPS, fOUT1 = 100 MHz, fOUT2 = 99 MHz (typical)
- DNL：±2.1LSB（典型值）/ DNL: ±2.1 LSB (typical)
- INL：±3.5LSB（典型值）/ INL: ±3.5 LSB (typical)
- 功耗：≤1.5W（典型值 0.6W）/ Power dissipation: ≤1.5 W (typical 0.6 W)
- 模拟输出范围：7.5mA~32.5mA / Analog output range: 7.5 mA to 32.5 mA
- 输入数据接口：CMOS 接口、SPI 接口 / Input data interface: CMOS interface, SPI interface
- ESD 等级：500V / ESD rating: 500 V
- 产品重量：0.67g±0.13g / Weight: 0.67 g ± 0.13 g

产品描述 / Product Description

SXD005 是一款双通道、16 位、高动态范围数模转换器。该转换器可提供高达 1GSPS 采样速率；并可以产生最高达奈奎斯特频率的多载波。本产品具有针对直接变频传输应用进行优化的特性，这些特性包括：数字实/复调制以及增益与失调补偿等功能。产品中的 DAC 内核输出级经过优化，可以与主流的模拟正交调制器无缝接口，如：ADI 公司的 ADL537X FMOD 系列调制器。三线式接口允许对许多内部参数进行编程和回读。DAC 内核满量程输出电流可以在 10mA 至 30mA 范围内进行编程调节。本产品具有 4 种插值模式，1×插值模式时的最大输入数据速率为 300MSPS，2×插值模式时的最大输入数据速率为 250MSPS，4×插值模式时的最大输入数据速率为 200MSPS，8×插值模式时的最大输入数据速率为 125MSPS。本产品采用先进的 0.18μm CMOS 工艺制造，采用 1.8V/3.3V 电源供电，最大总功耗为 1.5W。该产品采用 100 引脚的 LQFP100 封装进行封装。

The SXD005 is a dual-channel, 16-bit, high-dynamic-range digital-to-analog converter. It provides a sample rate of up to 1 GSPS and can generate multicarrier signals up to the Nyquist frequency. The product features functions optimized for direct-conversion transmit applications, including digital real/complex modulation and gain and offset compensation. The DAC core output stage is optimized for seamless interfacing with mainstream analog quadrature modulators, such as ADI's ADL537X FMOD series modulators. The three-wire interface allows programming and readback of many internal parameters. The DAC core full-scale output current can be programmed over the range of 10 mA to 30 mA. The product has four interpolation modes: the maximum input data rate is 300 MSPS in 1× interpolation mode, 250 MSPS in 2× mode, 200 MSPS in 4× mode, and 125 MSPS in 8× mode. The product is fabricated in an advanced 0.18 μm CMOS process, operates from 1.8 V/3.3 V supplies, and has a maximum total power dissipation of 1.5 W. It is housed in a 100-pin LQFP100 package.

SXD005 从功能上可以划分为数字滤波器单元、DAC 内核单元、时钟（包含内部锁相环）单元、辅助 DAC、多芯片同步单元等。DAC 输入时钟（REFCLK+, REFCLK-）作为差分输入信号，差分峰峰值电压范围为 600~1800mV，共模电压范围为 350~450mV，最大时钟速率为 1000MHz。同步信号（SYNC_I+, SYNC_I-）作为输入信号，LVDS 输入电压范围为 825~1575mV，最大输入速率为 250MSPS。SCLK 输入时钟为 CMOS 输入信号，最大时钟速率为 40MHz。数字部分对输入的信号进行数字内插和数字域实调制、复调制功能；DAC 内核对

数字信号进行数字到模拟的转换；SPI 对整个芯片进行配置；时钟单元为整个电路提供高质量的时钟、四个辅助 DAC 用于通道增益和失调校正、多芯片同步单元负责多个芯片间的同步功能。

Functionally, the SXD005 can be divided into a digital filter unit, a DAC core unit, a clock unit (including an internal phase-locked loop), auxiliary DACs, a multi-chip synchronization unit, and other blocks. The DAC input clock (REFCLK+, REFCLK−) is a differential input signal with a differential peak-to-peak voltage range of 600 mV to 1800 mV, a common-mode voltage range of 350 mV to 450 mV, and a maximum clock rate of 1000 MHz. The synchronization signal (SYNC_I+, SYNC_I−) is an input signal with an LVDS input voltage range of 825 mV to 1575 mV and a maximum input rate of 250 MSPS. The SCLK input clock is a CMOS input signal with a maximum clock rate of 40 MHz. The digital section performs digital interpolation and real/complex modulation in the digital domain on the input signals; the DAC core converts digital signals to analog; the SPI configures the whole chip; the clock unit provides high-quality clocks for the whole circuit; the four auxiliary DACs are used for channel gain and offset correction; and the multi-chip synchronization unit handles synchronization between multiple chips.

SXD005 功能框图如图 1 所示。

The functional block diagram of the SXD005 is shown in Figure 1.

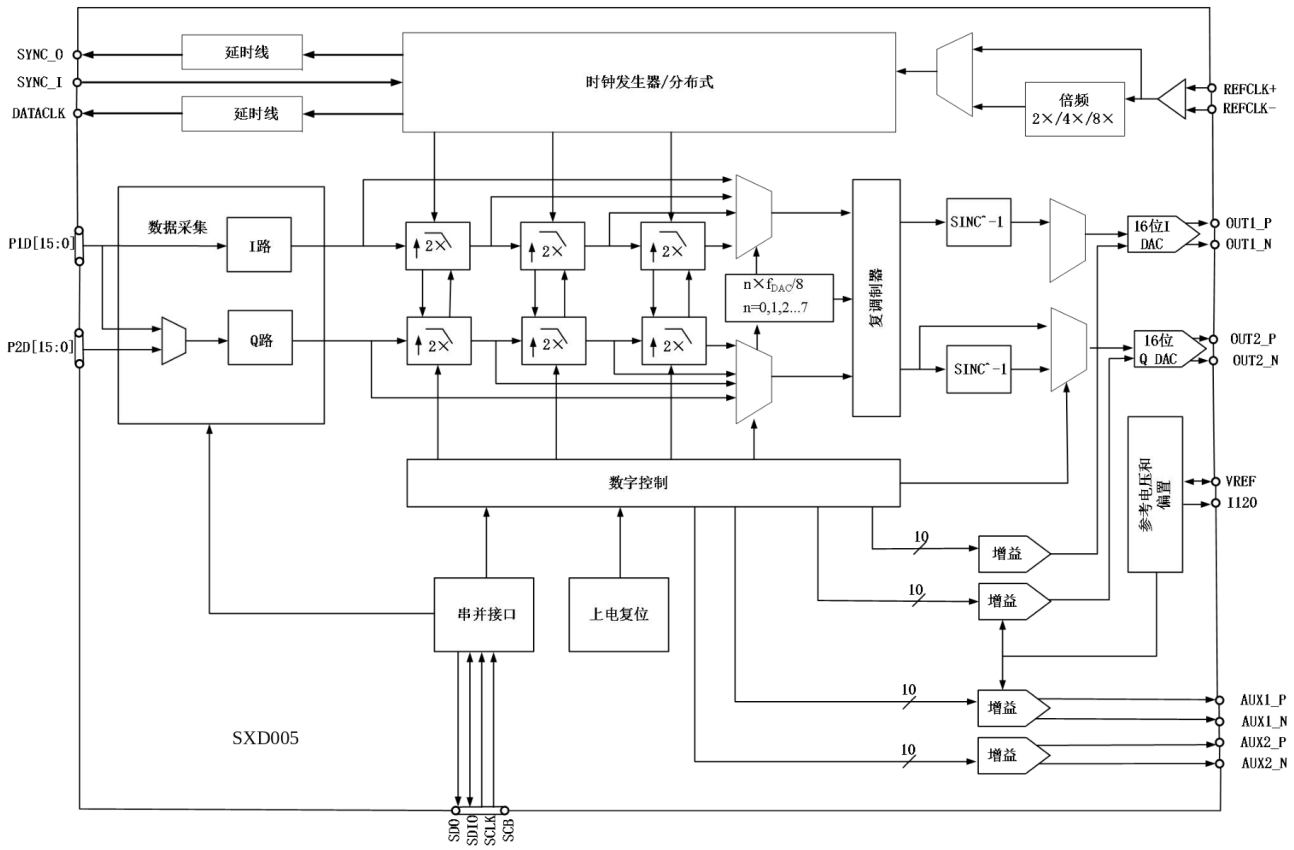


Figure 1: 功能框图

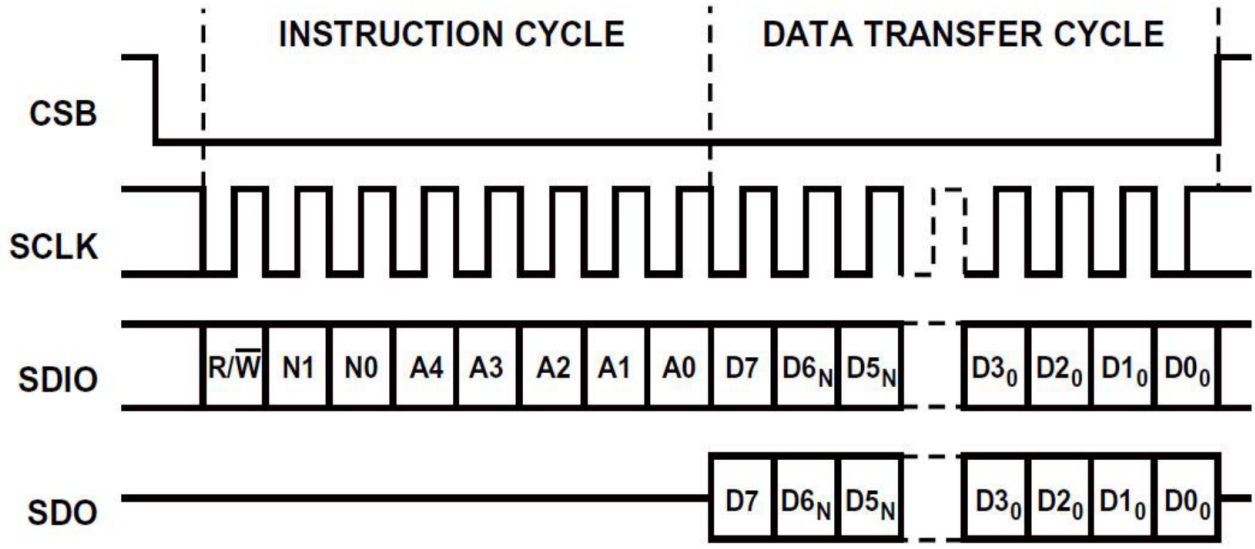


Figure 2: 串行接口时序，MSB 优先

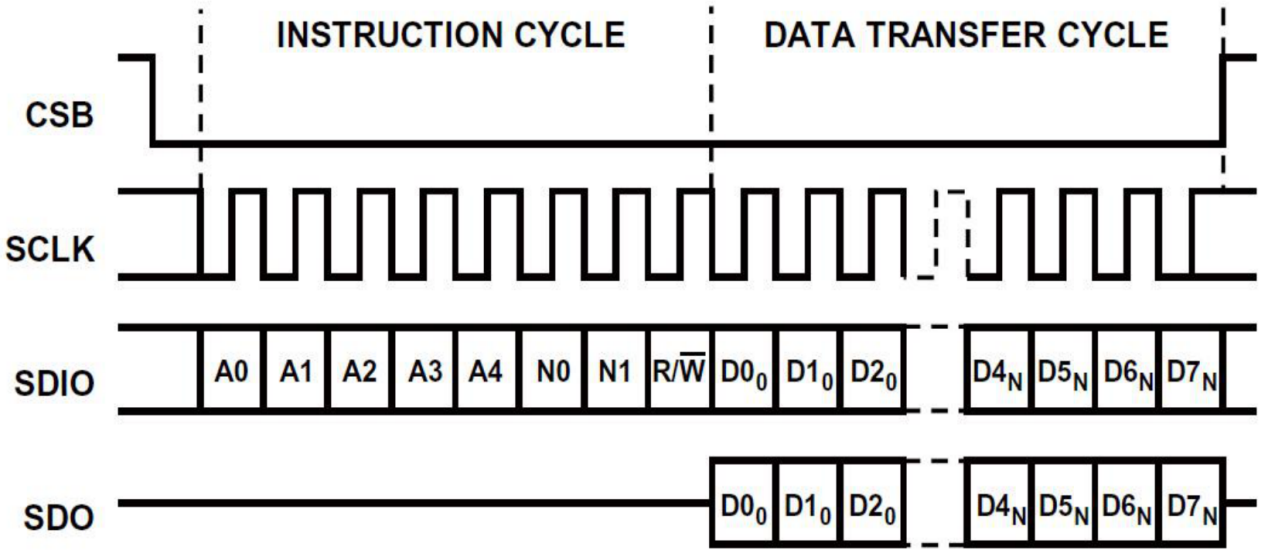


Figure 3: 串行接口时序，LSB 优先

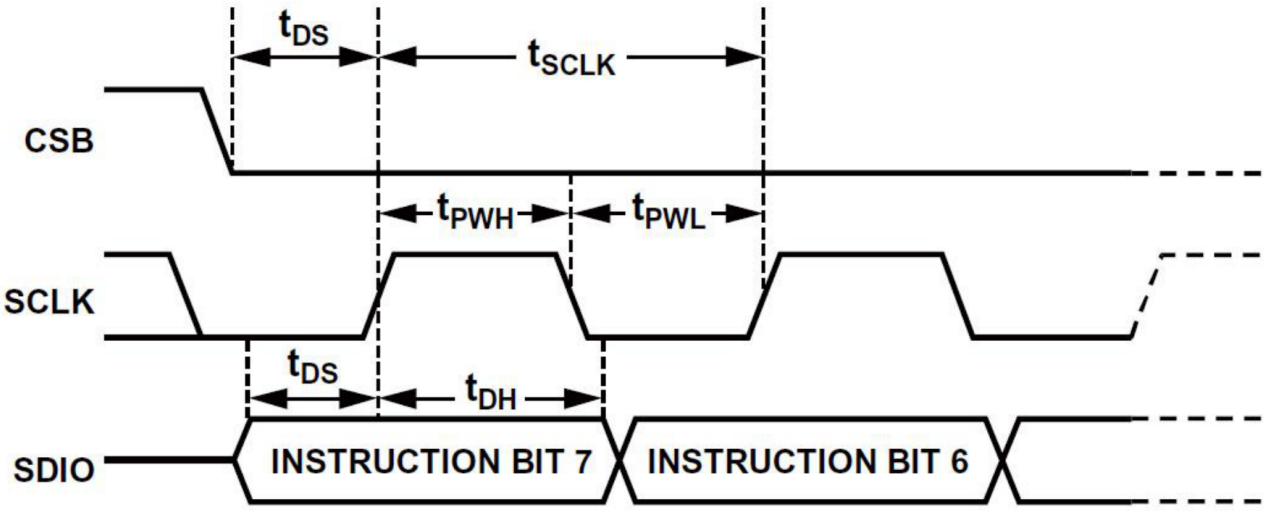


Figure 4: 三线式接口寄存器写操作时序图

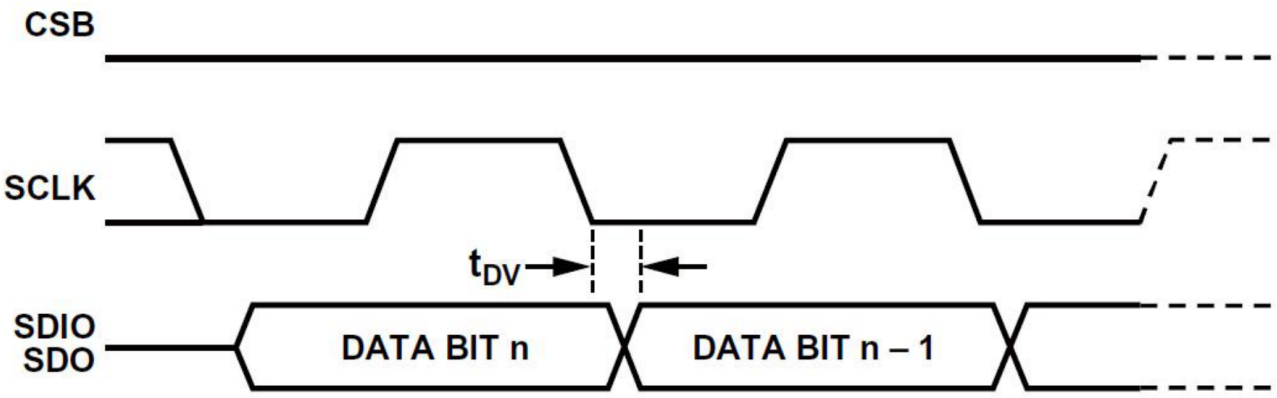


Figure 5: 三线式接口寄存器读操作时序图

产品外形图和实物图片 / Package Outline and Physical Pictures

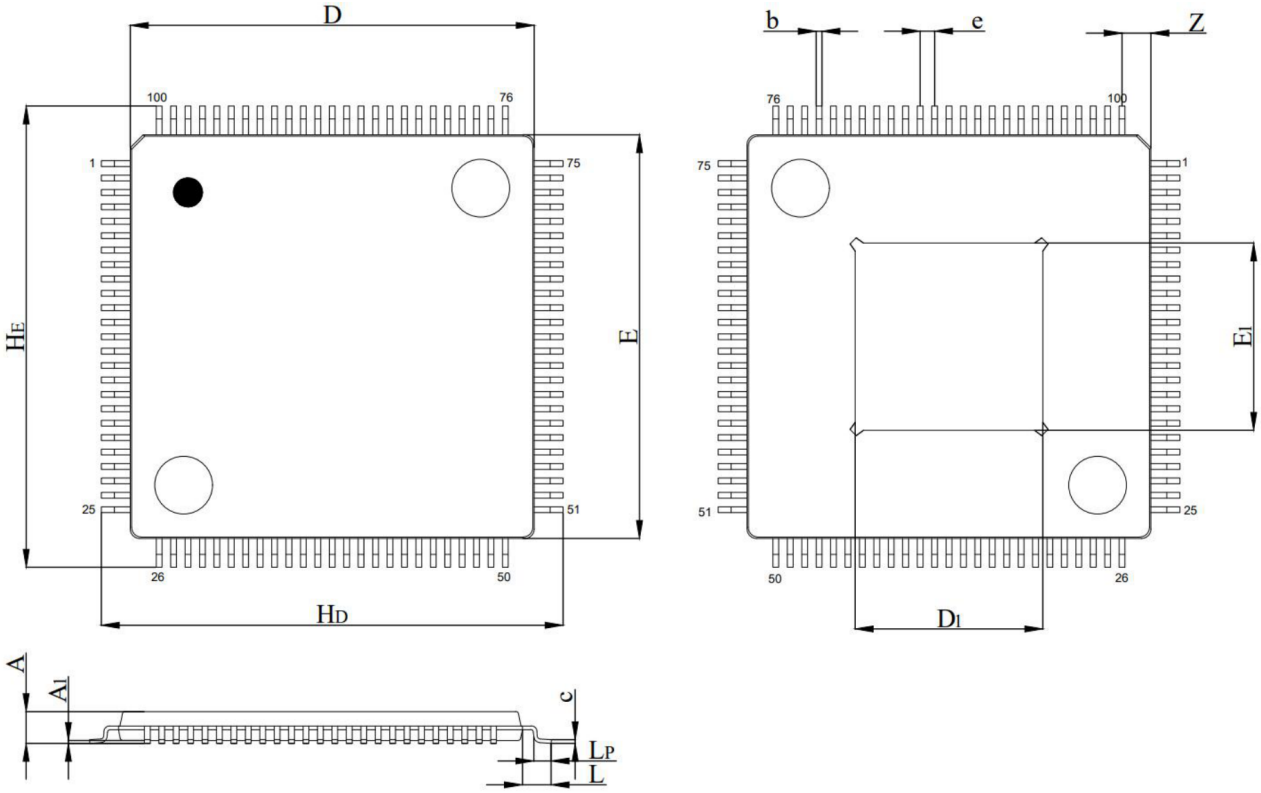


Figure 6: 产品外形尺寸图和实物照片

单位为毫米 / Units: mm

尺寸符号 / Symbol	数值 / Value			尺寸符号 / Symbol	数值 / Value		
	最小 / Min	公称 / Nom	最大 / Max		最小 / Min	公称 / Nom	最大 / Max
A	0.90	1.10a	1.30	E1	6.30	6.50a	6.70
A1	0.05	0.10a	0.15	e	—	0.50a	—
D	13.80	14.00a	14.20	b	0.17	0.22a	0.27
E	13.80	14.00a	14.20	c	0.09	0.15a	0.20
HD	15.80	16.00a	16.20	Lp	0.45	0.60a	0.75
HE	15.80	16.00a	16.20	L	0.80	1.00a	1.20
D1	6.30	6.50a	6.70	Z	—	1.00a	1.20

a 外壳实际公称值，推荐用户参考该尺寸设计使用； a: Actual nominal value of the package; users are recommended to refer to these dimensions for design.

注：推荐焊盘设计详见电装说明。 Note: See the assembly instructions for recommended pad layout.

引出端排列（俯视图）/ Pin Arrangement (Top View)

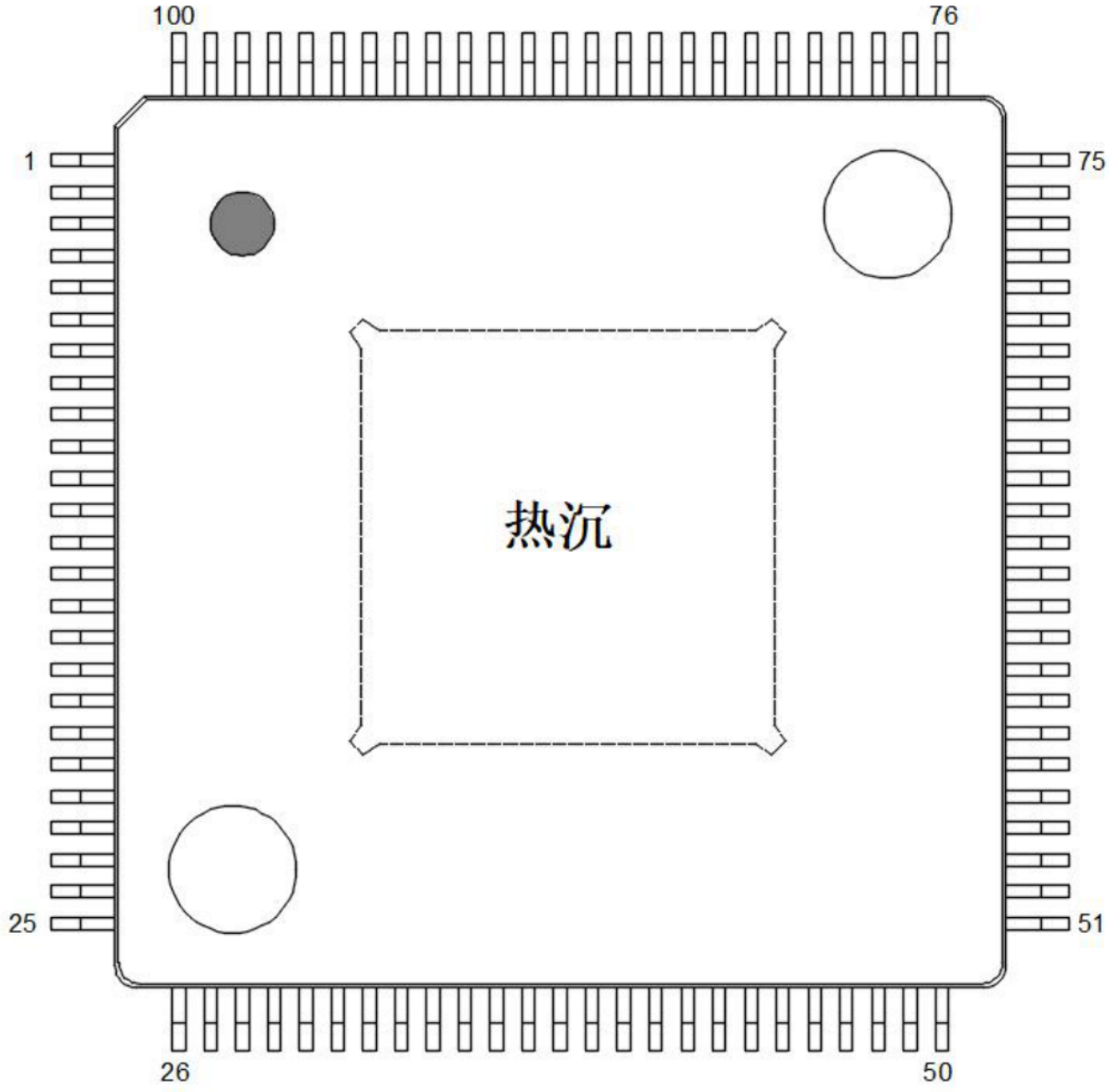


Figure 7: 引出端排列

引出端功能符号表 / Pin Function Table

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
1	VDDC	1.8V 时钟电源 / 1.8 V clock supply	/	51	P2B6	端口 Q 数据输入位 6 / Port Q data input bit 6	I
2	VDDC	1.8V 时钟电源 / 1.8 V clock supply	/	52	P2B5	端口 Q 数据输入位 5 / Port Q data input bit 5	I
3	GNDC	时钟地 / Clock ground	/	53	VDDD<1.8>		/

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
						1.8V 数字电源 / 1.8 V digital supply	
4	GNDC	时钟地 / Clock ground	/	54	GNDD	数字地 / Digital ground	/
5	CLK+	差分时钟输入正端 / Differential clock input, positive	I	55	P2B4	端口 Q 数据输入位 4 / Port Q data input bit 4	I
6	CLK-	差分时钟输入负端 / Differential clock input, negative	I	56	P2B3	端口 Q 数据输入位 3 / Port Q data input bit 3	I
7	GNDC	时钟地 / Clock ground	/	57	P2B2	端口 Q 数据输入位 2 / Port Q data input bit 2	I
8	GNDC	时钟地 / Clock ground	/	58	P2B1	端口 Q 数据输入位 1 / Port Q data input bit 1	I
9	VDDD	1.8V 数字电源 / 1.8 V digital supply	/	59	P2B0	端口 Q 数据输入位 0 / Port Q data input bit 0	I
10	VDDD	1.8V 数字电源 / 1.8 V digital supply	/	60	VDDD<1.8>	1.8V 数字电源 / 1.8 V digital supply	/
11	GNDC	时钟地 / Clock ground	/	61	VDDD<3.3>	3.3V 数字电源 / 3.3 V digital supply	/
12	GNDA	模拟地 / Analog ground	/	62	SYNC_O-	LVDS 差分同步输出负端 / LVDS differential sync output, negative	O
13	SYNC_I+	LVDS 差分同步输入正端 / LVDS differential sync input, positive	I	63	SYNC_O+	LVDS 差分同步输出正端 / LVDS differential sync output, positive	O
14	SYNC_I-	LVDS 差分同步输入负端 / LVDS differential sync input, negative	I	64	GNDD	数字地 / Digital ground	/
15	GNDD	数字地 / Digital ground	/	65	PLL_LOCK	PLL 锁定指示 / PLL lock indicator	O
16	VDDD<1.8>	1.8V 数字电源 / 1.8 V digital supply	/	66	SPI_SDO	串行接口数据输出 / Serial interface data output	O
17	P1B15	端口 I 数据输入位 15 / Port I data input bit 15	I	67	SPI_SDIO	串行接口数据输入/输出 / Serial interface data input/output	I/O
18	P1B14	端口 I 数据输入位 14 / Port I data input bit 14	I	68	SPI_CLK	串行接口时钟 / Serial interface clock	I
19	P1B13	端口 I 数据输入位 13 / Port I data input bit 13	I	69	SPI_CSB	串行接口片选信号 / Serial interface chip select	I
20	P1B12	端口 I 数据输入位 12 / Port I data input bit 12	I	70*	RESET	复位，高电平有效 / Reset, active high	I
21	P1B11	端口 I 数据输入位 11 / Port I data input bit 11	I	71	IRQ	中断请求 / Interrupt request	O
22	GNDD	数字地 / Digital ground	/	72	GNDA	模拟地 / Analog ground	/
23	VDDD<1.8>	1.8V 数字电源 / 1.8 V digital supply	/	73	IPTAT	工厂测试引脚 / Factory test pin	O
24	P1B10		I	74	VREFF		O

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
		端口 I 数据输入位 10 / Port I data input bit 10				基准电压输出 / Reference voltage output	
25	P1B9	端口 I 数据输入位 9 / Port I data input bit 9	I	75	I120	120μA 基准电流 / 120 μA reference current	/
26	P1B8	端口 I 数据输入位 8 / Port I data input bit 8	I	76	VDDA	3.3V 模拟电源 / 3.3 V analog supply	/
27	P1B7	端口 I 数据输入位 7 / Port I data input bit 7	I	77	GNDA	模拟地 / Analog ground	/
28	P1B6	端口 I 数据输入位 6 / Port I data input bit 6	I	78	VDDA	3.3V 模拟电源 / 3.3 V analog supply	/
29	P1B5	端口 I 数据输入位 5 / Port I data input bit 5	I	79	GNDA	模拟地 / Analog ground	/
30	P1B4	端口 I 数据输入位 4 / Port I data input bit 4	I	80	VDDA	3.3V 模拟电源 / 3.3 V analog supply	/
31	P1B3	端口 I 数据输入位 3 / Port I data input bit 3	I	81	GNDA	模拟地 / Analog ground	/
32	GNDD	数字地 / Digital ground	/	82	GNDA	模拟地 / Analog ground	/
33	VDDD<1.8>	1.8V 数字电源 / 1.8 V digital supply	/	83	IOUTA2	通道 2 差分 DAC 电流输出正端 / Channel 2 differential DAC current output, positive	O
34	P1B2	端口 I 数据输入位 2 / Port I data input bit 2	I	84	IOUTB2	通道 2 差分 DAC 电流输出负端 / Channel 2 differential DAC current output, negative	O
35	P1B1	端口 I 数据输入位 1 / Port I data input bit 1	I	85	GNDA	模拟地 / Analog ground	/
36	P1B0	端口 I 数据输入位 0 / Port I data input bit 0	I	86	AUX2_P	通道 2 辅助 DAC 电流输出正端 / Channel 2 auxiliary DAC current output, positive	O
37	DATACLK	数据时钟输出 / Data clock output	O	87	AUX2_N	通道 2 辅助 DAC 电流输出负端 / Channel 2 auxiliary DAC current output, negative	O
38	VDDD<3.3>	3.3V 数字电源 / 3.3 V digital supply	O	88	GNDA	模拟地 / Analog ground	/
39	TXENABLE	发生使能。单端口模式下，此引脚也用作 IQ 选择 / Transmit enable. In single-port mode, this pin also serves as IQ select	I	89	AUX1_N	通道 1 辅助 DAC 电流输出负端 / Channel 1 auxiliary DAC current output, negative	O
40	P2B15	端口 Q 数据输入位 15 / Port Q data input bit 15	I	90	AUX1_P	通道 1 辅助 DAC 电流输出正端 / Channel 1 auxiliary DAC current output, positive	O
41	P2B14	端口 Q 数据输入位 14 / Port Q data input bit 14	I	91	GNDA	模拟地 / Analog ground	/
42	P2B13	端口 Q 数据输入位 13 / Port Q data input bit 13	I	92	IOUTB1	通道 1 差分 DAC 电流输出负端 / Channel 1 differential DAC current output, negative	O
43	VDDD<1.8>	1.8V 数字电源 / 1.8 V digital supply	/	93	IOUTA1		O

引出端号 / Pin	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin	符号 / Symbol	名称 / Name	I/O
						通道 1 差分 DAC 电流输出正端 / Channel 1 differential DAC current output, positive	
44	GNDD	数字地 / Digital ground	/	94	GNDA	模拟地 / Analog ground	/
45	P2B12	端口 Q 数据输入位 12 / Port Q data input bit 12	I	95	GNDA	模拟地 / Analog ground	/
46	P2B11	端口 Q 数据输入位 11 / Port Q data input bit 11	I	96	VDDA	3.3V 模拟电源 / 3.3 V analog supply	/
47	P2B10	端口 Q 数据输入位 10 / Port Q data input bit 10	I	97	GNDA	模拟地 / Analog ground	/
48	P2B9	端口 Q 数据输入位 9 / Port Q data input bit 9	I	98	VDDA	3.3V 模拟电源 / 3.3 V analog supply	/
49	P2B8	端口 Q 数据输入位 8 / Port Q data input bit 8	I	99	GNDA	模拟地 / Analog ground	/
50	P2B7	端口 Q 数据输入位 7 / Port Q data input bit 7	I	100	VDDA	3.3V 模拟电源 / 3.3 V analog supply	/

注：0 端口为热沉，接地电位 AGND。 Note: Pin 0 is the thermal pad (heat sink), at AGND ground potential.

*此引脚可将所有寄存器复位至默认值。由于电源的慢速压摆率可能在数字模块中生成不正确的初始化状态，建议器件上电后在此引脚上生成一个脉冲。 *This pin can reset all registers to their default values. Because a slow power-supply slew rate may generate an incorrect initialization state in the digital module, it is recommended to generate a pulse on this pin after device power-up.

推荐工作条件 / Recommended Operating Conditions

- 输入数据率：≤300MSPS / Input data rate: ≤300 MSPS
- 工作频率：≤1000MHz / Operating frequency: ≤1000 MHz
- 3.3V 模拟电源模拟电源电压：3.1V~3.5V / 3.3 V analog supply voltage: 3.1 V to 3.5 V
- 3.3V 数字电源数字电源电压：3.1V~3.5V / 3.3 V digital supply voltage: 3.1 V to 3.5 V
- 1.8V 时钟电源模拟电源电压：1.7V~1.9V / 1.8 V clock supply voltage: 1.7 V to 1.9 V
- 1.8V 数字电源数字电源电压：1.7V~1.9V / 1.8 V digital supply voltage: 1.7 V to 1.9 V
- 工作环境温度：-40°C~85°C / Operating ambient temperature: -40°C to 85°C

绝对最大额定值 / Absolute Maximum Ratings

- 3.3V 模拟电源电压：-0.3V～3.6V / 3.3 V analog supply voltage: -0.3 V to 3.6 V
- 3.3V 数字电源电压：-0.3V～3.6V / 3.3 V digital supply voltage: -0.3 V to 3.6 V
- 1.8V 数字电源电压：-0.3V～1.98V / 1.8 V digital supply voltage: -0.3 V to 1.98 V
- 1.8V 数字电源电压：-0.3V～1.98V / 1.8 V digital supply voltage: -0.3 V to 1.98 V
- 贮存温度：-65°C～150°C / Storage temperature: -65°C to 150°C
- 结温：130°C / Junction temperature: 130°C
- 引线耐焊接温度：260°C / Lead soldering temperature: 260°C

性能指标 / Performance Specifications

除另有规定外，VDDC=VDDD<1.8>=1.8V，VDDD<3.3>=VDDA=3.3V，GNDC=GNDD=GNDA=0V，-40°C≤TA≤85°C。 Unless otherwise specified, VDDC = VDDD<1.8> = 1.8 V, VDDD<3.3> = VDDA = 3.3 V, GNDC = GNDD = GNDA = 0 V, -40°C ≤ TA ≤ 85°C.

参数 / Parameter	符号 / Symbol	条件 / Condition	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
线性误差 / Linearity error	EL	fCLK=250MHz，fIN=10MHz	-7	±4	7	LSB
分辨率 / Resolution	RES	—	—	16	—	bits
微分非线性 / Differential nonlinearity	EDL	—	-8	±2.1	+8	LSB
积分非线性 / Integral nonlinearity	EL	—	-16	±3.5	+16	LSB
失调误差 / Offset error	EO	—	-1	±0.0000	+1	%FSR
增益误差 / Gain error	EG	—	-8	-0.6	+8	%FSR
内部基准电压 / Internal reference voltage	VREF	—	1.00	1.19	1.5	V
内部基准输出电阻 / Internal reference output resistance	ROREF	—	3.5	5.77	7.5	kΩ
满量程输出电流 / Full-scale output current	IO	—	7.5	——	32.5	mA
DAC 输出顺从电压范围 / DAC output compliance voltage range	VOC	—	-1.0	——	+1.0	V
功耗 / Power dissipation	PW	2x 模式，PLL off，fDAC=320MSPS，IF=16MHz	——	528.70	650	mW
功耗（掉电模式）/ Power dissipation (power-down mode)	PW	掉电模式 / Power-down mode	——	2.23	20	mW
功耗 / Power dissipation	PW	8x 模式，fDAC/4 调制，fDAC=1GSPS，IF=262.5MHz	——	978.40	1500	mW
VDDA 电源电压抑制比 / VDDA power supply rejection ratio	PSRR	—	-2	0.15	2	%FSR/V
CMOS 输入逻辑高电平 / CMOS input logic high level	VIH	—	2.5	2.50	——	V
CMOS 输入逻辑低电平 / CMOS input logic low level	VIL	—	——	0.40	0.4	V
CMOS 输出逻辑高电平 / CMOS output logic high level	VOH	DATACLK	2.0	3.28	——	V
	VOL	DATACLK	——	0.04	0.8	V

参数 / Parameter	符号 / Symbol	条件 / Condition	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
CMOS 输出逻辑低电平 / CMOS output logic low level						
DATACLK 输出占空比 / DATACLK output duty cycle	ODC	DATACLK	35	49.50	65	%
工作频率 / Operating frequency	fCLK_PLL_OFF	PLL 关 / PLL off	1000	1000	——	MHz
最大时钟速率 / Maximum clock rate	fCLK_PLL_ON	PLL 开 / PLL on	200	200	——	MHz
无杂散动态范围 / Spurious-free dynamic range	SFDR	4 倍内插，fDAC=800MSPS，fOUT=70MHz / 4x interpolation, fDAC = 800 MSPS, fOUT = 70 MHz	60	87.90	——	dBc
双音互调失调 / Two-tone intermodulation distortion	IMD	4 倍内插，fDAC=800MSPS，fOUT1=100MHz，fOUT2=99MHz / 4x interpolation, fDAC = 800 MSPS, fOUT1 = 100 MHz, fOUT2 = 99 MHz	55	82.69	——	dBc

注：典型值为常温测试数据。 Note: Typical values are room-temperature test data.

主要特性曲线图（电特性测试图）/ Typical Performance Curves (Electrical Test Plots)

为了对芯片进行评估，在常温下对芯片的各种工作模式进行了动态参数和静态参数测试。动态参数主要包括无杂散动态范围和三阶交调失真。静态参数包括微分非线性和积分非线性参数的测试。具体的测试结果如下所示。

To evaluate the chip, dynamic and static parameters were tested at room temperature in the chip's various operating modes. The dynamic parameters mainly include spurious-free dynamic range and third-order intermodulation distortion. The static parameters include differential nonlinearity and integral nonlinearity tests. The detailed test results are as follows.

1、动态性能测试 / Dynamic Performance Tests

A 无杂散动态范围（SFDR）/ Spurious-Free Dynamic Range (SFDR)

表 1 无杂散动态范围测试值所示为芯片（贴片测试）在不同工作模式下的无杂散动态范围测试结果。表 2 所示的结果表示了外部直接送入转换时钟和内部开启锁相环两种情况下的测量值。在表 1 中，对应于 fdac=100MSPS，fout=20MHz 情况下，此时未开启锁相环。因为在此情况下，锁相环的 VCO 不能提供该转换频率（ADI 原始产品也为同样情况）。

Table 1 (SFDR test values) shows the spurious-free dynamic range test results of the chip (surface-mount test) in different operating modes. The results shown in Table 2 give the measured values for the two cases of an externally supplied conversion clock and the internal phase-locked loop enabled. In Table 1, for the

case fdac = 100 MSPS, fout = 20 MHz, the phase-locked loop is not enabled, because in this case the PLL VCO cannot provide that conversion frequency (the same applies to the original ADI product).

表 1 无杂散动态范围测试值 / Table 1 SFDR Test Values

测试条件 / Test Condition	测量值（外部时钟）/ Measured (External Clock)	测量值（内部锁相环）/ Measured (Internal PLL)
fdac=100MSPS, fout=20MHz，滤波器为 1×模式，无偏移，无调制 / fdac = 100 MSPS, fout = 20 MHz, filter in 1× mode, no offset, no modulation	84dBc	none
fdac=200MSPS, fout=50MHz，滤波器为 1×模式，无偏移，无调制 / fdac = 200 MSPS, fout = 50 MHz, filter in 1× mode, no offset, no modulation	90dBc	88dBc
fdac=400MSPS, fout=70MHz，滤波器为 2×模式，无偏移，无调制 / fdac = 400 MSPS, fout = 70 MHz, filter in 2× mode, no offset, no modulation	75dBc	75dBc
fdac=800MSPS, fout=70MHz，滤波器为 4×模式，无偏移，无调制 / fdac = 800 MSPS, fout = 70 MHz, filter in 4× mode, no offset, no modulation	76dBc	76dBc
fdac=1000MSPS, fout=10MHz，滤波器为 8×模式，无偏移，无调制 / fdac = 1000 MSPS, fout = 10 MHz, filter in 8× mode, no offset, no modulation	73dBc	72dBc
fdac=1000MSPS, fout=40MHz，滤波器为 8×模式，无偏移，无调制 / fdac = 1000 MSPS, fout = 40 MHz, filter in 8× mode, no offset, no modulation	85dBc	83dBc

图 8 所示为芯片在 70MHz 的中频输出，800MSPS 转换速率下的无杂散动态范围测试值。图中所示为 I 通道的测量结果。

Figure 8 shows the spurious-free dynamic range test value of the chip at a 70 MHz IF output and an 800 MSPS conversion rate. The figure shows the measurement result of the I channel.

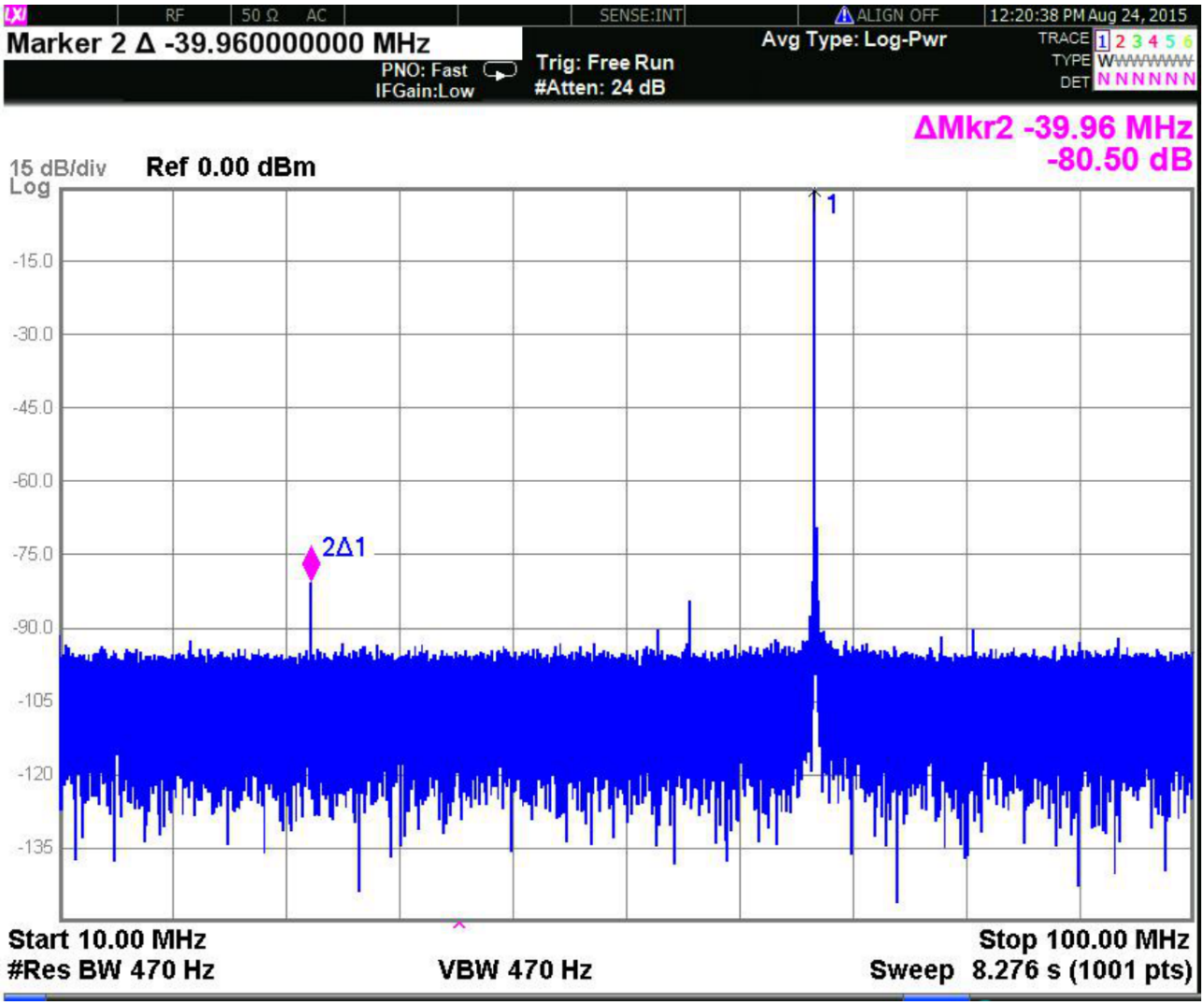


Figure 8: 杂散动态范围测试结果（中频输出 70MHz，转换率 800MSPS）

B 三阶交调失真（IMD）/ Third-Order Intermodulation Distortion (IMD)

表 2 所示为芯片（贴片测试）在不同工作模式下的三阶交调失真测试结果。

Table 2 shows the third-order intermodulation distortion test results of the chip (surface-mount test) in different operating modes.

表 2 三阶交调失真测试值 / Table 2 Third-Order IMD Test Values

测试条件 / Test Condition	测量值（外部时钟）/ Measured (External Clock)	测量值（内部锁相环）/ Measured (Internal PLL)
fdac=200MSPS, fout=50/49MHz，滤波器为 1×模式，无偏移，无调制 / fdac = 200 MSPS, fout = 50/49 MHz, filter in 1× mode, no offset, no modulation	79dBc	76dBc
fdac=400MSPS, fout=60/59MHz，滤波器为 1×模式，无偏移，无调制 / fdac = 400 MSPS, fout = 60/59 MHz, filter in 1× mode, no offset, no modulation	76dBc	80dBc
fdac=400MSPS, fout=80/79MHz，滤波器为 2×模式，无偏移，无调制 / fdac = 400 MSPS, fout = 80/79 MHz, filter in 2× mode, no offset, no modulation	73dBc	75dBc

测试条件 / Test Condition	测量值（外部时钟）/ Measured (External Clock)	测量值（内部锁相环）/ Measured (Internal PLL)
fdac=800MSPS, fout=100/99MHz，滤波器为 4×模式，偏移 fdata/2，无调制 / fdac = 800 MSPS, fout = 100/99 MHz, filter in 4× mode, offset fdata/2, no modulation	73dBc	67dBc

图 9 所示为芯片在 79MHz/80MHz 的中频输出，400MSPS 转换速率下的三阶双音互调测试值。图中所示为 I 通道的测量结果。

Figure 9 shows the third-order two-tone intermodulation test value of the chip at a 79 MHz/80 MHz IF output and a 400 MSPS conversion rate. The figure shows the measurement result of the I channel.

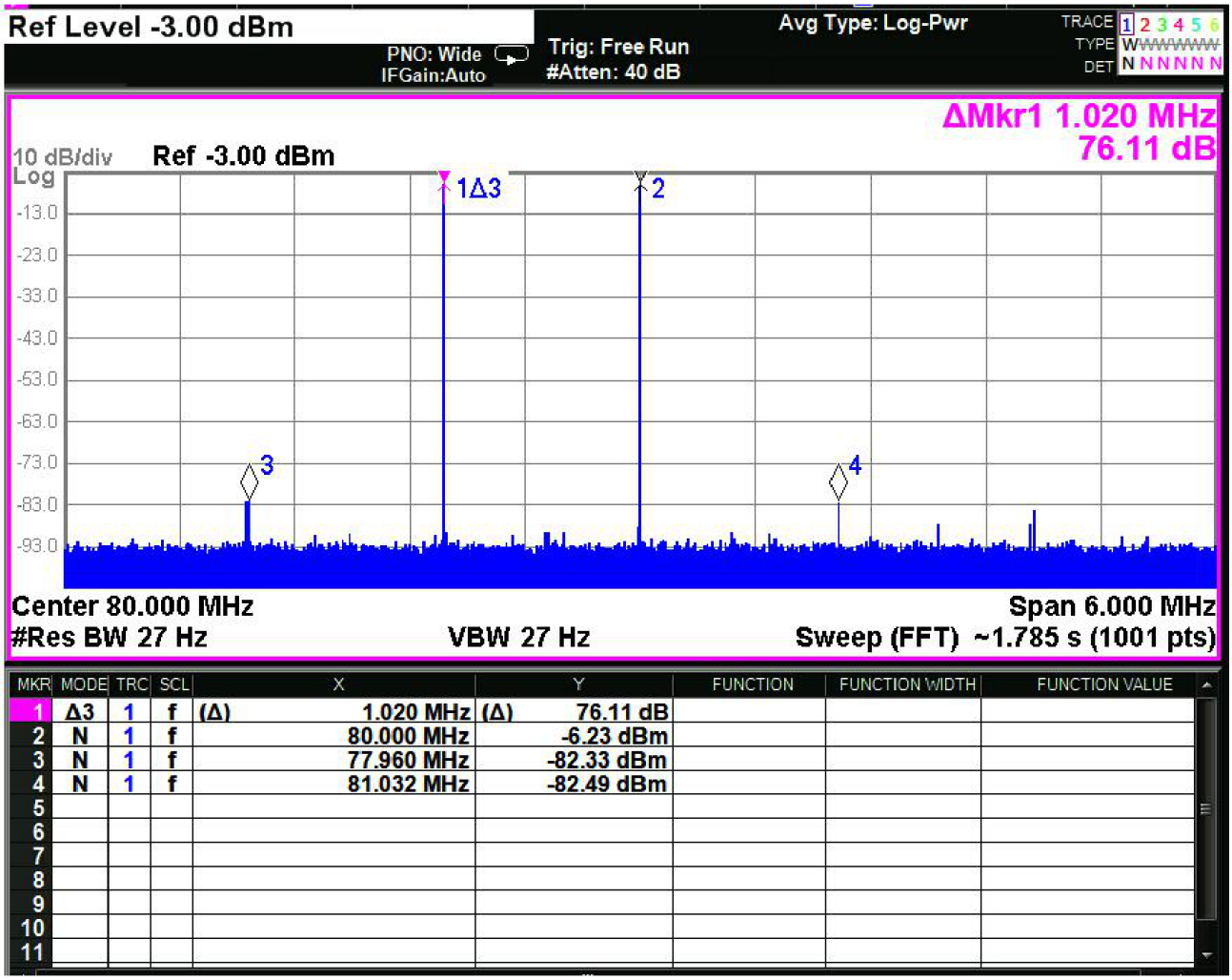


Figure 9: 三阶双音互调测试结果（中频输出 79MHz/80MHz，转换率 400MSPS）

2、静态测试 / Static Tests

表 3 芯片静态参数测试值 / Table 3 Chip Static Parameter Test Values

芯片编号 / Chip No.	电路 / Circuit	微分非线性（LSB）/ DNL (LSB)	积分非线性（LSB）/ INL (LSB)	失调误差（%FSR）/ Offset Error (%FSR)	增益误差（%FSR）/ Gain Error (%FSR)
1	I	-0.61~2.72	-2.34~5.45	0.003	-1.60

芯片编号 / Chip No.	电路 / Circuit	微分非线性（LSB）/ DNL (LSB)	积分非线性（LSB）/ INL (LSB)	失调误差（%FSR）/ Offset Error (%FSR)	增益误差（%FSR）/ Gain Error (%FSR)
1	Q	-1.14~1.75	-2.47~3.85	0.004	-1.60
2	I	-1.86~1.28	-3.08~3.24	0.003	-1.80
2	Q	-2.55~1.81	-6.85~2.76	0.004	-1.80
3	I	-2.69~1.33	-2.41~4.04	0.003	-1.60
3	Q	-3.62~0.08	-2.84~2.96	0.004	-1.60
4	I	-2.63~0.76	-5.18~1.51	0.003	-2.20
4	Q	-2.16~1.59	-3.49~3.29	0.004	-2.20
5	I	-1.75~2.16	-4.08~4.37	0.002	-1.60
5	Q	-2.74~0.814	-2.69~4.33	0.004	-1.60

表 4 所示为对五只随机选取的芯片进行静态测试的测试结果。

Table 4 shows the static test results of five randomly selected chips.

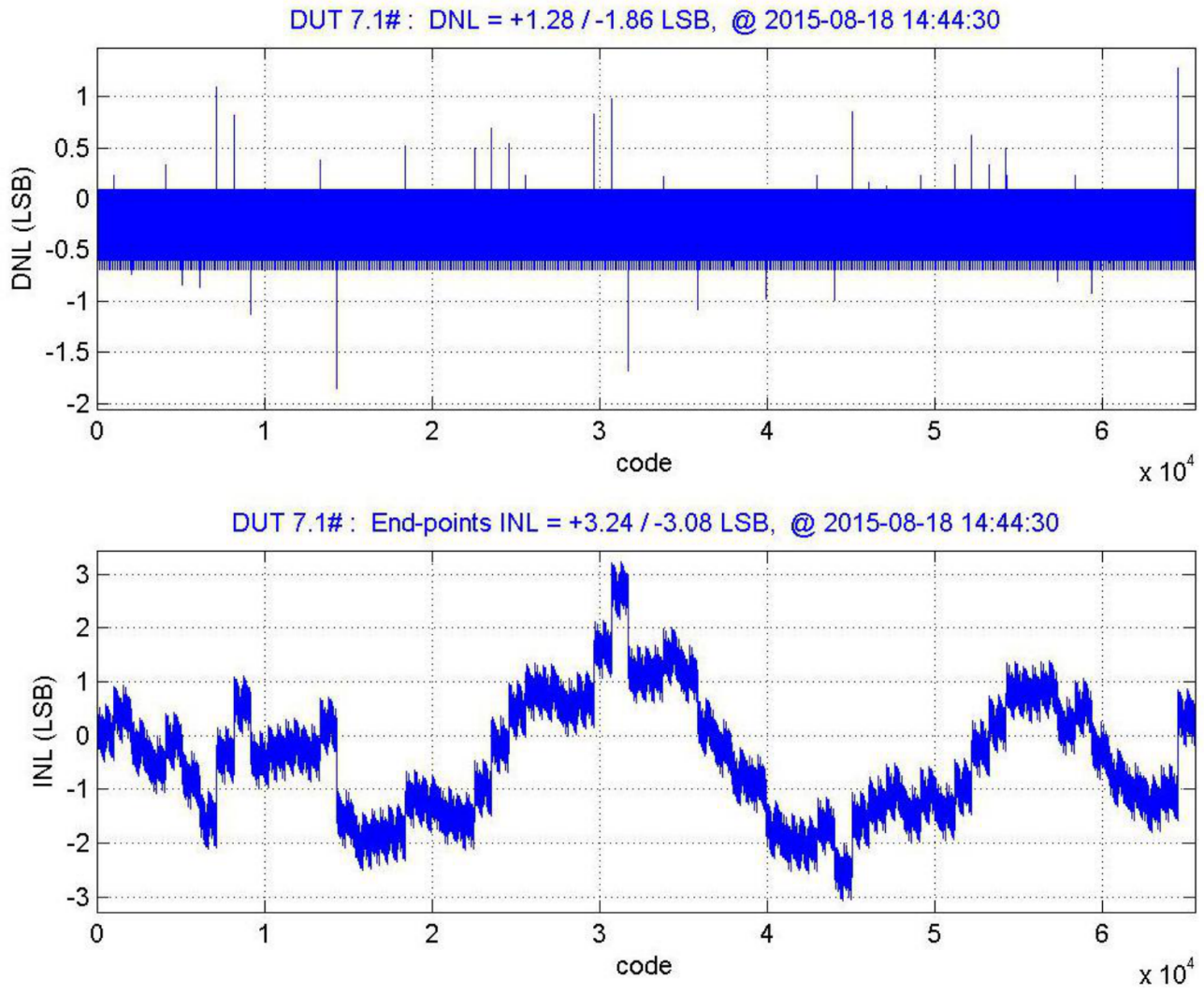


Figure 10: 典型微分非线性/积分非线性图

图 10 所示为典型的微分非线性和积分非线性的实测图形。

Figure 10 shows a typical measured plot of differential nonlinearity and integral nonlinearity.

典型应用线路图 / Typical Application Circuit

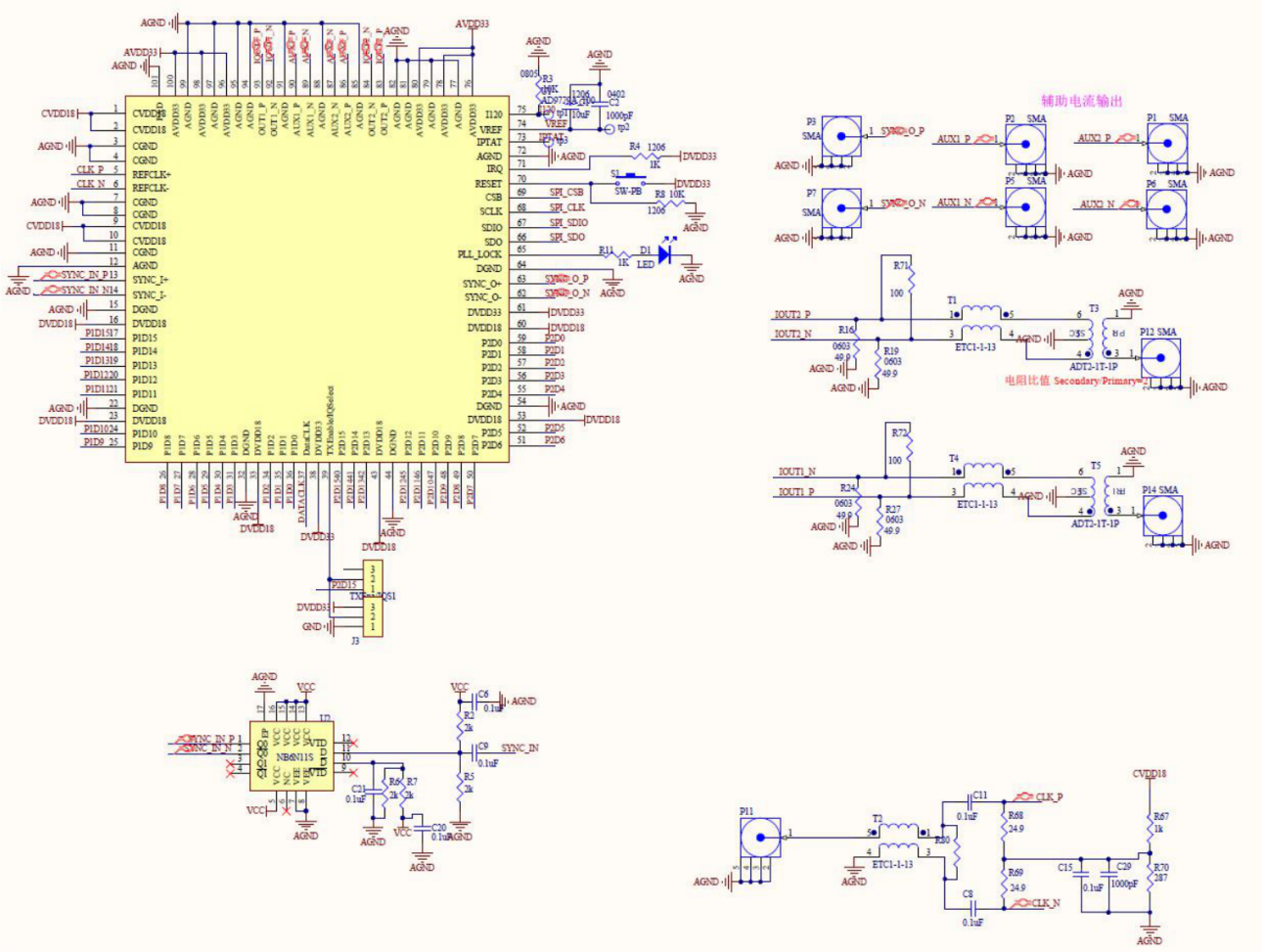


Figure 11: SXD005 PCB 板外围电路

单元模块及工作原理 / Functional Blocks and Theory of Operation

1、原理概述 / Principle Overview

SXD005 型高速高精度双通道 16 位 D/A 转换器是采用 CMOS 工艺制造的半导体集成电路。该产品具有采样率高、线性误差小、失调增益补偿和 SPI 接口控制等特点。通过 SPI 接口可对内部电路的工作状态和满度输入范围进行配置；模拟输入为 CMOS 接口输入；时钟输入为差分输入。

The SXD005 high-speed, high-precision dual-channel 16-bit D/A converter is a semiconductor integrated circuit fabricated in a CMOS process. The product features a high sample rate, small linearity error, offset/gain compensation, and SPI interface control. The operating state of the internal circuits and the full-scale input range can be configured through the SPI interface; the analog input is a CMOS interface input; and the clock input is a differential input.

2、模拟输入 / Analog Input

SXD005 的模拟输入为 CMOS 输入，输入逻辑高电平大于 2.5V，输入逻辑低电平小于 0.4V。本产品具有 4 种插值模式，1×插值模式时的最大输入数据速率为 300MSPS，2×插值模式时的最大输入数据速率为 250MSPS，4×插值模式时的最大输入数据速率为 200MSPS，8×插值模式时的最大输入数据速率为 125MSPS。

The analog input of the SXD005 is a CMOS input, with an input logic high level greater than 2.5 V and an input logic low level less than 0.4 V. The product has four interpolation modes: the maximum input data rate is 300 MSPS in 1× interpolation mode, 250 MSPS in 2× mode, 200 MSPS in 4× mode, and 125 MSPS in 8× mode.

3、时钟输入 / Clock Input

SXD005 的 DAC 输入时钟（REFCLK+, REFCLK-）作为差分输入信号，差分峰峰值电压范围为 600~1800mV，共模电压范围为 350~450mV，最大时钟速率为 1000MHz。同步信号（SYNC_I+, SYNC_I-）作为输入信号，LVDS 输入电压范围为 825~1575mV，最大输入速率为 250MSPS。SCLK 输入时钟为 CMOS 输入信号，最大时钟速率为 40MHz。

The DAC input clock (REFCLK+, REFCLK−) of the SXD005 is a differential input signal with a differential peak-to-peak voltage range of 600 mV to 1800 mV, a common-mode voltage range of 350 mV to 450 mV, and a maximum clock rate of 1000 MHz. The synchronization signal (SYNC_I+, SYNC_I−) is an input signal with an LVDS input voltage range of 825 mV to 1575 mV and a maximum input rate of 250 MSPS. The SCLK input clock is a CMOS input signal with a maximum clock rate of 40 MHz.

4、三线式接口 / Three-Wire Interface

SXD005 采用了三线式接口，三线式端口是一种灵活的同步串行通讯端口，可以很方便地与多种工业标准微控制器和微处理器接口。该端口兼容大多数同步传输格式，包括 Motorola SPI 和 Intel＊SSR 协议。

The SXD005 uses a three-wire interface. The three-wire port is a flexible synchronous serial communication port that interfaces conveniently with many industry-standard microcontrollers and microprocessors. The port is compatible with most synchronous transfer formats, including Motorola SPI and Intel* SSR protocols.

此接口可进行读写操作，访问用来配置 SXD005 的所有寄存器。支持单字节和多字节传输，以及 MSB 优先和 LSB 优先传输格式。通过单个双向引脚（SDIO）或两个单向引脚（SDIO／SDO），可以实现串行数据输入／输出。

This interface supports read and write operations and accesses all registers used to configure the SXD005. It supports single-byte and multi-byte transfers, as well as MSB-first and LSB-first transfer formats. Serial data input/output can be implemented through a single bidirectional pin (SDIO) or two unidirectional pins (SDIO/SDO).

串行端口配置由寄存器 0x00 位［7：6］控制。必须注意，对串行端口配置所做的任何更改，都会在写入此字节的最后一位时立即生效。因此，可以使用多字节传输写入此寄存器，并在通信周期进行中更改配置。必须注意，对于当前通信周期的剩余字节，要使用新的配置。更改串行端口配置时，建议使用单字节传输，以免器件发生无法预料的行为。

The serial port configuration is controlled by register 0x00, bits [7:6]. Note that any change to the serial port configuration takes effect immediately when the last bit of the byte is written. A multi-byte transfer can therefore be used to write this register and change the configuration in the middle of a communication cycle; note that the remaining bytes of the current communication cycle must use the new configuration. When changing the serial port configuration, single-byte transfers are recommended to avoid unpredictable device behavior.

如本节所述，写入器件或从器件读出的所有串行端口数据传输均与 SCLK 引脚同步。如果同步丢失，器件有能力异步终止 I／O 操作，将串行端口控制器置于已知状态，从而再次获得同步。

As described in this section, all serial port data transfers written to or read from the device are synchronized to the SCLK pin. If synchronization is lost, the device can asynchronously terminate the I/O operation and place the serial port controller in a known state so that synchronization can be regained.

5、串行接口的通用操作 / General Operation of the Serial Interface

SXD005 的一个通信周期有两个阶段。阶段 1 是指令周期，用来写入一个指令字节到 SXD005，对应于 SCLK 的第 1 组 8 个上升沿。阶段 1 的指令字节定义了即将到来的数据传递是读或是写，以及第一个字节的数据传输所对应的寄存器地址。每个通信周期的 SCLK 的第 1 组 8 个上升沿通常用于将指令字节写入 SXD005。

A communication cycle of the SXD005 has two phases. Phase 1 is the instruction cycle, in which an instruction byte is written to the SXD005, corresponding to the first group of eight SCLK rising edges. The phase-1 instruction byte defines whether the upcoming data transfer is a read or a write, and the register address corresponding to the data transfer of the first byte. The first group of eight SCLK rising edges of each communication cycle is normally used to write the instruction byte to the SXD005.

CSB 引脚的逻辑电平先高后低，使三线式接口端口的时序复位到指令周期的初始状态。由此状态开始，后续 8 个 SCLK 上升沿代表当前 I／O 操作的指令位，而与内部寄存器的状态或三线式接口端口输入的其它信号电平无关。如果此时三线式接口端口处于指令周期或数据传输周期，则不会写入任何现有数据。

A high-to-low transition of the CSB pin logic level resets the timing of the three-wire interface port to the initial state of the instruction cycle. Starting from this state, the following eight SCLK rising edges represent the instruction bits of the current I/O operation, regardless of the state of the internal registers or the levels of other signals at the three-wire interface port inputs. If the three-wire interface port is in an instruction cycle or a data transfer cycle at this time, no existing data is written.

其余 SCLK 沿用于通信周期的第二阶段。第二阶段是器件与系统控制器之间实际进行数据传输的阶段。根据指令字节所提供的信息，第二阶段传输一个、两个、三个或四个数据字节。最好使用一个多字节传输。当寄存器访问只需要一个字节时，可以使用单字节数据传输，以降低 CPU 开销。写入各传输字节的最后一位后，寄存器立即改变。

The remaining SCLK edges are used for the second phase of the communication cycle, in which data is actually transferred between the device and the system controller. Depending on the information provided by the instruction byte, the second phase transfers one, two, three, or four data bytes. A multi-byte transfer is preferred. When a register access requires only one byte, a single-byte data transfer can be used to reduce CPU overhead. After the last bit of each transferred byte is written, the register changes immediately.

6、指令字节 / Instruction Byte

指令字节所包含的信息见表 4。

The information contained in the instruction byte is shown in Table 4.

表 4 三线式接口指令字节 / Table 4 Three-Wire Interface Instruction Byte

	MSB							LSB
位 / Bit	17	16	15	14	13	12	11	10
内容 / Content	R/W	N1	NO	A4	A3	A2	A1	AO

指令字节位 7（R／W）决定指令字节写周期结束后是进行读操作还是写操作。逻辑 1 表示读操作。逻辑 0 表示写操作。

Bit 7 (R/W) of the instruction byte determines whether a read or a write operation follows the instruction byte write cycle. Logic 1 indicates a read operation; logic 0 indicates a write operation.

指令字节位 6（N1）和位 5（NO）决定数据传输周期需传输的字节数。表 5 列出了需传输的字节数对照表。

Bit 6 (N1) and bit 5 (NO) of the instruction byte determine the number of bytes to be transferred in the data transfer cycle. Table 5 lists the byte transfer count.

A4、A3、A2、A1 和 A0——指令字节的位 4、位 3、位 2、位 1 和位 0 决定通信周期的数据传输期间访问哪一个寄存器。对于多字节传输，此地址是起始字节地址。其余寄存器地址由器件根据 LSB 优先位（寄存器 0x00 位 6）产生。

A4, A3, A2, A1, and A0 — bits 4, 3, 2, 1, and 0 of the instruction byte — determine which register is accessed during the data transfer of the communication cycle. For a multi-byte transfer, this address is the starting byte address. The remaining register addresses are generated by the device according to the LSB-first bit (register 0x00, bit 6).

表 5 字节传输计数 / Table 5 Byte Transfer Count

N1	N0	描述 / Description
0	0	传输一个字节 / Transfer one byte
0	1	传输两个字节 / Transfer two bytes
1	0	传输三个字节 / Transfer three bytes
1	1	传输四个字节 / Transfer four bytes

7、串行接口端口引脚功能描述 / Serial Interface Port Pin Functions

7.1 串行时钟（SCLK）/ Serial Clock (SCLK)

串行时钟引脚用于同步输入／输出器件的数据，并控制内部状态机。SCLK 的最高频率为 40 MHz。所有数据输入都在 SCLK 的上升沿有效。所有数据都在 SCLK 的下降沿输出。

The serial clock pin synchronizes data input to and output from the device and controls the internal state machine. The maximum SCLK frequency is 40 MHz. All data inputs are valid on the rising edge of SCLK. All data is output on the falling edge of SCLK.

7.2 片选（CSB）/ Chip Select (CSB)

低电平有效输入启动并选通一个通信周期。它允许同一串行通信线路连接多个器件。当此输入高电平时，SDO 和 SDIO 引脚会进入高阻抗状态。在整个通信周期，片选应保持低电平。

The active-low input initiates and gates a communication cycle. It allows multiple devices to be connected to the same serial communication line. When this input is high, the SDO and SDIO pins enter a high-impedance state. The chip select should remain low throughout the communication cycle.

7.3 串行数据输入／输出（SDIO）/ Serial Data Input/Output (SDIO)

向器件写入数据必须通过此引脚进行。不过，该引脚也能作为双向数据线使用。寄存器 0x00 的位 7 控制此引脚配置。缺省为逻辑 0，将 SDIO 引脚配置为单向数据线。

Data written to the device must pass through this pin. However, the pin can also be used as a bidirectional data line. Bit 7 of register 0x00 controls the configuration of this pin. The default is logic 0, which configures the SDIO pin as a unidirectional data line.

7.4 串行数据输出（SDO）/ Serial Data Output (SDO)

如果协议选择用不同的通信线来发送和接收数据，那么数据是从该引脚读出的。当器件以单独的双向 I／O 模式运行时，此引脚不会输出数据，并置为高阻抗状态。

If the protocol uses different communication lines to send and receive data, data is read from this pin. When the device operates in a separate bidirectional I/O mode, this pin does not output data and is placed in a high-impedance state.

8、MSB／LSB 传输 / MSB/LSB Transfer

串行端口可以支持 MSB 优先和 LSB 优先两种数据格式。此功能由 LSB／MSB 优先寄存器位（寄存器 0x00 的位 6）控制。缺省为 MSB 优先格式（LSB／MSB 优先＝0）。

The serial port supports both MSB-first and LSB-first data formats. This function is controlled by the LSB/MSB-first register bit (register 0x00, bit 6). The default is the MSB-first format (LSB/MSB first = 0).

当选择 MSB 优先格式（LSB／MSB 优先＝0）时，指令和数据位必须按照从 MSB 到 LSB 的顺序写入。采用 MSB 优先格式的多字节数据传输以一个指令字节开始，该指令字节包括最高数据字节的寄存器地址。后续数据字节应按照从高地址到低地址的顺序传输。在 MSB 优先模式下，多字节通信周期每传输一个数据字节，串行端口内部字节地址发生器便递减 1。

When the MSB-first format is selected (LSB/MSB first = 0), instruction and data bits must be written in order from MSB to LSB. A multi-byte data transfer in MSB-first format begins with an instruction byte that includes the register address of the highest data byte. Subsequent data bytes should be transferred in order from high address to low address. In MSB-first mode, for each data byte transferred in a multi-byte communication cycle, the serial port internal byte address generator decrements by 1.

当 LSB／MSB 优先＝1（LSB 优先）时，指令和数据位必须按照从 LSB 到 MSB 的顺序写入。采用 LSB 优先格式的多字节数据传输以一个指令字节开始，该指令字节包括最低数据字节的寄存器地址，其后是多个数据字节。多字节通信周期每传输一个字节，串行端口内部字节地址发生器便递增 1。

When LSB/MSB first = 1 (LSB first), instruction and data bits must be written in order from LSB to MSB. A multi-byte data transfer in LSB-first format begins with an instruction byte that includes the register address of the lowest data byte, followed by multiple data bytes. For each byte transferred in a multi-byte communication cycle, the serial port internal byte address generator increments by 1.

如果 MSB 优先格式有效，对于多字节 I／O 操作，串行端口控制器数据地址将从写入 0x00 的数据地址开始递减。如果 LSB 优先格式有效，对于多字节 I／O 操作，串行端口控制器地址将从写入 0x1F 的数据地址开始递增。

If the MSB-first format is in effect, for a multi-byte I/O operation, the serial port controller data address decrements starting from the data address written to 0x00. If the LSB-first format is in effect, for a multi-byte I/O operation, the serial port controller address increments starting from the data address written to 0x1F.

9、插值滤波器结构 / Interpolation Filter Architecture

SXD005 可以提供最大高达 8×插值，也可以完全禁用插值滤波器。必须注意，为了避免插值滤波器溢出，输入信号应比满量程回退 0.01dB。

The SXD005 provides interpolation of up to 8×, and the interpolation filter can also be fully disabled. Note that, to avoid interpolation filter overflow, the input signal should be backed off 0.01 dB from full scale.

10、反 Sinc 滤波器 / Inverse-Sinc Filter

反 sinc 滤波器由一个 9 抽头 FIR 滤波器实现。它可以对最高达 0.4×fDATA 的频率提供 ±0.05dB 以下通带纹波。为了在通带的上端提供必要的增益，反 sinc 滤波器具有 3.4dB 的本征插入损耗。

The inverse-sinc filter is implemented as a 9-tap FIR filter. It provides passband ripple of less than ±0.05 dB for frequencies up to 0.4×fDATA. To provide the necessary gain at the upper end of the passband, the inverse-sinc filter has an intrinsic insertion loss of 3.4 dB.

11、DAC 采样时钟源 / DAC Sample Clock Source

SXD005 可以通过两种模式提供 DAC 的采样时钟（DACCLK）。第一种模式采用片内时钟倍频器，它可以接受一个以较低输入频率（通常是数据输入频率）工作的参考时钟。然后片内 PLL 将该参考时钟倍乘至较高频率，以用来产生 DAC 所需的全部内部时钟。该时钟倍频器提供的高质量时钟，可以满足所需的全部内部时钟。第二种模式是旁路时钟倍频器电路，让 DACCLK 直接通过 REFCLK 引脚提供。对于在较高输出频率时 DAC 输出噪声尽可能低的苛刻应用，通过 REFCLK 引脚直接提供 DACCLK 可能是必需的。两种模式均要求 REFCLK 信号的抖动很低，以尽可能提高 DAC 噪声性能。

The SXD005 can provide the DAC sample clock (DACCLK) in two modes. In the first mode, an on-chip clock multiplier accepts a reference clock operating at a lower input frequency (usually the data input frequency); the on-chip PLL then multiplies the reference clock to a higher frequency to generate all internal clocks required by the DAC. The high-quality clock provided by this clock multiplier can satisfy all required internal clocks. In the second mode, the clock multiplier circuit is bypassed and DACCLK is

provided directly through the REFCLK pin. For demanding applications requiring the lowest possible DAC output noise at higher output frequencies, providing DACCLK directly through the REFCLK pin may be necessary. Both modes require the REFCLK signal to have low jitter to maximize DAC noise performance.

11.1 时钟设置 / Clock Setup

（1）直接输入时钟：PLL 禁用时（0x09<7>=0），REFCLK 输入用作 DAC 采样时钟；(1) Direct input clock: when the PLL is disabled (0x09<7> = 0), the REFCLK input is used as the DAC sample clock;

（2）时钟倍频：PLL 使能时（0x09<7>=1），时钟倍频电路从较低频率的 REFCLK 输入产生 DAC 采样时钟。(2) Clock multiplication: when the PLL is enabled (0x09<7> = 1), the clock multiplier circuit generates the DAC sample clock from the lower-frequency REFCLK input.

寄存器 / Registers

1、寄存器初始化 / Register Initialization

上电后，内部寄存器必须初始化为默认值。可以通过以下方式来初始化：

After power-up, the internal registers must be initialized to their default values. Initialization can be performed as follows:

（1）通过软件重置。当使用串行接口时，将 RESET 位设置为高，此设置将内部寄存器初始化为默认值，然后将 RESET 位自动复位为低。在这种情况下，RESET 引脚将保持低电平。(1) Software reset. When the serial interface is used, setting the RESET bit high initializes the internal registers to their default values, after which the RESET bit automatically resets to low. In this case, the RESET pin remains low.

（2）串行接口时序特点 (2) Serial interface timing characteristics

参数 / Parameter	说明 / Description	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
tDS	数据与 SCLK 上升沿之间的建立时间 / Setup time between data and the SCLK rising edge	2.8	—	—	ns
tDH	数据与 SCLK 上升沿之间的保持时间 / Hold time between data and the SCLK rising edge	0.0	—	—	ns
tCLK	SCLK 周期 / SCLK period	40	—	—	ns
tS	CSB 与 SCLK 之间的建立时间 / Setup time between CSB and SCLK	2.8	—	—	ns
tH	CSB 与 SCLK 之间的保持时间 / Hold time between CSB and SCLK	2.0	—	—	ns
tHIGH	SCLK 应处于逻辑高电平状态的最短时间 / Minimum time SCLK should be at logic high	—	—	12.5	ns
tLOW	SCLK 应处于逻辑低电平状态的最短时间 / Minimum time SCLK should be at logic low	—	—	12.5	ns

2、寄存器地址 / Register Addresses

上电后，请先完成寄存器复位操作。请注意，所有不用的寄存器应保持器件默认值。

After power-up, complete the register reset operation first. Note that all unused registers should be kept at the device default values.

寄存器 / Register	地址 / Address	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	缺省值 / Default
通信 / Communication 0x00（十进制 00 / decimal 00）	0x00	SDIO 双向 / SDIO bidirectional	LSB/MSB 优先 / LSB/MSB first	软件复位 / Software reset	掉电模式 / Power-down mode	自动掉电使能 / Auto power-down enable	PLL 锁定指示（只读）/ PLL lock indicator (read-only)			0x00
数字控制 / Digital Control 0x01（01）	0x01	插值系数［1:0］/ Interpolation factor [1:0]		滤波器调制模式［3:0］/ Filter modulation mode [3:0]				DATACLK 延迟［4］/ DATACLK delay [4]	零值填充使能 / Zero-value fill enable	0x00
0x02（02）	0x02	数据格式 / Data format	单端口 / Single port	实数模式 / Real mode	DATACLK 延迟使能 / DATACLK delay enable	反 sinc 使能 / Inverse-sinc enable	DATACLK 反相 / DATACLK invert	TxEnable 反相 / TxEnable invert	Q 优先 / Q first	0x00
同步控制 / Synchronization Control 0x03（03）	0x03	DATACLK 延迟模式 / DATACLK delay mode	保留（置 1）/ Reserved (set to 1)	DATACLK 分频［1:0］/ DATACLK divide [1:0]		数据时序余量［3:0］/ Data timing margin [3:0]				0x00
0x04（04）	0x04	DATACLK 延迟［3:0］/ DATACLK delay [3:0]				SYNC_O 分频［2:0］/ SYNC_O divide [2:0]			SYNC_O 延迟［4］/ SYNC_O delay [4]	0x00
0x05（05）	0x05	SYNC_O 延迟［3:0］/ SYNC_O delay [3:0]				SYNC_I 比值［2:0］/ SYNC_I ratio [2:0]			SYNC_I 延迟［4］/ SYNC_I delay [4]	0x00
0x06（90）	0x06	SYNC_I 延迟［3:0］/ SYNC_I delay [3:0]				SYNC_I 时序余量［3:0］/ SYNC_I timing margin [3:0]				0x00
0x07（07）	0x07		SYNC_O 使能 /	SYNC_O 触发沿 /	时钟状态［4:0］/					0x00

寄存器 / Register	地址 / Address	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	缺省值 / Default
		SYNC_I 使能 / SYNC_I enable	SYNC_O enable	SYNC_O trigger edge	Clock status [4:0]					
PLL 控制 / PLL Control 0x08（08）	0x08	PLL 频段选择［5:0］/ PLL band select [5:0]						PLL VCO 驱动［1:0］/ PLL VCO drive [1:0]		0xE7
0x09（60）	0x09	PLL 使能 / PLL enable	PLL VCO 分频比［1:0］/ PLL VCO divide ratio [1:0]		PLL 环路分频比［1:0］/ PLL loop divide ratio [1:0]		PLL 偏置［2:0］/ PLL bias [2:0]			0x52
其它控制 / Other Control 0x0A（10）	0x0A	VCO 控制电压［2:0］（只读）/ VCO control voltage [2:0] (read-only)			PLL 环路带宽［4:0］/ PLL loop bandwidth [4:0]					0x1F
IDAC 控制 / IDAC Control 0x10（11）	0x10	IDAC 增益调整［7:0］/ IDAC gain adjustment [7:0]								0xF9
0x10（12）	0x10	IDAC 休眠 / IDAC sleep	IDAC 掉电 / IDAC power-down	IDAC 增益调整［9:8］/ IDAC gain adjustment [9:8]						0x01
DAC1 辅助控制 / DAC1 Auxiliary Control 0x0D（13）	0x0D	辅助 DAC1 数据［7:0］/ Auxiliary DAC1 data [7:0]								0x00
0x10（14）	0x10	辅助 DAC1 符号 / Auxiliary DAC1 sign	辅助 DAC1 电流方向 / Auxiliary DAC1 current direction	辅助 DAC1 掉电 / Auxiliary DAC1 power-down	辅助 DAC1 数据［9:8］/ Auxiliary DAC1 data [9:8]					0x00
QDAC 控制 / QDAC Control 0x0F（15）	0x0F	QDAC 增益调整［7:0］/ QDAC gain adjustment [7:0]								0xF9

寄存器 / Register	地址 / Address	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	缺省值 / Default
0x10（16）	0x10	QDAC 休眠 / Q DAC sleep	QDAC 掉电 / QDAC power-down	QDAC 增益调整［9:8］/ QDAC gain adjustment [9:8]						0x01
控制辅助 DAC2 / Auxiliary DAC2 Control 0x11（17）	0x11	辅助 DAC2 数据［7:0］/ Auxiliary DAC2 data [7:0]								0x00
0x12（18）	0x12	辅助 DAC2 符号 / Auxiliary DAC2 sign	辅助 DAC2 电流方向 / Auxiliary DAC2 current direction	辅助 DAC2 掉电 / Auxiliary DAC2 power-down	辅助 DAC2 数据［9:8］/ Auxiliary DAC2 data [9:8]					0x00
0x18（0x13 至 19 至 24）/ 0x18 (0x13 to 19 to 24)	0x18	保留 / Reserved								
中断 / Interrupt 0x19（25）	0x19	数据时序错误 IRQ / Data timing error IRQ	同步时序错误 IRQ / Sync timing error IRQ	数据时序错误类型 / Data timing error type	数据时序错误 IRQ 使能 / Data timing error IRQ enable	错误 IRQ 同步时序使能 / Error IRQ sync timing enable	回送内部同步 / Loopback internal sync			0x00
版本 / Version 0x1F（31）	0x1F	版本［7:0］/ Version [7:0]								0x07

寄存器地址表原件排版错位严重：多行寄存器名称缺失、地址十六进制/十进制两列互相串扰（如「0x06 90」「AOXO 10」「80X0 11」「00X0 12」「Ox0D 13」「30X0 14」「OxOF 15」「0x180x13to 19 至 24」等），本底稿已按上下文尽量复原行结构，地址与位定义务必对照原件寄存器表逐行核对后再发布。 The register address table in the original is severely misaligned: several register names are missing and the hexadecimal/decimal address columns are interleaved (e.g. "0x06 90", "AOXO 10", "80X0 11", "00X0 12", "Ox0D 13", "30X0 14", "OxOF 15", "0x180x13to 19 to 24"). This draft restores the row structure from context as far as possible; addresses and bit definitions must be verified row by row against the original register table before publication.

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电源地间保护 / ESD Protection Between Power Supplies

为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。

To improve the electrostatic resistance of the device, the following ESD protection circuits exist between the power supply pins inside the device. During power-up and normal use, avoid forward-conducting these ESD protection devices for extended periods.

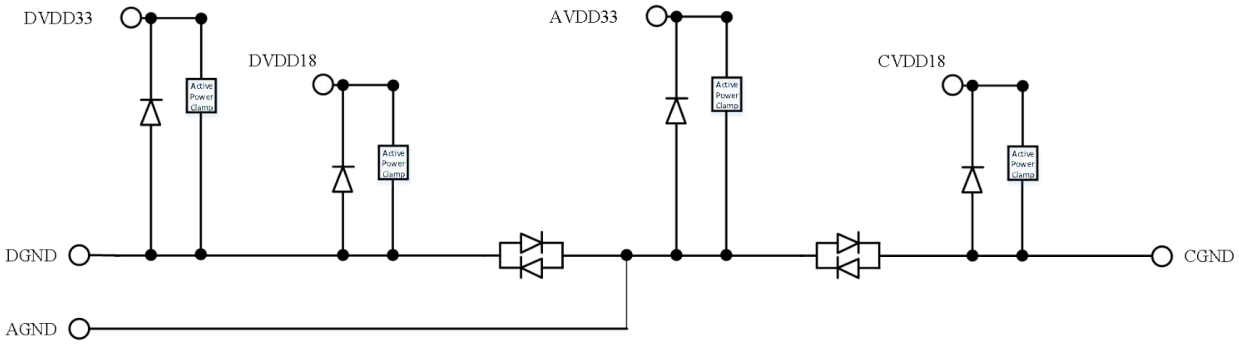


Figure 12: 内部电源间的 ESD 保护电路

注意事项 / Cautions

1、产品安装注意事项 / Mounting Cautions

1) 要求应用对象电路板有一个完整干净的地。 1) The application circuit board is required to have a complete, clean ground.

2) 要求应用对象为多层布线板且内含独立的地层。 2) The application should be a multilayer wiring board containing an independent ground layer.

3) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) Instruments and meters used for circuit debugging must have good unified grounding. In PCB design, be sure to maintain good grounding and power-supply decoupling.

4) 焊接时请注意器件方向，以免焊错。 4) Pay attention to device orientation when soldering to avoid soldering errors.

5) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。 5) Do not reverse the power supply or short input/output terminals to the power supply, as this may easily damage the circuit.

2、产品使用注意事项 / Usage Cautions

1) 要求应用对象电路板的数字地和模拟地尽量分离，不要将数字线布于模拟线旁边或于 DAC 底下。 1) Separate the digital ground and analog ground of the application circuit board as much as possible; do not route digital lines next to analog lines or underneath the DAC.

2) 输入连线应尽量短以最小化寄生电容和噪声引入。 2) Input connections should be as short as possible to minimize parasitic capacitance and noise introduction.

3) 很重要的是，芯片的地应该通过尽量多的渠道和足够多的面积与 PCB 板的地层相连。 3) Importantly, the chip ground should be connected to the PCB ground layer through as many paths and as much area as possible.

4) 推荐上电后首先对电路进行复位，再进行使用。 4) It is recommended to reset the circuit first after power-up before use.

5) 电路最大工作频率为 1000M。 5) The maximum operating frequency of the circuit is 1000M.

6) 热沉为模拟地，未使用引脚建议悬空。 6) The heat sink is analog ground; unused pins are recommended to be left floating.

3、产品防护注意事项 / Protection Cautions

1) 成品库贮存的温湿度和环境要求：温度 10°C～25°C，相对湿度 25%～70%、静电放电敏感度 1B 等级（500~999V）。该电路所有引出端均有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 1) Temperature, humidity, and environment requirements for finished-product storage: temperature 10°C to 25°C, relative humidity 25% to 70%, ESD sensitivity Class 1B (500 V to 999 V). All pins of this circuit have ESD protection structures; however, large-energy electric pulses may still damage the circuit, so ESD protection must be observed during testing, handling, and storage.

2) 产品贮存期：从检验批识别代码日期算起，入库产品贮存期超过 36 个月时产品应归入超期产品专柜存放，产品须复检合格后方能使用。 2) Product storage life: counted from the inspection-lot identification code date; when the storage period of warehoused products exceeds 36 months, the products shall be stored in the overdue-product cabinet and may only be used after passing re-inspection.

3) 建议拆封后 4 小时内使用，如在空气中暴露超过 4 小时，建议进行 150°C，8h 的高温烘焙后抽真空包装，放置于干燥柜中存放。 3) Use within 4 hours after opening is recommended; if exposed to air for more than 4 hours, high-temperature baking at 150°C for 8 h followed by vacuum packaging and storage in a dry cabinet is recommended.

4) 在使用过程中应避免跌落以免造成机械应力损伤。 4) Avoid dropping during use to prevent mechanical stress damage.

5) 超出绝对最大额定值可能会导致器件永久性损坏。额定最大值不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。长期在绝对最大额定值条件下工作会影响器件的可靠性。 5) Exceeding the absolute maximum ratings may cause permanent damage to the device. The maximum ratings do not imply that the device can operate normally under those conditions or under any other conditions beyond those shown in this manual. Long-term operation at the absolute maximum ratings will affect device reliability.

6) 塑封电路易吸潮导致分层，使用时应注意保持周围环境干燥，存储时应真空包装储存于常温、干燥环境下。 6) Plastic-packaged circuits easily absorb moisture, causing delamination; keep the surrounding environment dry during use, and store vacuum-packed at room temperature in a dry environment.

4、电装说明 / Assembly Instructions

1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； 1) The moisture sensitivity level of this product is MSL3. The allowable exposure time to the external environment from removal from the moisture-barrier bag, dry storage, or baking until reflow soldering is: ≤30°C/60% RH, 168 h;

2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； 2) If device storage conditions cannot be controlled or traced, strictly bake at 125°C for 8 h before assembly;

3) 若电装环境温湿度无法保证 ≤30°C/60RH%，请在烘烤后 12h 内完成焊接； 3) If the assembly environment temperature and humidity cannot be guaranteed at ≤30°C/60% RH, complete soldering within 12 h after baking;

4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； 4) After baking, the product generates static electricity very easily; observe ESD protection during all operations;

5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 5) For board-level assembly with leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C to 235°C and the maximum peak temperature should not exceed 235°C; dwell time within ±5°C of the peak temperature is ≤20 s; time above the liquidus is 60 s to 90 s; ramp-up rate 2°C/s to 4°C/s; ramp-down rate 2°C/s to 6°C/s;

6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度 ±5°C以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C； 6) For board-level assembly with lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C to 245°C and the maximum peak temperature should not exceed 260°C; dwell time within ±5°C of the peak temperature is ≤20 s; time above the liquidus is 60 s to 90 s; ramp-up rate 2°C/s to 4°C/s; ramp-down rate 2°C/s to 6°C/s;

7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）； 7) If a mixed assembly process requires a higher temperature, ensure the device body temperature does not exceed 260°C (the device body temperature measurement point is the top surface of the device during reflow);

8) 本产品焊接端表面处理方式为电镀纯锡。 8) The solder-terminal surface finish of this product is electroplated pure tin.

5、热阻 / Thermal Resistance

表 6 封装热阻 / Table 6 Package Thermal Resistance

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)	36.68 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2 integrated circuit natural-convection thermal test environment requirements and method

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard and Method
Rthjt（结到器件顶面的热阻）/ Rthjt (junction-to-device-top thermal resistance)	4.015 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14 transient dual interface test method for one-dimensional heat path
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-device-bottom thermal resistance)	2.095 K/W	JESD51-14 拐点理论器件内部结构分层得到 / JESD51-14, derived from device internal structure delamination by the inflection-point theory

常见故障及处理办法 / Troubleshooting

1、无输出信号：检查时钟引出端是否有时钟输入，检查电源、地信号连接是否正常，保证输入电压、基准电压准确。 1. No output signal: check whether there is clock input at the clock pins, check that power and ground signal connections are normal, and ensure the input voltage and reference voltage are accurate.

2、输出数据抖动：检查外部电路和连接，保证基准电压稳定。 2. Output data jitter: check the external circuit and connections, and ensure the reference voltage is stable.

3、器件工作不稳定：检查电源，保证电源电压稳定。 3. Unstable device operation: check the power supply and ensure the supply voltage is stable.

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附加说明 / Additional Notes

1. 本说明书首次发布日期：2026 年 6 月。
2. This manual was first issued in June 2026.
3. 本产品状态：☑生产（该产品型号目前已在生产，可以提供正式产品）☐预发布（该产品型号尚未投入正式生产，可以提供样品）
4. Product status: ☑ In production (this product model is currently in production; formal products are available) ☐ Pre-release (this product model has not yet entered formal production; samples are available)
5. 替代进口器件情况说明：
6. Notes on replacement of the imported device:

1）绝对最大额定值对比 / Absolute Maximum Ratings Comparison

附表 1 绝对最大额定值对比 / Additional Table 1 Absolute Maximum Ratings Comparison

参数 / Parameter	SXD005 规范要求 / SXD005 Specification	进口器件手册 / Imported Device Datasheet	比对结果 / Comparison
模拟电源电压（VDDA）/ Analog supply voltage (VDDA)	-0.3V-3.6V	-0.3V~3.6V	一致 / Match
1.8V 数字电源电压（VDDD<1.8>）/ 1.8 V digital supply voltage (VDDD<1.8>)	-0.3V-1.98V	-0.3V~2.1V	基本一致 / Essentially match
3.3V 数字电源电压（VDDD<3.3>）/ 3.3 V digital supply voltage (VDDD<3.3>)	-0.3V-3.6V	-0.3V~3.6V	一致 / Match
时钟电源电压（VDDC）/ Clock supply voltage (VDDC)	-0.3V-1.98V	-0.3V~2.1V	基本一致 / Essentially match
贮存温度（Tstg）/ Storage temperature (Tstg)	-65°C~150°C	-65°C~150°C	一致 / Match
结温（TJ）/ Junction temperature (TJ)	130°C	125°C	基本一致 / Essentially match

2）推荐工作条件对比 / Recommended Operating Conditions Comparison

附表 2 推荐工作条件对比 / Additional Table 2 Recommended Operating Conditions Comparison

参数 / Parameter	SXD005 规范要求 / SXD005 Specification	进口器件手册 / Imported Device Datasheet	比对结果 / Comparison
模拟电源电压（VDDA）/ Analog supply voltage (VDDA)	3.1V~3.5V	3.13V～3.47V	基本一致 / Essentially match
1.8V 数字电源电压（VDDD<1.8>）/ 1.8 V digital supply voltage (VDDD<1.8>)	1.7V~1.9V	1.7V～2.05V	基本一致 / Essentially match
3.3V 数字电源电压（VDDD<3.3>）/ 3.3 V digital supply voltage (VDDD<3.3>)	3.1V~3.5V	3.13V～3.47V	基本一致 / Essentially match
时钟电源电压（VDDC）/ Clock supply voltage (VDDC)	1.7V~1.9V	1.7V～2.05V	基本一致 / Essentially match
工作温度（TA）/ Operating temperature (TA)	-40°C~85°C	-40°C~85°C	一致 / Match

3）电特性对比 / Electrical Characteristics Comparison

附表 3 电特性对比 / Additional Table 3 Electrical Characteristics Comparison

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
分辨率 / Resolution	RES	—	16	16	一致 / Match	bits

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
微分非线性 / Differential nonlinearity	EDL	—	-6 / ±3 / 6	— / ±2.1 / —	相较于国外放宽 / Relaxed vs. foreign product	LSB
积分非线性 / Integral nonlinearity	EL	—	-10 / ±8 / 10	— / ±6 / —	—	LSB
失调误差 / Offset error	EO	—	-1 / ±0.01 / +1	-0.001 / — / 0.001	—	%FSR
增益误差 / Gain error	EG	—	-8 / ±3.5 / +8	— / ±2 / —	—	%FSR
满量程输出电流 / Full-scale output current	IO	—	7.5 / 19.47 / 32.5	8.66 / — / 31.66	—	mA
DAC 输出顺从电压范围 / DAC output compliance voltage range	VOC	—	-1.0 / ±1 / 1.0	-1.0 / — / 1.0	—	V
主 DAC 输出电阻 / Main DAC output resistance	RO	—	—	— / 10 / —	未纳入规范 / Not in specification	MΩ
主 DAC 输出单调性 / Main DAC output monotonicity	MONO	—	设计保证 / Guaranteed by design	设计保证 / Guaranteed by design	未纳入规范 / Not in specification	—
DAC 失调误差温度系数 / DAC offset error temperature coefficient	αEO	—	-300 / ±300 / 300	— / 0.04 / —	国外为典型值 / Foreign value is typical	ppm FSR/°C
DAC 增益误差温度系数 / DAC gain error temperature coefficient	αEG	—	-800 / ±800 / 800	— / 100 / —	—	ppm FSR/°C
基准电压温度系数 / Reference voltage temperature coefficient	αVREF	—	-250 / ±250 / 250	— / 30 / —	—	ppm/°C
辅助 DAC 精度 / Auxiliary DAC resolution	RESAUX	—	— / 10 / —	—	—	bits
辅助 DAC 满量程输出电流 / Auxiliary DAC full-scale output current	IAUX	—	-2.5 / ±2 / 2.5	-1.998 / — / 1.998	相较于国外放宽 / Relaxed vs. foreign product	mA

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
辅助 DAC 输出电压范围（源）/ Auxiliary DAC output voltage range (source)	VCOAUXSO	—	0 / — / 1.6	0 / — / 1.6	一致 / Match	V
辅助 DAC 输出电压范围（吸）/ Auxiliary DAC output voltage range (sink)	VCOAUXSI	—	0.8 / — / 1.6	0.8 / — / 1.6	一致 / Match	V
辅助 DAC 输出电阻 / Auxiliary DAC output resistance	RO_AUX	—	—	— / 1 / —	未纳入规范 / Not in specification	MΩ
辅助 DAC 输出单调性 / Auxiliary DAC output monotonicity	MONOAUX	—	设计保证 / Guaranteed by design	设计保证 / Guaranteed by design	一致 / Match	—
内部基准电压 / Internal reference voltage	VREF	—	1.0 / 1.2 / 1.5	— / 1.2 / —	国外为典型值 / Foreign value is typical	V
内部基准输出电阻 / Internal reference output resistance	ROREF	—	3.5 / 4.2 / 7.5	— / 5 / —	—	kΩ
3.3V 模拟电源电压 / 3.3 V analog supply voltage	VDDA	—	3.13 / — / 3.47	3.13 / — / 3.47	一致 / Match	V
1.8V 模拟电源电压 / 1.8 V analog supply voltage	VDDC	—	1.7 / — / 2.05	1.7 / — / 2.05	—	V
3.3V 数字电源电压 / 3.3 V digital supply voltage	VDDD<3.3>	—	3.13 / — / 3.47	3.13 / — / 3.47	—	V
1.8V 数字电源电压 / 1.8 V digital supply voltage	VDDD<1.8>	—	1.7 / — / 2.05	1.7 / — / 2.05	—	V
1X、PLL 关功耗 / 1X power, PLL off	PW	—	— / 279 / —	— / ⩽300 / —	—	mW
2X、PLL 关功耗 / 2X power, PLL off	PW	fDAC=320MSPS，IF=16MHz	— / 517 / 650	— / 498 / —	—	mW
2X、PLL 开功耗 / 2X power, PLL on	PW	—	— / 611 / —	— / 588 / —	—	mW
4X、QDAC 关功耗 / 4X power, QDAC off	PW	—	— / 565.5 / —	— / 572 / —	—	mW

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
8X 功耗 / 8X power	PW	fDAC/4 调制，fDAC=1GSPS，IF=262.5MHz / fDAC/4 modulation, fDAC = 1GSPS, IF = 262.5 MHz	— / 1087 / 1500	— / 980 / —	—	mW
掉电功耗 / Power-down power	PW	掉电模式 / Power-down mode	— / 1.93 / 20	— / — / 9.8	—	mW
VDDA 电源电压抑制比 / VDDA power supply rejection ratio	PSRR	TA=25°C	-2 / 0.3 / 2	-0.3 / — / 0.3	—	%FSR/V
CMOS 输入逻辑高电平 / CMOS input logic high level	VIH	—	2.5 / — / —	2.0 / — / —	—	V
CMOS 输入逻辑低电平 / CMOS input logic low level	VIL	—	— / — / 0.4	— / — / 0.8	—	V
1×模式插值时最大输入数据速率 / Max input data rate, 1× interpolation	fDAC	—	—	300 / — / —	未纳入规范 / Not in specification	MSPS
2×模式插值时最大输入数据速率 / Max input data rate, 2× interpolation	fDAC	—	—	250 / — / —	—	MSPS
4×模式插值时最大输入数据速率 / Max input data rate, 4× interpolation	fDAC	—	—	200 / — / —	—	MSPS
8×模式插值时最大输入数据速率 / Max input data rate, 8× interpolation	fDAC	—	100 / — / —	112.5 / — / —	相较于国外放宽 / Relaxed vs. foreign product	MSPS
CMOS 输出逻辑高电平 / CMOS output logic high level	VOH	DATACLK	2 / 3.27 / —	2.4 / — / —	—	V
CMOS 输出逻辑低电平 / CMOS output logic low level	VOL	DATACLK	— / 0.037 / 0.8	— / — / 0.4	—	V
DATACLK 输出占空比 / DATACLK output duty cycle	ODC	DATACLK	35 / 50 / 65	40 / — / 60	—	%
	VR_LVSD	—	—	825 / — / 1575		mV

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
LVDS 输入电压范围 / LVDS input voltage range					未纳入规范 / Not in specification	
LVDS 输入差分阈值电压 / LVDS input differential threshold voltage	VIDTH	—	—	-100 / — / 100	—	mV
LVDS 输入差分迟滞电压 / LVDS input differential hysteresis voltage	VIDTHH_L	—	—	— / 20 / —	—	mV
差分输入阻抗 / Differential input impedance	RIN	—	—	80 / — / 120	—	Ω
LVDS 输入数据率 / LVDS input data rate	fDAC_LVSD	—	—	— / — / 250	—	MSPS
SYNC_I 相对 REFCLK 建立时间 / SYNC_I setup time relative to REFCLK	tS_RS	—	—	0.4 / — / —	—	ns
SYNC_I 相对 REFCLK 保持时间 / SYNC_I hold time relative to REFCLK	tS_RH	—	—	0.55 / — / —	—	ns
LVDS 输出逻辑高电压 / LVDS output logic high voltage	VOH_LVSD	—	— / 1268 / —	— / — / 1375	未纳入规范 / Not in specification	mV
LVDS 输出逻辑低电平 / LVDS output logic low level	VOL_LVSD	—	— / 1097 / —	1025 / — / —	—	mV
LVDS 输出差分电压 / LVDS output differential voltage	VOD_LVSD	—	— / 155 / —	150 / — / 250	—	mV
LVDS 输出失调电压 / LVDS output offset voltage	VO_LVSD	—	— / 1170 / —	1150 / — / 1250	—	mV
LVDS 输出阻抗 / LVDS output impedance	RO_LVSD	—	—	80 / — / 120	—	Ω
DAC 时钟输入共模电压 / DAC clock input	VCLKR	—	350 / — / 450	400 / — / 2000	相较于国外规范收窄 / Narrower than	mV

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
common-mode voltage					foreign specification	
DAC 时钟输入差分峰峰值电压 / DAC clock input differential peak-to-peak voltage	VCLKS	—	600 / — / 1800	300 / — / 500	相较于国外规范放宽 / Relaxed vs. foreign specification	mV
工作频率 / Operating frequency	fCLK_PLL_OFF	PLL 关 / PLL off	1000 / — / —	900 / — / —	相较于国外规范更高 / Higher than foreign specification	MHz
最大时钟速率 / Maximum clock rate	fCLK_PLL_ON	PLL 开 / PLL on	200 / — / —	250 / — / —	相较于国外规范更低 / Lower than foreign specification	MHz
输入数据相对 DATACLK 建立时间 / Input data setup time relative to DATACLK	tDSD	—	—	3.0 / — / —	未纳入规范 / Not in specification	ns
输入数据相对 DATACLK 保持时间 / Input data hold time relative to DATACLK	tDHD	—	—	-0.05 / — / —	—	ns
输入数据相对 REFCLK 建立时间 / Input data setup time relative to REFCLK	tDSR	—	—	-0.80 / — / —	—	ns
输入数据相对 REFCLK 保持时间 / Input data hold time relative to REFCLK	tDHR	—	—	3.8 / — / —	—	ns
1×模式延迟 / Latency, 1× mode	—	—	—	— / 25 / —	未纳入规范 / Not in specification	DACCLK 周期 / DACCLK cycles
2×模式延迟 / Latency, 2× mode	—	—	—	— / 70 / —	—	DACCLK 周期 / DACCLK cycles
	—	—	—	— / 146 / —	—	DACCLK 周期 /

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
4×模式延迟 / Latency, 4× mode						DACCLK cycles
8×模式延迟 / Latency, 8× mode	—	—	—	— / 297 / —	—	DACCLK 周期 / DACCLK cycles
反 SINC 模式延迟 / Latency, inverse-SINC mode	—	—	—	— / 18 / —	—	DACCLK 周期 / DACCLK cycles
三线式接口最大时钟速率 / Three-wire interface maximum clock rate	SCLK	—	6 / 40 / —	40 / — / —	相较于国外手册放宽 / Relaxed vs. foreign datasheet	MHz
时钟高脉冲最小宽度 / Minimum clock high pulse width	tPWH	—	— / 12.5 / —	12.5 / — / —	未纳入规范 / Not in specification	ns
时钟低脉冲最小宽度 / Minimum clock low pulse width	tPWL	—	— / 12.5 / —	12.5 / — / —	—	ns
SDIO 建立时间 / SDIO setup time	tDS	—	— / 2.8 / —	2.8 / — / —	—	ns
SDIO 保持时间 / SDIO hold time	tDH	—	— / 0.0 / —	0.0 / — / —	—	ns
CSB 建立时间 / CSB setup time	tDS	—	— / 2.8 / —	2.8 / — / —	—	ns
SDO 数据有效时间 / SDO data valid time	tDV	—	— / 2.0 / —	2.0 / — / —	—	ns
上电时间 / Power-up time	tPU	—	—	— / 260 / —	—	mS
复位信号最小脉冲宽度 / Minimum reset signal pulse width	tWMIN	—	—	— / — / 2	—	DACCLK 周期 / DACCLK cycles
无杂散动态范围 / Spurious-free dynamic range	SFDR	fDAC=100MSPS，fout=20MHz	65 / 73 / —	— / 82 / —	相较于国外手册放宽 / Relaxed vs. foreign datasheet	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	fDAC=200MSPS，fout=50MHz	— / 70 / —	— / 82 / —	未纳入规范 / Not in specification	dBc
	SFDR		—	— / 80 / —	—	dBc

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
无杂散动态范围 / Spurious-free dynamic range		fDAC=400MSPS，fout=70MHz				
无杂散动态范围 / Spurious-free dynamic range	SFDR	fDAC=800MSPS，fout=70MHz	60 / — / —	— / 87 / —	相较于国外手册放宽 / Relaxed vs. foreign datasheet	dBc
双音互调失调 / Two-tone intermodulation distortion	IMD	fDAC=200MSPS，fout=50MHz	65 / — / —	— / 91 / —	相较于国外手册放宽 / Relaxed vs. foreign datasheet	dBc
双音互调失调 / Two-tone intermodulation distortion	IMD	fDAC=200MSPS，fout=50MHz	—	— / 85 / —	未纳入规范 / Not in specification	dBc
双音互调失调 / Two-tone intermodulation distortion	IMD	fDAC=400MSPS，fout=80MHz	—	— / 81 / —	未纳入规范 / Not in specification	dBc
双音互调失调 / Two-tone intermodulation distortion	IMD	fDAC=800MSPS，fout=100MHz	55 / — / —	— / 81 / —	相较于国外手册放宽 / Relaxed vs. foreign datasheet	dBc
噪声谱密度 / Noise spectral density	NSD	fDAC=200MSPS，fout=80MHz	—	— / -158 / —	未纳入规范 / Not in specification	dBm/Hz
噪声谱密度 / Noise spectral density	NSD	fDAC=400MSPS，fout=80MHz	—	— / -160 / —	—	dBm/Hz
噪声谱密度 / Noise spectral density	NSD	fDAC=800MSPS，fout=80MHz	—	— / -161 / —	—	dBm/Hz
第一临信道泄露 / First adjacent channel leakage ratio	ACLR	fDAC=491.52MSPS，fout=100MHz	—	— / 79 / —	未纳入规范 / Not in specification	dBc
第一临信道泄露 / First adjacent channel leakage ratio	ACLR	fDAC=491.52MSPS，fout=200MHz	—	— / 74 / —	—	dBc
第二临信道泄露 / Second adjacent channel leakage ratio	ACLR	fDAC=491.52MSPS，fout=100MHz	—	— / 81 / —	—	dBc
第二临信道泄露 / Second adjacent	ACLR		—	— / 78 / —	—	dBc

参数 / Parameter	符号 / Symbol	条件 / Condition	SXD005 参考值（最小/典型/最大）/ SXD005 Reference (Min/Typ/Max)	进口器件手册参考值（最小/典型/最大）/ Imported Device Reference (Min/Typ/Max)	说明 / Note	单位 / Unit
channel leakage ratio		fDAC=491.52MSPS，fout=200MHz				

附表 3 原件跨页排版破碎：多行最小/典型/最大三列数值在提取文本中串位（如各插值模式最大输入数据速率、LVDS 输出逻辑低电平等行），本底稿按提取顺序归列，发布前须对照原件逐行核对；表中两行「双音互调失调（fDAC=200MSPS，fout=50MHz）」条件相同、数值不同，按原件两行保留。 Additional Table 3 is fragmented across pages in the original: in several rows the min/typ/max values are interleaved in the extracted text (e.g. the maximum input data rate rows for the interpolation modes and the LVDS output logic low row). This draft assigns values in extraction order; verify row by row against the original before publication. The two "Two-tone IMD (fDAC = 200 MSPS, fout = 50 MHz)" rows have identical conditions but different values and are kept as two rows as in the original.

4）其它指标对比 / Other Specifications Comparison

附表 4 其它指标对比 / Additional Table 4 Other Specifications Comparison

参数 / Parameter	SXD005	进口器件 / Imported Device	比对结果 / Comparison
封装形式 / Package	LQFP100	SV-100-1	基本一致 / Essentially match
质量等级 / Quality grade	企标 / Enterprise standard	工业级 / Industrial grade	有差异 / Differs
尺寸 / Dimensions	16mm16mm1.5mm	16mm16mm1.2mm	基本一致 / Essentially match
替代建议 / Replacement recommendation	☐直接替代 / ☐Drop-in replacement ☐有效替代 / ☐Effective alternative ☑功能替代 / ☑Functional replacement		

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