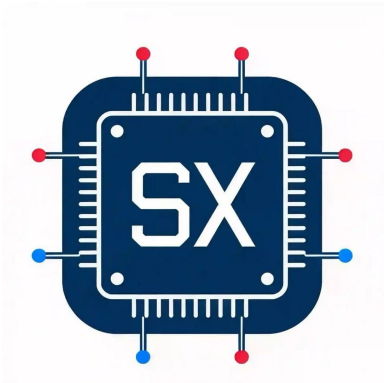


SXD014

14-Bit, 2.5 GSPS D/A Converter

14 位 2.5GSPS D/A 转换器

14-bit | 1 channel | 2.5 GSPS | BGA160 | Parallel LVDS

14位 | 单通道 | 2.5GSPS | BGA160 | 并行LVDS

对标 / Cross Reference: AD9739 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

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SXD014 14-Bit, 2.5 GSPS D/A Converter — Product Manual (Bilingual)

SXD014 型 14 位 2.5GSPS D/A 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深信科技 **V1.20260721**

对标 / Cross Reference: AD9739 — pin-to-pin compatible alternative

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版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1	2026.07.21	/	首次发布 / Initial release	

产品用途及应用范围 / Applications and Scope

English: Broadband communication systems; automatic test instruments; base stations, handheld devices; radar, avionics equipment.

中文： 宽带通信系统；自动测试仪器；基站、手持设备；雷达、航空电子装备。

标准 / Standards

English: Detailed specification: Q/GC 0202-2026 — Detailed Specification for Semiconductor Integrated Circuit SXD014 14-Bit 2.5GSPS D/A Converter. Quality grade / quality assurance requirements: enterprise standard.

中文： 详细规范：Q/GC 0202-2026 《半导体集成电路 SXD014 型 14 位 2.5GSPS D/A 转换器详细规范》；质量等级/质量保证要求：企标。

产品特点 / Features

English: - Analog supply voltage: 1.8V/3.3V - Digital supply voltage: 1.8V/3.3V - Maximum sampling rate: 2.5GSPS - Spurious-free dynamic range: ⩾46dBc @fout=950MHz - Differential linearity error: -3~3LSB - Integral linearity error: -3~3LSB - Power consumption: ⩽1.25W - Analog output range: 8.66mA~31.66mA - Circuit interface: LVDS - ESD rating: Class 1C, HBM model: 1000V - Weight: 0.41g±0.08g - Package: BGA160

中文： - 模拟电源电压：1.8V/3.3V - 数字电源电压：1.8V/3.3V - 最高采样率：2.5GSPS - 无杂散动态范围：⩾46dBc@fout=950MHz - 微分线性误差：-3~3LSB - 积分线性误差：-3~3LSB - 功耗：⩽1.25W - 模拟输出范围：8.66mA~31.66mA - 电路接口：LVDS - ESD 等级：1C 级，HBM 模型：1000V - 重量：0.41g±0.08g - 封装形式：BGA160

产品描述 / Product Description

English: The SXD014 is a semiconductor integrated circuit manufactured in CMOS technology. The product has a segmented current-steering architecture; the circuit internally includes an LVDS receiver, timing synchronization circuit, bandgap reference source, SPI interface circuit, clock receiving circuit, and a 14-bit DAC core. This product is a high-performance high-frequency digital-to-analog converter that can provide a sampling rate of up to 2500 MSPS and can support multicarrier signal generation within the Nyquist frequency; it has an SPI interface that allows programming of numerous internal parameters and readback of status registers; it uses an LVDS interface to obtain a high sampling rate; the output current can be programmed within the range of 8.66 mA to 31.66 mA; the input clock frequency range is 0.8 GHz~2.5 GHz, and the clock driver chip ADCLK914 is recommended for driving the clock terminal.

The product package is a plastic BGA160.

The functional block diagram of this product is shown in Figure 1.

中文： SXD014 是采用 CMOS 工艺制造的半导体集成电路。该产品为分段式电流舵结构，电路内部包含 LVDS 接收器、时序同步电路、带隙基准源、SPI 接口电路、时钟接收电路和 14 位 DAC 核等电路。本产品是高性能高频

数模转换器，能提供高达 2500MSPS 的采样率，并可以支撑 Nyquist 频率内的多载波信号产生；具有 SPI 接口，能够对众多的内部参量进行编程设置，可回读状态寄存器；采用 LVDS 接口获得高采样速率；输出电流可以在 8.66mA 到 31.66mA 范围内编程设置；输入时钟的频率范围为 0.8GHz~2.5GHz，时钟端推荐使用时钟驱动芯片 ADCLK914 来进行驱动。

该产品封装采用了塑封 BGA160。

该产品功能框图如图 1 所示。

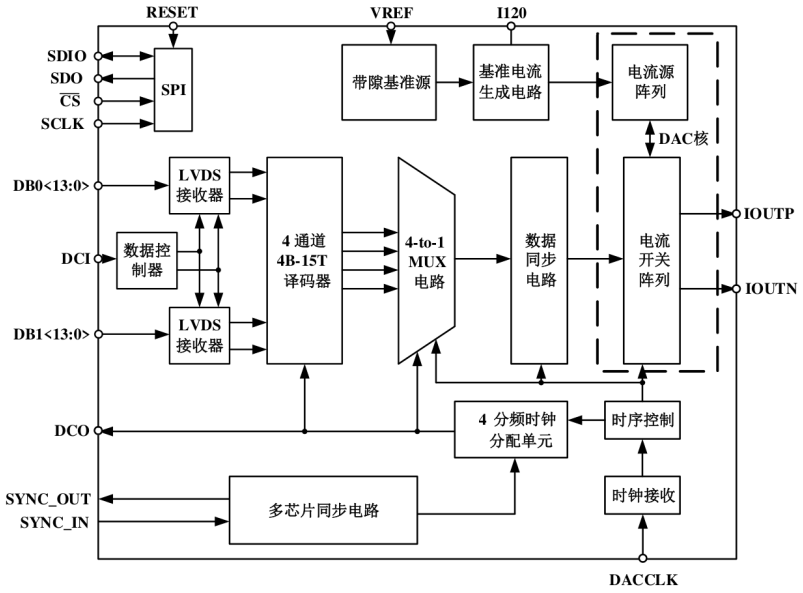


Figure 1: Functional block diagram

产品外形图 / Package Outline

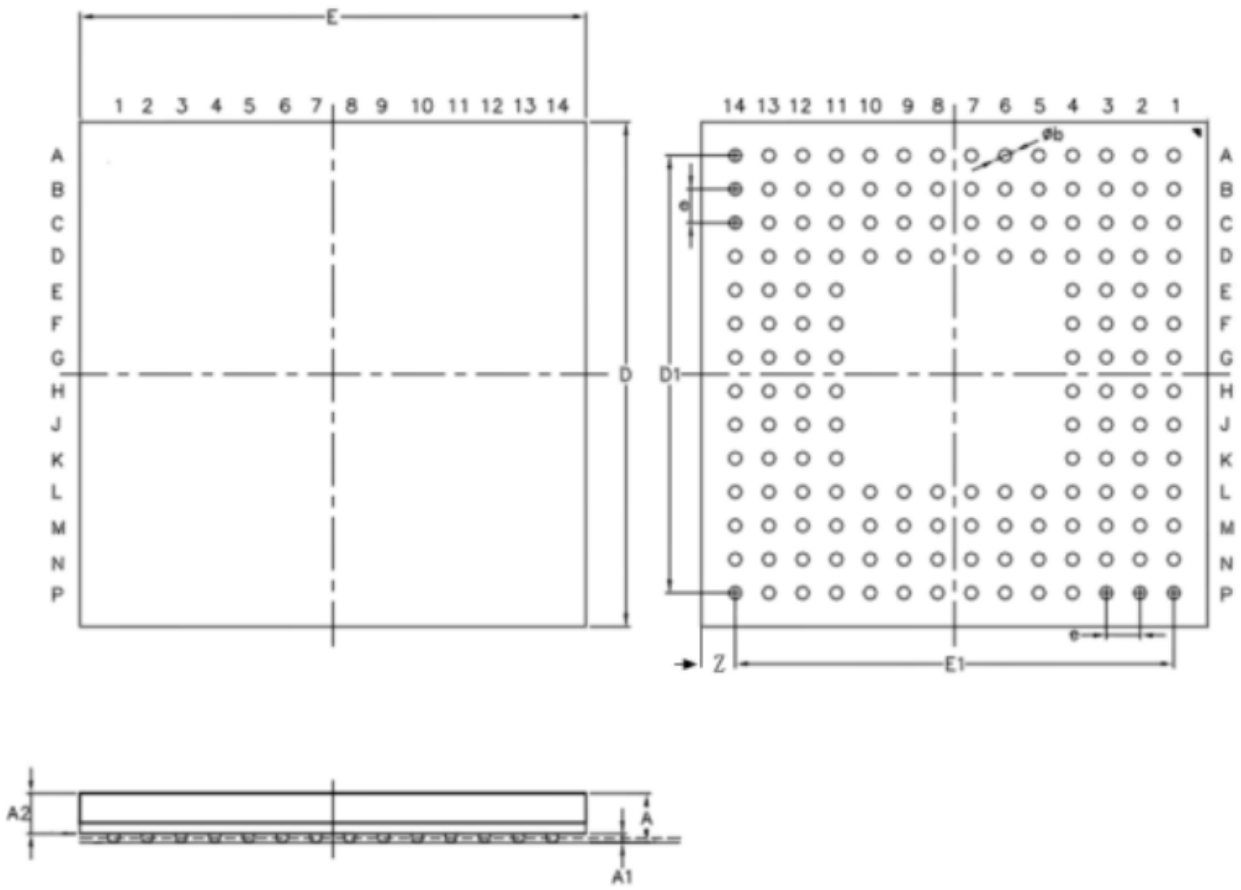


Figure 2: Package outline dimensions

单位为毫米 / Units in mm

尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max	尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max
A	--	1.41[a]	1.60	E	11.90	12.00[a]	12.10
A1	0.30	0.38[a]	0.50	D1	—	10.40[a]	—
A2	0.90	1.03[a]	1.10	E1	—	10.40[a]	—
Φb	0.45	0.50[a]	0.55	e	—	0.80[a]	—
D	11.90	12.00[a]	12.10	Z	—	0.80[a]	0.85

[a] 设计保证，不进行考核。/ Guaranteed by design, not subject to acceptance testing.

注：推荐焊盘设计详见电装说明。/ Note: see the assembly instructions for recommended pad layout.

引出端排列（俯视图）/ Pin Arrangement (Top View)

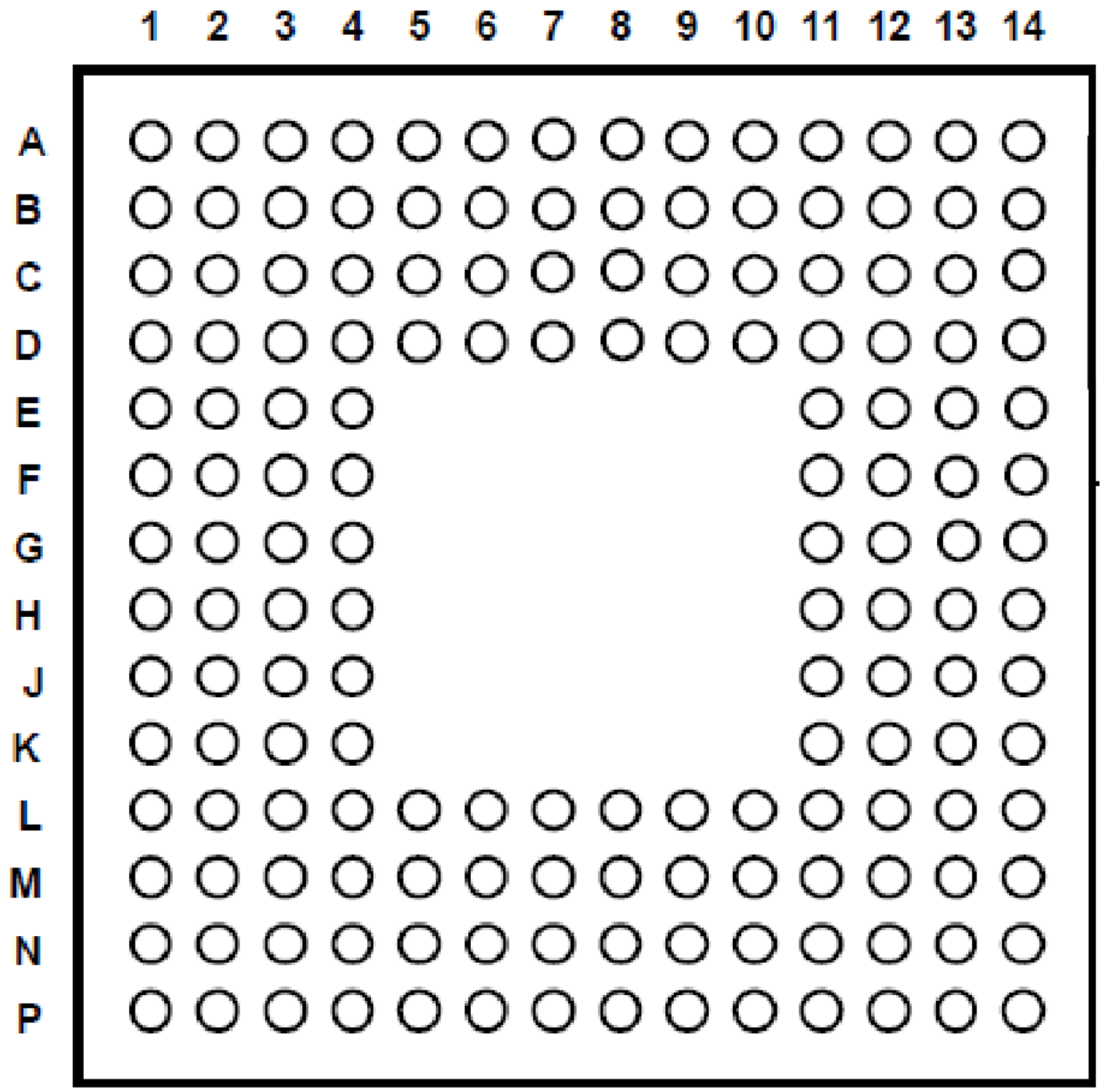


Figure 3: Pin arrangement (top view)

引出端功能符号表 / Pin Function Table

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
A1	GNDC	时钟电源地 / Clock supply ground	/	H1	GNDD	数字地 / Digital ground	/
A2	GNDC	时钟电源地 / Clock supply ground	/	H2	GNDD	数字地 / Digital ground	/
A3	GNDC		/	H3	GNDD	数字地 / Digital ground	/

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
		时钟电源地 / Clock supply ground					
A4	GNDC	时钟电源地 / Clock supply ground	/	H4	GNDD	数字地 / Digital ground	/
A5	GNDC	时钟电源地 / Clock supply ground	/	H11	GNDD	数字地 / Digital ground	/
A6	GNDAS	模拟地屏蔽 / Analog ground shield	/	H12	GNDD	数字地 / Digital ground	/
A7	IOUTN	负输出端 / Negative output	O	H13	SCLK	串口时钟端 / Serial port clock	/
A8	IOUTP	正输出端 / Positive output	O	H14	SDO	串口数据输出 / Serial data output	O
A9	GNDAS	模拟地屏蔽 / Analog ground shield	/	J1	SYNC_OUT_P	多芯片同步正端输出 / Multi-chip sync output, positive	O
A10	VDDA	模拟电源 / Analog supply	/	J2	SYNC_OUT_N	多芯片同步负端输出 / Multi-chip sync output, negative	O
A11	VDDA	模拟电源 / Analog supply	/	J3	VDD33	3.3V 数字电源 / 3.3V digital supply	/
A12	GNDA	模拟地 / Analog ground	/	J4	VDD33	3.3V 数字电源 / 3.3V digital supply	/
A13	GNDA	模拟地 / Analog ground	/	J11	VDD33	3.3V 数字电源 / 3.3V digital supply	/
A14	NC	悬空 / No connect	/	J12	VDD33	3.3V 数字电源 / 3.3V digital supply	/
B1	GNDC	时钟电源地 / Clock supply ground	/	J13	DCO_P	数据时钟输出正端 / Data clock output, positive	O
B2	GNDC	时钟电源地 / Clock supply ground	/	J14	DCO_N	数据时钟输出负端 / Data clock output, negative	O
B3	GNDC	时钟电源地 / Clock supply ground	/	K1	SYNC_IN_P	多芯片同步正端输入 / Multi-chip sync input, positive	I
B4	GNDC	时钟电源地 / Clock supply ground	/	K2	SYNC_IN_N	多芯片同步负端输入 / Multi-chip sync input, negative	I
B5	GNDC	时钟电源地 / Clock supply ground	/	K3	GNDD	数字地 / Digital ground	/
B6	GNDAS	模拟地屏蔽 / Analog ground shield	/	K4	GNDD	数字地 / Digital ground	/
B7	IOUTN	负输出端 / Negative output	O	K11	GNDD	数字地 / Digital ground	/
B8	IOUTP	正输出端 / Positive output	O	K12	GNDD	数字地 / Digital ground	/
B9	GNDAS	模拟地屏蔽 / Analog ground shield	/	K13	DCI_P	数据时钟输入正端 / Data clock input, positive	I
B10	VDDA	模拟电源 / Analog supply	/	K14	DCI_N	数据时钟输入负端 / Data clock input, negative	I
B11	VDDA	模拟电源 / Analog supply	/	L1	DB1[0]P	端口 1 正数据输入位 0 / Port 1 positive data input bit 0	I

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
B12	GNDA	模拟地 / Analog ground	/	L2	DB1[1]P	端口 1 正数据输入位 1 / Port 1 positive data input bit 1	I
B13	GNDA	模拟地 / Analog ground	/	L3	DB1[2]P	端口 1 正数据输入位 2 / Port 1 positive data input bit 2	I
B14	I120	基准电流 / Reference current	/	L4	DB1[3]P	端口 1 正数据输入位 3 / Port 1 positive data input bit 3	I
C1	VDDC	时钟电源 / Clock supply	/	L5	DB1[4]P	端口 1 正数据输入位 4 / Port 1 positive data input bit 4	I
C2	VDDC	时钟电源 / Clock supply	/	L6	DB1[5]P	端口 1 正数据输入位 5 / Port 1 positive data input bit 5	I
C3	CLKN	时钟负输入 / Clock input, negative	I	L7	DB1[6]P	端口 1 正数据输入位 6 / Port 1 positive data input bit 6	I
C4	GNDC	时钟电源地 / Clock supply ground	/	L8	DB1[7]P	端口 1 正数据输入位 7 / Port 1 positive data input bit 7	I
C5	GNDC	时钟电源地 / Clock supply ground	/	L9	DB1[8]P	端口 1 正数据输入位 8 / Port 1 positive data input bit 8	I
C6	GNDAS	模拟地屏蔽 / Analog ground shield	/	L10	DB1[9]P	端口 1 正数据输入位 9 / Port 1 positive data input bit 9	I
C7	IOUTN	负输出端 / Negative output	O	L11	DB1[10]P	端口 1 正数据输入位 10 / Port 1 positive data input bit 10	I
C8	IOUTP	正输出端 / Positive output	O	L12	DB1[11]P	端口 1 正数据输入位 11 / Port 1 positive data input bit 11	I
C9	GNDAS	模拟地屏蔽 / Analog ground shield	/	L13	DB1[12]P	端口 1 正数据输入位 12 / Port 1 positive data input bit 12	I
C10	VDDA	模拟电源 / Analog supply	/	L14	DB1[13]P	端口 1 正数据输入位 13 / Port 1 positive data input bit 13	I
C11	VDDA	模拟电源 / Analog supply	/	M1	DB1[0]N	端口 1 负数据输入位 0 / Port 1 negative data input bit 0	I
C12	GNDA	模拟地 / Analog ground	/	M2	DB1[1]N	端口 1 负数据输入位 1 / Port 1 negative data input bit 1	I
C13	GNDA	模拟地 / Analog ground	/	M3	DB1[2]N	端口 1 负数据输入位 2 / Port 1 negative data input bit 2	I
C14	VREF	基准电压 / Reference voltage	/	M4	DB1[3]N	端口 1 负数据输入位 3 / Port 1 negative data input bit 3	I
D1	VDDC	时钟电源 / Clock supply	/	M5	DB1[4]N	端口 1 负数据输入位 4 / Port 1 negative data input bit 4	I
D2	VDDC	时钟电源 / Clock supply	/	M6	DB1[5]N	端口 1 负数据输入位 5 / Port 1 negative data input bit 5	I
D3	CLKP	时钟正输入 / Clock input, positive	I	M7	DB1[6]N	端口 1 负数据输入位 6 / Port 1 negative data input bit 6	I
D4	GNDC	时钟电源地 / Clock supply ground	/	M8	DB1[7]N	端口 1 负数据输入位 7 / Port 1 negative data input bit 7	I
D5	GNDC		/	M9	DB1[8]N		I

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
		时钟电源地 / Clock supply ground				端口 1 负数据输入位 8 / Port 1 negative data input bit 8	
D6	GNDAS	模拟地屏蔽 / Analog ground shield	/	M10	DB1[9]N	端口 1 负数据输入位 9 / Port 1 negative data input bit 9	I
D7	IOUTN	负输出端 / Negative output	O	M11	DB1[10]N	端口 1 负数据输入位 10 / Port 1 negative data input bit 10	I
D8	IOUTP	正输出端 / Positive output	O	M12	DB1[11]N	端口 1 负数据输入位 11 / Port 1 negative data input bit 11	I
D9	GNDAS	模拟地屏蔽 / Analog ground shield	/	M13	DB1[12]N	端口 1 负数据输入位 12 / Port 1 negative data input bit 12	I
D10	VDDA	模拟电源 / Analog supply	/	M14	DB1[13]N	端口 1 负数据输入位 13 / Port 1 negative data input bit 13	I
D11	VDDA	模拟电源 / Analog supply	/	N1	DB0[0]P	端口 0 正数据输入位 0 / Port 0 positive data input bit 0	I
D12	GNDA	模拟地 / Analog ground	/	N2	DB0[1]P	端口 0 正数据输入位 1 / Port 0 positive data input bit 1	I
D13	GNDA	模拟地 / Analog ground	/	N3	DB0[2]P	端口 0 正数据输入位 2 / Port 0 positive data input bit 2	I
D14	IPTAT	测试引脚 / Test pin	/	N4	DB0[3]P	端口 0 正数据输入位 3 / Port 0 positive data input bit 3	I
E1	VDDC	时钟电源 / Clock supply	/	N5	DB0[4]P	端口 0 正数据输入位 4 / Port 0 positive data input bit 4	I
E2	VDDC	时钟电源 / Clock supply	/	N6	DB0[5]P	端口 0 正数据输入位 5 / Port 0 positive data input bit 5	I
E3	VDDC	时钟电源 / Clock supply	/	N7	DB0[6]P	端口 0 正数据输入位 6 / Port 0 positive data input bit 6	I
E4	VDDC	时钟电源 / Clock supply	/	N8	DB0[7]P	端口 0 正数据输入位 7 / Port 0 positive data input bit 7	I
E11	GNDAS	模拟地屏蔽 / Analog ground shield	/	N9	DB0[8]P	端口 0 正数据输入位 8 / Port 0 positive data input bit 8	I
E12	GNDAS	模拟地屏蔽 / Analog ground shield	/	N10	DB0[9]P	端口 0 正数据输入位 9 / Port 0 positive data input bit 9	I
E13	GNDAS	模拟地屏蔽 / Analog ground shield	/	N11	DB0[10]P	端口 0 正数据输入位 10 / Port 0 positive data input bit 10	I
E14	GNDAS	模拟地屏蔽 / Analog ground shield	/	N12	DB0[11]P	端口 0 正数据输入位 11 / Port 0 positive data input bit 11	I
F1	GNDAS	模拟地屏蔽 / Analog ground shield	/	N13	DB0[12]P	端口 1 正数据输入位 12 / Port 1 positive data input bit 12	I
F2	GNDAS	模拟地屏蔽 / Analog ground shield	/	N14	DB0[13]P	端口 0 正数据输入位 13 / Port 0 positive data input bit 13	I
F3	GNDAS	模拟地屏蔽 / Analog ground shield	/	P1	DB0[0]N	端口 0 负数据输入位 0 / Port 0 negative data input bit 0	I
F4	GNDAS		/	P2	DB0[1]N		I

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
		模拟地屏蔽 / Analog ground shield				端口 0 负数据输入位 1 / Port 0 negative data input bit 1	
F11	GNDAS	模拟地屏蔽 / Analog ground shield	/	P3	DB0[2]N	端口 0 负数据输入位 2 / Port 0 negative data input bit 2	I
F12	GNDAS	模拟地屏蔽 / Analog ground shield	/	P4	DB0[3]N	端口 0 负数据输入位 3 / Port 0 negative data input bit 3	I
F13	IRQ	中断请求 / Interrupt request	/	P5	DB0[4]N	端口 0 负数据输入位 4 / Port 0 negative data input bit 4	I
F14	RESET	复位 / Reset	/	P6	DB0[5]N	端口 0 负数据输入位 5 / Port 0 negative data input bit 5	I
G1	VDD	1.8V 数字电源 / 1.8V digital supply	/	P7	DB0[6]N	端口 0 负数据输入位 6 / Port 0 negative data input bit 6	I
G2	VDD	1.8V 数字电源 / 1.8V digital supply	/	P8	DB0[7]N	端口 0 负数据输入位 7 / Port 0 negative data input bit 7	I
G3	VDD	1.8V 数字电源 / 1.8V digital supply	/	P9	DB0[8]N	端口 0 负数据输入位 8 / Port 0 negative data input bit 8	I
G4	VDD	1.8V 数字电源 / 1.8V digital supply	/	P10	DB0[9]N	端口 0 负数据输入位 9 / Port 0 negative data input bit 9	I
G11	VDD	1.8V 数字电源 / 1.8V digital supply	/	P11	DB0[10]N	端口 0 负数据输入位 10 / Port 0 negative data input bit 10	I
G12	VDD	1.8V 数字电源 / 1.8V digital supply	/	P12	DB0[11]N	端口 0 负数据输入位 11 / Port 0 negative data input bit 11	I
G13	CS	串口使能端 / Serial port enable	/	P13	DB0[12]N	端口 0 负数据输入位 12 / Port 0 negative data input bit 12	I
G14	SDIO	串口数据输入/输出 / Serial data input/output	I/O	P14	DB0[13]N	端口 0 负数据输入位 13 / Port 0 negative data input bit 13	I

绝对最大额定值 / Absolute Maximum Ratings

English: - Analog supply voltage (VDDA): 3.6V - 1.8V digital supply voltage (VDD): 1.98V - 3.3V digital supply voltage (VDD33): 3.63V - Clock supply voltage (VDDC): 1.98V - Storage temperature (Tstg): -65°C~150°C

中文： - 模拟电源电压（VDDA）： 3.6V - 1.8V 数字电源电压（VDD）： 1.98V - 3.3V 数字电源电压（VDD33）： 3.63V - 时钟电源电压（VDDC）： 1.98V - 贮存温度（Tstg）： -65°C~150°C

推荐工作条件 / Recommended Operating Conditions

English: - Analog supply voltage (VDDA): 3.135V~3.465V - 1.8V digital supply voltage (VDD): 1.71V~1.89V - 3.3V digital supply voltage (VDD33): 3.135V~3.465V - Clock supply voltage (VDDC): 1.71V~1.89V - Operating temperature (TA): -40°C~85°C

Note: please see the description of replacement of foreign products in the appendix notes.

中文： - 模拟电源电压（VDDA）：3.135V~3.465V； - 1.8V 数字电源电压（VDD）：1.71V~1.89V； - 3.3V 数字电源电压（VDD33）：3.135V~3.465V； - 时钟电源电压（VDDC）：1.71V~1.89V； - 工作温度（TA）：-40°C~85°C

注：请查看附件说明中替代国外产品情况说明。

性能指标 / Performance Specifications

Conditions / 条件（除另有规定外 / unless otherwise specified）: VDDA=3.3V, VDD33=3.3V, VDDC=1.8V, VDD=1.8V, fCLK=2.5GHz, -40°C≤TA≤85°C.

特性 / Parameter	符号 / Symbol	条件 / Conditions	最小 / Min	典型值 / Typical	最大 / Max	单位 / Unit
基准电压 / Reference voltage	VREF	—	1.15		1.25	V
线性误差 / Integral linearity error	EL	—	-3		3	LSB
微分线性误差 / Differential linearity error	EDL	—	-3		3	LSB
功耗 / Power consumption	PW	fo=100MHz	—		1.25	W
无杂散动态范围 / SFDR	SFDR	fo=100MHz, normal mode	62		—	dBc
无杂散动态范围 / SFDR	SFDR	fo=950MHz, normal mode	46		—	dBc

功能测试 / Functional test:

English: mu-delay timing control function: after power-up configuration of the circuit and enabling the mudelay timing control function, read back register 0x2A bit<0>; a value of 1 indicates the function is normal. LVDS interface timing control function: after power-up configuration of the circuit and enabling the LVDS interface timing control function, read back register 0x21 bit<0>; a value of 1 indicates the function is normal.

中文： mudelay 时序控制功能：上电配置电路，开启 mudelay 时序控制功能后，回读 0x2A 寄存器 bit<0>，为 1 说明功能正常。LVDS 接口时序控制功能：上电配置电路，开启 LVDS 接口时序控制功能后，回读 0x21 寄存器 bit<0>，为 1 说明功能正常。

注：典型值为常温测试数据。/ Note: typical values are room-temperature test data.

主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

English: 1. FFT spectrum at analog input 100 MHz. Test conditions: sampling rate fCLK=2500MHz; input signal frequency fOUT=100MHz; test result: SFDR=70dBc. 2. FFT spectrum at analog input 950 MHz. Test conditions: sampling rate fCLK=2500MHz; input signal frequency fOUT=950MHz; test result: SFDR=56dBc.

中文： 1、模拟输入 100MHz 条件下 FFT 谱线。测试条件：采样率：fCLK=2500MHz；输入信号频率 fOUT=100MHz；测试结果：SFDR=70dBc。2、模拟输入 950MHz 条件下 FFT 谱线。测试条件：采样率：fCLK=2500MHz；输入信号频率 fOUT=950MHz；测试结果：SFDR=56dBc。

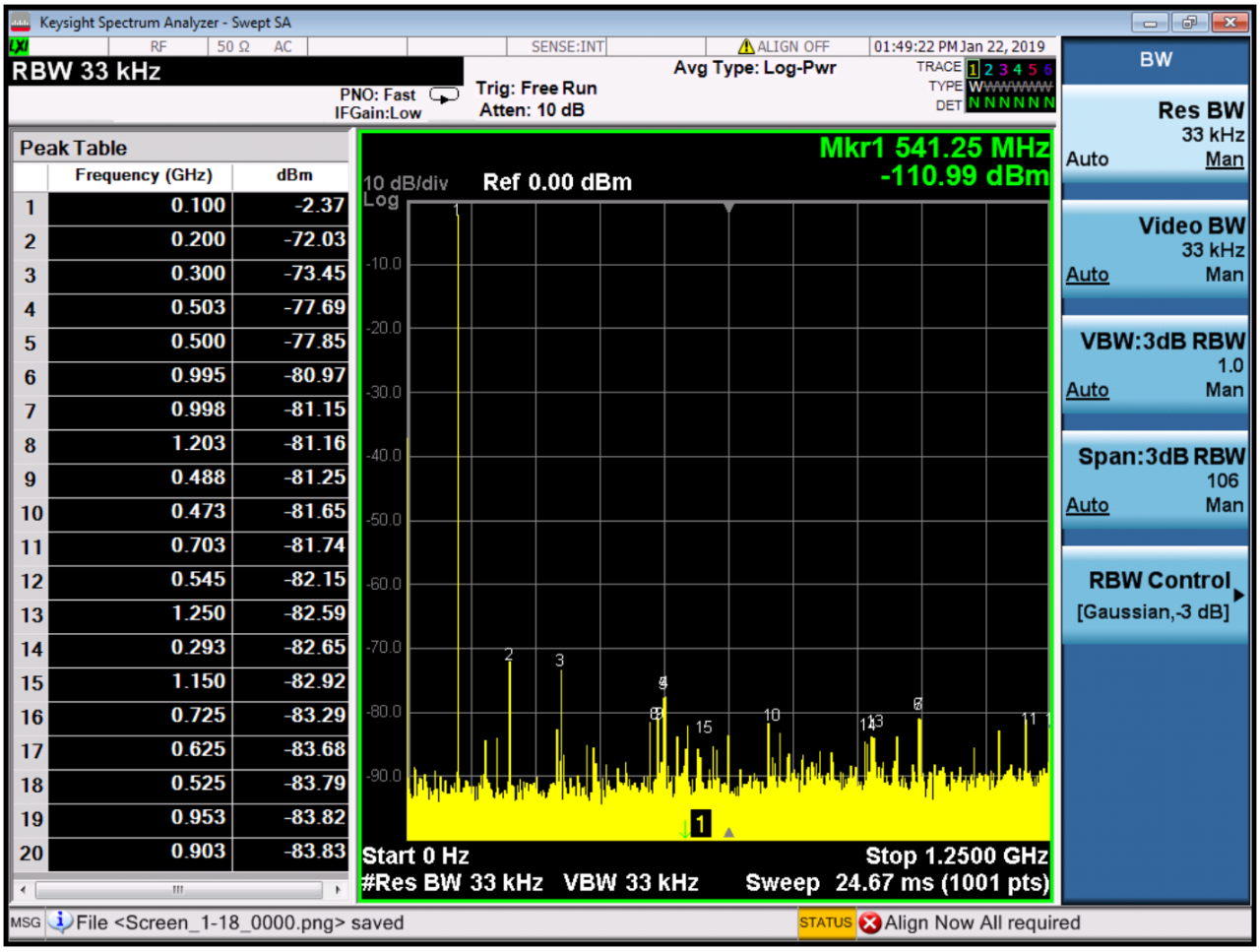


Figure 4: Output spectrum at fOUT=100MHz

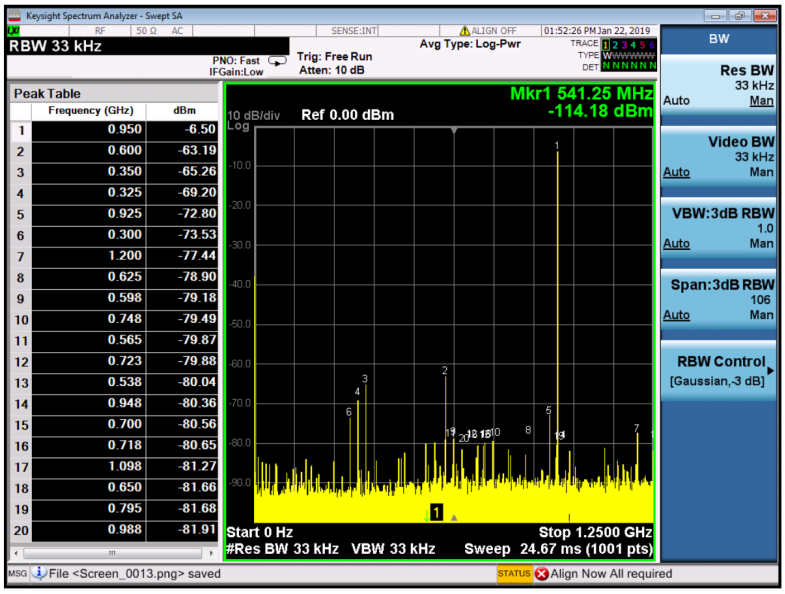


Figure 5: Output spectrum at fOUT=950MHz

典型应用线路图 / Typical Application Circuit

单元模块及工作原理 / Functional Blocks and Operating Principles

1、SPI 接口 / SPI Interface

English: The SXD014 uses an SPI interface that can be easily connected to many industry-standard microcontrollers and microprocessors. This serial I/O port is compatible with most synchronous transmission formats, including Motorola SPI and Inter SSR protocols. The interface allows read/write access to all registers that configure the SXD014. Single- or multi-byte transfers are supported, as are MSB-first or LSB-first transfer formats. The SXD014 serial interface port can be configured as one bidirectional pin I/O (SDIO) or two unidirectional input/output pins (SDIO/SDO).

1.1 串行接口通常工作情况 / Normal Operation of the Serial Interface

English: A communication cycle of the SXD014 has two phases. Phase 1 is the instruction cycle, used to write an instruction byte to the SXD014, corresponding to the first set of 8 rising edges of SCLK, as shown in Table 1. The instruction byte of phase 1 defines whether the coming data transfer is a read or a write, and the register address corresponding to the first byte of data transfer. The first set of 8 rising edges of SCLK in each communication cycle is normally used to write the instruction byte to the SXD014.

表 1 / Table 1: 指令字节描述 / Instruction byte description

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
读/写 Read/Write	A6	A5	A4	A3	A2	A1	A0

English: The remaining SCLK edges are used for phase 2 of the communication cycle. Phase 2 is the actual data transfer between the SXD014 and the system controller.

CSB (chip-select signal) can be raised after every 8 bits to stop the transfer path. When CSB goes low again, the unfinished data continues to be transferred. If the stop is not at a byte boundary, the SPI is reset.

The SPI read/write operation timing is shown in Figure 6. For both read and write operations, the instruction cycle writes information on the rising edge of the clock; in a write operation the communication cycle writes input data on the rising edge of the clock, and in a read operation the communication cycle updates the output data on the falling edge of the clock.

中文： SXD014 采用了 SPI 接口，可轻松的与许多工业标准的微控制器和微处理器连接。该串行 I/O 端口与大多数同步传输格式兼容，包括 Motorola SPI 和 Inter SSR 协议。该接口允许读/写访问所有设置 SXD014 的寄存器。支持单或多字节传输，支持先 MSB（MSB-first）或先 LSB（LSB-first）传输格式。SXD014 串行接口端口可设置为一个双向管脚 I/O（SDIO）或两个单向的输入/输出管脚（SDIO/SDO）。

SXD014 的一个通信周期有两个阶段。阶段 1 是指令周期，用来写入一个指令字节到 SXD014，对应于 SCLK 的第 1 组 8 个上升沿，如表 1 所示。阶段 1 的指令字节定义了即将到来的数据传递是读或是写，以及第一个字节的数据传输所对应的寄存器地址。每个通信周期的 SCLK 的第 1 组 8 个上升沿通常用于将指令字节写入 SXD014。

余下的 SCLK 边沿用于通信周期的阶段 2。阶段 2 是 SXD014 和系统控制器间实际的数据传输。

CSB（片选信号）可以在每 8 个 bits 后升高以停止传输通路。当 CSB 变低后继续传输未完的数据。如果没有停止在字节边界处则复位 SPI。

SPI 读/写操作时序如图 6 所示，无论读操作还是写操作，指令周期都是时钟上升沿触发写入信息，写操作时通信周期在时钟上升沿写入输入数据，读操作时通信周期在时钟下降沿更新输出数据。

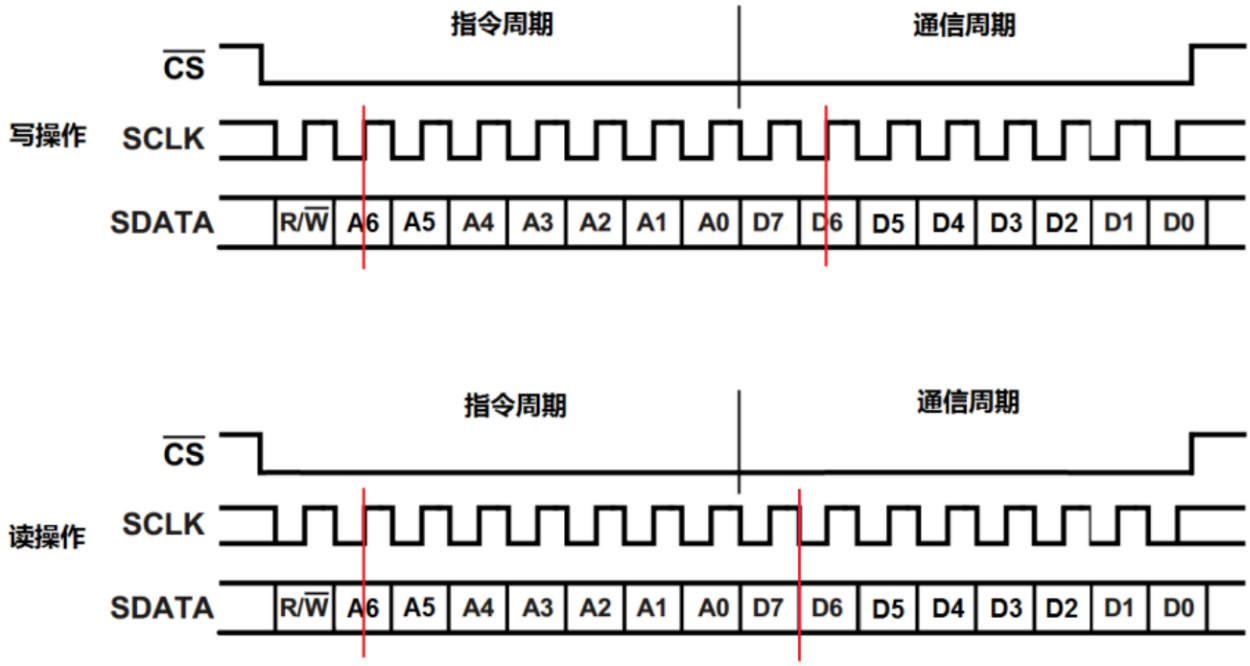


Figure 6: SPI read/write operation timing

1.2 SPI 端口描述 / SPI Port Description

English: - **SCLK — serial clock.** The maximum operating frequency of SCLK is 20 MHz. - **CSB — chip-select signal.** Active low; starts the input and defines a communication cycle. It allows multiple devices to use the same serial channel. When this port input is high, the ports SDO and SDIO become high-impedance. The chip-select signal should remain low throughout the entire communication cycle. - **SDIO — serial data I/O port.** Data is always written to the SXD014 from this port. In addition, this port can also be used as a bidirectional data line. This port is configured by SDIO_DIR (Reg. 0, Bit 7). The default value is 0, and SDIO is configured as a unidirectional port. - **SDO — serial data output.** Data is read out from this port. When the SXD014 works in bidirectional I/O mode, this port cannot output data and is set to high-impedance. - **MSB/LSB transfer.** The SXD014 supports both MSB-first and LSB-first data formats. This function is controlled by LSBFIRST (Reg. 0, Bit 6). The default is MSB first (LSBFIRST = 0). When LSBFIRST = 0 (MSB first), instruction and data bytes must be written in order from the most significant bit to the least significant bit. When LSBFIRST = 1 (LSB first), instruction and data bytes must be written in order from the least significant bit to the most significant bit.

中文： - SCLK—串行时钟。SCLK 的最大工作频率为 20MHz。 - CSB—片选信号。低有效开始输入及定义一个通信周期。允许多个器件使用相同的串行通道。当该端口输入为高时，端口 SDO 和 SDIO 变为高阻态。在整个通信周期内片选信号应该保持为低。 - SDIO—串行数据 I/O 端口。数据总是从该端口写入 SXD014。另外，该端口还可以用作双向数据线。由 SDIO_DIR（Reg. 0，Bit 7）对该端口配置。默认值为 0，SDIO 配置成单向端口。 - SDO—串行数据输出。数据从该端口读出。当 SXD014 工作于双向 I/O 模式时，该端口不能进行数据输出，并被设置成高阻态。 - MSB/LSB 传输。SXD014 即支持 MSB-first 数据格式，也支持 LSB-first 数据格式。该功能受 LSBFIRST（Reg. 0，Bit 6）控制。默认为 MSB first（LSBFIRST＝0）。当 LSBFIRST＝0（MSB first）时，指令和数据字节必须按从最高位到最低位的顺序写入。当 LSBFIRST＝1（LSB first）时，指令和数据字节必须按从最低位到最高位的顺序写入。

1.3 SPI 工作时的注意事项 / Notes on SPI Operation

English: The SXD014 serial port configuration is controlled by Reg. 0, Bit 4, Bit 5, Bit 6, and Bit 7. Note that the configuration changes immediately after the last bit is written to the register.

When the last bit of the instruction is written to the SDIO port, the turnaround drive signal of the path must be set to high-impedance in time.

The serial output signal of the SXD014 is enabled by the falling edge of SCLK. This causes the first output data bit to be shorter than the other data bits.

中文： SXD014 串口配置受 Reg. 0，Bit 4，Bit 5，Bit 6，Bit 7 控制。注意到配置会在最后一位写入寄存器后立刻改变。

指令的最后一位写入 SDIO 端口时，由于通路回转驱动信号必须及时设置成高阻态。

SXD014 的串行输出信号是由 SCLK 的下降沿使能的。这样造成了第一个输出数据 bit 比其他的数据 bits 短。

2、工作模式 / Operating Modes

English: The SXD014 can work in 3 modes: normal mode, return-to-zero mode, and mixing mode. Normal mode is suitable for working in the first Nyquist zone, where the signal power is maximum; return-to-zero mode is suitable for working in the second Nyquist zone, where the roll-off is minimum; mixing mode is suitable for working in the second/third Nyquist zones, where the signal power is maximum. Different operating modes can be implemented by modifying Bit<1:0> of 0x08 through SPI. The corresponding relationship is shown in Table 2.

中文： SXD014 可以工作于 3 种模式：正常模式，归零模式和混频模式。其中正常模式适合工作在第一 Nyquist 区，信号功率最大，归零模式适合工作在第二 Nyquist 区，滚降最小，混频模式适合工作在第二/三 Nyquist 区，信号功率最大。可以通过 SPI 对 0x08 的 Bit<1:0> 修改实现不同的工作模式。对应的关系如表 2 所示。

表 2 / Table 2: SXD014 工作模式 / Operating modes

0x08: Bit<1:0>	功能 / Function
00	正常模式 / Normal mode
01	归零模式 / Return-to-zero mode
10	混频模式 / Mixing mode

3、驱动 DACCLK 输入 / Driving the DACCLK Input

English: The common mode of the SXD014 clock input terminal is generated internally by the circuit as CLKVDD/2 (0.9 V). Therefore, the clock provided to the SXD014 must use AC coupling. The input clock frequency range is 0.8 GHz~2.5 GHz, and the clock driver chip ADCLK914 is recommended for driving the clock terminal.

To optimize the clock duty cycle, the SXD014 adds a clock common-mode point adjustment circuit, configured through SPI via DIR_P, DIR_N, CLKP_OFFSET, and CLKN_OFFSET. DIR_P and DIR_N indicate the change direction of the common-mode point of the P terminal and N terminal of CLK: a low level indicates the clock common-mode point decreases, and a high level indicates the clock common-mode point increases; CLKP_OFFSET and CLKN_OFFSET indicate the change amplitude of the common-mode point of the P terminal and N terminal, which can be set to a maximum of 15. Because the SXD014 uses a pseudo-differential input structure, the common-mode points of the P terminal and N terminal of CLK can be set independently: when the common-mode points of the P and N terminals of the clock change in the same direction, what is adjusted is the duty cycle of the differential clock; when the common-mode points of the P and N terminals of the clock change in opposite directions, what is adjusted is the crossing point of the P-terminal and N-terminal clocks.

中文： SXD014 时钟输入端的共模由电路内部产生，为 CLKVDD/2（0.9V）。因此为 SXD014 提供时钟需采用交流耦合方式。输入时钟的频率范围为 0.8GHz~2.5GHz，时钟端推荐使用时钟驱动芯片 ADCLK914 来进行驱动。

为了优化时钟占空比，SXD014 增加了时钟共模点调节电路，通过 SPI 对 DIR_P、DIR_N、CLKP_OFFSET 和 CLKN_OFFSET 进行设置。其中 DIR_P、DIR_N 表示 CLK 的 P 端和 N 端共模点变化方向，低电平时表示时钟共模点降低，高电平时表示时钟共模点升高；CLKP_OFFSET、CLKN_OFFSET 表示 P 端和 N 端共模点变化的幅度，最大可设置为 15。由于 SXD014 采用的是伪差分输入结构，因此 CLK 的 P 端和 N 端共模点可以独立设置，当时钟 P 端和 N 端共模点同方向变化时，调节的是差分时钟的占空比，当时钟 P 端和 N 端共模点反方向变化时，调节的是 P 端和 N 端时钟的交叉点。

4、微延迟时序调节设置 / Micro-Delay Timing Adjustment Settings

English: The SXD014 uses a delay-locked loop to optimize the timing between its internal digital domain and analog domain, so that the DAC core can still receive data correctly at a high rate of 2.5 GSPS. The DAC clock is divided into an analog path and a digital path: the analog path clock is input directly to the DAC core (to reduce jitter), and the digital path clock is input to a programmable delay line. The output clock of the delay line is the entire internal digital master clock, from which all other internal and external digital clocks are provided. The mu delay controller controls the total delay of the digital path to optimize the timing between the two clock domains, while continuously tracking any changes (in tracking mode) to ensure correct data reception.

The mu delay controller adjusts the timing between the digital domain and the analog domain through a tapped digital delay line with a total delay of 864 ps. Using the MUDEL register, the delay value is digitized into a 9-bit-precision binary number (i.e., a decimal number from 0 to 432), so one LSB is 2 ps. Because at a fixed clock frequency one delay corresponds to one phase offset, the control loop essentially compares the phase relationship between the two clock domains and adjusts the phase of the digital domain clock (through the tapped delay line) to make it equal to the set phase offset (SET_PHS).

After the mu delay controller completes the search and locks onto the target mu phase value, it maintains a fixed timing relationship between the two clock domains within the specified temperature and supply ranges. If the mu delay setting required by the mu delay controller exceeds the range of the tapped delay line (less than 0 or greater than 432), it may lose lock and cause a system interruption (at this time an IRQ can be generated or the search restarted). To avoid this hypothetical situation, it is recommended to use symmetrical guard bands at both ends of the mu delay value range. The recommended guard band setting is 11 (Register 0x29 = 0xCB), corresponding to 88 LSBs of MUDEL.

mu delay controller operating states. The mu delay controller is enabled through register 0x26 Bit 0. Before enabling, the phase comparator (Register 0x24 Bits[5:4]) and the mu delay controller duty-cycle adjustment circuit (Register 0x25 Bit 7) should be turned on. The mu delay controller has three operating modes, determined by Mode[1:0], Bits[5:4] of Register 0x26, as follows: - Search and track (0x0) (best setting) - Track only (0x1) - Search only (0x2)

Search mode. The search algorithm starts from an initial value, which can be set through MUDEL[8:0] (MUDEL[0], Bit 7 of Register 0x27, and MUDEL[8:1], Bits[7:0] of Register 0x28). Although the delay line has 9-bit precision, the maximum mu delay value is 432 (decimal). The best starting point for the search is the middle of the delay line, i.e., 216.

The initial search algorithm scans different mu delay values until it finds the set phase value; this target phase value is set by SetPhs, Bits[4:0] of Register 0x27, with a maximum value of 16. When the set phase value is found, the phase slope is calculated and compared with the set slope, set through the Slope bit of Register 0x26. A positive slope indicates that the phase value increases as mu delay increases, and a negative slope indicates that the phase value decreases as mu delay increases.

If both the phase value and the slope match, the search algorithm ends. The Search_Tol bit (Register 0x29, Bit 7) is used to specify the search precision: - Imprecise (0x0) — a phase value within two values of the specified phase value can be found - Precise (0x1) — finds the specified phase value (best setting)

The search direction can be specified through SrchMode[1:0], Bits[6:5] of Register 0x27. There are three options: - Down only (0x0) - Up only (0x1) - Alternating up and down (0x2) (best setting)

If the mode is alternating up and down, the search proceeds in both directions until one side reaches the guard band. At this time the search continues, but only in the opposite direction. If the set phase value is still not found before reaching the guard band in this direction, the search changes back to alternating up-and-down mode and continues searching within the guard band. If the mu delay controller reaches an endpoint, the search fails. If the controller does not find the set phase value in any of the searches described above, ContRst, Bit 5 of Register 0x29, determines the corrective action: - Continue (0x0) — continue searching (best setting) - Reset (0x1)

Tracking mode. In tracking mode, a control loop is used to increase the mu delay value by 1, decrease it by 1, or leave it unchanged according to the measured phase value. The controller decides whether the mu delay value should decrease or increase according to the set slope.

The user can identify the operating state of the control loop through two status bits, MU_LKD (Register 0x2A, Bit 0) and MU_LOST (Register 0x2A, Bit 1). If the current phase is more than 5 steps away from the set phase, MU_LKD is cleared; if lock was previously obtained, MU_LOST is set to 1. In addition, if lock is lost, the controller can choose to continue tracking or restart the search.

By setting the read bit high (Register 0x26, Bit 3), the user can read back the mu delay value and phase value at the time the controller locked (through MUDEL[8:0] and SetPhs[4:0]). At this time, the mu delay value and set phase value set at the start of the search can no longer be read back. The typical locking time of the mu delay controller is approximately 180K DAC cycles (approximately 90 µs at 2 GSPS).

Table 3 provides the recommended target mu delay slope and phase at different sampling rates.

中文： SXD014 使用一个延迟锁相环来优化其内部数字域与模拟域之间时序，使 DAC 核在 2.5GSPS 高速率下依然可以正确地接收数据。DAC 时钟被分成了一个模拟通路和一个数字通路，模拟通路时钟直接输入 DAC 核（为了减小抖动），数字通路时钟输入到可编程延迟线。延迟线的输出时钟为整个内部数字主时钟，其他的所有内部和外部数字时钟都由它提供。mu delay controller 控制着数字通路的总延迟从而优化两个时钟域之间时序，同时连续地跟踪任何变化（在跟踪模式）以确保数据的正确接收。

mu delay controller 通过一根总延迟为 864ps 的抽头数字延迟线来调节数字域和模拟域之间的时序。用 MUDEL 寄存器把延迟值数字化为 9 位精度的二进制数（即 0 到 432 的十进制数），则一个 LSB 就为 2ps。因为在固定时钟频率下一个延迟就对应了一个相位偏移，所以控制环实质上是比较两个时钟域之间的相位关系然后调节数字域时钟的相位（通过抽头延迟线），使其等于设定的相位偏移（SET_PHS）。

在 mu delay controller 完成了搜索和锁定在目标 mu phase 值之后，它会在指定的温度和供电范围内在两个时钟域之间维持一个固定的时序关系。如果 mu delay controller 要求的 mu delay 设置值超过了抽头延迟线的范围（小于 0 或者大于 432），它可能会失锁从而导致系统中断（这时可以产生 IRQ 或者重启搜索）。为了避免这个假想情况，推荐在 mu delay 值范围的两端使用对称的保护带。推荐的保护带设置为 11（Register 0x29=0xCB）对应于 MUDEL 的 88LSBs。

mu delay controller 工作状态：mu delay controller 通过寄存器 0x26 Bit0 使能。在使能之前应该打开相位比较器（Register 0x24 Bits[5:4]）和 mu delay controller 占空比调节电路（Register 0x25 Bit7）。mu delay controller 有三种工作模式，由 Mode[1:0] Register 0x26 的 Bits[5:4] 确定如下：搜索和跟踪（0x0）（最佳设置）；只跟踪（0x1）；只搜索（0x2）。

搜索模式：搜索算法开始于一个初始值，该初始值可以通过 MUDEL[8:0]（MUDEL[0]，Register 0x27 的 Bit7 和 MUDEL[8:1]，Register 0x28 的 Bits[7:0]）设定。虽然延迟线有 9 位精度，但是最大的 mu delay 值为 432（十进制）。搜索开始的最佳点为延迟线的中间，即 216。初始搜索算法扫描不同的 mu delay 值直到找到设置的相位值，该目标相位值由 SetPhs Register 0x27 的 Bits[4:0] 设置，最大值为 16。当找到设置的相位值，则计算相位斜率然后将其与所设置的斜率比较，通过 Register 0x26 的 Slope 位设置。正斜率表示 mu delay 增加时相位值增加，负斜率表示 mu delay 增加时相位值减少。如果相位值和斜率都匹配，搜索算法结束。Search_Tol 位（Register 0x29，Bit7）用来指定搜索精度：不精确（0x0）—可以找到指定相位值两个值以内相位值；精确（0x1）—找到指定相位值（最佳设置）。搜索方向可以通过 SrchMode[1:0]，Register 0x27 的 Bits[6:5] 指定。共有三种选择：只向下（0x0）；只向上（0x1）；交替上下（0x2）（最佳设置）。如果模式为交替上下，搜索在两个方向进行直到一边到达保护带。此时搜索继续，但是只在相反方向进行。如果在到达此方向的保护带之前设置相位值仍然没找到，则搜索变回交替上下模式后在保护带内继续搜索。如果 mu delay controller 达到了端点则搜索失败。如果 controller 在此前描述的搜索中都没有找到设置的相位值，则 ContRst，Register 0x29 的 Bit5 决定纠正的行动：继续（0x0）—继续搜索（最佳设置）；重置（0x1）。

跟踪模式：在跟踪模式下，用一个控制环路来对 mu delay 值根据测量到的相位值增加 1，减少 1 或不变化。控制器根据设置的斜率来决定 mu delay 值该减少还是增加。用户可以通过两个状态位，MU_LKD（Register 0x2A，Bit0）和 MU_LOST（Register 0x2A，Bit1）来识别控制环路的工作状态。如果当前相位离设置相位超过 5 步，MU_LKD 清零，如果之前获得锁定 MU_LOST 置为 1。此外，如果失锁 controller 可以选择是继续保持跟踪还是重启搜索。通过设置读位为高（Register 0x26，Bit3），用户可以读回 controller 锁定时的 mu delay 值

和相位值（通过 MUDEL[8:0] 和 SetPhs[4:0]）。这时不能再读回开始搜索时设置的 mu delay 值和设置相位值。mu delay controller 的典型锁定时间大概为 180K DAC 周期（在 2GSPS 时约为 90us）。

表 3 提供了不同采样率下推荐的目标 mu delay 斜率和相位。

表 3 / Table 3: 推荐的目标 mu delay 斜率和相位与采样率的关系表 / Recommended target mu delay slope and phase vs. sampling rate

采样率（GSPS）/ Sampling Rate (GSPS)	斜率 / Slope	相位 / Phase
0.8	+	6
0.9	+	7
1.0	+	11
1.1	-	10
1.2~1.8	-	9
1.9-2.5	-	12

5、LVDS 接口时序设置 / LVDS Interface Timing Settings

English: The SXD014 uses a dual 14-bit LVDS data interface. Due to data skew, jitter, etc., in order to ensure the reliability of data transmission, the skew and jitter on the FPGA and the PCB should be minimized as much as possible, and the clock sampling instant should be located in the middle of the eye. To optimize the data reception timing, a companion clock (DCI) must be provided; this companion clock is generated in the same way as the data, except that it is a set of "010101……" data. The DCI transition edge is used to characterize the data edge; by comparing the phases of DCI and the sampling clock, the best sampling instant is found, i.e., the sampling instant is located in the middle of the data stable-valid period.

In its specific implementation, the SXD014 uses the interface structure shown in Figure 7. This structure adjusts the DCI delay line so that the 0° divide-by-4 clock aligns with the DCI edge, and assigns the DCI delay setting value at this time to the SMP delay line; because this delay line is a 90° divide-by-4 clock, this clock sampling edge is exactly located in the middle of the data stable-valid period.

Both automatic mode (controller enabled) and manual mode (controller not enabled) are available for use. Through the SPI control register, the window width setting range is 1~7 (default 2), and the delay line setting range is 0~334 (default 167); automatic mode takes 135k DAC clock cycles by default.

Recommended operating steps are as follows: 1. Set the window width to 2, i.e., 0x13 = 72 ; at this time DCI_DEL and SMP_DEL are 167, the default optimal values. 2. Do not enable the controller, i.e., 0x10 = 0x00. 3. Enable the controller through two operations, i.e., 0x10 = 0x02, 0x10 = 0x13. 4. Wait for 135k DAC clock cycles. 5. Read back and confirm the value in register 0x21; if it is 0x09, the search succeeded and tracking mode has been entered. 6. If the input data rate is less than 1.6 GSPS, read back the DCI_DEL value and confirm whether it is within the range set by the user; if not, flip CLKDIVPH (i.e., 0x14, Bit[7:6]) and return to step 2.

中文： SXD014 采用双路 14 位 LVDS 数据接口。由于数据的偏斜（skew）、抖动（jitter）等，为保证数据传输的可靠性，要尽量减小 FPGA 和 PCB 板上的偏斜和抖动，并使得时钟采样时刻位于眼睛的中间位置。为优化数据接收时序，需提供一路随路时钟（DCI），该随路时钟采用和数据一样的产生方式，只是一组"010101……"的

数据。用 DCI 的变化沿来表征数据的边沿，通过比较 DCI 和采样时钟的相位，找到采样的最佳时刻，即采样时刻位于数据稳定有效周期的中间位置。

具体实现上 SXD014 采用了如图 7 所示的接口结构。该结构通过调节 DCI 延迟线使 0°四分频时钟与 DCI 边沿对齐，并将此时的 DCI 延迟设置值赋于 SMP 延迟线，由于该延迟线是 90°四分频时钟，因此该时钟采样沿正好位于数据稳定有效周期的中间位置。

使用时，有自动模式（使能控制器）和手动模式（不使能控制器）可供选择。通过 SPI 控制寄存器，窗口宽度设定范围 1~7（默认为 2），延迟线设定范围 0~334（默认为 167），自动模式在默认情况下耗时 135k 个 DAC 时钟周期。

推荐操作步骤如下： 1. 设定窗口宽度为 2，即 0x13=72，此时 DCI_DEL、SMP_DEL 为 167，是默认的优值。 2. 不使能控制器，即 0x10 = 0x00。 3. 通过两个操作使能控制器，即 0x10 = 0x02，0x10 = 0x13； 4. 等待 135k 个 DAC 时钟周期。 5. 回读并确认寄存器 0x21 中的值，若为 0x09 则搜索成功并进入了追踪模式。 6. 如果输入数据率小于 1.6GSPS。回读 DCI_DEL 值，确认其是否位于用户所设定的范围内，如果不是则翻转 CLKDIVPH（即 0x14，Bit[7:6]），并返回步骤 2。

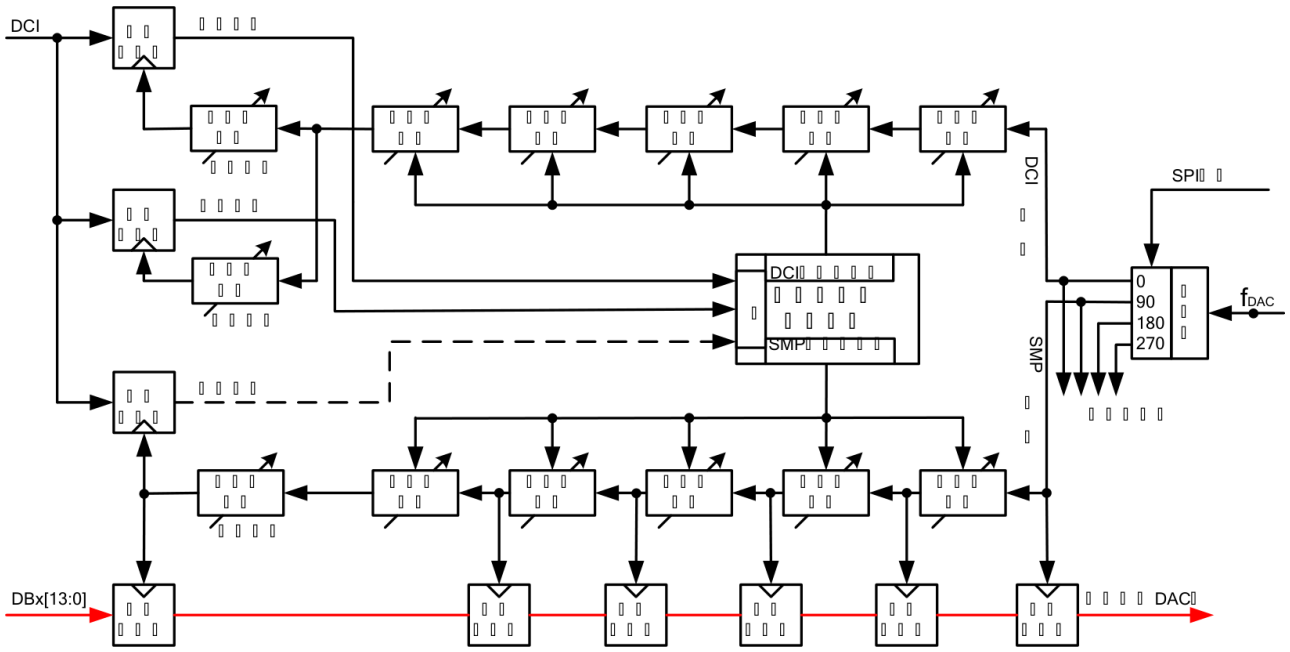


Figure 7: LVDS receiver circuit schematic

6、上电顺序 / Power-Up Sequence

English: The 1.8 V supply needs to be valid before the 3.3 V supply. When the 1.8 V supply is powered down, the 3.3 V supply must no longer be applied.

中文： 1.8V 电源需要在 3.3V 电源前有效。当 1.8V 电源掉电时，不能再加 3.3V 电源。

7、推荐配置流程 / Recommended Configuration Flow

表 4 / Table 4: 多芯片同步未使能时的 SPI 配置流程 / SPI configuration flow with multi-chip synchronization not enabled

步骤 / Step	地址 / Address	写入的值 / Value Written	描述 / Description
1	0x00	0x00	配置四线 SPI 模式，位 [7:5] 必须被镜像到位 [2:0]，因为在上电时 MSB/LSB 格式未知 / Configure four-wire SPI mode; bits [7:5] must be mirrored to bits [2:0] because the MSB/LSB format is unknown at power-up
2	0x00	0x20	软件复位到默认的 SPI 值 / Software reset to default SPI values
3	0x00	0x00	去除复位位 / Remove the reset bit
4	0x22	0x0F	设置输入差分时钟 DACCLK_P 和 DACCLK_N 的共模电压 / Set the common-mode voltage of the input differential clock DACCLK_P and DACCLK_N
5	0x23	0x0F	同上 / Same as above
6	0x24	0x30	配置微延迟单元控制器，在不同的主时钟频率下微延迟单元目标斜率和目标相位值的设定要参考表 3 / Configure the micro-delay unit controller; for the target slope and target phase settings at different master clock frequencies, refer to Table 3
7	0x25	0x80	同上 / Same as above
8	0x27	0x4C	同上 / Same as above
9	0x28	0x6C	同上 / Same as above
10	0x29	0xCB	同上 / Same as above
11	0x26	0x02	同上 / Same as above
12	0x26	0x03	使能微延迟单元控制器的查找和跟踪模式 / Enable the search and tracking mode of the micro-delay unit controller
13	未应用 / Not applied	未应用 / Not applied	等待 160k 个主时钟周期 / Wait for 160k master clock cycles
14	0x2A	（回读 / read back)	回读 0x2A 寄存器，确信它的值为 0x01 以保证 DLL 环路是锁定的。如果未锁定，则回到步骤 10 并重复操作。如此尝试了 3 次仍不锁定，就断开环路并报告微延迟单元失败 / Read back register 0x2A and ensure its value is 0x01 to guarantee the DLL loop is locked. If not locked, return to step 10 and repeat. If it still does not lock after 3 attempts, disconnect the loop and report micro-delay unit failure
15	未应用 / Not applied	未应用 / Not applied	确保 SXD014 的数据输入是由 DCI 时钟送入 / Ensure that the data input of the SXD014 is fed by the DCI clock
16	0x13	0x72	设置窗口宽度为 2 / Set the window width to 2
17	0x10	0x00	在使能数据接收控制器以前，先不使能数据接收控制器 / Before enabling the data receiver controller, first disable it
18	0x10	0x02	使能数据接收控制器以建立环路和中断响应 / Enable the data receiver controller to establish the loop and interrupt response
19	0x10	0x03	使能数据接收控制器以进入查找和跟踪模式 / Enable the data receiver controller to enter search and tracking mode
20	未应用 / Not applied	未应用 / Not applied	等待 135k 个主时钟周期 / Wait for 135k master clock cycles
21	0x21	（回读 / read back)	回读 0x21 寄存器，确信它等于 0x09 以确保 DLL 环路是锁定的并处于跟踪状态。如果不是，则翻转 0x14 寄存器的位 [7:6] 再回到步骤 17 并重复操作。如此尝试了 3 次仍不锁定，就断开环路并报告数据接收锁定失败 / Read back register 0x21 and ensure it equals 0x09 to ensure the DLL loop is locked and in the tracking state. If not, flip bits [7:6] of register 0x14, return to step 17, and

步骤 / Step	地址 / Address	写入的值 / Value Written	描述 / Description
			repeat. If it still does not lock after 3 attempts, disconnect the loop and report data receiver lock failure
22	0x06, 0x07	0x00, 0x02	可选择的：修改 DAC 的满幅度输出电流（默认为 20mA)/ Optional: modify the DAC full-scale output current (default 20 mA)
23	0x08	0x00	可选择的：修改 DAC 的工作模式（默认为普通模式）/ Optional: modify the DAC operating mode (default normal mode)

表 5 / Table 5: 多芯片同步使能时的 SPI 配置流程 / SPI configuration flow with multi-chip synchronization enabled

步骤 / Step	地址 / Address	写入的值 / Value Written	描述 / Description
1	0x00	0x00	配置四线 SPI 模式，位 [7:5] 必须被镜像到位 [2:0]，因为在上电时 MSB/LSB 格式未知 / Configure four-wire SPI mode; bits [7:5] must be mirrored to bits [2:0]
2	0x00	0x20	软件复位到默认的 SPI 值 / Software reset to default SPI values
3	0x00	0x00	去除复位位 / Remove the reset bit
4	0x22	0x0F	设置输入差分时钟 DACCLK_P 和 DACCLK_N 的共模电压 / Set the common-mode voltage of DACCLK_P and DACCLK_N
5	0x23	0x0F	同上 / Same as above
6	0x24	0x30	配置微延迟单元控制器，目标斜率和目标相位值的设定参考表 3 / Configure the micro-delay unit controller; refer to Table 3 for target slope and phase
7	0x25	0x80	同上 / Same as above
8	0x27	0x4C	同上 / Same as above
9	0x28	0x6C	同上 / Same as above
10	0x29	0xCB	同上 / Same as above
11	0x26	0x02	同上 / Same as above
12	0x26	0x03	使能微延迟单元控制器的查找和跟踪模式 / Enable search and tracking mode of the micro-delay unit controller
13	未应用 / Not applied	未应用 / Not applied	等待 160k 个主时钟周期 / Wait for 160k master clock cycles
14	0x2A	（回读 / read back)	回读 0x2A 寄存器，确信它的值为 0x01 以保证 DLL 环路是锁定的。如果未锁定，则回到步骤 10 并重复操作。如此尝试了 3 次仍不锁定，就断开环路并报告微延迟单元失败 / Read back 0x2A; ensure 0x01 for DLL lock; if not locked, return to step 10; after 3 failed attempts, disconnect the loop and report micro-delay unit failure
15	0x15	0x42	配置多芯片同步 / Configure multi-chip synchronization
16	0x10	0x00	在使能多芯片同步控制器前，先不使能多芯片控制器 / Before enabling the multi-chip sync controller, first disable it
17	0x10	0x60 或 0x40 / 0x60 or 0x40	使能多芯片控制器以建立环路和中断响应；0x60 = 主芯片模式，0x40 = 从芯片模式 / Enable the multi-chip controller to establish the loop and interrupt response; 0x60 = master-chip mode, 0x40 = slave-chip mode

步骤 / Step	地址 / Address	写入的值 / Value Written	描述 / Description
18	0x10	0x70 或 0x50 / 0x70 or 0x50	使能多芯片控制器；0x70 = 主芯片模式，0x50 = 从芯片模式 / Enable the multi-chip controller; 0x70 = master-chip mode, 0x50 = slave-chip mode
19	未应用 / Not applied	未应用 / Not applied	让 DLL 锁定需等待 160k 个主时钟周期 / Wait for 160k master clock cycles for DLL lock
20	0x21	（回读 / read back)	回读 0x21 寄存器以确认合适的操作；0x90 = 主芯片模式，0x00 = 从芯片模式。如果不是，回到步骤 15，重复操作。如此尝试了 3 次仍不正确，就断开环路并报告多芯片同步锁定失败 / Read back 0x21 to confirm proper operation; 0x90 = master mode, 0x00 = slave mode. If not, return to step 15; after 3 failed attempts, disconnect the loop and report multi-chip sync lock failure
21	0x0D	（回读 / read back)	回读 0x0D 寄存器，确认为 [5:4] = 10 = 10. If not, return to step 2; after 3 failed attempts, disconnect the loop and report multi-chip sync lock failure
22	未应用 / Not applied	未应用 / Not applied	确保 SXD014 的数据输入是由 DCI 时钟送入 / Ensure the data input is fed by the DCI clock
23	0x13	0x72	设置窗口宽度为 2 / Set the window width to 2
24	0x10	0x00	在使能数据接收控制器以前，先不使能数据接收控制器 / Disable the data receiver controller before enabling it
25	0x10	0x02	使能数据接收控制器以建立环路和中断响应 / Enable the data receiver controller to establish the loop and interrupt response
26	0x10	0x03	使能数据接收控制器以进入查找和跟踪模式 / Enable the data receiver controller to enter search and tracking mode
27			等待 135k 个主时钟周期 / Wait for 135k master clock cycles
28	0x21	（回读 / read back)	回读 0x21 寄存器，确信它等于 0x09 以确保 DLL 环路是锁定的并处于跟踪状态。如果不是，则翻转 0x14 寄存器的位 [7:6] 再回到步骤 17 并重复操作。如此尝试了 3 次仍不锁定，就断开环路并报告数据接收锁定失败 / Read back 0x21; ensure 0x09 for DLL lock and tracking state. If not, flip bits [7:6] of 0x14, return to step 17, and repeat; after 3 failed attempts, disconnect the loop and report data receiver lock failure
29	未应用 / Not applied	未应用 / Not applied	回读主、从芯片中寄存器 0x1B 和 0x1C 中 DCI_DEL 的值，如果主、从芯片的回读值差异超过了 40 个码值，则需要重新指定 DCI_DEL 的目标值为主芯片和从芯片回读的 DCI_DEL 值的平均值 / Read back the DCI_DEL values in registers 0x1B and 0x1C of the master and slave chips; if the difference exceeds 40 codes, re-specify the DCI_DEL target value as the average of the master and slave readback DCI_DEL values
30	0x06, 0x07	0x00, 0x02	可选择的：修改 DAC 的满幅度输出电流（默认为 20mA)/ Optional: modify the DAC full-scale output current (default 20 mA)
31	0x08	0x00	可选择的：修改 DAC 的工作模式（默认为普通模式）/ Optional: modify the DAC operating mode (default normal mode)

寄存器 / Registers

1、SPI 寄存器表 / SPI Register Table

位定义按 Bit7 → Bit0 顺序列出 / Bit definitions are listed in Bit7 → Bit0 order.

Name	Hex Addr	Bit7 → Bit0	Default
Mode	0x00	SDIO DIR; LSB/MSB; Reset; N/A; N/A; N/A; N/A; N/A	0x00
Power Down	0x01	N/A; N/A; LVDS DRVR PD; LVDS RCVR PD; N/A; N/A; CLK RCVR PD; DAC BIAS PD	0x00
CNT_CLK DIS	0x02	N/A; N/A; N/A; N/A; CLKGEN PD; N/A; REC CNT CLK; MU CNT CLK	0x03
IRQ EN	0x03	N/A; N/A; SYNC_LST EN; SYNC_LCK EN; MU LST EN; MU LCK EN; RCV_LST EN; RCV_LCK EN	0x00
IRQ REQ	0x04	N/A; N/A; SYNC_LST IRQ; SYNC_LCK IRQ; MU LST IRQ; MU LCK IRQ; RCVLST IRQ; RCVLCK IRQ	0x00
RSVD	0x05	N/A ×8	N/A
FSC 1	0x06	FSC[7]; FSC[6]; FSC[5]; FSC[4]; FSC[3]; FSC[2]; FSC[1]; FSC[0]	0x00
FSC 2	0x07	Sleep; N/A; N/A; N/A; N/A; N/A; FSC[9]; FSC[8]	0x02
DEC_CNT	0x08	N/A; N/A; N/A; N/A; N/A; N/A; DAC DEC[1]; DAC DEC[0]	0x00
RSVD	0x09	N/A ×8	N/A
LVDS_CNT	0x0A	N/A; N/A; N/A; N/A; HNDOFF_CHK RST; N/A; LVDS_Bias[1]; LVDS_Bias[0]	0x00
DIG_STAT	0x0B	HNDOFF Fall[3]; HNDOFF Fall[2]; HNDOFF Fall[1]; HNDOFF Fall[0]; HNDOFF_Rise[3]; HNDOFF Rise[2]; HNDOFF Rise[1]; HNDOFF Rise[0]	RNDM
LVDS_STAT1	0x0C	SUP/HLD Edge1; N/A; DCI_PHS3; DCI_PHS1; DCI PRE_PH2; DCI PRE PH0; DCI PST PH2; DCI PST PH0	RNDM
LVDS STAT2	0x0D	SUP/HLD SYNC; SUP/HLD_Edge0; SYNC_SAMP1; SYNC_SAMP0; LVDS1 HI; LVDS1 LO; LVDS0 HI; LVDS0 LO	RNDM/ 0
RSVD	0x0E	N/A ×8	N/A
RSVD	0x0F	N/A ×8	N/A
LVDS REC CNT1	0x10	SYNC_FLG RST; SYNC_LOOP ON; SYNC_MST/SLV; SYNC_CNT ENA; N/A; RCVR_FLG RST; RCVR_LOOP ON; RCVR_CNT ENA	0x42
LVDS REC CNT2	0x11	SMP DEL[1]; SMP_DEL[0]; FINE_DEL_MID[3]; FINE_DEL_MID[2]; FINE_DEL_MID[1]; FINE_DEL_MID[0]; RCVR_GAIN[1]; RCVR_GAIN[0]	0xDD
LVDS REC CNT3	0x12	SMP DEL[9]; SMP DEL[8]; SMP DEL[7]; SMP DEL[6]; SMP DEL[5]; SMP DEL[4]; SMP DEL[3]; SMP DEL[2]	0x29
LVDS REC CNT4	0x13	DCI DEL[3]; DCI DEL[2]; DCI DEL[1]; DCI DEL[0]; FINE DEL_SKW[3]; FINE DEL_SKW[2]; FINE DEL_SKW[1]; FINE DEL_SKW[0]	0×71
LVDS REC CNT5	0x14	CLKDIVPH[1]; CLKDIVPH[0]; DCI DEL[9]; DCI DEL[8]; DCI DEL[7]; DCI DEL[6]; DCI DEL[5]; DCI DEL[4]	0x0A
LVDS REC_CNT6	0x15	SYNC_GAIN[1]; SYNC_GAIN[0]; SYNCOUT_PH[1]; SYNCOUT PH[0]; LCKTHR[3]; LCKTHR[2]; LCKTHR[1]; LCKTHR[0]	0x42
LVDS REC CNT7	0x16	N/A; SYNCO_DEL[6]; SYNCO_DEL[5]; SYNCO_DEL[4]; SYNCO_DEL[3]; SYNCO_DEL[2]; SYNCO_DEL[1]; SYNCO_DEL[0]	0x00
LVDS_REC_CNT8	0x17	SYNCSH_DEL[0]; N/A; N/A; N/A; N/A; N/A; N/A; N/A	0x00
LVDS_REC_CNT9	0x18	SYNCSH_DEL[8]; SYNCSH_DEL[7]; SYNCSH_DEL[6]; SYNCSH_DEL[5]; SYNCSH_DEL[4]; SYNCSH_DEL[3]; SYNCSH_DEL[2]; SYNCSH_DEL[1]	0x00
LVDS_REC_STAT1	0x19	SMP DEL[1]; SMP DEL[0]; N/A; N/A; SMP_FINE_DEL[3]; SMP_FINE_DEL[2]; SMP_FINE_DEL[1]; SMP_FINE_DEL[0]	0xC7
LVDS_REC_STAT2	0x1A		0x29

Name	Hex Addr	Bit7 → Bit0	Default
		SMP DEL[9]; SMP DEL[8]; SMP DEL[7]; SMP DEL[6]; SMP DEL[5]; SMP DEL[4]; SMP DEL[3]; SMP DEL[2]	
LVDS_REC_STAT3	0x1B	DCI_DEL[1]; DCI_DEL[0]; N/A; N/A; SYNCOUT PH[1]; SYNCOUT PH[0]; CLKDIV PH[1]; CLKDIV PH[0]	0xC0
LVDS_REC_STAT4	0x1C	DCI_DEL[9]; DCI_DEL[8]; DCI_DEL[7]; DCI_DEL[6]; DCI_DEL[5]; DCI_DEL[4]; DCI_DEL[3]; DCI_DEL[2]	0x29
LVDS_REC_STAT5	0x1D	FINE_DEL_PST[3]; FINE_DEL_PST[2]; FINE_DEL_PST[1]; FINE_DEL_PST[0]; FINE_DEL_PRE[3]; FINE_DEL_PRE[2]; FINE_DEL_PRE[1]; FINE_DEL_PRE[0]	0x86
LVDS_REC_STAT6	0x1E	N/A; SYNCO_DEL[6]; SYNCO_DEL[6]; SYNCO_DEL[6]; SYNCO_DEL[6]; SYNCO_DEL[6]; SYNCO_DEL[6]; SYNCO_DEL[6]	0x00
LVDS_REC_STAT7	0x1F	SYNCSH_DEL[0]; N/A; N/A; N/A; N/A; N/A; N/A; N/A	0x00
LVDS_REC_STAT8	0x20	SYNCSH_DEL[8]; SYNCSH_DEL[7]; SYNCSH_DEL[6]; SYNCSH_DEL[5]; SYNCSH_DEL[4]; SYNCSH_DEL[3]; SYNCSH_DEL[2]; SYNCSH_DEL[1]	0x00
LVDS_REC_STAT9	0x21	SYNC_TRK_ON; SYNC_INIT_ON; SYNC_LST_LCK; SYNC_LCK; RCVR_TRK_ON; RCVR_FE_ON; RCVR_LST; RCVR_LCK	0x00
CROSS_CNT1	0x22	N/A; N/A; N/A; DIR_P; CLKP_OFFSET[3]; CLKP_OFFSET[2]; CLKP_OFFSET[1]; CLKP_OFFSET[0]	0x00
CROSS_CNT2	0x23	N/A; N/A; N/A; DIR_N; CLKN_OFFSET[3]; CLKN_OFFSET[2]; CLKN_OFFSET[1]; CLKN_OFFSET[0]	0x00
PHS_DET	0x24	N/A; N/A; CMP_BST; PHS_DET AUTO_EN; Bias[3]; Bias[2]; Bias[1]; Bias[0]	0x00
MU_DUTY	0x25	MU_DUTYAUTO_EN; POS/NEG; ADJ[5]; ADJ[4]; ADJ[3]; ADJ[2]; ADJ[1]; ADJ[0]	0x00
MU_CNT1	0x26	N/A; Slope; Mode[1]; Mode[0]; Read; Gain[1]; Gain[0]; Enable	0x42
MU_CNT2	0x27	MUDEL[0]; SRCH_MODE[1]; SRCH_MODE[0]; SET_PHS[4]; SET_PHS[3]; SET_PHS[2]; SET_PHS[1]; SETPHS[0]	0x40
MU_CNT3	0x28	MUDEL[8]; MUDEL[7]; MUDEL[6]; MUDEL[5]; MUDEL[4]; MUDEL[3]; MUDEL[2]; MUDEL[1]	0x00
MU_CNT4	0x29	SEARCH_TOL; Retry; CONTRST; Guard[4]; Guard[3]; Guard[2]; Guard[1]; Guard[0]	0x0B
MU_STAT1	0x2A	N/A; N/A; N/A; N/A; N/A; N/A; MU_LOST; MU_LKD	0x00
RSVD	0x2B	N/A ×8	N/A
RSVD	0x2C	N/A ×8	N/A
ANA_CNT1	0x32	HDRM[7]; HDRM[6]; HDRM[5]; HDRM[4]; HDRM[3]; HDRM[2]; HDRM[1]; HDRM[0]	0xCA
ANA_CNT2	0x33	N/A; N/A; N/A; N/A; N/A; N/A; MSEL[1]; MSEL[0]	0x03
RSVD	0x34	N/A ×8	N/A
PART ID	0x35	ID[7]; ID[6]; ID[5]; ID[4]; ID[3]; ID[2]; ID[1]; ID[0]	0x20

电源地间保护 / Power-to-Ground Protection

English: To improve the antistatic capability of the device, the following ESD protection circuits exist between the power pins inside the device. The forward conduction voltage drop of each ESD protection device is approximately 0.6 V. During power-up and normal use, avoid these ESD protection devices conducting in the forward direction for extended periods.

中文： 为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.6V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。

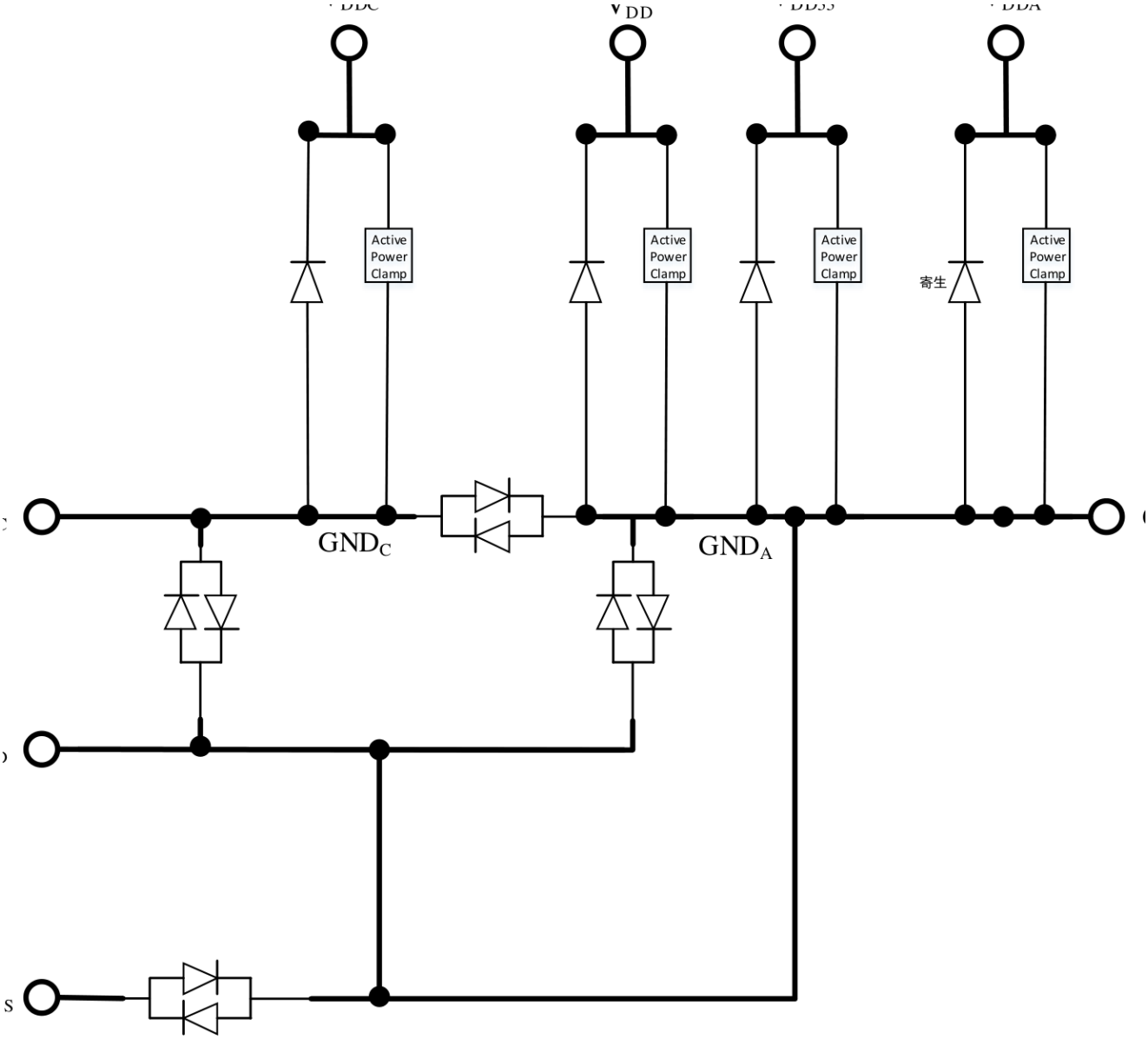


Figure 8: ESD protection circuits between internal power supplies

注意事项 / Precautions

1、产品安装注意事项 / Product Installation Notes

English: 1) Pay attention to the device orientation when soldering to avoid soldering it incorrectly. 2) Instruments and meters used for circuit debugging must have good common grounding. PCB design must maintain good grounding and power-supply decoupling. 3) Take care not to reverse the power supply or short the input/output terminals to the power supply, which can easily cause circuit damage.

中文： 1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2、产品使用注意事项 / Product Usage Notes

English: 1) Use 0.1 μF/10 μF capacitors for power-supply decoupling as close to the power terminals as possible. 2) To ensure the performance of the device, do not exceed the maximum operating frequency of the device during use. 3) The analog ground and digital ground should be kept isolated to avoid digital signals flowing through the analog ground and causing analog noise. The analog ground and digital ground are not connected internally; to make the device work, they must be connected externally. This connection point is a single-point connection and should be as close to the device as possible. 4) It is recommended to first reset the circuit after power-up before use. 5) The input clock frequency range is 0.8 GHz~2.5 GHz, and the clock driver chip ADCLK914 is recommended for driving the clock terminal.

中文： 1) 尽可能在靠近电源端处使用 0.1μF/10μF 电容进行电源去耦。 2) 为了保证器件的性能，在使用时不要超过器件最高工作频率。 3) 模拟地和数字地应该保持隔离，以避免数字信号流经模拟地导致模拟噪声。模拟地和数字地在内部是不相连的，为了使器件工作，它们必须在外部相连接。这个连接点仅是一点相连，并且要尽可能靠近器件。 4) 推荐上电后首先对电路进行复位，再进行使用。 5) 输入时钟的频率范围为 0.8GHz~2.5GHz，时钟端推荐使用时钟驱动芯片 ADCLK914 来进行驱动。

3、产品防护注意事项 / Product Protection Notes

English: 1) Provided rain and snow do not directly affect them, cartons containing the product can be transported by safe means of transport. However, they must not be stacked together with acidic, alkaline, or other corrosive objects. The packaging should be secure, and existing means of transport can be used. 2) The storage environment for packaged products shall meet the Class I warehouse conditions specified in Q/W 657A, Section 8.1 (temperature: 15°C~25°C, humidity: 25%~65%), with no acidic, alkaline, or other corrosive gases around, good ventilation, and appropriate ESD protection measures. 3) It is recommended to use the product within 4 hours after unpacking; if exposed to air for more than 4 hours, it is recommended to perform high-temperature baking at 125°C for 8 h, then vacuum-package it and place it in a drying cabinet.

中文： 1) 在避免雨、雪直接影响的条件下，装有产品的包装箱可以用安全的运输工具运输。但不能和带有酸性、碱性和其它腐蚀性物体堆放在一起。包装应是安全的，可以采用现有的运输工具。 2) 包装好的产品贮存环境应满足 Q/W 657A 第 8.1 规定的 I 类库房条件要求（温度：15°C~25°C，湿度：25%~65%），周围没有酸、碱或其它腐蚀性气体，通风良好，且具备相应防静电措施。 3) 建议拆封后 4 小时内使用，如在空气中暴露超过 4 小时，建议进行 125°C，8h 的高温烘焙后抽真空包装，放置于干燥柜中。

4、电装说明 / Assembly Instructions

English: 1) The moisture sensitivity level of this product is MSL3. The allowable exposure time to the external environment after the product is removed from the moisture-proof bag, dry-stored, or baked until before reflow soldering is: ≤30°C/60%RH, 168 h; 2) If the device storage conditions cannot be controlled or traced, strictly perform baking at 125°C for 8 h before assembly; 3) If the assembly environment temperature and humidity cannot be guaranteed at ≤30°C/60%RH, complete soldering within 12 h after baking; 4) After baking, the product is very prone to generating static electricity; all operations require attention to ESD protection; 5) When leaded reflow soldering (Sn63Pb37) is used for board-level assembly, the recommended peak temperature range is 210°C~220°C; the maximum peak temperature is recommended not to exceed 235°C; dwell time within ±5°C of the peak temperature ≤20 s; time above the liquidus line 60~90 s; ramp-up rate 2~4°C/s; ramp-down rate 2~6°C/s; 6) When lead-free

reflow soldering (SAC305) is used for board-level assembly, the recommended peak temperature range is 230°C~245°C; the maximum peak temperature is recommended not to exceed 260°C; dwell time within ±5°C of the peak temperature ≤20 s; time above the liquidus line 60~90 s; ramp-up rate 2~4°C/s; ramp-down rate ≤2°C~6°C ; 7) If a mixed assembly process requires a higher temperature, ensure that the device body temperature does not exceed 260°C at most. (The device body temperature measurement point is located on the top surface of the device during reflow soldering.) 8) This product uses lead-free/leaded solder balls, with material SAC305.

中文： 1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； 3) 若电装环境温湿度无法保证 ≤30°C/60RH%，请在烘烤后 12h 内完成焊接； 4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~220°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s，升温速率 ≤2°C~6°C； 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C。（器件本体温度测量点位于回流焊时器件上表面）； 8) 本产品采用无铅/有铅焊球，材料为 SAC305。

5、热阻 / Thermal Resistance

English: Package thermal resistance.

中文： 封装热阻。

项目 / Item	实测值 / Measured Value	依据标准及方法 / Basis Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient)	48.32 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2 natural-convection thermal test environment requirements and methods
Rthjt（结到器件顶面的热阻）/ Rthjt (junction-to-top)	7.578 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14 dual-interface separation method
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-bottom)	5.173 K/W	JESD51-14 拐点理论器件内部结构分层得到 / JESD51-14, obtained by layering per inflection-point theory
Rthj-board（结到 PCB 板背面的热阻）/ Rthj-board (junction-to-board back)	20.19 K/W	JEDEC51-14 一维传热路径双界面分离法 / JEDEC51-14 dual-interface separation method

常见故障及处理办法 / Common Faults and Troubleshooting

English: 1. No signal output: check whether the voltage at the I120 terminal is normal to ensure the reference works normally; check whether the OUTDATACLK terminal is normal to ensure the clock can be received correctly. 2. Device functions abnormally: clarify the device operating mode; it is recommended to reset the circuit first after power-up so that the internal registers of the circuit enter their default states. 3. Device operates unstably: check the power supply and ensure that the supply voltage is stable.

中文： 1、 无信号输出：检查 I120 端电压是否正常，确保基准工作正常；检查 OUTDATACLK 端是否正常，确保时钟能正确接收。 2、 器件功能不正常：明确器件工作模式，建议电路上电后先进行复位，使电路内部寄存器进入默认状态。 3、 器件工作不稳定：检查电源，保证电源电压稳定。

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附加说明 / Additional Notes

English: 1. First release date of this manual: July 2026. 2. Product status: ☒ In production (this product model is currently in production; formal products can be provided) / ☐ Pre-release (this product model has not yet entered formal production; samples can be provided). 3. Model suffix difference description (for series products, model suffixes are described as in the following example; add this part when needed): None. 4. Description of replacement of foreign products: 1) Comparison of absolute maximum ratings — see Appendix Table 1. 2) Comparison of recommended operating conditions — see Appendix Table 2. 3) Comparison of performance specifications — see Appendix Table 3. 5) Register comparison : When configuring the micro-delay unit controller, the settings of the target slope and target phase values of the micro-delay unit at different master clock frequencies differ from those of the foreign product; refer to Table 3. 6) Comparison of other specifications — see Appendix Table 4. Note: the height H of the SXD014 is a typical value, while that of the foreign product is a maximum value.

中文： 1. 本说明书首次发布日期：2026 年 7 月。 2. 本产品状态：☒生产（该产品型号目前已在生产，可以提供正式产品）☐预发布（该产品型号尚未投入正式生产，可以提供样品） 3. 型号后缀差异性说明（系列化产品需对型号后缀说明如下示例，需要时增加此部分）：无 4. 替代国外产品情况说明： 1）绝对最大额定值对比：见附表 1。 2）推荐工作条件对比：见附表 2。 3）性能指标对比：见附表 3。 5）寄存器对比：配置微延迟单元控制器，在不同的主时钟频率下微延迟单元目标斜率和目标相位值的设定与国外不一致，参考表 3。 6）其它指标对比：见附表 4。注：其中 SXD014 高度 H 为典型值，国外产品为最大值。

附表 1 / Appendix Table 1: 绝对最大额定值对比 / Absolute maximum ratings comparison

参数 / Parameter	SXD014 规范要求 / Specification Requirement	国外产品器件手册 / Foreign Product Datasheet	比对结果 / Comparison Result
模拟电源电压（VDDA）/ Analog supply voltage (VDDA)	3.6V	-0.3V~3.6V	一致 / Consistent
1.8V 数字电源电压（VDD）/ 1.8V digital supply voltage (VDD)	1.98V	-0.3V~1.98V	一致 / Consistent
3.3V 数字电源电压（VDD33）/ 3.3V digital supply voltage (VDD33)	3.63V	-0.3V~3.6V	基本一致 / Basically consistent
时钟电源电压（VDDC）/ Clock supply voltage (VDDC)	1.98V	-0.3V~1.98V	一致 / Consistent
贮存温度（Tstg）/ Storage temperature (Tstg)	-65°C~150°C	-65°C~150°C	一致 / Consistent
结温（TJ）/ Junction temperature (TJ)	150°C	150°C	一致 / Consistent

附表 2 / Appendix Table 2: 推荐工作条件对比 / Recommended operating conditions comparison

参数 / Parameter	SXD014 规范要求 / Specification Requirement	国外产品器件手册 / Foreign Product Datasheet	比对结果 / Comparison Result
模拟电源电压（VDDA）/ Analog supply voltage (VDDA)	3.135V~3.465V	3.1V～3.5V	基本一致 / Basically consistent
1.8V 数字电源电压（VDD）/ 1.8V digital supply voltage (VDD)	1.71V~1.89V	1.7V～1.9V	基本一致 / Basically consistent
3.3V 数字电源电压（VDD33）/ 3.3V digital supply voltage (VDD33)	3.135V~3.465V	3.1V～3.5V	基本一致 / Basically consistent
时钟电源电压（VDDC）/ Clock supply voltage (VDDC)	1.71V~1.89V	1.7V～1.9V	基本一致 / Basically consistent
工作温度（TA）/ Operating temperature (TA)	-40°C~85°C	-40°C~85°C	一致 / Consistent

附表 3 / Appendix Table 3: 主要性能指标对比 / Main performance specifications comparison

参数 / Parameter	符号 / Symbol	条件 / Conditions	SXD014（实测）最小 / Min	SXD014（实测）典型 / Typ	SXD014（实测）最大 / Max	国外产品（数据手册）最小 / Min	国外产品（数据手册）典型 / Typ	国外产品（数据手册）最大 / Max	单位 / Unit	比对结果 / Result
分辨率 / Resolution			14	14	14	14	14	14	Bits	一致 / Consistent
基准电压 / Reference voltage			1.15	1.18	1.25	1.15	1.2	1.25	V	一致 / Consistent
线性误差 / Integral linearity error			-3	±2.5	3	—	±1.8	—	LSB	典型值有差异 / Typical values differ
微分线性误差 / Differential linearity error			-3	±0.8	3	—	±0.5	—	LSB	典型值有差异 / Typical values differ
增益误差 / Gain error			—	3	—	—	2	—	%FSR	典型值有差异 / Typical values differ
功耗 / Power consumption			—	0.95	1.25	—	0.98	—	W	典型值有差异 / Typical values differ
无杂散动态范围 / SFDR		fo=100MHz, normal mode	62	70	—	—	69	—	dBc	典型值有差异 / Typical values differ
无杂散动态范围 / SFDR		fo=350MHz, normal mode	—	59	—	—	58	—	dBc	典型值有差异 / Typical values differ
无杂散动态范围 / SFDR		fo=550MHz, normal mode	—	56	—	—	55	—	dBc	典型值有差异 / Typical values differ
			46	57	—	—	57	—	dBc	

参数 / Parameter	符号 / Symbol	条件 / Conditions	SXD014（实测）最小 / Min	SXD014（实测）典型 / Typ	SXD014（实测）最大 / Max	国外产品（数据手册）最小 / Min	国外产品（数据手册）典型 / Typ	国外产品（数据手册）最大 / Max	单位 / Unit	比对结果 / Result
无杂散动态范围 / SFDR		fo=950MHz, normal mode								一致 / Consistent
无杂散动态范围 / SFDR		fo=1400MHz, mix mode	—	47	—	—	49	—	dBc	典型值有差异 / Typical values differ
无杂散动态范围 / SFDR		fo=1900MHz, mix mode	—	53	—	—	53	—	dBc	一致 / Consistent
无杂散动态范围 / SFDR		fo=2400MHz, mix mode	—	45	—	—	47	—	dBc	典型值有差异 / Typical values differ

注：SXD014、国外产品典型值均为常温实测值，SXD014 极限值为规范要求，国外产品极限值为数据手册值。/ Note: the typical values of both the SXD014 and the foreign product are room-temperature measured values; the limit values of the SXD014 are specification requirements, and the limit values of the foreign product are datasheet values.

附表 4 / Appendix Table 4: 其它指标对比 / Other specifications comparison

注：其中 SXD014 高度 H 为典型值，国外产品为最大值。/ Note: the height H of the SXD014 is a typical value, while that of the foreign product is a maximum value.

参数 / Parameter	SXD014	国外产品 / Foreign Product	比对结果 / Comparison Result
封装形式 / Package	BGA160	BGA160	一致 / Consistent
质量等级 / Quality grade	企标 / Enterprise standard	工业级 / Industrial grade	有差异 / Different
尺寸（L×W×H）/ Dimensions (L×W×H)	12mm12mm1.41mm	12mm12mm1.4mm	有差异 / Different
替代建议 / Replacement recommendation	□直接替代 / Direct replacement □有效替代 / Effective replacement ☒功能替代 / Functional replacement		