SXD015

12-Bit, 3 GSPS D/A Converter

12 位 3GSPS D/A 转换器

12-bit | 1 channel | 3 GSPS | CBGA196 | LVDS

12位 | 单通道 | 3GSPS | CBGA196 | LVDS

对标 / Cross Reference: EV12DS130A — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

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SXD015 12-Bit 3GSPS D/A Converter — Product Manual (Bilingual)

SXD015 型 12 位 3GSPS D/A 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深圳市深信科技有限公司 / 深信科技
V1.20260710

对标 / Cross Reference: EV12DS130A — pin-to-pin compatible alternative

> 版本说明 / Version note: 原件封面版本号为 V1.202060716、版本修订记录为 V1.20260716、正文页眉为 V1.20260710，三者不一致。Pin-to-pin 仅指封装/引脚层面兼容 / Pin-to-pin refers to package/pin-level compatibility only.

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版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20260716	2026.7.16	——	首次发布 / Initial release	

产品用途及应用范围 / Applications and Scope

English: Broadband signal direct digital synthesis; automatic test equipment; arbitrary waveform generators; electronic-countermeasure signal synthesis.

中文： 宽带信号直接数字综合；自动测试设备；任意波形产生器；电子对抗信号综合。

标准 / Standards

English: Quality grade: enterprise military standard (product inspection controlled to Grade B as specified in GJB597B-2012).

中文： 质量等级：企军标（产品检验按 GJB597B-2012 中规定的 B 级控制）。

产品特点 / Features

English: - 12-bit D/A converter - 3GSPS conversion rate - Low latency: 3.5 clock cycles - Multiple output operating modes: non-return-to-zero, return-to-zero, narrow return-to-zero, mixing mode - LVDS data input interface - Supply voltages: digital 3.3V, analog 3.3V & 5V - Power consumption: 1.56W (typical) - ESD: ≥500V (human body model) - Product weight: 2.18g±0.2g

中文： - 12 位 D/A 转换器 - 3GSPS 转换速率 - 低延迟时间：3.5 个时钟周期 - 多种输出工作模式：非归零、归零、窄归零、混频模式 - LVDS 数据输入接口 - 电源电压：数字 3.3V、模拟 3.3V&5V - 功耗：1.56W（典型值） - ESD：≥500V（人体模型） - 产品重量：2.18g±0.2g

产品描述 / Product Description

English: The SXD015 12-bit 3GSPS D/A converter uses a segmented current-steering architecture. The product includes four parallel LVDS interfaces, achieving a total input data rate of up to 3Gsps. The four 0.75Gsps data streams are then combined by a MUX into 3Gsps high-speed data. After decoding, the high-speed data is sent to the DAC core for conversion and output. It integrates four operating modes: return-

to-zero mode (RTZ), non-return-to-zero mode (NRZ), narrow return-to-zero mode (NRTZ), and mixing mode (RF).

The circuit is housed in a 196-pin ceramic ball grid array package (CBGA196), implements standard GJB597B, and its quality assurance requirements are controlled to Grade B as specified in GJB597B-2012. Chips and other package forms can also be provided according to the user's actual needs.

The functional block diagram of the product is as follows:

中文： SXD015 型 12 位 3GSPS D/A 转换器采用分段电流舵架构。该产品包括四路并行 LVDS 接口，实现输入总数据率高达 3Gsps。然后通过 MUX 将四路 0.75Gsps 数据合成 3Gsps 的高速数据。高速数据经过译码后送入 DAC 内核转换输出。它集成四种工作模式：归零模式（RTZ）、非归零模式（NRZ）、窄归零模式（NRTZ）和混频模式（RF）。

该电路采用 196 引脚陶瓷焊球阵列外壳（CBGA196），执行标准 GJB597B，质量保证要求按 GJB597B-2012 中规定的 B 级控制。也可根据用户实际需要，提供芯片及其它封装形式。

该产品功能框图如下：

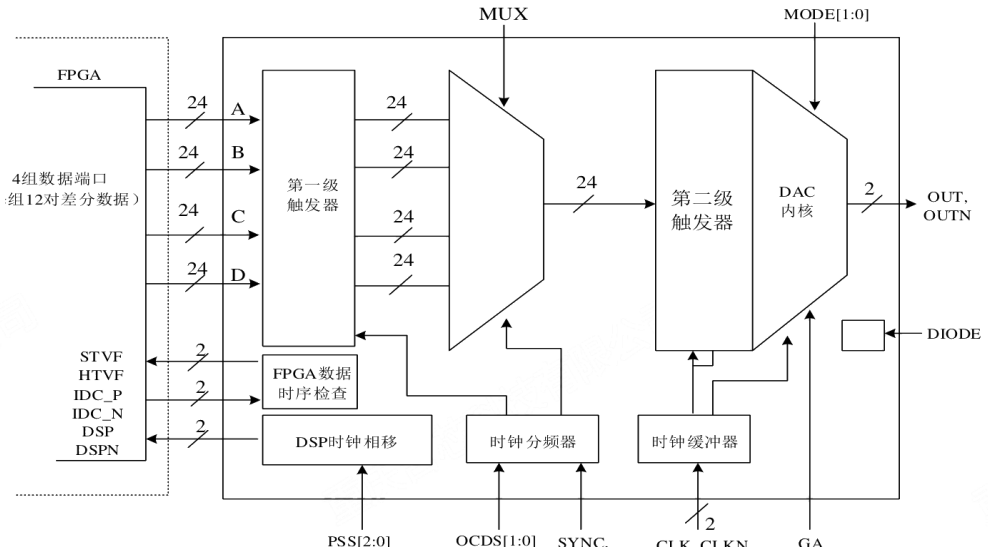


Figure 1: Functional block diagram

English: The operating timing of the product is as follows:

中文： 该产品工作时序如下：

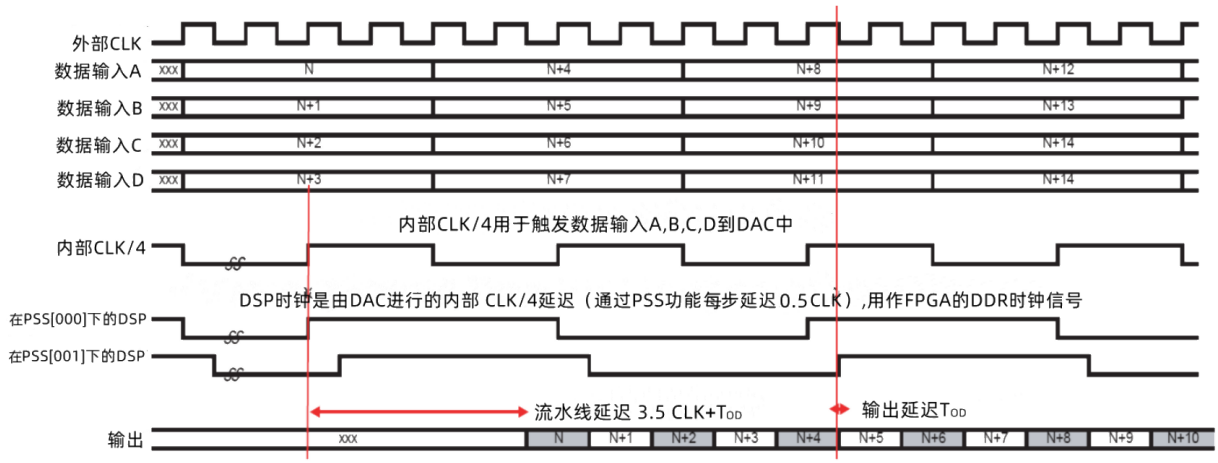


Figure 2: Timing diagram (4:1 MUX mode)

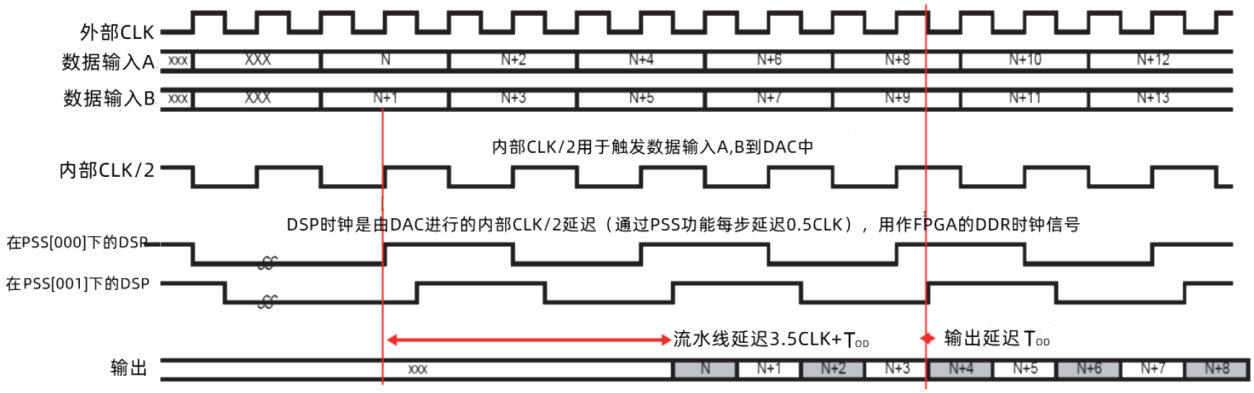
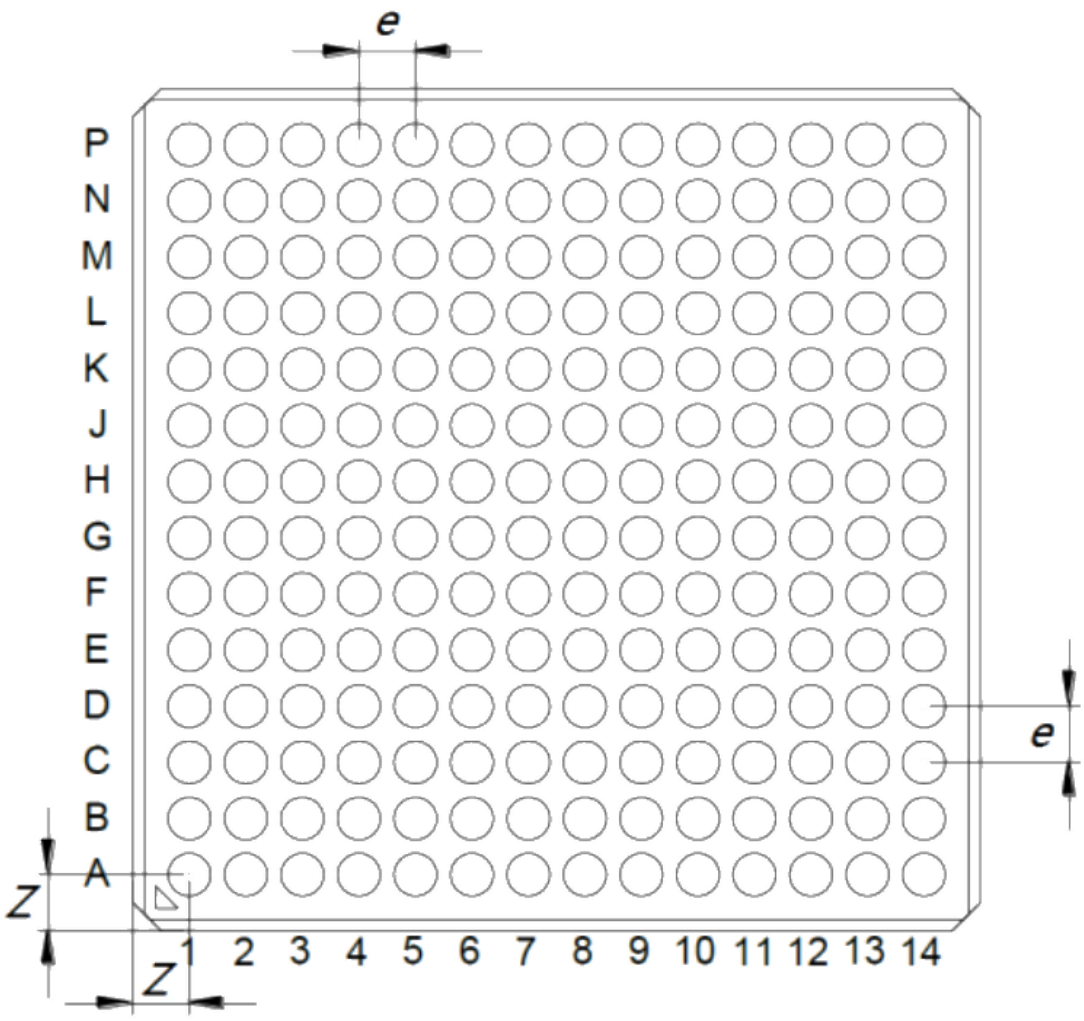


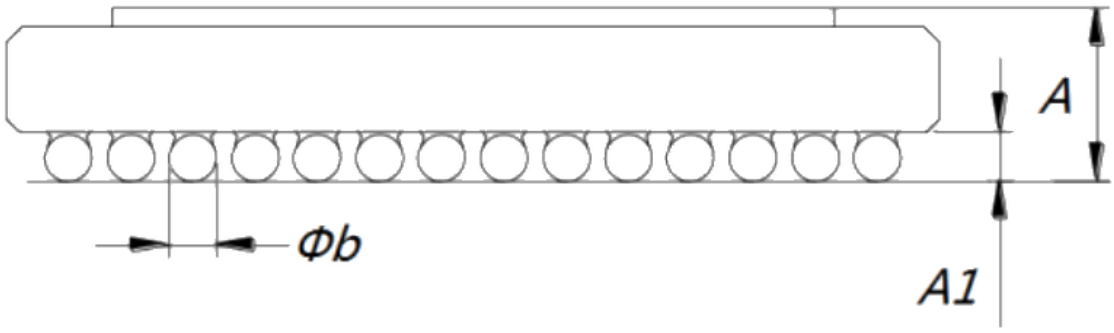
Figure 3: Timing diagram (2:1 MUX mode)

产品外形图和实物图片 / Package Outline and Product Photos

English: The product package form is shown in Figure 2 ; the pin arrangement is fully compatible with the foreign product. If the user requires other package forms, customization is available on request.

中文： 产品封装形式如图 2，管脚排列与国外产品完全兼容。用户若有其它封装形式需要，可根据要求进行订制。


e
P
N
M
L
K
J
H
G
F
E
D
C
B
A
e
Z
1 2 3 4 5 6 7 8 9 10 11 12 13 14
Z


A
Φb
A1

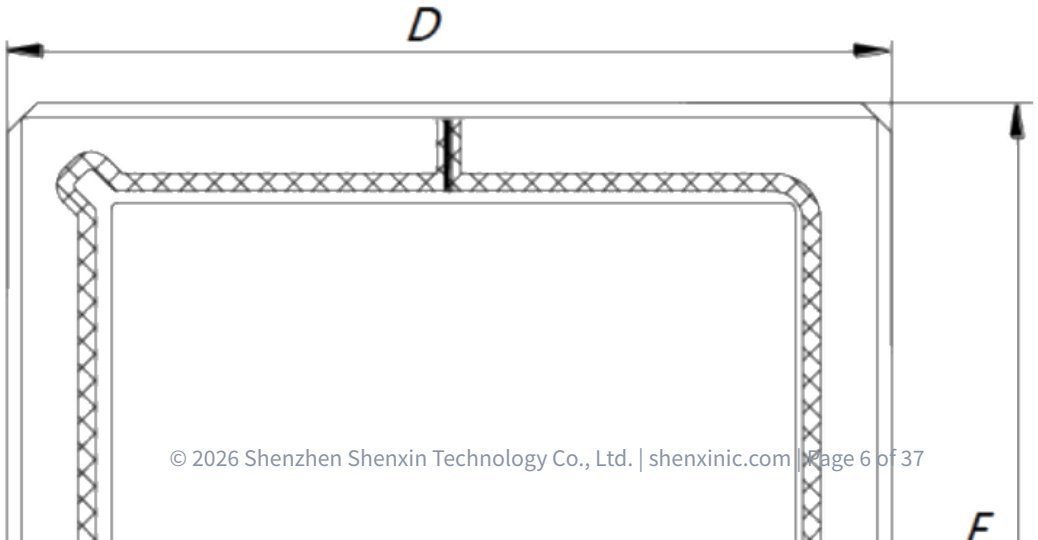

D
E

Figure 4: Package outline dimensions and product photo

单位为毫米 / Units in mm

尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max	尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max
A	—	2.76[a]	3.20	D	14.85	15.00[a]	15.05
A1	0.61	0.76[a]	0.91	E	14.85	15.00[a]	15.05
Φb	0.71	0.76[a]	0.81	Z	—	1.00[a]	1.10
e	—	1.00	—				

注：a：设计保证，不进行考核 / Note: a: guaranteed by design, not subject to testing.

引出端排列（俯视图）/ Pin Arrangement (Top View)

English: The pin arrangement shall be as specified in Figure 5. The pin arrangement is a top view.

中文： 引出端排列应按图 5 的规定。引出端排列为俯视图。

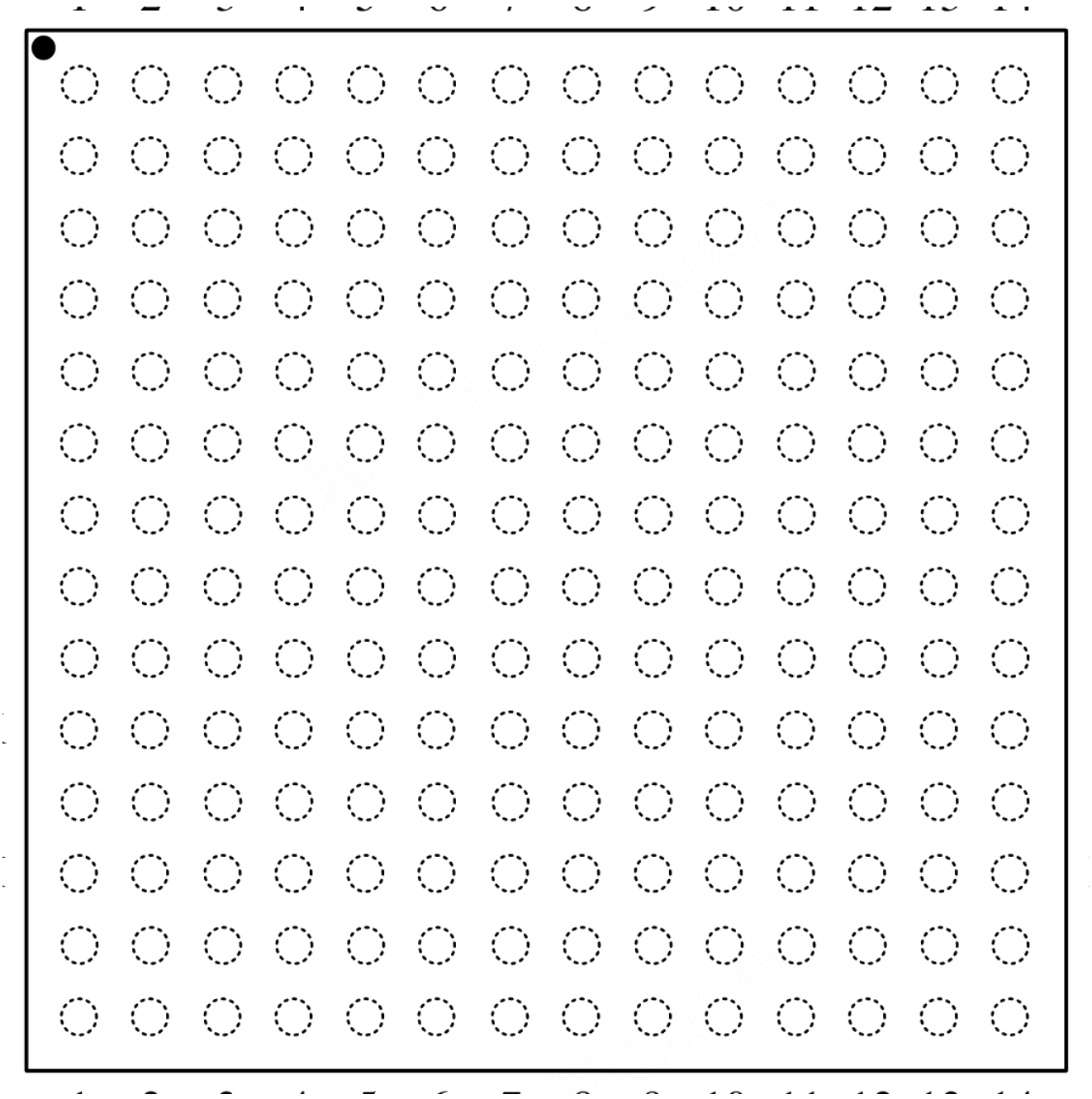


Figure 5: Pin arrangement (top view)

引出端功能符号表 / Pin Function Table

引出端号 / Pin No.	符号 / Symbol	名称 / Name	引出端号 / Pin No.	符号 / Symbol	名称 / Name
A1	GNDD	数字地 / Digital ground	H1	A6	差分数据输入位 A6 / Differential data input bit A6
A2	B5	差分数据输入位 B5 / Differential data input bit B5	H2	A6N	差分数据输入位 A6N / Differential data input bit A6N
A3	B6	差分数据输入位 B6 / Differential data input bit B6	H3	A7	差分数据输入位 A7 / Differential data input bit A7

引出端号 / Pin No.	符号 / Symbol	名称 / Name	引出端号 / Pin No.	符号 / Symbol	名称 / Name
A4	B6N	差分数据输入位 B6N / Differential data input bit B6N	H4	A7N	差分数据输入位 A7N / Differential data input bit A7N
A5	B9	差分数据输入位 B9 / Differential data input bit B9	H5	GNDD	数字地 / Digital ground
A6	B9N	差分数据输入位 B9N / Differential data input bit B9N	H6	GNDA	模拟地 / Analog ground
A7	B11	差分数据输入位 B11（最高位）/ Differential data input bit B11 (MSB)	H7	GNDA	模拟地 / Analog ground
A8	C11	差分数据输入位 C11（最高位）/ Differential data input bit C11 (MSB)	H8	GNDA	模拟地 / Analog ground
A9	C9N	差分数据输入位 C9N / Differential data input bit C9N	H9	GNDA	模拟地 / Analog ground
A10	C9	差分数据输入位 C9 / Differential data input bit C9	H10	GNDD	数字地 / Digital ground
A11	C6N	差分数据输入位 C6N / Differential data input bit C6N	H11	D7N	差分数据输入位 D7N / Differential data input bit D7N
A12	C6	差分数据输入位 C6 / Differential data input bit C6	H12	D7	差分数据输入位 D7 / Differential data input bit D7
A13	C5	差分数据输入位 C5 / Differential data input bit C5	H13	D6N	差分数据输入位 D6N / Differential data input bit D6N
A14	GNDD	数字地 / Digital ground	H14	D6	差分数据输入位 D6 / Differential data input bit D6
B1	B3	差分数据输入位 B3 / Differential data input bit B3	J1	A3N	差分数据输入位 A3N / Differential data input bit A3N
B2	B4	差分数据输入位 B4 / Differential data input bit B4	J2	A5	差分数据输入位 A5 / Differential data input bit A5
B3	B5N	差分数据输入位 B5N / Differential data input bit B5N	J3	A5N	差分数据输入位 A5N / Differential data input bit A5N
B4	B7	差分数据输入位 B7 / Differential data input bit B7	J4	VCCA3	3.3V 模拟电源 / 3.3V analog supply
B5	B8	差分数据输入位 B8 / Differential data input bit B8	J5	VCCA3	3.3V 模拟电源 / 3.3V analog supply
B6	B10	差分数据输入位 B10 / Differential data input bit B10	J6	GNDA	模拟地 / Analog ground
B7	B11N	差分数据输入位 B11N（最高位）/ Differential data input bit B11N (MSB)	J7	GNDA	模拟地 / Analog ground
B8	C11N	差分数据输入位 C11N（最高位）/ Differential data input bit C11N (MSB)	J8	GNDA	模拟地 / Analog ground
B9	C10		J9	GNDA	模拟地 / Analog ground

引出端号 / Pin No.	符号 / Symbol	名称 / Name	引出端号 / Pin No.	符号 / Symbol	名称 / Name
		差分数据输入位 C10 / Differential data input bit C10			
B10	C8	差分数据输入位 C8 / Differential data input bit C8	J10	VCCA3	3.3V 模拟电源 / 3.3V analog supply
B11	C7	差分数据输入位 C7 / Differential data input bit C7	J11	VCCA3	3.3V 模拟电源 / 3.3V analog supply
B12	C5N	差分数据输入位 C5N / Differential data input bit C5N	J12	D5N	差分数据输入位 D5N / Differential data input bit D5N
B13	C4	差分数据输入位 C4 / Differential data input bit C4	J13	D5	差分数据输入位 D5 / Differential data input bit D5
B14	C3	差分数据输入位 C3 / Differential data input bit C3	J14	D3N	差分数据输入位 D3N / Differential data input bit D3N
C1	B1N	差分数据输入位 B1N / Differential data input bit B1N	K1	A3	差分数据输入位 A3 / Differential data input bit A3
C2	B3N	差分数据输入位 B3N / Differential data input bit B3N	K2	A4	差分数据输入位 A4 / Differential data input bit A4
C3	B4N	差分数据输入位 B4N / Differential data input bit B4N	K3	A4N	差分数据输入位 A4N / Differential data input bit A4N
C4	B7N	差分数据输入位 B7N / Differential data input bit B7N	K4	GNDD	数字地 / Digital ground
C5	B8N	差分数据输入位 B8N / Differential data input bit B8N	K5	GNDD	数字地 / Digital ground
C6	B10N	差分数据输入位 B10N / Differential data input bit B10N	K6	GNDA	模拟地 / Analog ground
C7	GNDD	数字地 / Digital ground	K7	VCCA5	5V 模拟电源 / 5V analog supply
C8	GNDD	数字地 / Digital ground	K8	VCCA5	5V 模拟电源 / 5V analog supply
C9	C10N	差分数据输入位 C10N / Differential data input bit C10N	K9	GNDA	模拟地 / Analog ground
C10	C8N	差分数据输入位 C8N / Differential data input bit C8N	K10	GNDD	数字地 / Digital ground
C11	C7N	差分数据输入位 C7N / Differential data input bit C7N	K11	GNDD	数字地 / Digital ground
C12	C4N	差分数据输入位 C4N / Differential data input bit C4N	K12	D4N	差分数据输入位 D4N / Differential data input bit D4N
C13	C3N	差分数据输入位 C3N / Differential data input bit C3N	K13	D4	差分数据输入位 D4 / Differential data input bit D4
C14	C1N	差分数据输入位 C1N / Differential data input bit C1N	K14	D3	差分数据输入位 D3 / Differential data input bit D3
D1	B1	差分数据输入位 B1 / Differential data input bit B1	L1	A1N	差分数据输入位 A1N / Differential data input bit A1N
D2	B2	差分数据输入位 B2 / Differential data input bit B2	L2	A2	差分数据输入位 A2 / Differential data input bit A2

引出端号 / Pin No.	符号 / Symbol	名称 / Name	引出端号 / Pin No.	符号 / Symbol	名称 / Name
D3	B2N	差分数据输入位 B2N / Differential data input bit B2N	L3	A2N	差分数据输入位 A2N / Differential data input bit A2N
D4	GNDD	数字地 / Digital ground	L4	GNDD	数字地 / Digital ground
D5	GNDD	数字地 / Digital ground	L5	Diode	芯片结温测试二极管 / Die junction-temperature test diode
D6	VCCD	3.3V 数字电源 / 3.3V digital supply	L6	VCCA5	5V 模拟电源 / 5V analog supply
D7	VCCD	3.3V 数字电源 / 3.3V digital supply	L7	VCCA5	5V 模拟电源 / 5V analog supply
D8	VCCD	3.3V 数字电源 / 3.3V digital supply	L8	VCCA5	5V 模拟电源 / 5V analog supply
D9	VCCD	3.3V 数字电源 / 3.3V digital supply	L9	VCCA5	5V 模拟电源 / 5V analog supply
D10	GNDD	数字地 / Digital ground	L10	GNDD	数字地 / Digital ground
D11	GNDD	数字地 / Digital ground	L11	MUX	多路复用（MUX）模式选择 / Multiplex (MUX) mode select
D12	C2N	差分数据输入位 C2N / Differential data input bit C2N	L12	D2N	差分数据输入位 D2N / Differential data input bit D2N
D13	C2	差分数据输入位 C2 / Differential data input bit C2	L13	D2	差分数据输入位 D2 / Differential data input bit D2
D14	C1	差分数据输入位 C1 / Differential data input bit C1	L14	D1N	差分数据输入位 D1N / Differential data input bit D1N
E1	A10N	差分数据输入位 A10N / Differential data input bit A10N	M1	A1	差分数据输入位 A1 / Differential data input bit A1
E2	B0	差分数据输入位 B0（最低位）/ Differential data input bit B0 (LSB)	M2	A0N	差分数据输入位 A0N（最低位）/ Differential data input bit A0N (LSB)
E3	B0N	差分数据输入位 B0N（最低位）/ Differential data input bit B0N (LSB)	M3	GA	增益调整 / Gain adjustment
E4	GNDD	数字地 / Digital ground	M4	HTVF	保持时间违反标志 / Hold-time violation flag
E5	GNDD	数字地 / Digital ground	M5	STVF	建立时间违反标志 / Setup-time violation flag
E6	VCCD	3.3V 数字电源 / 3.3V digital supply	M6	VCCA5	5V 模拟电源 / 5V analog supply
E7	VCCD	3.3V 数字电源 / 3.3V digital supply	M7	VCCA5	5V 模拟电源 / 5V analog supply
E8	VCCD	3.3V 数字电源 / 3.3V digital supply	M8	GNDA	模拟地 / Analog ground
E9	VCCD	3.3V 数字电源 / 3.3V digital supply	M9	GNDA	模拟地 / Analog ground
E10	GNDD	数字地 / Digital ground	M10	MODE0	DAC 模式选择位 0 / DAC mode select bit 0
E11	GNDD	数字地 / Digital ground	M11	MODE1	DAC 模式选择位 1 / DAC mode select bit 1
E12	C0N	差分数据输入位 C0N（最低位）/ Differential data input bit C0N (LSB)	M12	PSS2	输出数据时钟相位选择端 PSS2（最高位）/ Output data clock phase select terminal PSS2 (MSB)
E13	C0	差分数据输入位 C0（最低位）/ Differential data input bit C0 (LSB)	M13	D0N	差分数据输入位 D0N（最低位）/ Differential data input bit D0N (LSB)

引出端号 / Pin No.	符号 / Symbol	名称 / Name	引出端号 / Pin No.	符号 / Symbol	名称 / Name
E14	D10N	差分数据输入位 D10N / Differential data input bit D10N	M14	D1	差分数据输入位 D1 / Differential data input bit D1
F1	A10	差分数据输入位 A10 / Differential data input bit A10	N1	A0	差分数据输入位 A0（最低位）/ Differential data input bit A0 (LSB)
F2	A11	差分数据输入位 A11（最高位）/ Differential data input bit A11 (MSB)	N2	DSPN	数据时钟反相输出 / Data clock complementary output
F3	A11N	差分数据输入位 A11N（最高位）/ Differential data input bit A11N (MSB)	N3	IDC_P	数据时钟同相输入 / Data clock in-phase input
F4	VCCD	3.3V 数字电源 / 3.3V digital supply	N4	SYNCN	同步输入负端 / Sync input, negative
F5	VCCD	3.3V 数字电源 / 3.3V digital supply	N5	CLKN	DAC 采样时钟输入负 / DAC sampling clock input, negative
F6	GNDA	模拟地 / Analog ground	N6	GNDA	模拟地 / Analog ground
F7	GNDA	模拟地 / Analog ground	N7	GNDA	模拟地 / Analog ground
F8	GNDA	模拟地 / Analog ground	N8	GNDA	模拟地 / Analog ground
F9	GNDA	模拟地 / Analog ground	N9	GNDA	模拟地 / Analog ground
F10	VCCD	3.3V 数字电源 / 3.3V digital supply	N10	GNDA	模拟地 / Analog ground
F11	VCCD	3.3V 数字电源 / 3.3V digital supply	N11	GNDA	模拟地 / Analog ground
F12	D11N	差分数据输入位 D11N（最高位）/ Differential data input bit D11N (MSB)	N12	OCDS1	输出时钟分频选择位 1 / Output clock divider select bit 1
F13	D11	差分数据输入位 D11（最高位）/ Differential data input bit D11 (MSB)	N13	OCDS0	输出时钟分频选择位 0 / Output clock divider select bit 0
F14	D10	差分数据输入位 D10 / Differential data input bit D10	N14	D0	差分数据输入位 D0（最低位）/ Differential data input bit D0 (LSB)
G1	A8	差分数据输入位 A8 / Differential data input bit A8	P1	GNDD	数字地 / Digital ground
G2	A8N	差分数据输入位 A8N / Differential data input bit A8N	P2	DSP	数据时钟同相输出 / Data clock in-phase output
G3	A9	差分数据输入位 A9 / Differential data input bit A9	P3	IDC_N	数据时钟反相输入 / Data clock complementary input
G4	A9N	差分数据输入位 A9N / Differential data input bit A9N	P4	SYNC	同步输入正端 / Sync input, positive
G5	GNDD	数字地 / Digital ground	P5	CLK	DAC 采样时钟输入正 / DAC sampling clock input, positive
G6	GNDA	模拟地 / Analog ground	P6	GNDA	模拟地 / Analog ground
G7	GNDA	模拟地 / Analog ground	P7	GNDA	模拟地 / Analog ground
G8	GNDA	模拟地 / Analog ground	P8	GNDA	模拟地 / Analog ground
G9	GNDA	模拟地 / Analog ground	P9	OUT	

引出端号 / Pin No.	符号 / Symbol	名称 / Name	引出端号 / Pin No.	符号 / Symbol	名称 / Name
					DAC 电流同相输出 / DAC current in-phase output
G10	GNDD	数字地 / Digital ground	P10	OUTN	DAC 电流反相输出 / DAC current complementary output
G11	D9N	差分数据输入位 D9N / Differential data input bit D9N	P11	GNDA	模拟地 / Analog ground
G12	D9	差分数据输入位 D9 / Differential data input bit D9	P12	PSS0	输出数据时钟相位选择端 PSS0（最低位）/ Output data clock phase select terminal PSS0 (LSB)
G13	D8N	差分数据输入位 D8N / Differential data input bit D8N	P13	PSS1	输出数据时钟相位选择端 PSS1 / Output data clock phase select terminal PSS1
G14	D8	差分数据输入位 D8 / Differential data input bit D8	P14	GNDD	数字地 / Digital ground

推荐工作条件 / Recommended Operating Conditions

English: - Supply voltages: - VCCA5 = 4.75V~5.25V - VCCA3 = 3.15V~3.45V - VCCD = 3.15V~3.45V - LVDS digital input low voltage: 1.075V - LVDS digital input high voltage: 1.425V - Digital input differential swing: 350mVp - Clock input power (differential mode) PCLK: -4dBm~+8dBm - Control function input low voltage: 0V - Control function input high voltage: VCCD - Gain adjustment range (GA): 0~VCCA3 - Operating temperature range (TC): -55°C~125°C - Operating temperature range (TA): -55°C~99°C

中文： - 电源电压： - VCCA5=4.75V~5.25V - VCCA3=3.15V~3.45V - VCCD=3.15V~3.45V - LVDS 数字输入低电压：1.075V - LVDS 数字输入高电压：1.425V - 数字输入差分摆幅：350mVp - 时钟输入功率（差分模式）PCLK：-4dBm~+8dBm - 控制功能输入低电压：0V - 控制功能输入高电压：VCCD - 增益调整范围（GA）：0~VCCA3 - 工作温度范围（TC）：-55°C~125°C - 工作温度范围（TA）：-55°C~99°C

绝对最大额定值 / Absolute Maximum Ratings

English: - Supply voltages: - VCCA5 = -0.6V~+6.0V - VCCA3 = -0.6V~+4.0V - VCCD = -0.6V~+4.0V - Junction temperature: 150°C - Lead soldering temperature (10s): 300°C - Thermal resistance, junction-to-case (Rth(J-C)): 14°C/W

中文： - 电源电压： - VCCA5= -0.6V~ +6.0V - VCCA3= -0.6V~ +4.0V - VCCD= -0.6V~ +4.0V - 结温：150°C； - 引线耐焊接温度（10s）：300°C - 热阻，结到壳（Rth(J-C)）：14°C/W

性能指标 / Performance Specifications

表 1 电特性 / Table 1. Electrical Characteristics

参数名称 / Parameter	符号 / Symbol	条件 / Conditions	性能指标 / Specification — 最小值 / Min	性能指标 / Specification — 典型值 / Typ	性能指标 / Specification — 最大值 / Max	单位 / Unit
分辨率 / Resolution	RES			12		Bits
5V 模拟电源电流 / 5V analog supply current	ICCA5	4:1 MUX 模式 / 4:1 MUX mode	—	85.5	90	mA
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3		—	112.5	122	mA
3.3V 数字电源电流 / 3.3V digital supply current	ICCD		—	234.5	270	mA
功耗 / Power consumption	PW		—	1.56	1.8	W
5V 模拟电源电流 / 5V analog supply current	ICCA5	2:1 MUX 模式 / 2:1 MUX mode	—	85	90	mA
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3		—	112.5	122	mA
3.3V 数字电源电流 / 3.3V digital supply current	ICCD3		—	183.2	200	mA
功耗 / Power consumption	PW		—	1.39	1.6	W
数字差分输入电压 / Digital differential input voltage	VID		100	—	500	mVp
数字差分输入电阻 / Digital differential input resistance	RILVDS		80	113	130	Ω
时钟输入共模电压 / Clock input common-mode voltage	VICLKCM		2.3	2.45	2.6	V
时钟差分输入电阻 / Clock differential input resistance	RICLK		80	112.5	130	Ω
时钟差分输出电压 / Clock differential output voltage	VOD		240	391	450	mVp
满幅度差分输出电压 / Full-scale differential output voltage	VOUT		0.87	0.945	1.1	Vpp
模拟输出内部差分电阻 / Analog output	ROUT		90	107	120	Ω

参数名称 / Parameter	符号 / Symbol	条件 / Conditions	性能指标 / Specification — 最小值 / Min	性能指标 / Specification — 典型值 / Typ	性能指标 / Specification — 最大值 / Max	单位 / Unit
internal differential resistance						
差分非线性 / Differential nonlinearity	EDL		-4	-2.8～0.6	+4	LSB
积分非线性 / Integral nonlinearity	EL		-5	-3.0～2.8	+5	LSB
无杂散动态范围 / Spurious-free dynamic range	SFDR	非归零模式（NRZ）/ NRZ mode: fCLK=3Gsps，fout=100MHz，0dBFS，4:1 MUX	56	64	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	非归零模式（NRZ）/ NRZ mode: fCLK=3Gsps，fout=400MHz，0dBFS，4:1 MUX	54	59.5	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	窄归零模式（NRTZ）/ NRTZ mode: fCLK=3Gsps，fout=700MHz，0dBFS，4:1 MUX	52	58	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	窄归零模式（NRTZ）/ NRTZ mode: fCLK=1.5Gsps，fout=700MHz，0dBFS，2:1 MUX	45	52	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	归零模式（RTZ）/ RTZ mode: fCLK=3Gsps，fout=1600MHz，0dBFS，4:1 MUX	50	57	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	归零模式（RTZ）/ RTZ mode: fCLK=3Gsps，fout=2900MHz，0dBFS，4:1 MUX	42	49	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	混频模式（RF）/ RF mode: fCLK=3Gsps，fout=2900MHz，0dBFS，4:1 MUX	38	46	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	混频模式（RF）/ RF mode: fCLK=3Gsps，fout=3800MHz，0dBFS，4:1 MUX	37	46	—	dBc
最大转换速率 / Maximum conversion rate	fCLK	4:1 MUX 模式 / 4:1 MUX mode	3	3	—	GSPS
最大转换速率 / Maximum conversion rate	fCLK	2:1 MUX 模式 / 2:1 MUX mode	1.5	1.5	—	GSPS

参数名称 / Parameter	符号 / Symbol	条件 / Conditions	性能指标 / Specification — 最小值 / Min	性能指标 / Specification — 典型值 / Typ	性能指标 / Specification — 最大值 / Max	单位 / Unit
最大输入数据率 / Maximum input data rate	fDATA	4:1 MUX 模式 / 4:1 MUX mode	750	750	—	MSPS
最大输入数据率 / Maximum input data rate	fDATA	2:1 MUX 模式 / 2:1 MUX mode	750	750	—	MSPS

主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

English: 1. Spurious-free dynamic range of the 100MHz output signal in non-return-to-zero mode.

中文： 1、非归零模式下 100MHz 输出信号无杂散动态范围

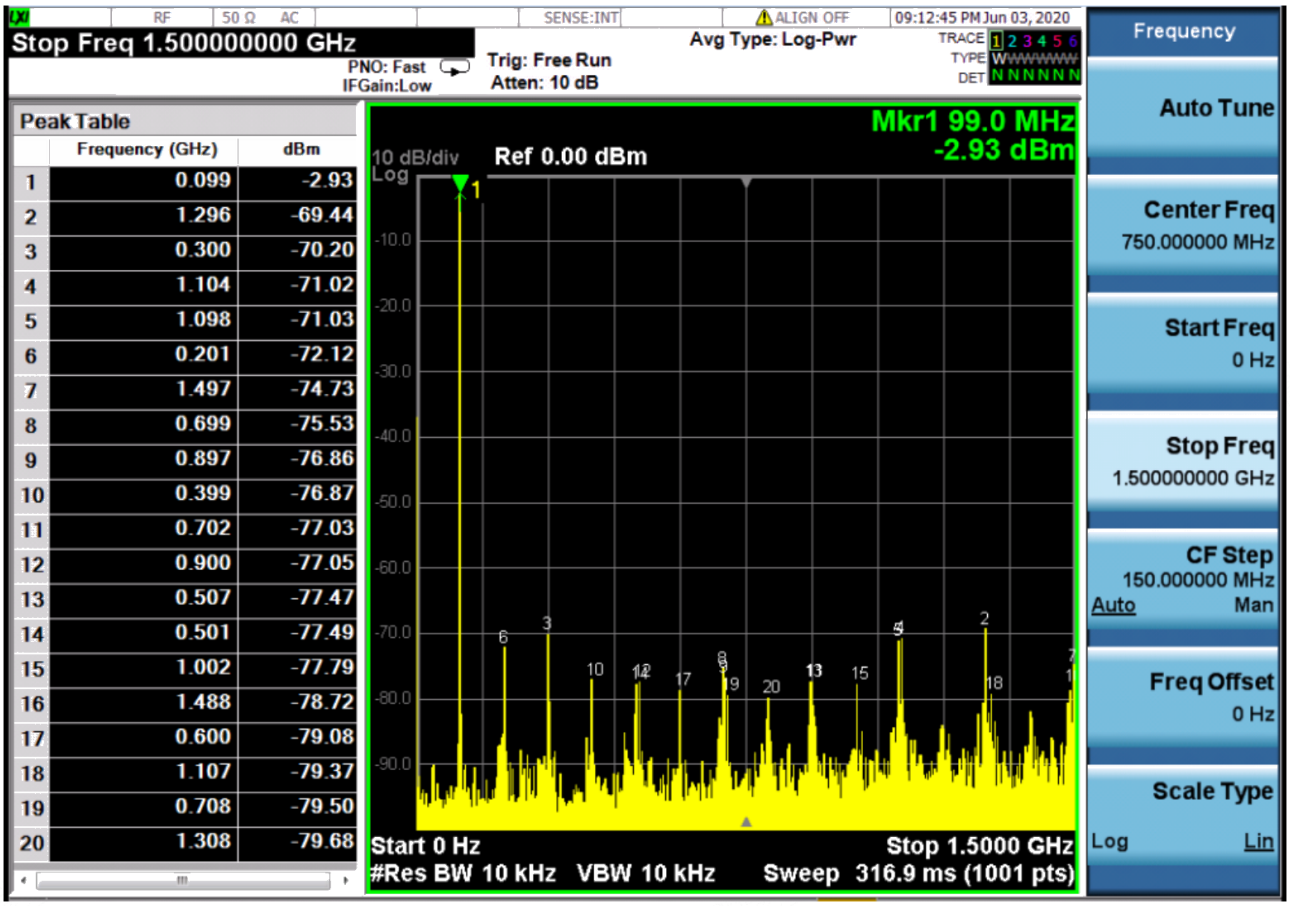
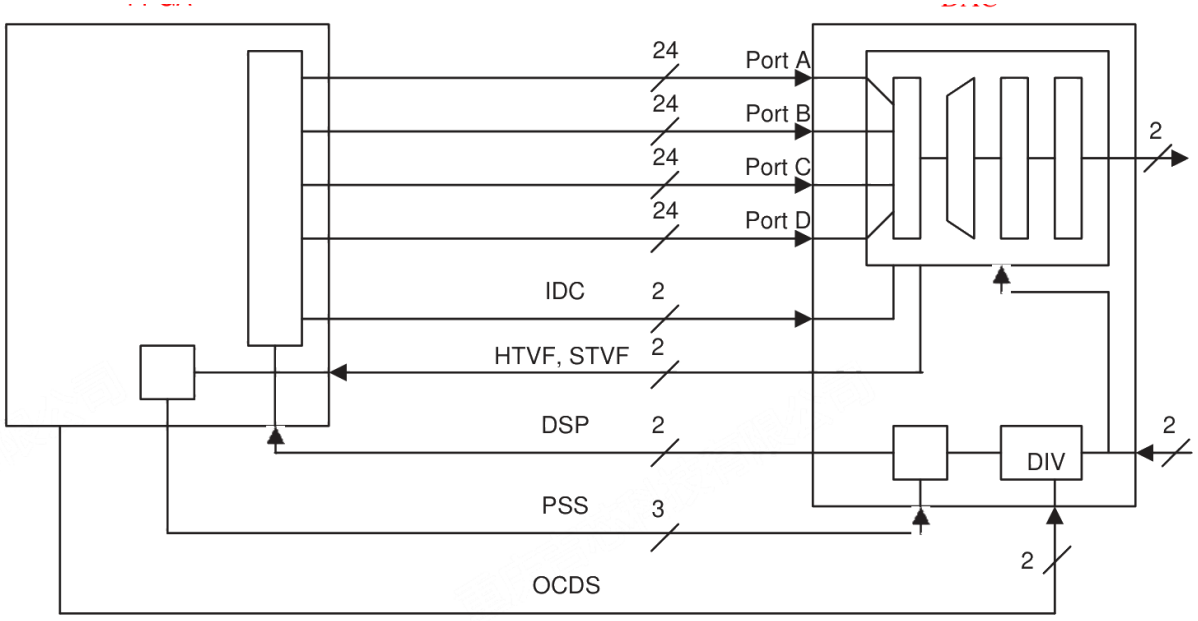


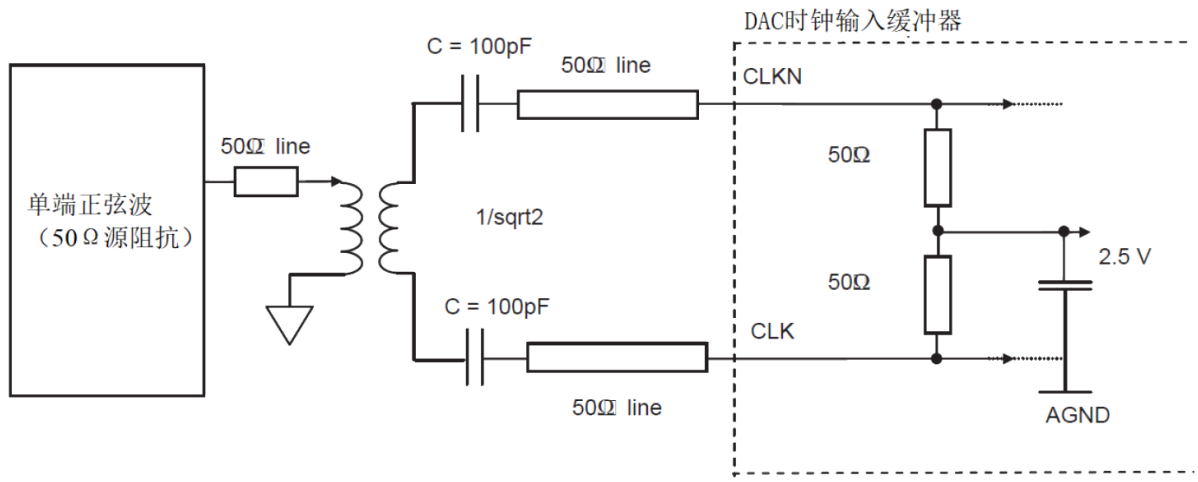
Figure 6: NRZ mode, fCLK=3Gsps, fOUT=100MHz, 0dBFS

典型应用线路图 / Typical Application Circuit

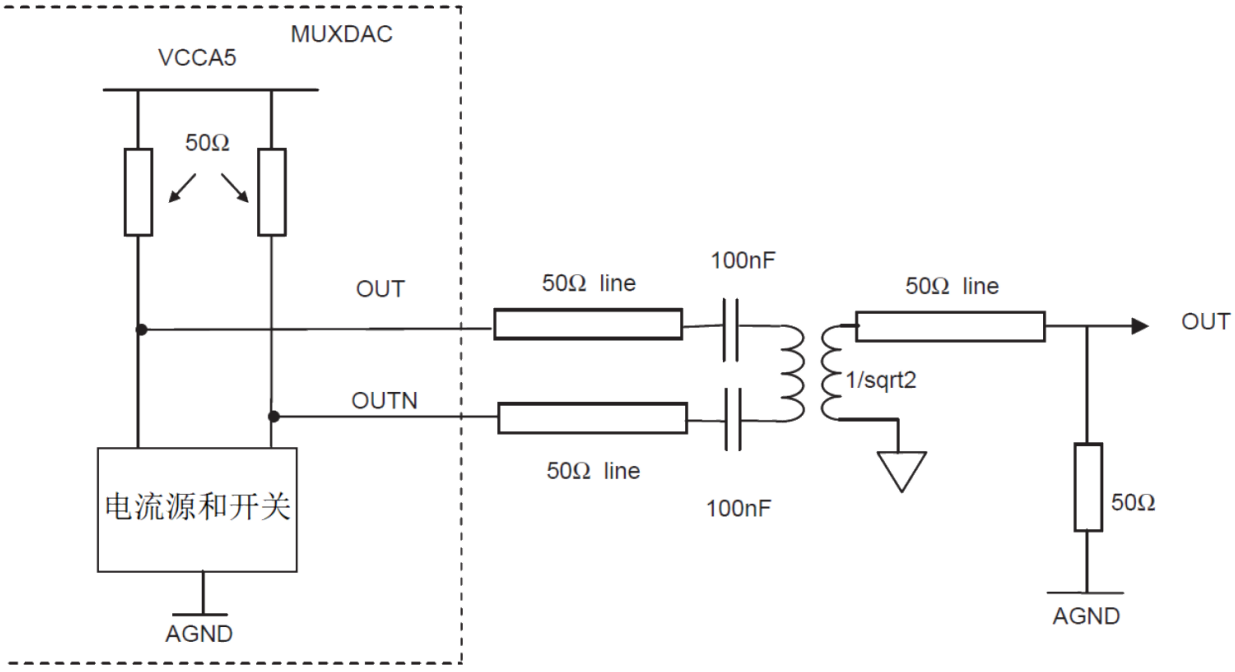
English: Figure 7 comprises: (a) data-port and FPGA application circuit; (b) clock input application circuit; (c) analog output application circuit; (d) MUX, MODE, PSS and OCDS control-signal configuration ; (e) gain-adjustment GA signal configuration.

中文： 图 7 包括：（a）数据端与 FPGA 应用线路图；（b）时钟输入端应用线路图；（c）模拟输出端应用线路图；（d）MUX、MODE、PSS 和 OCDS 控制信号配置（图内器件标注原为内部代号，成品图已按 SXD015 重绘）；（e）增益调节 GA 信号配置。





（b）时钟输入端应用线路图



（c）模拟输出端应用线路图

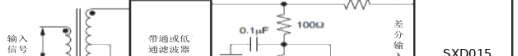


Figure 7: SXD015 typical application circuit

单元模块及工作原理 / Functional Blocks and Operating Principles

1. 几种输出模式的说明 / 1. Output Modes

a. 非归零（NRZ）输出模式 / a. Non-Return-to-Zero (NRZ) Output Mode

English: This mode operates in the 1st Nyquist zone, with less overall attenuation than the return-to-zero (RTZ) mode. However, due to the sin(x)/x gain roll-off, operation in the 2nd Nyquist zone is not recommended.

中文： 这种模式工作在 1st Nyquist 区，总体衰减比归零（RTZ）模式小。但由于 sin(x)/x 的增益滚降，不建议在 2st Nyquist 区工作。

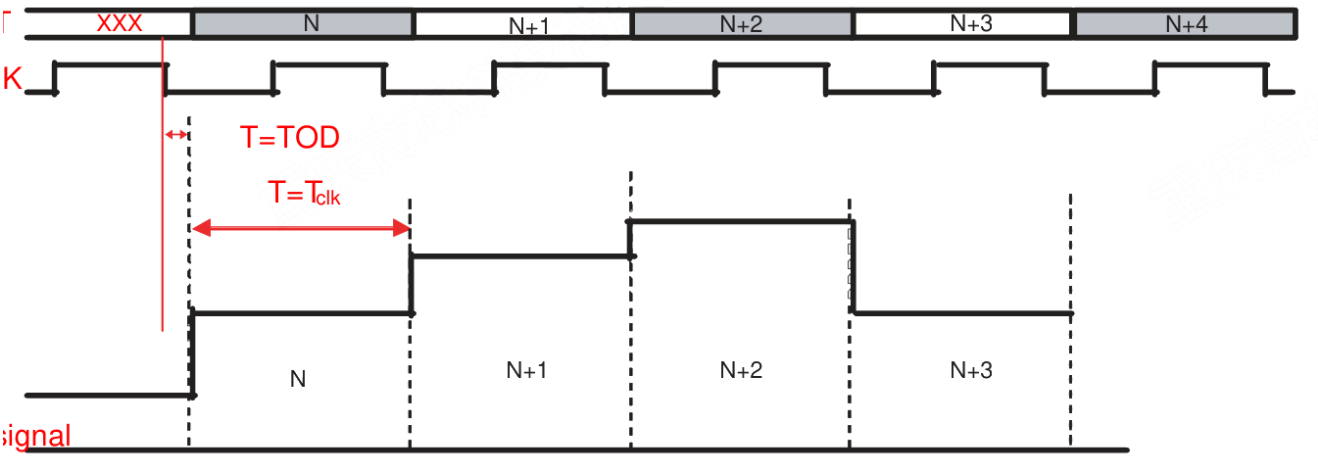


Figure 8: Non-return-to-zero mode timing diagram

b. 窄归零（NRTZ）输出模式 / b. Narrow Return-to-Zero (NRTZ) Output Mode

English: This mode has the following advantages: - Optimizes the fundamental power in the 1st Nyquist zone and the beginning of the 2nd Nyquist zone. - Improves dynamic performance. - Improves noise-floor performance. - Is a compromise between the NRZ and RTZ modes.

中文： 这种模式有以下一些优点： - 优化了 1st Nyquist 区和 2nd Nyquist 区开始部分基波功率。 - 提升了动态性能。 - 改善了噪底性能。 - 是 NRZ 和 RTZ 两种模式之间的折中。

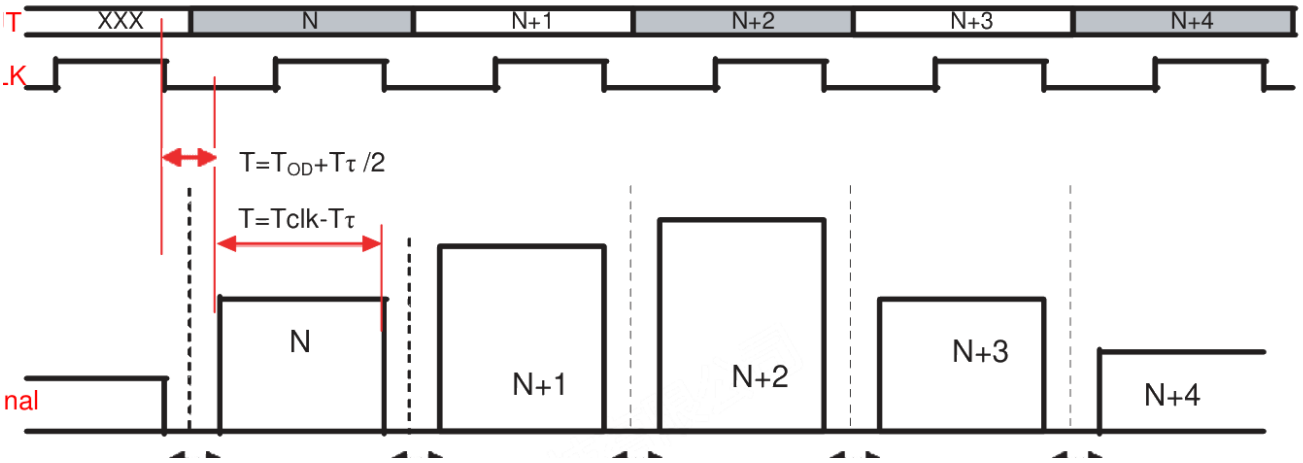


Figure 9: Narrow return-to-zero mode timing diagram

c. 归零（RTZ）输出模式 / c. Return-to-Zero (RTZ) Output Mode

English: In return-to-zero mode, the circuit can operate in the 2nd Nyquist zone, but the disadvantage is greater attenuation than in the 1st Nyquist zone. Advantages are as follows: - Sinc-function roll-off. - Improved dynamic performance.

中文： 归零模式下，电路可以工作在 2nd Nyquist 区工作，但缺点是衰减比 1st Nyquist 区大。优点如下： - Sinc 函数滚降。 - 改善动态性能。

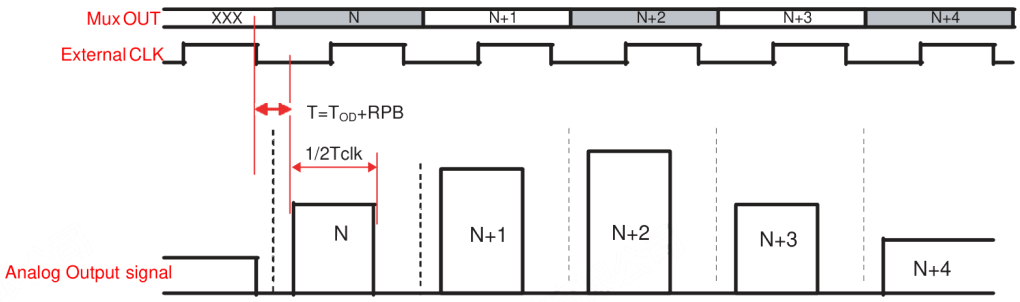


Figure 10: Return-to-zero mode timing diagram

d. 混频（RF）模式 / d. Mixing (RF) Mode

English: The advantage of RF mode is that it can output relatively high-frequency signals, with less attenuation in the 2nd Nyquist zone than RTZ mode. Unlike NRZ and RTZ modes, RF mode has large attenuation near DC and 2N*fCLK, but very small attenuation at fout=fCLK. Advantages are as follows: - Suitable for operation in the 2nd and 3rd Nyquist zones. - Extrapolated dynamic envelope curve; the spectrum does not degrade abruptly at fCLK.

中文： RF 模式的优点是可以输出比较高的频率信号，在 2nd Nyquist 区衰减比 RTZ 模式小。和 NRZ 及 RTZ 模式不同，RF 模式在 DC 和 2N*fCLK 附近衰减很大，但在 fout=fCLK 处衰减很小。优点如下： - 适合工作于 2nd 和 3rd Nyquist 区。 - 外推动态包络曲线，fCLK 处频谱不会陡然变差。

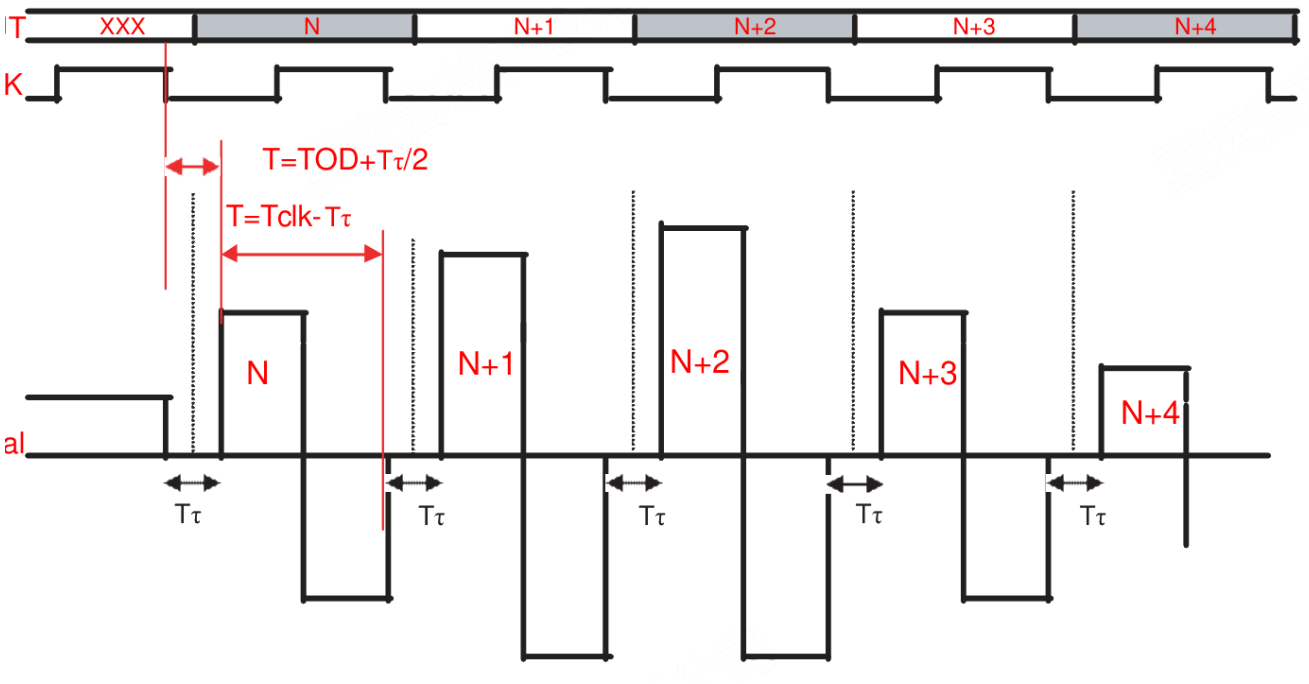


Figure 11: Mixing mode timing diagram

2. 相移选择功能（PSS）/ 2. Phase Shift Select (PSS)

English: This circuit can adjust the phase relationship between the input sampling clock (CLK) and the DSP output clock. The DSP clock output phase can be adjusted over a range of 3.5 input clock (CLK) cycles, in steps of 0.5 input clock (CLK) cycle. The three-bit SPI control code word PSS[2:0] can be used for the phase selection function.

By changing the 0s and 1s of these three bits, the DSP clock delay can be changed, thereby synchronizing the DAC input data with the sampling clock (the DSP clock can be provided to the FPGA for generating the DAC input data).

中文： 本电路可以调整输入采样时钟（CLK）和 DSP 输出时钟之间的相位关系。DSP 时钟输出相位可以在 3.5 个输入时钟（CLK）周期范围内进行调节，每步 0.5 个输入时钟（CLK）周期。三位 SPI 控制码字 PSS[2:0] 可用于相位选择功能。

通过改变此三位 0 或 1 可以改变 DSP 时钟延迟，从而可以同步 DAC 输入数据和采样时钟（DSP 时钟可提供给 FPGA 用于产生 DAC 输入数据）。

表 2 PSS[2:0] 码值表 / Table 2. PSS[2:0] Code Values

符号 / Symbol	数值 / Value	含义 / Meaning
PSS[2:0]	000	DSP 输出没有延迟 / No DSP output delay
PSS[2:0]	001	DSP 输出延迟 0.5 个主时钟周期 / DSP output delayed by 0.5 main clock cycle
PSS[2:0]	010	DSP 输出延迟 1 个主时钟周期 / DSP output delayed by 1 main clock cycle
PSS[2:0]	011	DSP 输出延迟 1.5 个主时钟周期 / DSP output delayed by 1.5 main clock cycles
PSS[2:0]	100	DSP 输出延迟 2.0 个主时钟周期 / DSP output delayed by 2.0 main clock cycles
PSS[2:0]	101	DSP 输出延迟 2.5 个主时钟周期 / DSP output delayed by 2.5 main clock cycles

符号 / Symbol	数值 / Value	含义 / Meaning
PSS[2:0]	110	DSP 输出延迟 3.0 个主时钟周期 / DSP output delayed by 3.0 main clock cycles
PSS[2:0]	111	DSP 输出延迟 3.5 个主时钟周期 / DSP output delayed by 3.5 main clock cycles

English: To ensure synchronization between the sampling clock and the input data, the HTVF and STVF signals can be monitored to determine how many steps the DSP clock needs to be delayed.

Note: In 4:1 MUX mode, all 8 settings are meaningful; in 2:1 MUX mode, only the first 4 settings are meaningful, and the last four settings produce the same result.

中文： 为了确保采样时钟与输入数据间同步，可以通过监控 HTVF 和 STVF 信号确定 DSP 时钟需要延迟多少步。

注：在 4:1 MUX 模式，8 个设置均有意义；在 2:1 MUX 模式，只有前 4 个设置有意义，后面四个设置产生相同的结果。

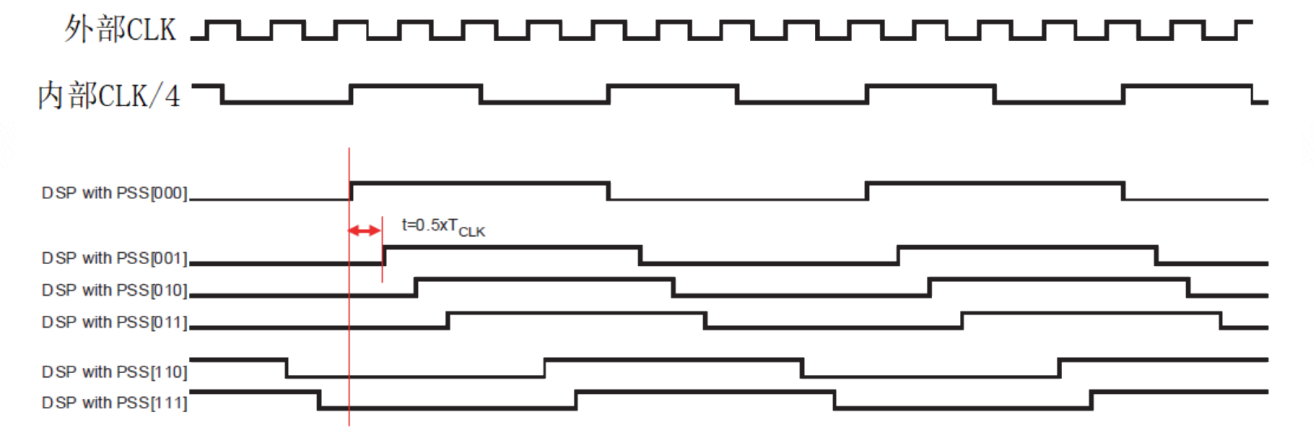


Figure 12: PSS timing diagram (4:1 MUX, OCDS=00)

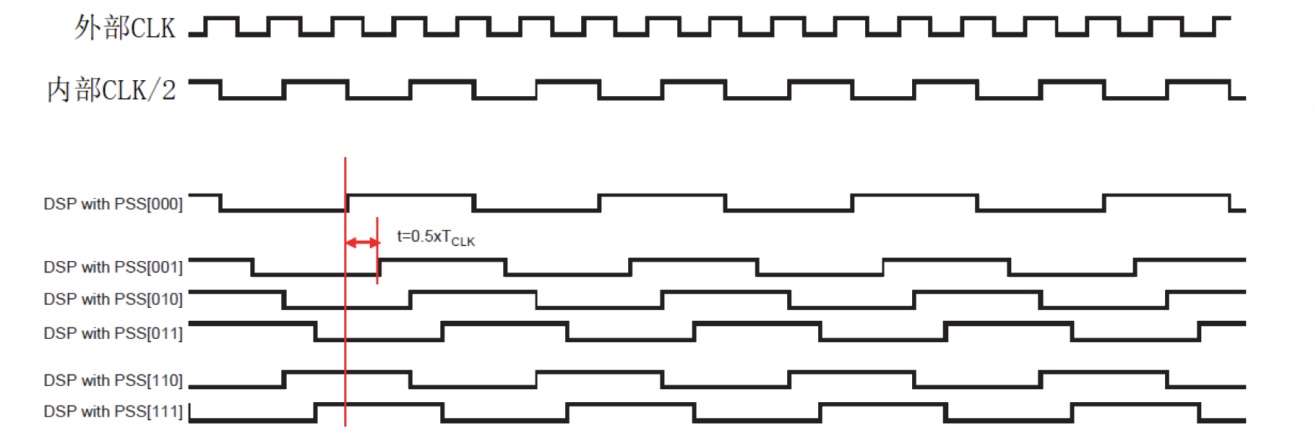


Figure 13: PSS timing diagram (2:1 MUX, OCDS=00)

3. 输出时钟分频选择功能（OCDS）/ 3. Output Clock Divider Select (OCDS)

English: The internal DSP clock division ratio can be adjusted to 1 or 2. Configuring this value changes the DSP clock frequency, as shown in the table below.

When the FPGA receiving the DSP clock requires a sufficiently low frequency, the OCDS function allows the FPGA to avoid dividing the DSP clock, thereby avoiding the phase uncertainty of FPGA division. In this case, the phase of the FPGA internal clock is the phase of the DSP clock. When a system uses multiple DACs and multiple FPGAs, after all DACs are synchronized, the OCDS function makes it easier to ensure a deterministic phase relationship among all FPGAs.

中文： DSP 内部时钟分频比可以调整为 1 或 2。通过这个值得配置 DSP 时钟频率会有变化，具体如下表所示。

当 FPGA 接收 DSP 时钟要求频率足够低时，使用 OCDS 功能可以让 FPGA 不需要对 DSP 时钟进行分频，从而避免了 FPGA 分频相位的不确定性。这种情况下 FPGA 内部时钟的相位就是 DSP 时钟的相位。当一个系统使用多个 DAC 和多个 FPGA 时，在同步所有 DAC 后，OCDS 功能可以更容易确保所有 FPGA 之间确定的相位关系。

表 3 OCDS 码值表 / Table 3. OCDS Code Values

符号 / Symbol	数值 / Value	含义 / Meaning
OCDS[1:0]	00	DSP 时钟频率 = fCLK/(2N) / DSP clock frequency = fCLK/(2N)
OCDS[1:0]	01	DSP 时钟频率 = fCLK/(2N2) / DSP clock frequency = fCLK/(2N2)
OCDS[1:0]	10	无意义 / Not meaningful
OCDS[1:0]	11	无意义 / Not meaningful

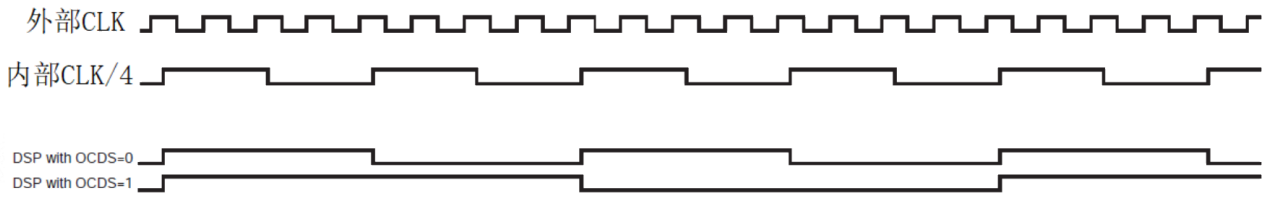


Figure 14: OCDS timing diagram (4:1 MUX)

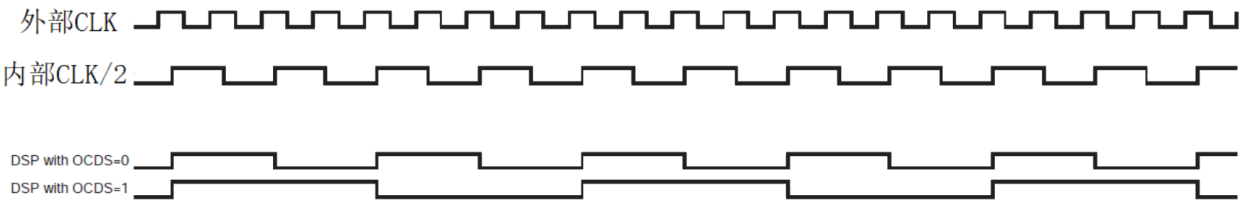


Figure 15: OCDS timing diagram (2:1 MUX)

4. FPGA 与 DAC 的同步：IDC_P、IDC_N、HTVF 和 STVF 功能 / 4. FPGA–DAC Synchronization: IDC_P, IDC_N, HTVF and STVF

English: - IDC_P, IDC_N: input data check function (LVDS signals). - HTVF: hold-time violation flag (3.3V CMOS signal). - STVF: setup-time violation flag (3.3V CMOS signal).

The IDC_P and IDC_N signals are LVDS signals; this pair of signals is synchronized with the other data bits and toggles every data cycle. This pair of signals shall be generated by the FPGA, so that the DAC can check in real time whether the timing between the FPGA and the DAC is synchronized. Synchronization information can be indicated by the TVF flags. The IDC signal routing should be consistent with the other

data signals (same layout rules and same length). When not used, the IDC signals should be set to an LVDS low or high level.

中文： - IDC_P, IDC_N：输入数据检查功能（LVDS 信号）。 - HTVF：保持时间违反标志。（3.3V 的 CMOS 信号）。 - STVF：建立时间违反标志。（3.3V 的 CMOS 信号）。

IDC_P, IDC_N 信号是 LVDS 信号，这对信号与其它数据位同步，并且每个数据周期都翻转。这对信号应由 FPGA 产生，从而 DAC 可以实时检查 FPGA 与 DAC 之间时序是否同步。是否同步信息可以通过 TVF 标志表征。IDC 信号布线方式应该与其它数据信号保持一致（相同版图规则和相同长度）。当不使用时，IDC 信号应设置为 LVDS 低或高电平。

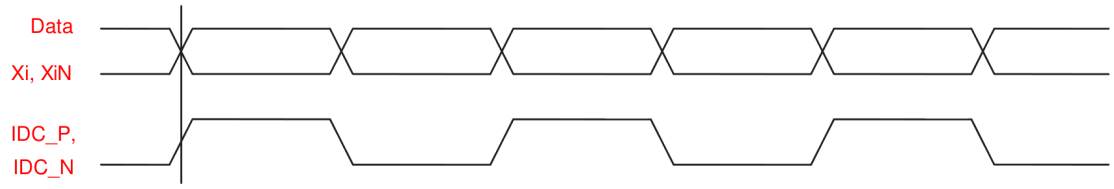


Figure 16: Timing diagram between IDC and input data

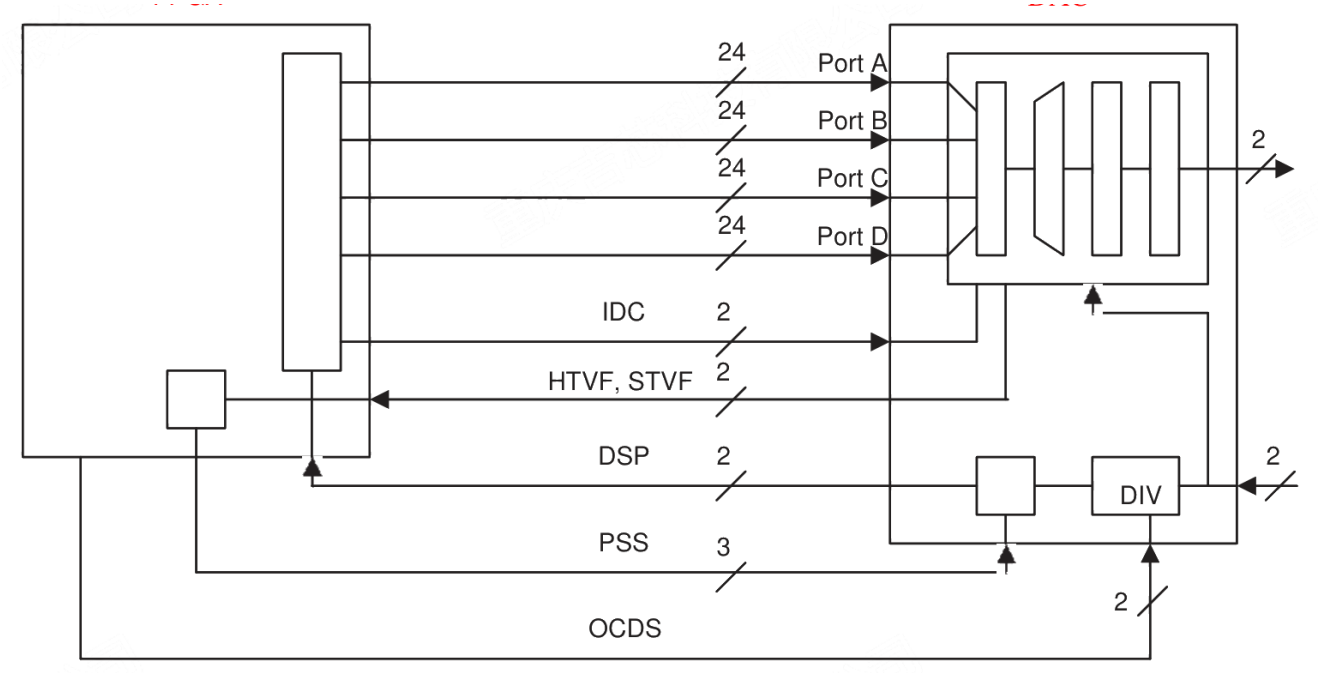


Figure 17: Logic diagram between FPGA and DAC

表 4 TVF 信号码值表 / Table 4. TVF Signal Code Values

符号 / Symbol	数值 / Value	含义 / Meaning
HTVF	0	时序同步正常 / Timing synchronization normal
HTVF	1	检测到数据保持时间违反 / Data hold-time violation detected
STVF	0	时序同步正常 / Timing synchronization normal
STVF	1	检测到数据建立时间违反 / Data setup-time violation detected

English: The data-accompanying clock (IDC_P, IDC_N) is sampled 3 times; the isolation between these 3 samples is half a main clock cycle. The 3 sampling results are compared, and then it is judged whether there is a timing violation. - STVF high: setup-time violation. - HTVF high: hold-time violation.

When the HTVF or STVF signal is 1, one of the following measures is recommended: - Move the DSP output clock timing (via the PSS function). - Move the phase of the clock generated by the FPGA PLL, thereby changing the input data phase.

中文： 数据随路时钟（IDC_P，IDC_N）会被采样 3 次，这 3 次采样之间的隔离是半个主时钟周期，3 个采样结果会被对比，然后判断时序是否有违例。 - STVF 是高电平：建立时间违例。 - HTVF 是高电平：保持时间违例。

当 HTVF 或 STVF 信号为 1 时，建议采用以下任一种措施： - 移动 DSP 输出时钟时序（可以通过 PSS 功能）。 - 移动 FPGA PLL 产生时钟相位，从而改变输入数据相位。

5. OCDS、MUX 组合 / 5. OCDS and MUX Combinations

表 5 OCDS、MUX、PSS 组合表 / Table 5. OCDS, MUX and PSS Combinations

MUX 引脚 / MUX Pin	模式 / Mode	OCDS	fDSP	PSS Range	Data Rate
0	4:1	00	fDSP=fCLK/8	总共 7 步（单步长 0.5 个主时钟周期）/ 7 steps in total (single step 0.5 main clock cycle)	fCLK/4
0	4:1	01	fDSP=fCLK/16	同上 / As above	fCLK/4
0	4:1	10	无意义 / Not meaningful		
0	4:1	11	无意义 / Not meaningful		
1	2:1	00	fDSP=fCLK/4	总共 7 步（单步长 0.5 个主时钟周期）/ 7 steps in total (single step 0.5 main clock cycle)	fCLK/2
1	2:1	01	fDSP=fCLK/8	同上 / As above	fCLK/2
1	2:1	10	无意义 / Not meaningful		
1	2:1	11	无意义 / Not meaningful		

6. 多芯片同步 / 6. Multi-Chip Synchronization

English: To achieve multi-chip synchronization, a SYNC synchronization operation needs to be generated.

When a pulse signal is applied to the SYNC/SYNCN input, the DSP clock signal stops for a determinable period of time, and then the DSP clock restarts. The SYNC signal needs to be synchronized with the main clock signal, and its length is an integer multiple of the main clock cycle.

中文： 为了实现多芯片同步，需要产生一个 SYNC 同步操作。

当一个脉冲信号应用到 SYNC/SYNCN 输入后，DSP 时钟信号会停止一段可确定的时间，然后 DSP 时钟重启。SYNC 信号需要和主时钟信号同步，并且长度是主时钟周期的整数倍。

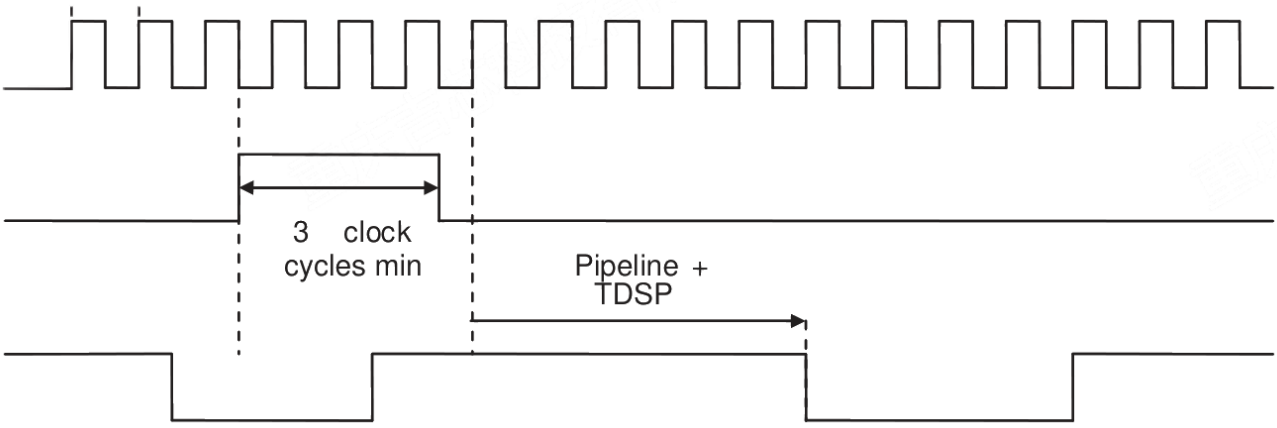


Figure 18: Synchronous reset timing diagram (4:1 MUX)

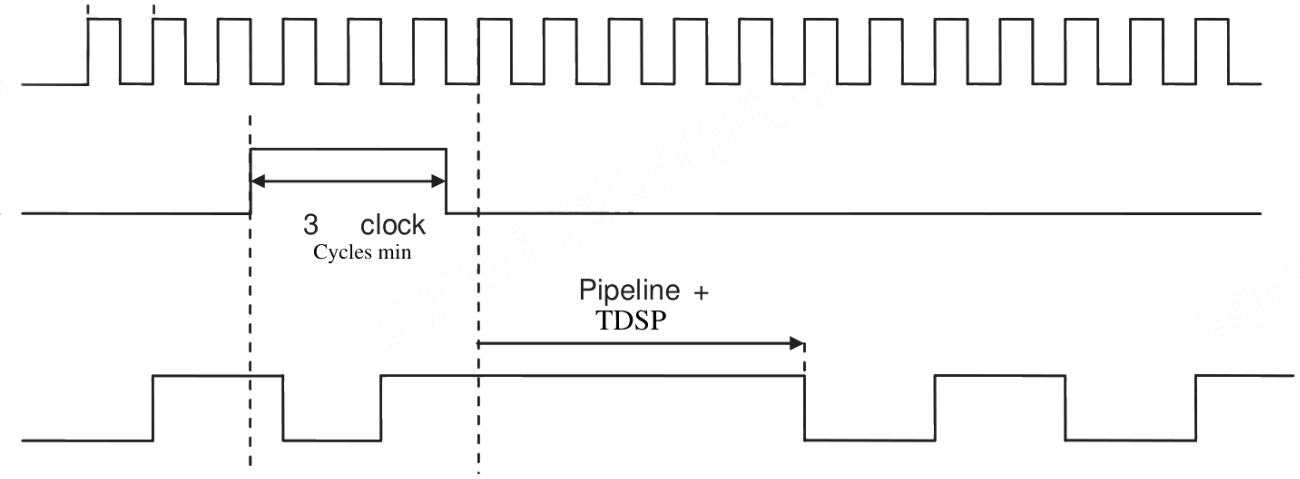


Figure 19: Synchronous reset timing diagram (2:1 MUX)

7. 增益调节功能 / 7. Gain Adjustment

English: This function is used to adjust the output gain of the DAC, with an adjustment range of output voltage × (1±11%). The adjustment voltage range of the GA port is 0~VCCA3. When GA=0, the output gain is maximum; when GA=VCCA3, the output gain is minimum.

中文： 这个功能用于调节 DAC 的输出增益，调节范围为输出电压*（1±11%）。GA 端口的调节电压范围是 0~VCCA3。当 GA=0 时，输出增益最大；当 GA=VCCA3 时，输出增益最小。

8. 端口信息 / 8. Port Information

8.1 模拟输出端口 / 8.1 Analog Output Port

English: The analog output needs to use a differential form, as shown in the figure below. If a single-ended signal output is needed in the application, a differential-to-single-ended balun needs to be used.

中文： 模拟输出需要使用差分形式，具体方式如下图所示。如果应用中需要输出单端信号，则需要使用差分转单端的 balun。

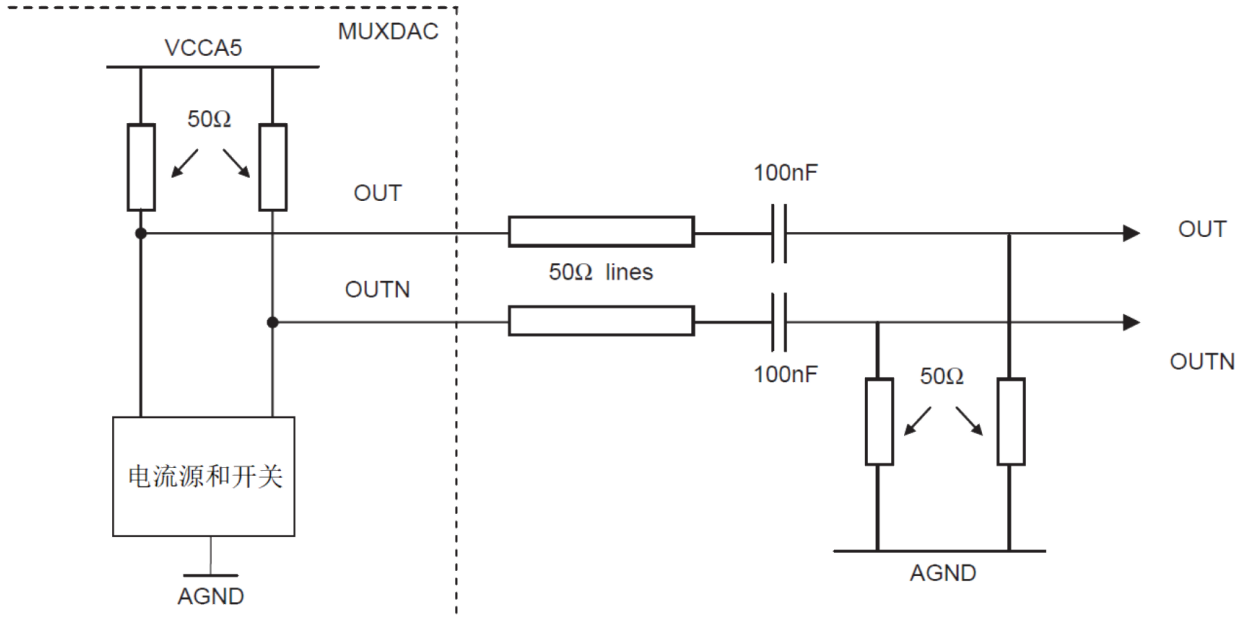


Figure 20: Differential analog output connection

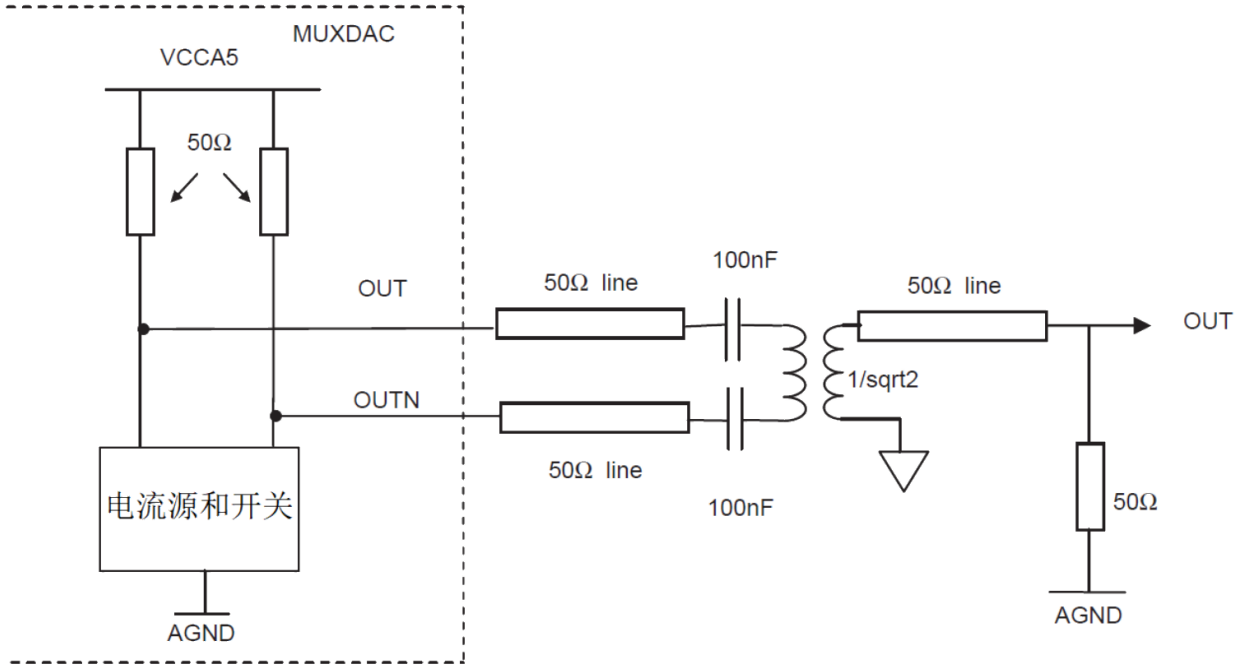


Figure 21: Analog output differential termination using a 1/2 transformer

注释：根据应用的需要，选取合适的耦合电容。/ Note: select a suitable coupling capacitor according to the needs of the application.

8.2 时钟端口 / 8.2 Clock Port

English: The clock input should use differential mode.

Note: the on-chip clock buffer self-bias voltage is approximately 2.5V.

中文： 时钟输入应该使用差分模式。

注：片内时钟缓冲器自偏置电压约 2.5V。

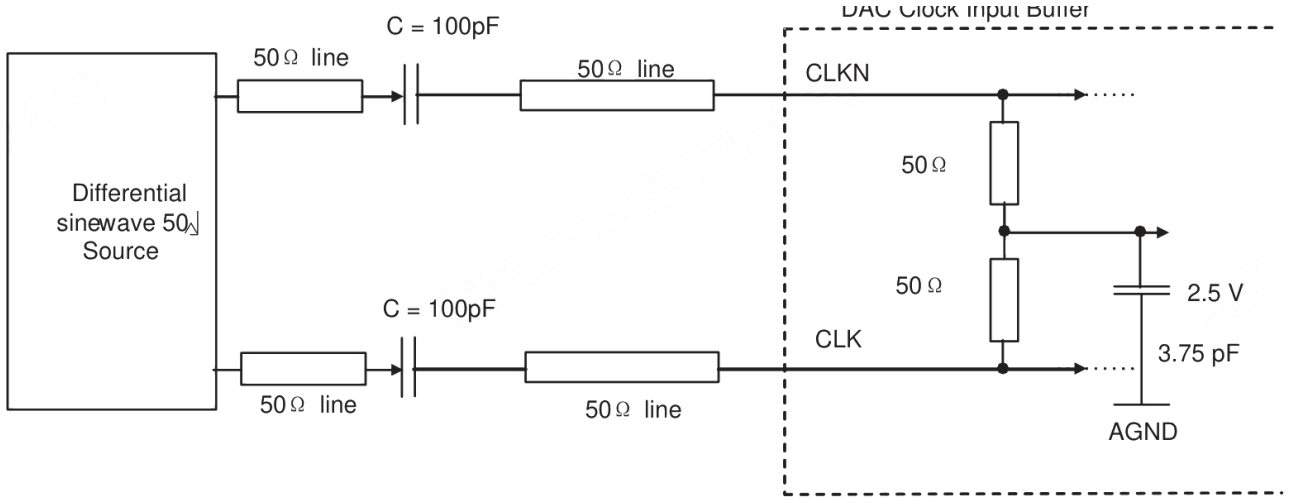


Figure 22: Differential clock connection

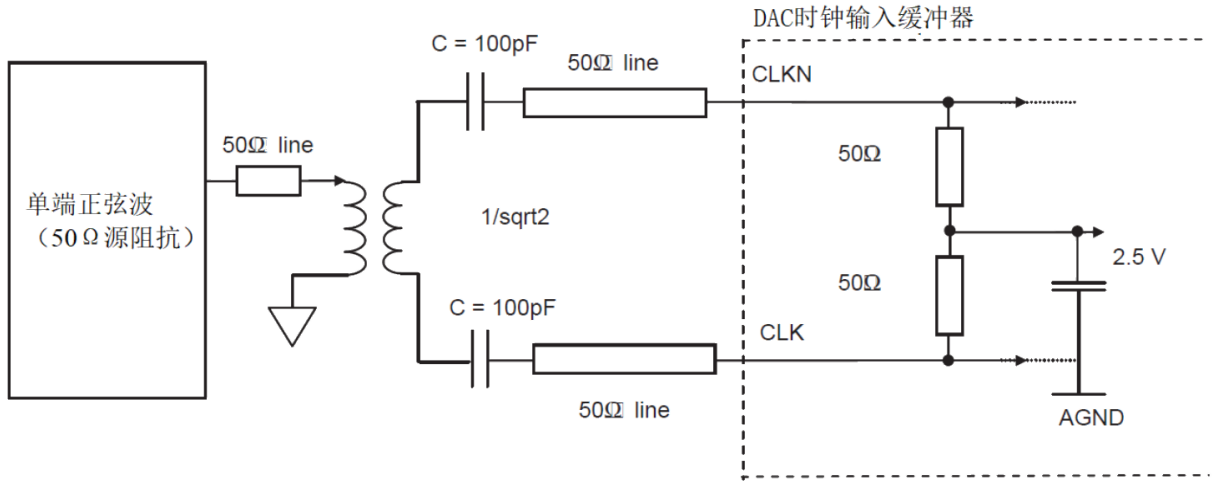


Figure 23: Differential clock connection with transformer

8.3 DATA、SYNC 和 IDC 输入端口 / 8.3 DATA, SYNC and IDC Input Ports

English: All three signals have on-chip LVDS buffers; the buffer structure is shown in the figure below.

Notes: 1. When only two ports are used (2:1 MUX), the unused data ports should be left floating. 2. DATA and IDC signals use the same routing rules, and their lengths also need to be the same. 3. When SYNC is not used, it is recommended to connect SYNC to 1.1V and SYNCN to 1.4V.

中文： 三种信号片内都有 LVDS 缓冲器，缓冲器结构如下图所示。

注： 1. 在仅使用两路端口的情况下（2:1 MUX），未使用的数据端口应悬空。 2. DATA 和 IDC 信号使用同样的布线规则，长度也需要一样。 3. SYNC 不使用时，建议 SYNC 接 1.1V、SYNCN 接 1.4V。

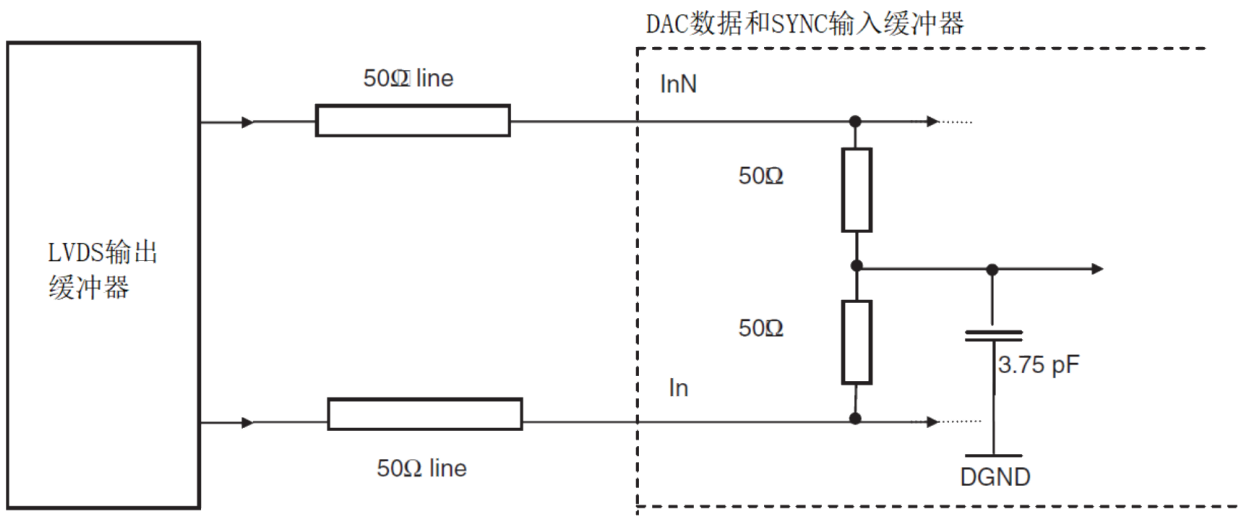


Figure 24: DATA, SYNC and IDC signal termination

8.4 DSP 时钟端口 / 8.4 DSP Clock Port

English: The DSP and DSPN output clock signals are in LVDS format. An external 100Ω differential termination resistor is required.

中文： DSP，DSPN 输出时钟信号是 LVDS 格式的。外部需要端接 100Ω 差分电阻。

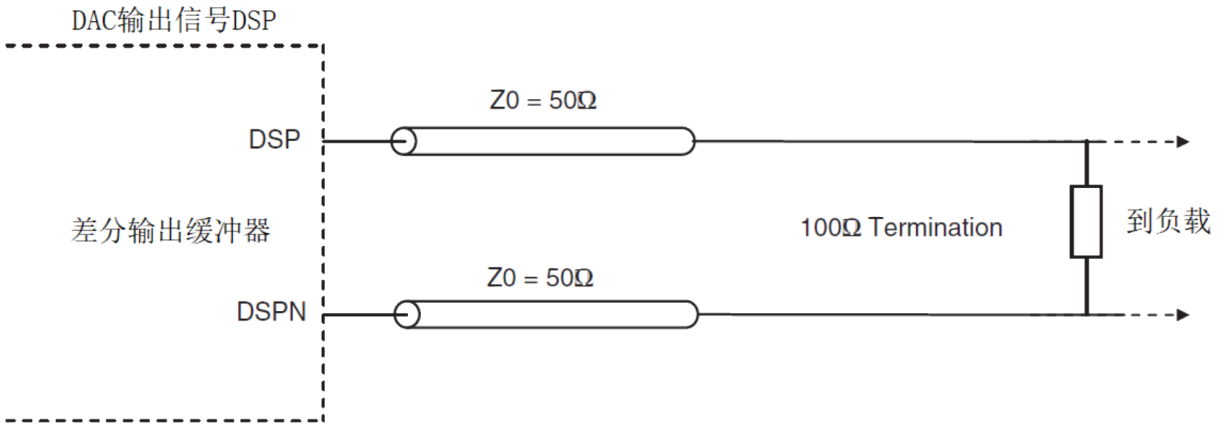


Figure 25: DSP port connection

8.5 控制信号配置 / 8.5 Control Signal Configuration

English: The MUX, MODE, PSS and OCDS control signals use the same input buffer. - Logic "1": 200KΩ to ground, or connected to a place at VCCD = 3.3V, or left floating. - Logic "0": 10Ω to ground.

Control signals driven by the FPGA: - Logic "1" > VIH or VCCD = 3.3V - Logic "0" < VIL or equal to 0V

中文： MUX、MODE、PSS 和 OCDS 控制信号使用同样的输入 buffer。 - Logic "1"：200 KΩ 接地，或者连接到 VCCD =3.3V 的地方，或者保持悬空 - Logic "0"：10Ω 接地

控制信号由 FPGA 驱动： - Logic "1" > VIH 或者 VCCD = 3.3V - Logic "0" < VIL 或者等于 0V

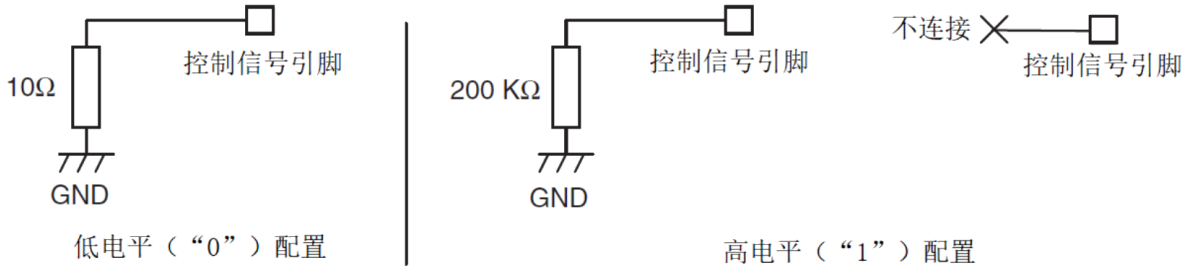


Figure 26: Control signal configuration



Figure 27: Control signals configured via FPGA

8.6 HTVF 和 STVF 控制信号 / 8.6 HTVF and STVF Control Signals

English: HTVF and STVF are 3.3V CMOS output signals; the FPGA can capture these signals.

To change the VOL/VOH values, pull-up/pull-down resistors or a potentiometer need to be used.

中文： HTVF 和 STVF 是 3.3V 的 CMOS 输出信号，FPGA 可以捕获该信号。

为了改变 VOL/VOH 的值，需要使用上拉/下拉电阻或电位器。

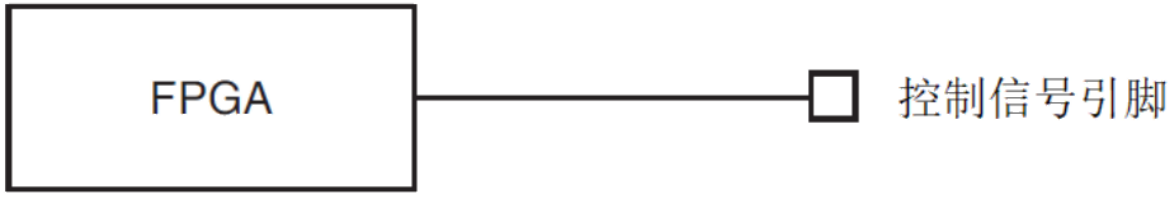


Figure 28: Control signals configured via FPGA

8.7 增益调节 GA 信号 / 8.7 Gain Adjustment GA Signal

English: Applying a voltage of 0~VCCA3 to the GA pin can change the internal gain of the DAC. The FPGA or MCU can generate the analog input control voltage GA signal by controlling a DAC.

中文： GA 引脚应用一个 0~VCCA3 的电压可以改变 DAC 内部增益。FPGA 或 MCU 通过控制一个 DAC 就可以产生模拟输入控制电压 GA 信号。



Figure 29: Control signal GA generation

9. 电源及解耦电容 / 9. Power Supplies and Decoupling Capacitors

English: The DAC requires 3 different power supplies: VCCA5=5V (for the analog core), VCCA3=3.3V (for the analog section), and VCCD=3.3V (for the digital section).

When configuring power-to-ground decoupling, the capacitors need to be as close to the chip as possible, using 100pF capacitors in parallel with 10nF capacitors. The minimum number of decoupling capacitors required can be calculated from the number of adjacent pins.

For the VCCA5 supply, 4 pairs of 100pF-in-parallel-with-10nF capacitors are needed; VCCA3 needs 4 pairs of the above capacitors; VCCD needs 10 pairs of the above capacitors.

Each supply rail needs decoupling capacitors as close as possible; one possible value is 100nF in parallel with 22uF (the more precise value depends on the DC/DC regulator).

中文： DAC 需要 3 种不同的电源：VCCA5=5V（用于模拟核）、VCCA3=3.3V（用于模拟部分）和 VCCD=3.3V（用于数字部分）。

当配置电源到地解耦电源时，电容需要尽可能地靠近芯片，使用 100pF 并联 10nF 的电容器。可以通过临近的 Pin 脚数量来计算所需要的最少解耦电容数量。对 VCCA5 电源而言，需要 4 对 100pF 并联 10nF 的电容器，VCCA3 需要 4 对上述电容，VCCD 需要 10 对上述电容。

每一路电源都需要尽可能近的设置解耦电容，一个可能的值是 100nF 和 22uF 并联的电容器（更精确的取值取决于 DC/DC 调整器）。

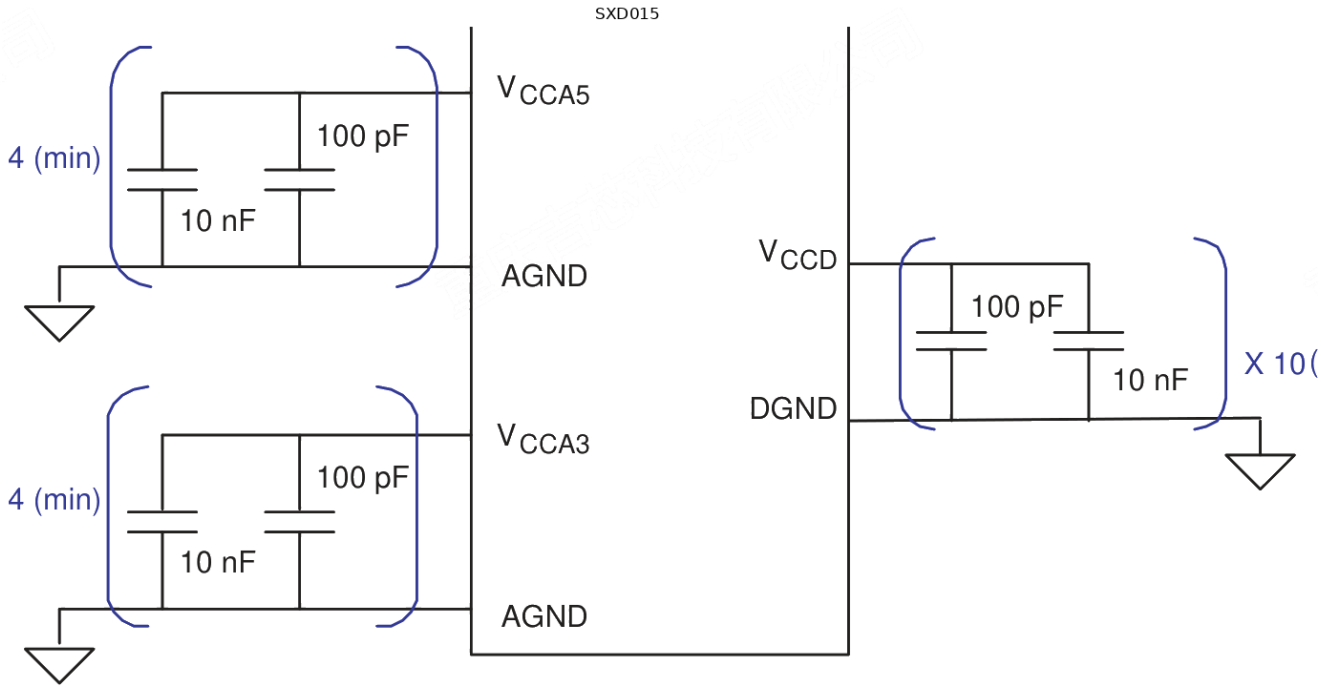


Figure 30: Decoupling capacitor configuration

10. 上电/断电要求 / 10. Power-Up / Power-Down Requirements

English: During power-up of this circuit's supplies VCCA3 and VCCD, the maximum voltage difference between the two supplies is required to be ≤1.2V, as shown in Figure 32. To meet this requirement, the following supply methods are recommended for VCCA3 and VCCD: - Use the same LDO to power up VCCA3 and VCCD simultaneously, with the two supplies isolated from each other by ferrite beads; - Use two LDOs of the same model to supply VCCA3 and VCCD separately and independently. The two LDOs have the same power-up time setting (i.e., soft start), the same enable signal, and the same input supply.

If VCCA3 and VCCD do not use the above supply methods, the maximum voltage difference between the two supplies is still required to be ≤1.2V.

This circuit has no specific power-down requirements.

中文： 本电路电源 VCCA3 和 VCCD 在上电过程中，要求两个电源间最大电压差 ≤1.2V，如图 32 所示。为满足此要求，VCCA3 和 VCCD 供电建议采用以下方式： - 使用同一个 LDO 对 VCCA3 和 VCCD 同时上电，两个电源间利用磁珠相互隔离； - 使用两个同型号 LDO 各自对 VCCA3 和 VCCD 专用独立供电。这两个 LDO 上电时间设置（即软启动）相同，使能信号相同，输入电源相同。

如果 VCCA3 和 VCCD 未采用以上供电方式，则要求两个电源间最大电压差 ≤1.2V。

本电路断电没有特定要求。

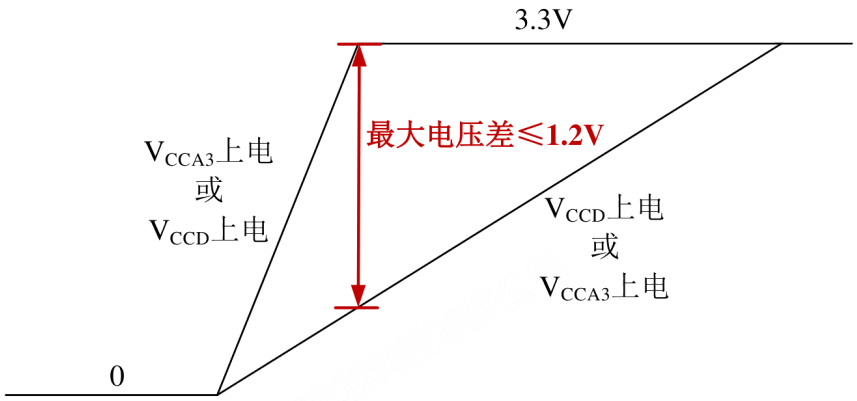


Figure 31: Power-up timing requirements

电源地间保护 / Power-to-Ground Protection

English: To improve the anti-static capability of the device, the following ESD protection loops exist between the various supply pins inside the device. The forward conduction voltage drop of each ESD protection device is approximately 1.15V; during power-up and normal use, prolonged forward conduction of these ESD protection devices should be avoided. (Figure annotations in the source include: R3: 343~356Ω; R1: 2.2kΩ (GA floating); R1: 1.95kΩ (GA grounded); R2: 1.65Ω; PowerClamp1; PowerClamp2.)

中文： 为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 1.15V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。（图内标注：R3：343~356Ω；R1：2.2kΩ（GA 悬空）；R1：1.95kΩ（GA 接地）；R2：1.65Ω；PowerClamp1；PowerClamp2。）

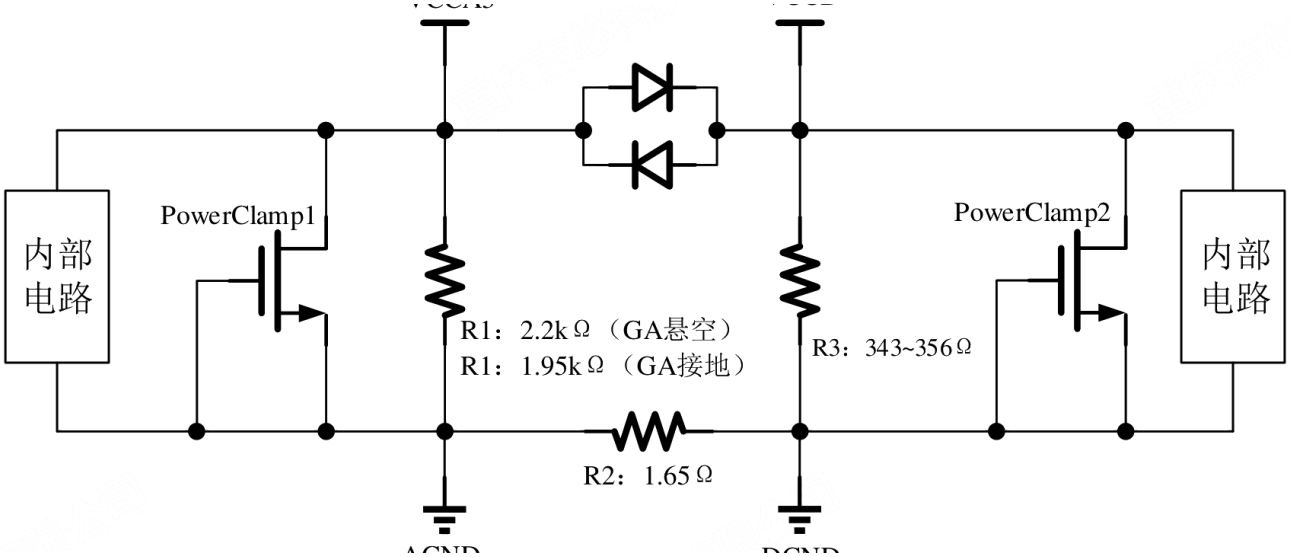


Figure 32: Power-to-ground protection

注意事项 / Precautions

1. 产品安装注意事项 / 1. Product Installation Precautions

English: 1) This product is in a ceramic hermetic package; no baking is required before assembly. To prevent solder-ball oxidation, it is recommended that the device be stored in a nitrogen environment after unpacking; 2) When assembly uses leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C~220°C; the maximum peak temperature is recommended not to exceed 235°C; the dwell time within ±5°C of the peak temperature is ≤20s; the time above liquidus is 60~90s. Ramp-up rate 2~4°C/s; ramp-down rate ≤2°C~6°C ; 3) If a mixed assembly process requires a temperature increase, ensure the device body temperature does not exceed 260°C at maximum; 4) The terminals use high-lead solder balls, specifically Sn10Pb90.

中文： 1) 本产品为陶瓷气密性封装，电装前无烘烤要求。为防止焊球氧化，建议拆包后器件储存在氮气环境下； 2) 电装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~220°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s。升温速率 2~4°C/s，降温速率 ≤2°C~6°C； 3) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C； 4) 引出端采用高铅焊球，具体材料为 Sn10Pb90。

2. 产品使用注意事项 / 2. Product Usage Precautions

English: 1) During testing, handling, and storage, pay attention to ESD protection. 2) Pay attention to the pin sequence during installation to avoid pin misalignment. 3) It is recommended to pay attention to the ambient temperature during actual use, and to pay attention to heat dissipation. 4) During power-up of this circuit's supplies VCCA3 and VCCD, the maximum voltage difference between the two supplies is required to be ≤1.2V.

中文： 1) 在测试、搬运、储藏过程中，应注意静电防护。 2) 安装时注意引脚顺序，以免引脚错位。 3) 建议实际使用时关注环境温度，并注意散热。 4) 本电路电源 VCCA3 和 VCCD 在上电过程中，要求两个电源间最大电压差 ≤1.2V。

3. 产品防护注意事项 / 3. Product Protection Precautions

English: During storage and transportation, the circuit should be placed in tin foil, special conductive foam plastic, or a special anti-static box; never place the circuit in an ordinary plastic box.

中文： 在贮存及运输时，应将电路放入锡箔、特制导电泡沫塑料或特制防静电盒子内，切忌将电路放在一般塑料盒中。

常见故障及处理办法 / Common Faults and Troubleshooting

1. 输出信号频谱异常 / 1. Abnormal Output Signal Spectrum

English: When the output signal spectrum is abnormal, the following check items can usually be checked one by one: 1) Check whether the input data interface timing is suitable: change PSS[2:0] from all 0 to all 1, and judge whether the input interface timing is suitable by observing the STVF and HTVF output values. 2) Whether the FPGA output data [A0..A11], [A0N..A11N], [B0..B11], [B0N..B11N], [C0..C11], [C0N..C11N],

[D0..D11], [D0N..D11N] correspond correctly one-to-one with the DAC input data pins [A0..A11], [A0N..A11N], [B0..B11], [B0N..B11N], [C0..C11], [C0N..C11N], [D0..D11], [D0N..D11N]. 3) Check whether the device output pins OUT and OUTN are normal: test whether the differential resistance between the output pins OUT and OUTN is the nominal value of 100Ω.

中文： 当输出信号频谱异常时，通常可以按照下面的检查项目逐项检查： 1) 检查输入数据接口时序是否合适：从全 0 到全 1 改变 PSS[2:0]，通过观察 STVF、HTVF 输出值，判断输入接口时序是否合适。 2) FPGA 输出数据 [A0..A11]、[A0N..A11N]、[B0..B11]、[B0N..B11N]、[C0..C11]、[C0N..C11N]、[D0..D11]、[D0N..D11N] 与 DAC 输入数据引脚 [A0..A11]、[A0N..A11N]、[B0..B11]、[B0N..B11N]、[C0..C11]、[C0N..C11N]、[D0..D11]、[D0N..D11N] 是否正确一一对应。 3) 检查该器件输出引脚 OUT、OUTN 是否正常：测试输出引脚 OUT、OUTN 之间差分电阻是否为标称值 100Ω。

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附加说明 / Additional Notes

English: 1. First release date of this manual: July 2026. 2. Product status: ☑ Production (this model is currently in production; formal products can be provided). 3. Explanation of substitution for the foreign product: 3.1 External dimension comparison: the dimension comparison between the device and the corresponding foreign product is shown in Table 1 ; dimensions are consistent and plug-in replacement can be achieved. 3.2 Standard comparison: see Tables 2–4 below.

中文： 1. 本说明书首次发布日期：2026 年 7 月。 2. 本产品状态：☑ 生产（该产品型号目前已在生产，可以提供正式产品） 3. 替代国外产品情况说明： 3.1 外形尺寸对比：器件尺寸与对应国外产品尺寸对比见表 1，从表中可以看出尺寸一致，可实现插拔替换。 3.2 标准对比：见下表 2–表 4。

附表 1 实测器件尺寸对比表 / Additional Table 1. Measured Device Dimension Comparison

型号 / Model	样品（L×W×H）/ Sample (L×W×H)	对比结果 / Comparison Result
SXD015	15mm x 15mm x 2.76mm	长宽一致、高度国产器件略高 / Length and width consistent; domestic device slightly taller
国外产品 / Foreign product	15mm x 15mm x 1.66mm	

附表 2 绝对最大额定值对比 / Additional Table 2. Absolute Maximum Ratings Comparison

参数 / Parameter	采购规范要求 / Procurement Specification Requirement	国外产品手册 / Foreign Product Datasheet	比对结果 / Comparison Result
VCCA5	-0.6V~+6.0V	6.0V	一致 / Consistent
VCCA3	-0.6V~+4.0V	4.0V	一致 / Consistent
VCCD	-0.6V~+4.0V	4.0V	一致 / Consistent

参数 / Parameter	采购规范要求 / Procurement Specification Requirement	国外产品手册 / Foreign Product Datasheet	比对结果 / Comparison Result
结温 / Junction temperature	150°C	170°C	有差异 / Different
引线耐焊接温度（10s）/ Lead soldering temperature (10s)	300°C	无 / None	
热阻，结到壳（Rth(J-C)）/ Thermal resistance, junction-to-case	14°C/W	14°C/W	一致 / Consistent

English: From the absolute maximum ratings comparison, it can be seen that, except for junction temperature, all other maximum ratings of the device are consistent with the foreign product datasheet.

中文： 通过最大额定值对比可知，器件除结温外，其余最大额定值与国外产品手册一致。

附表 3 推荐工作条件对比 / Additional Table 3. Recommended Operating Conditions Comparison

参数 / Parameter	采购规范要求 / Procurement Specification Requirement	国外产品手册 / Foreign Product Datasheet	比对结果 / Comparison Result
VCCA5	4.75V~5.25V	4.75V~5.25V	一致 / Consistent
VCCA3	3.15V~3.45V	3.15V~3.45V	一致 / Consistent
VCCD	3.15V~3.45V	3.15V~3.45V	一致 / Consistent
LVDS 数字输入低电压 / LVDS digital input low voltage	1.075V	1.075V	一致 / Consistent
LVDS 数字输入高电压 / LVDS digital input high voltage	1.425V	1.425V	一致 / Consistent
数字输入差分摆幅 / Digital input differential swing	350mVp	350mVp	一致 / Consistent
时钟输入功率（差分模式）/ Clock input power (differential mode)	-4dBm~+8dBm	-4dBm~+8dBm	一致 / Consistent
控制功能输入低电压 / Control function input low voltage	0	0	一致 / Consistent
控制功能输入高电压 / Control function input high voltage	VCCD	VCCD	一致 / Consistent
增益调整范围 / Gain adjustment range	0~VCCA3	0~VCCA3	一致 / Consistent
工作温度范围 / Operating temperature range	-55°C≤TC≤125°C	-40°C≤TC，Tj≤110°C	有差异 / Different

English: From the recommended operating conditions comparison, it can be seen that, except for the operating temperature range, the procurement specification requirements are consistent with the foreign product datasheet.

中文： 通过推荐工作条件对比可知，器件除工作温度范围外，采购规范要求与国外产品手册一致。

附表 4 电特性对比 / Additional Table 4. Electrical Characteristics Comparison

English: The conformity of the device technical specifications with the foreign product datasheet is shown in Table 4. From Table 4, it can be seen that there are certain differences between the device procurement specification requirements and the foreign product datasheet requirements.

中文： 器件技术指标与国外产品手册的符合性见表 4。从表 4 中可看出，器件采购规范要求与国外产品手册的要求存在一定差异。

参数 / Parameter	符号 / Symbol	条件 / Conditions	采购规范要求 / Procurement Spec.		国外产品手册 / Foreign Datasheet		单位 / Unit	对比结果 / Result
			最小值 / Min	最大值 / Max	最小值 / Min	最大值 / Max		
分辨率 / Resolution	RES		12		12		Bits	一致 / Consistent
5V 模拟电源电流 / 5V analog supply current	ICCA5	4:1 MUX 模式 / 4:1 MUX mode	—	90	—	90	mA	一致 / Consistent
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3		—	122	—	122	mA	一致 / Consistent
3.3V 数字电源电流 / 3.3V digital supply current	ICCD		—	270	—	205	mA	有差异 / Different
功耗 / Power consumption	PW		—	1.8	—	1.6	W	有差异 / Different
5V 模拟电源电流 / 5V analog supply current	ICCA5	2:1 MUX 模式 / 2:1 MUX mode	—	90	—	90	mA	一致 / Consistent
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3		—	122	—	122	mA	一致 / Consistent
3.3V 数字电源电流 / 3.3V digital supply current	ICCD		—	200	—	177	mA	有差异 / Different
功耗 / Power consumption	PW		—	1.6	—	1.5	W	有差异 / Different
数字差分输入电压 / Digital differential input voltage	VID		100	500	100	500	mVp	一致 / Consistent
数字差分输入电阻 / Digital differential input resistance	RILVDS		80	130	80	120	Ω	有差异 / Different
时钟输入共模电压 / Clock input common-mode voltage	VICLKCM		2.3	2.6	2.4	2.6	V	有差异 / Different
时钟差分输入电阻 / Clock differential input resistance	RICLK		80	130	80	120	Ω	有差异 / Different
时钟差分输出电压 / Clock differential output voltage	VOD		240	450	240	450	mVp	一致 / Consistent
满幅度差分输出电压 / Full-scale differential output voltage	VOUT		0.87	1.1	0.92	1.08	Vpp	有差异 / Different
模拟输出内部差分电阻 / Analog output internal differential resistance	ROUT		90	120	90	110	Ω	有差异 / Different
差分非线性 / Differential nonlinearity	EDL		-4	+4	-0.95	+0.95	LSB	有差异 / Different
积分非线性 / Integral nonlinearity	EL		-5	+5	-3	+3	LSB	有差异 / Different
无杂散动态范围 / SFDR	SFDR	非归零模式（NRZ）/ NRZ: fCLK=3Gsps，fout=100MHz，0dBFS，4:1 MUX	56	—	59	—	dBc	有差异 / Different
无杂散动态范围 / SFDR	SFDR	非归零模式（NRZ）/ NRZ: fCLK=3Gsps，fout=400MHz，0dBFS，4:1 MUX	54	—	—	—	dBc	
无杂散动态范围 / SFDR	SFDR	窄归零模式（NRTZ）/ NRTZ: fCLK=3Gsps，fout=700MHz，0dBFS，4:1 MUX	52	—	—	—	dBc	
无杂散动态范围 / SFDR	SFDR	窄归零模式（NRTZ）/ NRTZ: fCLK=1.5Gsps，fout=700MHz，0dBFS，2:1 MUX	45	—	53	—	dBc	有差异 / Different
无杂散动态范围 / SFDR	SFDR	归零模式（RTZ）/ RTZ: fCLK=3Gsps，fout=1600MHz，0dBFS，4:1 MUX	50	—	50	—	dBc	一致 / Consistent
无杂散动态范围 / SFDR	SFDR	归零模式（RTZ）/ RTZ: fCLK=3Gsps，fout=2900MHz，0dBFS，4:1 MUX	42	—	—	—	dBc	有差异 / Different
无杂散动态范围 / SFDR	SFDR	混频模式（RF）/ RF: fCLK=3Gsps，fout=2900MHz，0dBFS，4:1 MUX	38	—	—	—	dBc	
无杂散动态范围 / SFDR	SFDR	混频模式（RF）/ RF: fCLK=3Gsps，fout=3800MHz，0dBFS，4:1 MUX	37	—	—	—	dBc	
最大转换速率 / Maximum conversion rate	fCLK	4:1 MUX 模式 / 4:1 MUX mode	3	—	3	—	GSPS	一致 / Consistent
最大转换速率 / Maximum conversion rate	fCLK	2:1 MUX 模式 / 2:1 MUX mode	1.5	—	1.5	—	GSPS	一致 / Consistent
最大输入数据率 / Maximum input data rate	fDATA	4:1 MUX 模式 / 4:1 MUX mode	750	—	750	—	MSPS	一致 / Consistent
最大输入数据率 / Maximum input data rate	fDATA	2:1 MUX 模式 / 2:1 MUX mode	750	—	750	—	MSPS	一致 / Consistent

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