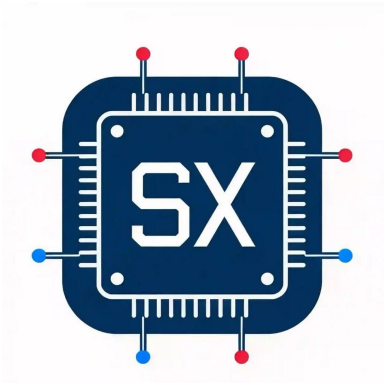


SXD016

12-Bit, 6.4 GSPS D/A Converter

12 位 6.4GSPS D/A 转换器

12-bit | 1 channel | 6.4 GSPS | PBGA196 | LVDS

12位 | 单通道 | 6.4GSPS | PBGA196 | LVDS

对标 / Cross Reference: EV12DS460 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

felix@shenxinic.com | +852 51367095 | shenxinic.com

SXD016 — 12-Bit, 6.4 GSPS D/A Converter / 12 位 6.4GSPS D/A 转换器

Document type / 文档类型： Product specification and user manual / 产品说明书、使用手册

Applicable standard / 执行标准： GJB7400A-2024 (quality grade: enterprise standard / 质量等级：企标; QA requirements controlled at Grade N1 per GJB7400A-2024 / 质量保证要求按 GJB7400A-2024 中规定的 N1 级控制)

产品用途及应用范围 / Applications

English: - Broadband signal direct digital synthesis - Automatic test equipment - Arbitrary waveform generators - Electronic countermeasures signal synthesis

中文： - 宽带信号直接数字综合 - 自动测试设备 - 任意波形产生器 - 电子对抗信号综合

产品特点 / Features

English: - 12-bit D/A converter - 6.4 GSPS conversion rate - Low latency: 3 clock cycles - Multiple output operating modes: non-return-to-zero, return-to-zero, narrow return-to-zero, mixing mode - Circuit interface: LVDS - Supply voltages: digital 3.3 V, analog 3.3 V & 5 V - Power consumption: 2.7 W (typical) - ESD: ⩾500 V (human body model) - Product weight: 0.58 g ± 0.12 g

中文： - 12 位 D/A 转换器 - 6.4GSPS 转换速率 - 低延迟时间：3 个时钟周期 - 多种输出工作模式：非归零、归零、窄归零、混频模式 - 电路接口：LVDS - 电源电压：数字 3.3V、模拟 3.3V&5V - 功耗：2.7W（典型值） - ESD：⩾500V（人体模型） - 产品重量：0.58g±0.12g

---

产品描述 / General Description

English: The SXD016 12-bit, 6.4 GSPS D/A converter uses a segmented current-steering architecture. The product includes four parallel LVDS interfaces, achieving a total input data rate of up to 6.4 Gbps. The four 1.6 Gbps data streams are then combined by a MUX into 6.4 Gbps high-speed data. After decoding, the high-speed data is sent to the DAC core for conversion and output. It integrates four operating modes: return-to-zero mode (RTZ), non-return-to-zero mode (NRZ), narrow return-to-zero mode (NRTZ), and mixing mode (RF).

The circuit uses a 196-pin plastic ball grid array package (PBGA196), implements standard GJB7400A-2024, and its quality assurance requirements are controlled at Grade N1 as specified in GJB7400A-2024. The chip and other package forms can also be provided according to the user's actual needs. The functional block diagram of the product is shown in Figure 1.

中文： SXD016 型 12 位 6.4GSPS D/A 转换器采用分段电流舵架构。该产品包括四路并行 LVDS 接口，实现输入总数据率高达 6.4Gbps。然后通过 MUX 将四路 1.6Gbps 数据合成 6.4Gbps 的高速数据。高速数据经过译码后送入 DAC 内核转换输出。它集成四种工作模式：归零模式（RTZ）、非归零模式（NRZ）、窄归零模式（NRTZ）和混频模式（RF）。

该电路采用 196 引脚塑料球栅阵列封装（PBGA196），执行标准 GJB7400A-2024，质量保证要求按 GJB7400A-2024 中规定的 N1 级控制。也可根据用户实际需要，提供芯片及其它封装形式。该产品功能框图如图 1 所示。

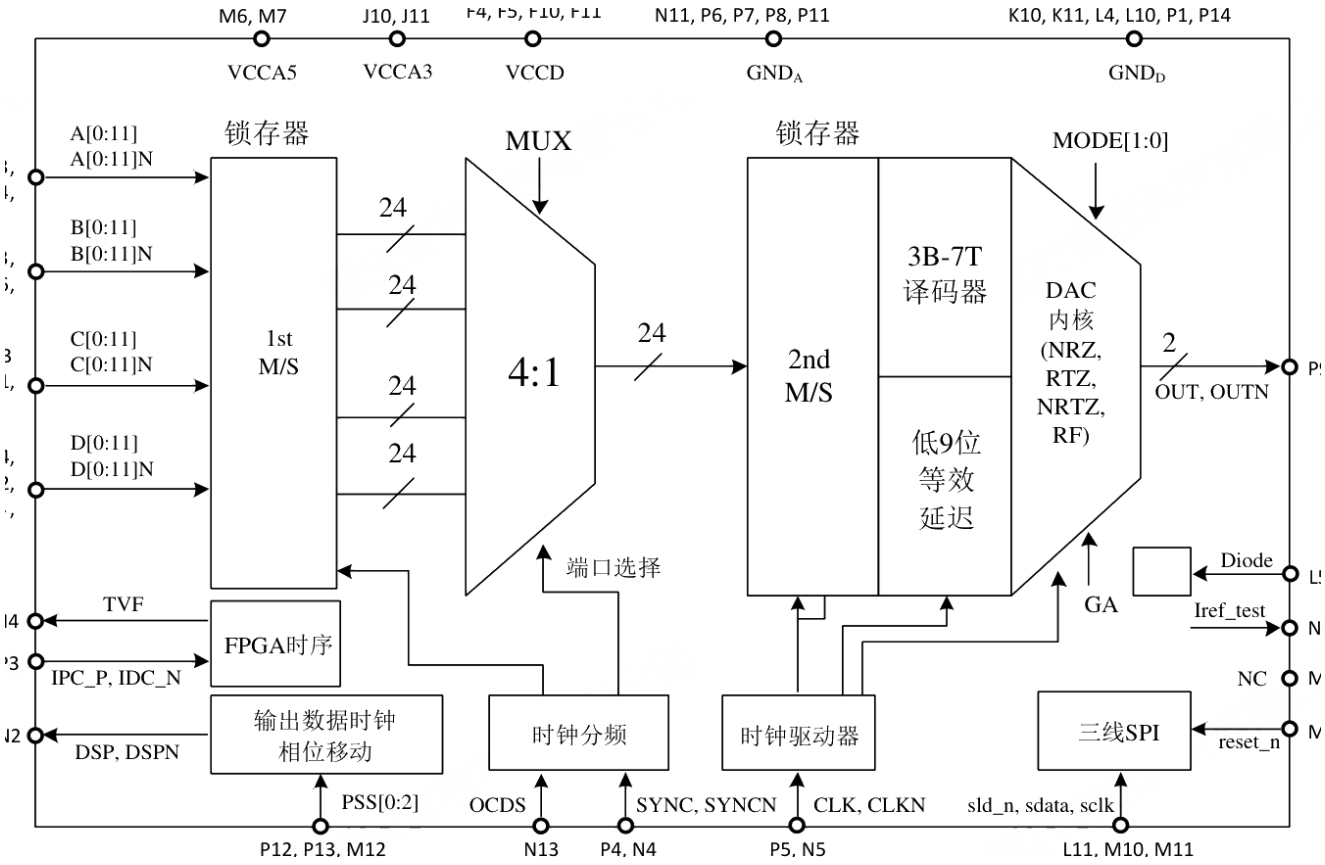


Figure 1: Functional block diagram

English: The operating timing of the product is as follows:

中文： 该产品工作时序如下：

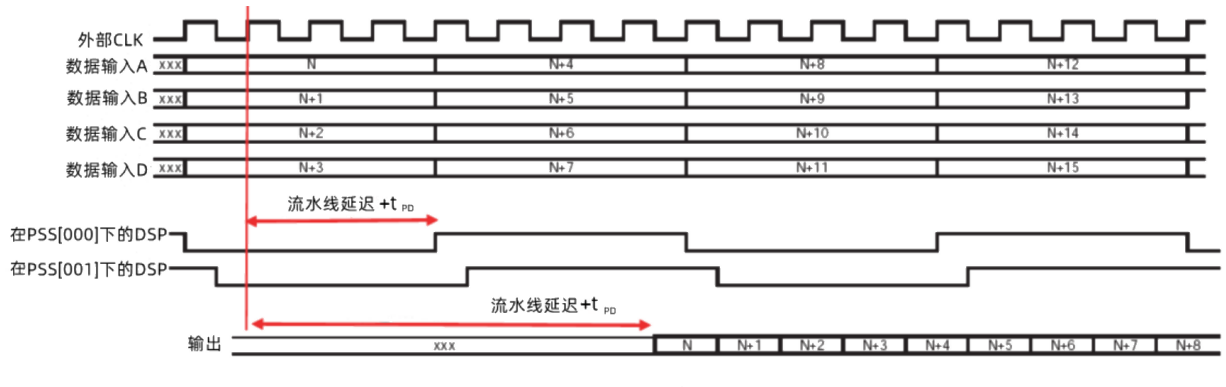


Figure 2: Timing diagram (4:1 MUX mode, OCDS1, IUCM1)

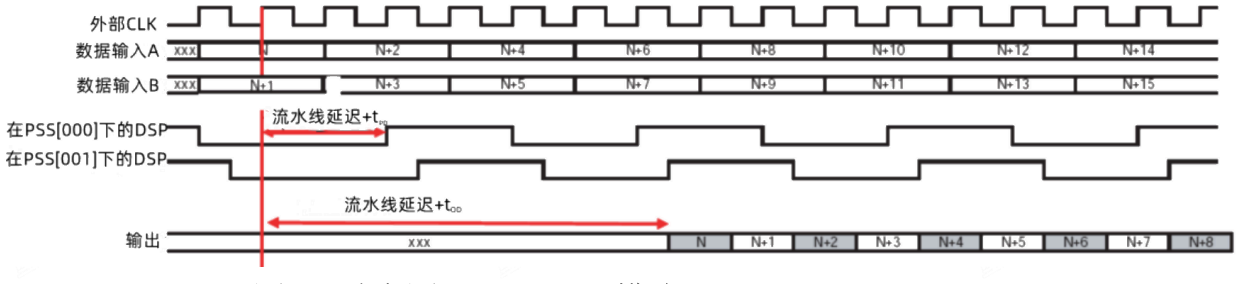
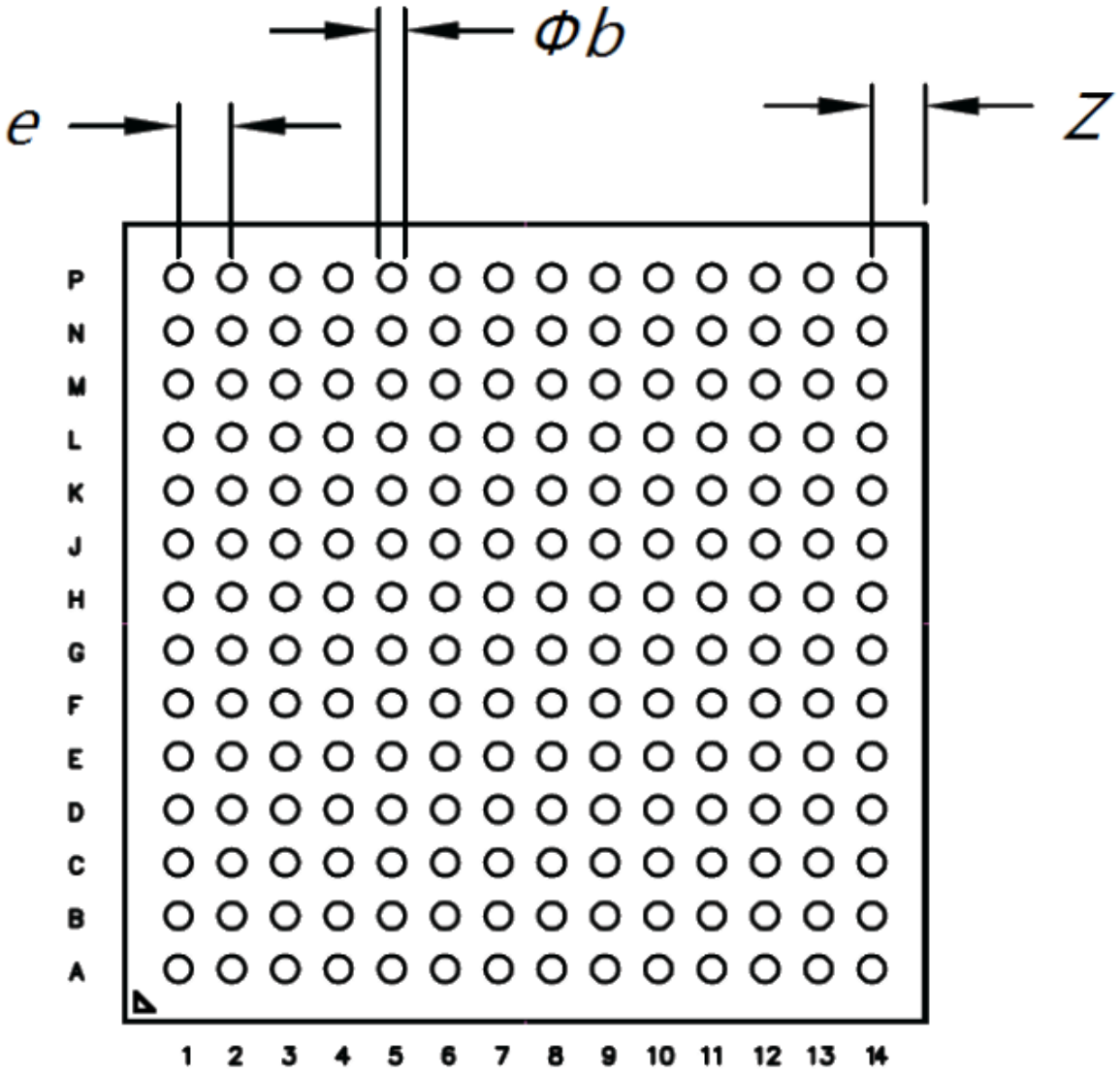
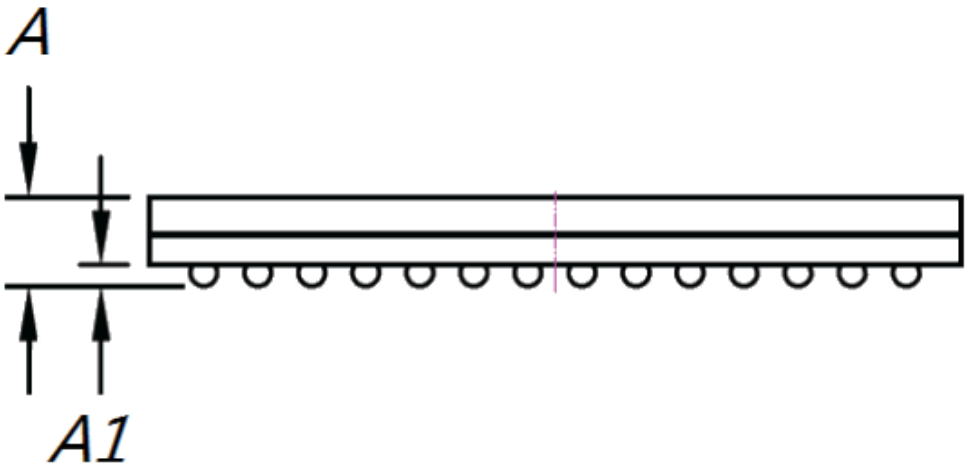


Figure 3: Timing diagram (2:1 MUX mode, OCDS1, IUCM1)

产品外形图 / Package Outline





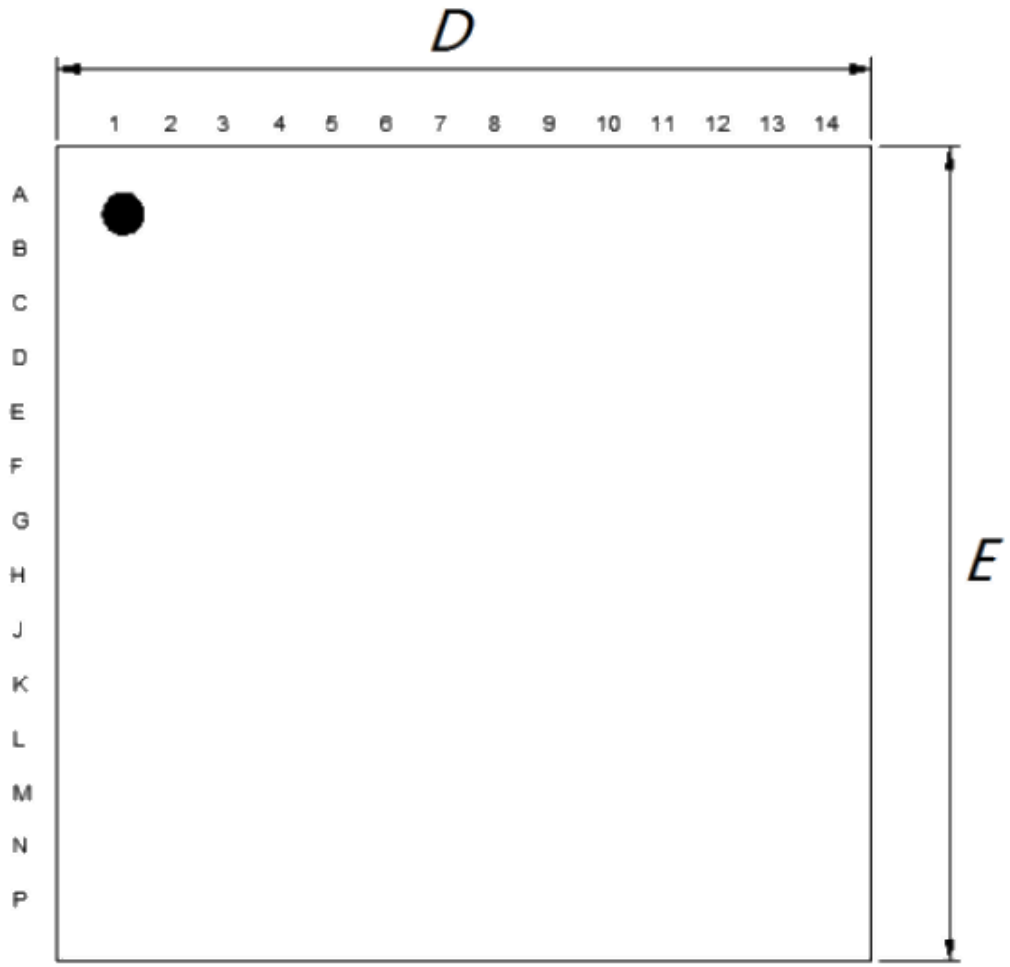

D
1 2 3 4 5 6 7 8 9 10 11 12 13 14
A
B
C
D
E
F
G
H
J
K
L
M
N
P
E

Figure 4: Package outline drawing

单位为毫米 / Unit: mm

尺寸符号 / Symbol	最小 / Min	公称 / Nom	最大 / Max	尺寸符号 / Symbol	最小 / Min	公称 / Nom	最大 / Max
A	—	1.31	1.70	D	14.90	15.00a	15.10
A1	0.30	—	0.50	E	14.90	15.00a	15.10
Φb	0.45	0.50a	0.55	Z	—	1.00a	1.10
e	—	1.00	—				

English: Note: a: guaranteed by design, not tested. Note: for the recommended pad design, see the assembly instructions.

中文： 注：a：设计保证，不进行考核。注：推荐焊盘设计详见电装说明。

引出端排列（俯视图）/ Pin Configuration (Top View)

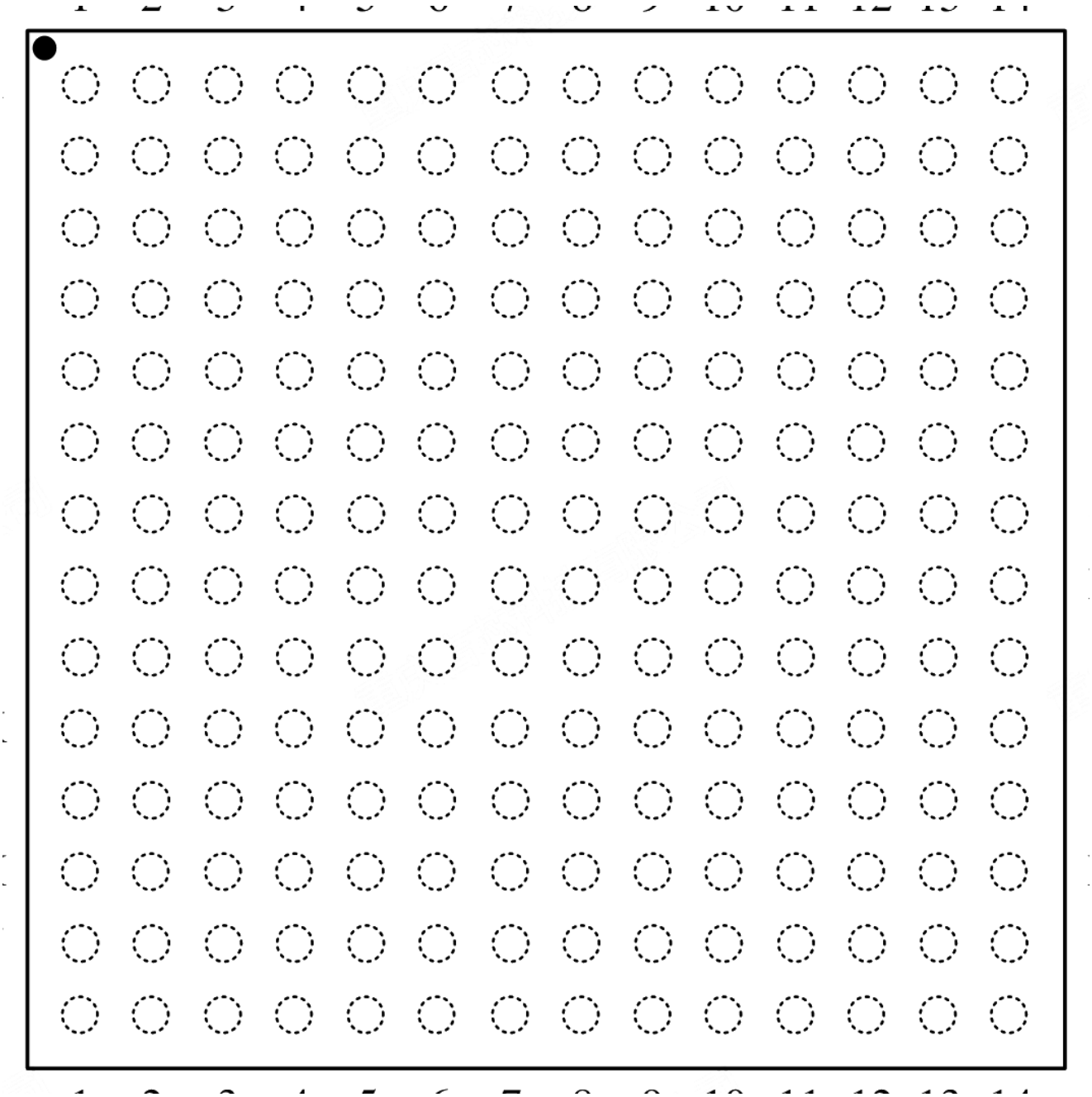


Figure 5: Pin configuration

引出端功能符号表 / Pin Function Descriptions

引出端号 / Pin	符号 / Symbol	名称 / Name (EN / 中文)	I/O
A1	GNDD	Digital ground / 数字地	/
A2	B5	Differential data input bit B5 / 差分数据输入位B5	I
A3	B6	Differential data input bit B6 / 差分数据输入位B6	I
A4	B6N	Differential data input bit B6N / 差分数据输入位B6N	I

引出端号 / Pin	符号 / Symbol	名称 / Name (EN / 中文)	I/O
A5	B9	Differential data input bit B9 / 差分数据输入位B9	I
A6	B9N	Differential data input bit B9N / 差分数据输入位B9N	I
A7	B11	Differential data input bit B11(MSB) / 差分数据输入位B11（最高位）	I
A8	C11	Differential data input bit C11(MSB) / 差分数据输入位C11（最高位）	I
A9	C9N	Differential data input bit C9N / 差分数据输入位C9N	I
A10	C9	Differential data input bit C9 / 差分数据输入位C9	I
A11	差分数据输入位A11（最	/ 高位）	I
A12	C6	Differential data input bit C6 / 差分数据输入位C6	I
A13	C5	Differential data input bit C5 / 差分数据输入位C5	I
A14	GNDD	Digital ground / 数字地	/
B1	B3	Differential data input bit B3 / 差分数据输入位B3	I
B2	B4	Differential data input bit B4 / 差分数据输入位B4	I
B3	B5N	Differential data input bit B5N / 差分数据输入位B5N	I
B4	B7	Differential data input bit B7 / 差分数据输入位B7	I
B5	B8	Differential data input bit B8 / 差分数据输入位B8	I
B6	B10	Differential data input bit B10 / 差分数据输入位B10	I
B7	B11N	Differential data input bit B11N(MSB) / 差分数据输入位B11N（最高位）	I
B8	C11N	Differential data input bit C11N(MSB) / 差分数据输入位C11N（最高位）	I
B9	C10	Differential data input bit C10 / 差分数据输入位C10	I
B10	C8	Differential data input bit C8 / 差分数据输入位C8	I
B11	差分数据输入位B11（最	/ 高位）	I
B12	C5N	Differential data input bit C5N / 差分数据输入位C5N	I
B13	C4	Differential data input bit C4 / 差分数据输入位C4	I
B14	C3	Differential data input bit C3 / 差分数据输入位C3	I
C1	B1N	Differential data input bit B1N / 差分数据输入位B1N	I
C2	B3N	Differential data input bit B3N / 差分数据输入位B3N	I
C3	B4N	Differential data input bit B4N / 差分数据输入位B4N	I
C4	B7N	Differential data input bit B7N / 差分数据输入位B7N	I
C5	B8N	Differential data input bit B8N / 差分数据输入位B8N	I
C6	B10N	Differential data input bit B10N / 差分数据输入位B10N	I
C7	GNDD	Digital ground / 数字地	/
C8	GNDD	Digital ground / 数字地	/
C9	C10N	Differential data input bit C10N / 差分数据输入位C10N	I
C10	C8N	Differential data input bit C8N / 差分数据输入位C8N	I

引出端号 / Pin	符号 / Symbol	名称 / Name (EN / 中文)	I/O
C11	C7N	Differential data input bit C7N / 差分数据输入位C7N	I
C12	C4N	Differential data input bit C4N / 差分数据输入位C4N	I
C13	C3N	Differential data input bit C3N / 差分数据输入位C3N	I
C14	C1N	Differential data input bit C1N / 差分数据输入位C1N	I
D1	B1	Differential data input bit B1 / 差分数据输入位B1	I
D2	B2	Differential data input bit B2 / 差分数据输入位B2	I
D3	B2N	Differential data input bit B2N / 差分数据输入位B2N	I
D4	GNDD	Digital ground / 数字地	/
D5	GNDD	Digital ground / 数字地	/
D6	VCCD	3.3V digital supply / 3.3V 数字电源	/
D7	VCCD	3.3V digital supply / 3.3V 数字电源	/
D8	VCCD	3.3V digital supply / 3.3V 数字电源	/
D9	VCCD	3.3V digital supply / 3.3V 数字电源	/
D10	GNDD	Digital ground / 数字地	/
D11	差分数据输入位D11（最	/ 高位）	I
D12	C2N	Differential data input bit C2N / 差分数据输入位C2N	I
D13	C2	Differential data input bit C2 / 差分数据输入位C2	I
D14	C1	Differential data input bit C1 / 差分数据输入位C1	I
E1	A10N	Differential data input bit A10N / 差分数据输入位A10N	I
E2	B0	Differential data input bit B0(LSB) / 差分数据输入位B0（最低位）	I
E3	B0N	Differential data input bit B0N(LSB) / 差分数据输入位B0N（最低位）	I
E4	GNDD	Digital ground / 数字地	/
E5	GNDD	Digital ground / 数字地	/
E6	VCCD	3.3V digital supply / 3.3V 数字电源	/
E7	VCCD	3.3V digital supply / 3.3V 数字电源	/
E8	VCCD	3.3V digital supply / 3.3V 数字电源	/
E9	VCCD	3.3V digital supply / 3.3V 数字电源	/
E10	GNDD	Digital ground / 数字地	/
E11	GNDD	Digital ground / 数字地	/
E12	C0N	Differential data input bit C0N(LSB) / 差分数据输入位C0N（最低位）	I
E13	C0	Differential data input bit C0(LSB) / 差分数据输入位C0（最低位）	I
E14	D10N	Differential data input bit D10N / 差分数据输入位D10N	I
F1	A10	Differential data input bit A10 / 差分数据输入位A10	I
F2	A11	Differential data input bit A11(MSB) / 差分数据输入位A11（最高位）	I
F3	A11N	Differential data input bit A11N(MSB) / 差分数据输入位A11N（最高位）	I

引出端号 / Pin	符号 / Symbol	名称 / Name (EN / 中文)	I/O
F4	VCCD	3.3V digital supply / 3.3V 数字电源	/
F5	VCCD	3.3V digital supply / 3.3V 数字电源	/
F6	GNDA	Analog ground / 模拟地	/
F7	GNDA	Analog ground / 模拟地	/
F8	GNDA	Analog ground / 模拟地	/
F9	GNDA	Analog ground / 模拟地	/
F10	VCCD	3.3V digital supply / 3.3V 数字电源	/
F11	VCCD	3.3V digital supply / 3.3V 数字电源	/
F12	D11N	Differential data input bit D11N(MSB) / 差分数据输入位D11N（最高位）	I
F13	D11	Differential data input bit D11(MSB) / 差分数据输入位D11（最高位）	I
F14	D10	Differential data input bit D10 / 差分数据输入位D10	I
G1	A8	Differential data input bit A8 / 差分数据输入位A8	I
G2	A8N	Differential data input bit A8N / 差分数据输入位A8N	I
G3	A9	Differential data input bit A9 / 差分数据输入位A9	I
G4	A9N	Differential data input bit A9N / 差分数据输入位A9N	I
G5	GNDD	Digital ground / 数字地	/
G6	GNDA	Analog ground / 模拟地	/
G7	GNDA	Analog ground / 模拟地	/
G8	GNDA	Analog ground / 模拟地	/
G9	GNDA	Analog ground / 模拟地	/
G10	GNDD	Digital ground / 数字地	/
G11	D9N	Differential data input bit D9N / 差分数据输入位D9N	I
G12	D9	Differential data input bit D9 / 差分数据输入位D9	I
G13	D8N	Differential data input bit D8N / 差分数据输入位D8N	I
G14	D8	Differential data input bit D8 / 差分数据输入位D8	I
H1	A6	Differential data input bit A6 / 差分数据输入位A6	I
H2	A6N	Differential data input bit A6N / 差分数据输入位A6N	I
H3	A7	Differential data input bit A7 / 差分数据输入位A7	I
H4	A7N	Differential data input bit A7N / 差分数据输入位A7N	I
H5	GNDD	Digital ground / 数字地	/
H6	GNDA	Analog ground / 模拟地	/
H7	GNDA	Analog ground / 模拟地	/
H8	GNDA	Analog ground / 模拟地	/
H9	GNDA	Analog ground / 模拟地	/
H10	GNDD	Digital ground / 数字地	/
H11	D7N	Differential data input bit D7N / 差分数据输入位D7N	I

引出端号 / Pin	符号 / Symbol	名称 / Name (EN / 中文)	I/O
H12	D7	Differential data input bit D7 / 差分数据输入位D7	I
H13	D6N	Differential data input bit D6N / 差分数据输入位D6N	I
H14	D6	Differential data input bit D6 / 差分数据输入位D6	I
J1	A3N	Differential data input bit A3N / 差分数据输入位A3N	I
J2	A5	Differential data input bit A5 / 差分数据输入位A5	I
J3	A5N	Differential data input bit A5N / 差分数据输入位A5N	I
J4	VCCA3	3.3V analog supply / 3.3V 模拟电源	/
J5	VCCA3	3.3V analog supply / 3.3V 模拟电源	/
J6	GNDA	Analog ground / 模拟地	/
J7	GNDA	Analog ground / 模拟地	/
J8	GNDA	Analog ground / 模拟地	/
J9	GNDA	Analog ground / 模拟地	/
J10	VCCA3	3.3V analog supply / 3.3V 模拟电源	/
J11	VCCA3	3.3V analog supply / 3.3V 模拟电源	/
J12	D5N	Differential data input bit D5N / 差分数据输入位D5N	I
J13	D5	Differential data input bit D5 / 差分数据输入位D5	I
J14	D3N	Differential data input bit D3N / 差分数据输入位D3N	I
K1	A3	Differential data input bit A3 / 差分数据输入位A3	I
K2	A4	Differential data input bit A4 / 差分数据输入位A4	I
K3	A4N	Differential data input bit A4N / 差分数据输入位A4N	I
K4	GNDD	Digital ground / 数字地	/
K5	GNDD	Digital ground / 数字地	/
K6	GNDA	Analog ground / 模拟地	/
K7	VCCA5	5V analog supply / 5V 模拟电源	/
K8	VCCA5	5V analog supply / 5V 模拟电源	/
K9	GNDA	Analog ground / 模拟地	/
K10	GNDD	Digital ground / 数字地	/
K11	GNDD	Digital ground / 数字地	/
K12	D4N	Differential data input bit D4N / 差分数据输入位D4N	I
K13	D4	Differential data input bit D4 / 差分数据输入位D4	I
K14	D3	Differential data input bit D3 / 差分数据输入位D3	I
L1	A1N	Differential data input bit A1N / 差分数据输入位A1N	I
L2	A2	Differential data input bit A2 / 差分数据输入位A2	I
L3	A2N	Differential data input bit A2N / 差分数据输入位A2N	I
L4	GNDD	Digital ground / 数字地	/
L5	Diode	Die junction-temperature test diode / 芯片结温测试二极管	O

引出端号 / Pin	符号 / Symbol	名称 / Name (EN / 中文)	I/O
L6	VCCA5	5V analog supply / 5V 模拟电源	/
L7	VCCA5	5V analog supply / 5V 模拟电源	/
L8	VCCA5	5V analog supply / 5V 模拟电源	/
L9	VCCA5	5V analog supply / 5V 模拟电源	/
L10	GNDD	Digital ground / 数字地	/
L11	sldn	3-wire SPI serial input enable / 三线SPI 串行输入使能	I
L12	D2N	Differential data input bit D2N / 差分数据输入位D2N	I
L13	D2	Differential data input bit D2 / 差分数据输入位D2	I
L14	D1N	Differential data input bit D1N / 差分数据输入位D1N	I
M1	A1	Differential data input bit A1 / 差分数据输入位A1	I
M2	A0N	Differential data input bit A0N(LSB) / 差分数据输入位A0N（最低位）	I
M3	NC	No connect / 悬空	/
M4	TVF	Setup/hold time violation flag / 建立/保持时间违反标志	O
M5	reset_n	SPI register reset / 复位SPI 寄存器	I
M6	VCCA5	5V analog supply / 5V 模拟电源	/
M7	VCCA5	5V analog supply / 5V 模拟电源	/
M8	GNDA	Analog ground / 模拟地	/
M9	GNDA	Analog ground / 模拟地	/
M10	sdata	3-wire SPI serial data input / 三线SPI 串行数据输入	I
M11	sclk	3-wire SPI clock / 三线SPI 时钟	I
M12	PSS2	Output data clock phase select terminal PSS2(MSB) / 输出数据时钟相位选择端PSS2（最高位）	I
M13	D0N	Differential data input bit D0N(LSB) / 差分数据输入位D0N（最低位）	I
M14	D1	Differential data input bit D1 / 差分数据输入位D1	I
N1	A0	Differential data input bit A0(LSB) / 差分数据输入位A0（最低位）	I
N2	DSPN	Data clock out-of-phase output / 数据时钟反相输出	O
N3	IDC_P	Data clock in-phase input / 数据时钟同相输入	I
N4	SYNCN	Sync input negative terminal / 同步输入负端	I
N5	CLKN	DAC sampling clock input negative / DAC 采样时钟输入负	I
N6	GNDA	Analog ground / 模拟地	/
N7	GNDA	Analog ground / 模拟地	/
N8	GNDA	Analog ground / 模拟地	/
N9	GNDA	Analog ground / 模拟地	/
N10	GNDA	Analog ground / 模拟地	/
N11	GNDA	Analog ground / 模拟地	/
N12	iref_test	Reference voltage test terminal / 基准电压测试端	O

引出端号 / Pin	符号 / Symbol	名称 / Name (EN / 中文)	I/O
N13	OCDS	Output data clock divide select / 输出数据时钟分频选择	I
N14	D0	Differential data input bit D0(LSB) / 差分数据输入位D0（最低位）	I
P1	GNDD	Digital ground / 数字地	/
P2	DSP	Data clock in-phase output / 数据时钟同相输出	O
P3	IDC_N	Data clock out-of-phase input / 数据时钟反相输入	I
P4	SYNC	Sync input positive terminal / 同步输入正端	I
P5	CLK	DAC sampling clock input positive / DAC 采样时钟输入正	I
P6	GNDA	Analog ground / 模拟地	/
P7	GNDA	Analog ground / 模拟地	/
P8	GNDA	Analog ground / 模拟地	/
P9	OUT	DAC current in-phase output / DAC 电流同相输出	O
P10	OUTN	DAC current out-of-phase output / DAC 电流反相输出	O
P11	GNDA	Analog ground / 模拟地	/
P12	PSS0	Output data clock phase select terminal PSS0(LSB) / 输出数据时钟相位选择端PSS0（最低位）	I
P13	PSS1	Output data clock phase select terminal PSS1 / 输出数据时钟相位选择端PSS1	I
P14	GNDD	Digital ground / 数字地	/

推荐工作条件 / Recommended Operating Conditions

English: - Supply voltages: - VCCA5 = 4.75 V ~ 5.25 V - VCCA3 = 3.15 V ~ 3.45 V - VCCD = 3.15 V ~ 3.45 V - Digital input low voltage: 1.075 V - Digital input high voltage: 1.425 V - Digital input differential swing: 350 mVp - Clock input differential swing: 0.6 Vpp ~ 2.4 Vpp - Clock input power (differential mode) PCLK: -4.0 dBm ~ +8.5 dBm - Control function input low voltage: 0 V - Control function input high voltage: VCCD - Operating temperature range: -55°C < TC < 125°C - Operating temperature range: -55°C < TA < 90°C

Note: please see the replacement-of-foreign-products description in the additional notes.

中文： - 电源电压： - VCCA5=4.75V~5.25V - VCCA3=3.15V~3.45V - VCCD=3.15V~3.45V - 数字输入低电压：1.075V - 数字输入高电压：1.425V - 数字输入差分摆幅：350mVp - 时钟输入差分摆幅：0.6Vpp~2.4Vpp - 时钟输入功率（差分模式）PCLK：-4.0dBm~+8.5dBm - 控制功能输入低电压：0V - 控制功能输入高电压：VCCD - 工作温度范围：-55°C<TC<125°C - 工作温度范围：-55°C<TA<90°C

注：请查看附件说明中替代国外产品情况说明。

绝对最大额定值 / Absolute Maximum Ratings

English: - Supply voltages: - VCCA5 = -0.6 V ~ +6.0 V - VCCA3 = -0.6 V ~ +4.0 V - VCCD = -0.6 V ~ +4.0 V - Lead soldering temperature (10 s): 300°C - Storage temperature (Tstg): -65°C ~ 150°C

中文： - 电源电压： - VCCA5=-0.6V~+6.0V - VCCA3=-0.6V~+4.0V - VCCD=-0.6V~+4.0V - 引线耐焊接温度（10s）：300°C - 贮存温度（Tstg）： -65°C~150°C

性能指标 / Performance Specifications

Conditions (unless otherwise specified): VCCA5 = 5 V, VCCA3 = VCCD = 3.3 V, GNDA = GNDD = 0 V, -55°C < TC < 125°C. / 条件（除另有规定外，VCCA5=5V，VCCA3=VCCD=3.3V，GNDA= GNDD=0V，-55°C<TC<125°C）

注：典型值为常温测试数据。/ Note: typical values are room-temperature test data.

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
分辨率 / Resolution	RES			12		Bits
5V 模拟电源电流 / 5V analog supply current	ICCA5	4:1 MUX 模式 / mode	—	104	120	mA
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3	4:1 MUX 模式 / mode	—	172	240	mA
3.3V 数字电源电流 / 3.3V digital supply current	ICCD3	4:1 MUX 模式 / mode	—	475	520	mA
功耗 / Power consumption	PW	4:1 MUX 模式 / mode	—	2.67	3.3	W
5V 模拟电源电流 / 5V analog supply current	ICCA5	2:1 MUX 模式 / mode	—	103	120	mA
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3	2:1 MUX 模式 / mode	—	173	240	mA
3.3V 数字电源电流 / 3.3V digital supply current	ICCD3	2:1 MUX 模式 / mode	—	415	460	mA
功耗 / Power consumption	PW	2:1 MUX 模式 / mode	—	2.47	3.1	W
数字差分输入电压 / Digital differential input voltage	VID		100	100~500	500	mVp
数字输入共模电压 / Digital input common-mode voltage	VICM		1	1.27	1.6	V
数字差分输入电阻 / Digital differential input resistance	RILVDS		80	115	130	Ω
时钟输入共模电压 / Clock input	VICLKCM		2.4	2.49	2.6	V

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
common-mode voltage						
时钟差分输入电阻 / Clock differential input resistance	RICLK		80	107	130	Ω
时钟差分输出电压 / Clock differential output voltage	VOD		240	325	450	mVp
时钟输出共模电压 / Clock output common-mode voltage	VOCLKCM		1.125	1.27	1.375	V
模拟输出内部差分电阻 / Analog output internal differential resistance	ROUT		90	106	120	Ω
sdata, sld_n, sclk, reset_n 低电平输入电流 / low-level input current	IIL		-120	-59	-10	uA
sdata, sld_n, sclk, reset_n 高电平输入电流 / high-level input current	IIH		10	59	120	uA
OCDS, PSS 输入低电平电流 / input low-level current	IIL		-150	-110	-50	uA
OCDS, PSS 输入高电平电流 / input high-level current	IIH		50	110	150	uA
微分非线性 / Differential nonlinearity	EDL		-4	-0.65~0.94	+4	LSB
积分非线性 / Integral nonlinearity	EL		-6	-1.55~1.53	+6	LSB
DAC 输出差分电压 / DAC output differential voltage	VOUT	GA<9:0>=0x200	0.88	0.92	1.08	Vpp
DAC 输出电压调节步进电压 / DAC output voltage adjustment step	VADJ		-5	0.28	+5	mV
DAC 输出电压电源敏感度 / DAC output voltage supply sensitivity	VSEN		-5	2	+5	%

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
无杂散动态范围 / SFDR	SFDR	非归零模式 / NRZ: fCLK=6.4GSPS, fout=64MHz, 0dBFS, 4:1 MUX	60	66	—	dBc
无杂散动态范围 / SFDR	SFDR	非归零模式 / NRZ: fCLK=3.2Gsps, fout=32MHz, 0dBFS, 2:1 MUX	58	68	—	dBc
无杂散动态范围 / SFDR	SFDR	窄归零模式 / NRTZ: fCLK=6.4GSPS, fout=3.136GHz, 0dBFS, 4:1 MUX	40	50	—	dBc
无杂散动态范围 / SFDR	SFDR	窄归零模式 / NRTZ: fCLK=3.2Gsps, fout=32MHz, 0dBFS, 2:1 MUX	54	64	—	dBc
无杂散动态范围 / SFDR	SFDR	归零模式 / RTZ: fCLK=6.4GSPS, fout=6.336GHz, 0dBFS, 4:1 MUX	40	51	—	dBc
无杂散动态范围 / SFDR	SFDR	归零模式 / RTZ: fCLK=3.2Gsps, fout=3168MHz, 0dBFS, 2:1 MUX	50	57	—	dBc
无杂散动态范围 / SFDR	SFDR	混频模式 / RF: fCLK=6.4GSPS, fout=6.336GHz, 0dBFS, 4:1 MUX	40	51	—	dBc
无杂散动态范围 / SFDR	SFDR	混频模式 / RF: fCLK=3.2Gsps, fout=3168MHz, 0dBFS, 2:1 MUX	50	56	—	dBc
最大工作时钟频率 / Maximum operating clock frequency	fCLK	4:1 MUX	6.4	6.4	—	GSPS
最大工作时钟频率 / Maximum operating clock frequency	fCLK	2:1 MUX	3.2	3.2	—	GSPS
最大输入数据率 / Maximum input data rate	fDATA	4:1 MUX	1600	1600	—	MSPS
最大输入数据率 / Maximum input data rate	fDATA	2:1 MUX	1600	1600	—	MSPS
DSP 时钟相位调整步长 / DSP clock phase adjustment step	PSS	分别采用 PIN 模式和 SPI 模式对 PSS<2:0> 进行配置，使用示波器测试 DSP 输出时钟相位。若 PSS<2:0> 步进每增加 1，DSP 时钟相位移动 0.4Tclk~0.6Tclk，则满足相位调整步长要求 / Configure PSS<2:0> in PIN mode and SPI mode respectively and measure the DSP output clock phase with an oscilloscope. If each increment of 1 in PSS<2:0> moves the DSP clock phase by 0.4Tclk~0.6Tclk, the phase adjustment step requirement is met	—			
DSP 输出时钟分频选择功能 / DSP output clock divide select function	OCDS	分别采用 PIN 模式和 SPI 模式对 OCDS 进行配置，使用示波器测试 DSP 输出时钟频率 fDSP。若 OCDS=1 时 fDSP 是 OCDS=0 时 fDSP 的二分频，则器件满足 OCDS 分频选择功能要求 / Configure OCDS in PIN mode and SPI mode respectively and measure the DSP output clock frequency fDSP with an oscilloscope. If fDSP at OCDS=1 is one-half of fDSP at OCDS=0, the divide select function requirement is met	—			

特性 / Characteristic	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
输入下分频功能 / Input down-divide function	IUCM	对 IUCM<1:0> 进行配置，使用示波器测试 DSP 输出时钟频率 fDSP。若 IUCM<1:0>=10 时 fDSP 是 IUCM<1:0>=00、01 时 fDSP 的二分频，IUCM<1:0>=11 时 fDSP 是 IUCM<1:0>=10 时 fDSP 的二分频，则器件满足 IUCM 输入下分频功能要求 / Configure IUCM<1:0> and measure fDSP with an oscilloscope. If fDSP at IUCM<1:0>=10 is one-half of fDSP at 00/01, and fDSP at 11 is one-half of fDSP at 10, the IUCM function requirement is met	—			

主要特性曲线图（电特性测试图）/ Typical Performance Characteristics

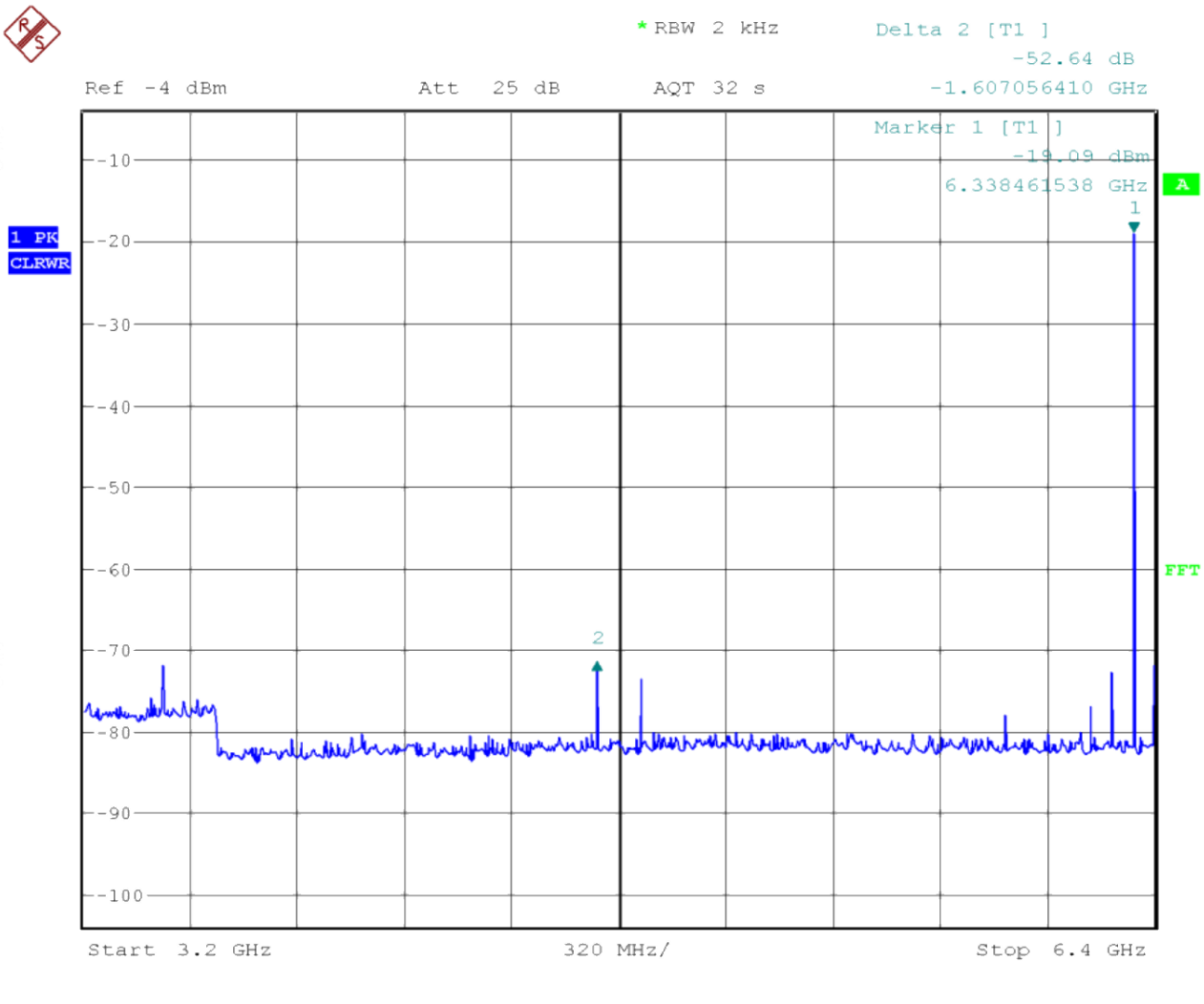


Figure 6: SFDR performance (fCLK = 6.4 GSPS, fOUT = 6.34 GHz)

典型应用线路图 / Typical Application Circuit

1 模拟输出端口 / Analog Output Port

English: The analog output needs to use a differential form, as shown in the following figures. If a single-ended signal output is needed in the application, a differential-to-single-ended balun must be used.

Note: select the appropriate coupling capacitance according to the needs of the application. (Figure 8 note.)

中文： 模拟输出需要使用差分形式，具体方式如下图所示。如果应用中需要输出单端信号，则需要使用差分转单端的 balun。

注释：根据应用的需要，选取合适的耦合电容。

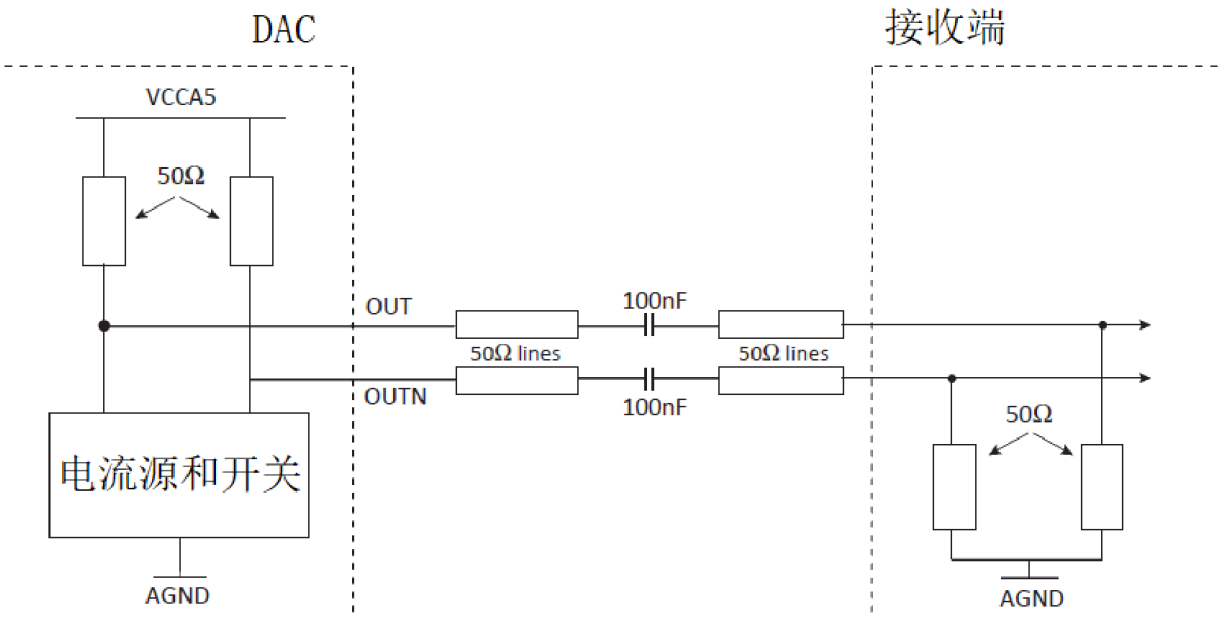


Figure 7: Differential analog output connection

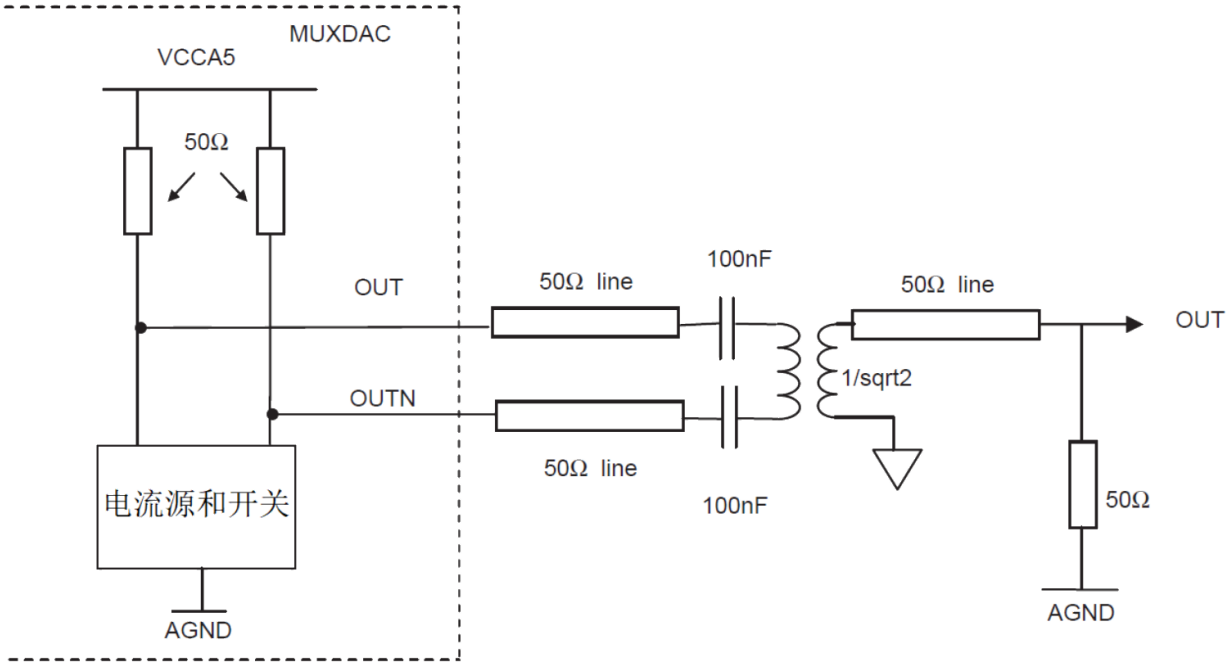


Figure 8: Analog output differential termination using a 1/2 transformer

2 时钟端口 / Clock Port

English: The clock input should use differential mode. Note: the on-chip clock buffer self-bias voltage is approximately 2.5 V.

中文： 时钟输入应该使用差分模式。注：片内时钟缓冲器自偏置电压约 2.5V。

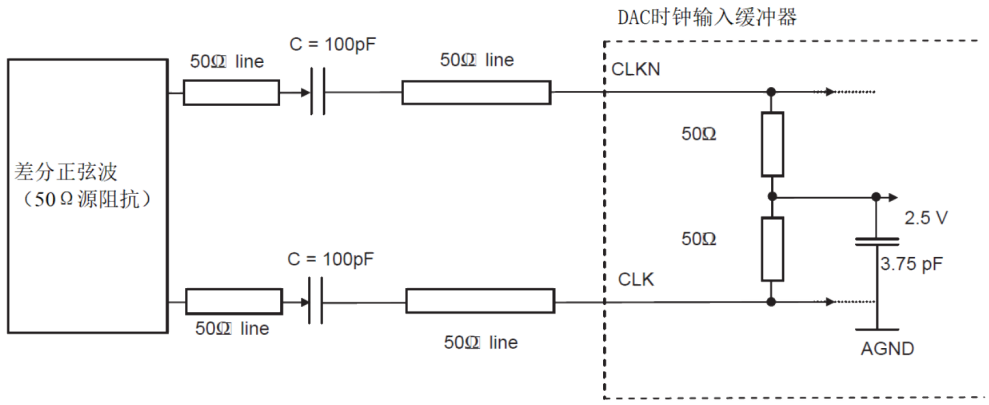


Figure 9: Differential clock connection

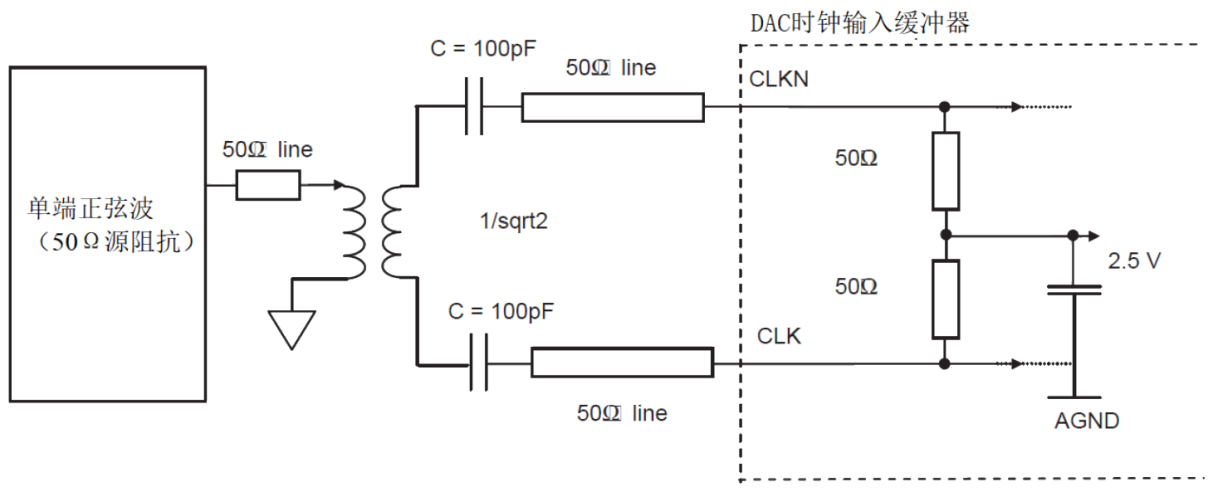


Figure 10: Differential clock connection with transformer

3 DATA、SYNC 和 IDC 输入端口 / DATA, SYNC and IDC Input Ports

English: All three signals have on-chip LVDS buffers, whose structure is shown in the following figure.

Notes: - When only two ports are used (2:1 MUX), the unused data ports should be left floating. - DATA and IDC signals use the same routing rules, and their lengths also need to be the same. - When SYNC is not used, it is recommended to connect SYNC to 1.1 V and SYNCN to 1.4 V.

中文： 三种信号片内都有 LVDS 缓冲器，缓冲器结构如下图所示。

注： - 在仅使用两路端口的情况下（2:1 MUX），未使用的数据端口应悬空。 - DATA 和 IDC 信号使用同样的布线规则，长度也需要一样。 - SYNC 不使用时，建议 SYNC 接 1.1V、SYNCN 接 1.4V。

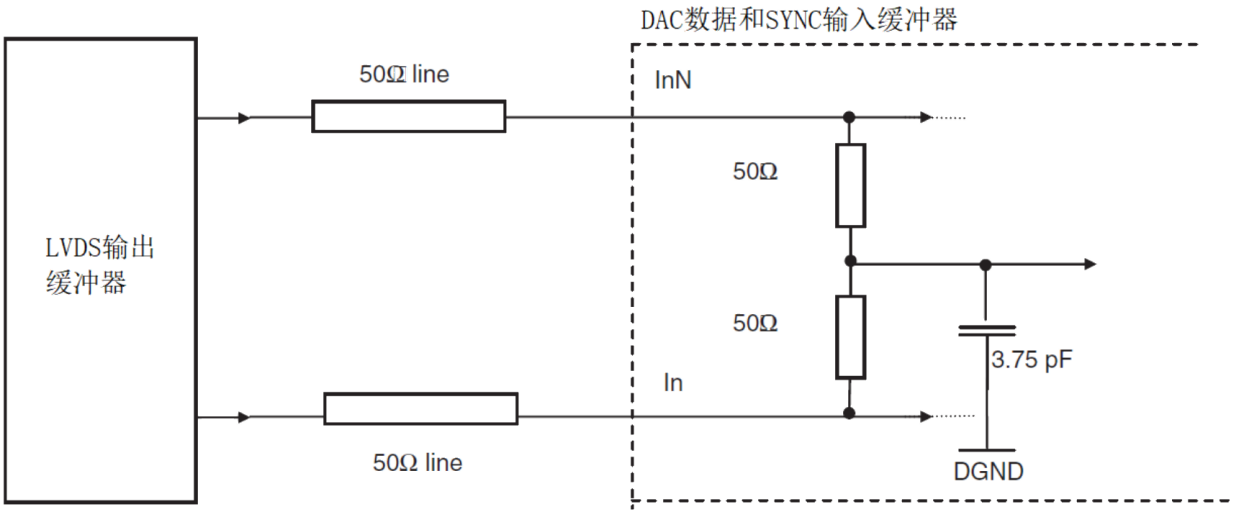


Figure 11: DATA, SYNC, IDC signal termination

4 DSP 时钟端口 / DSP Clock Port

English: The DSP and DSPN output clock signals are in LVDS format. An external 100 Ω differential termination resistor is required.

中文： DSP，DSPN 输出时钟信号是 LVDS 格式的。外部需要端接 100Ω 差分电阻。

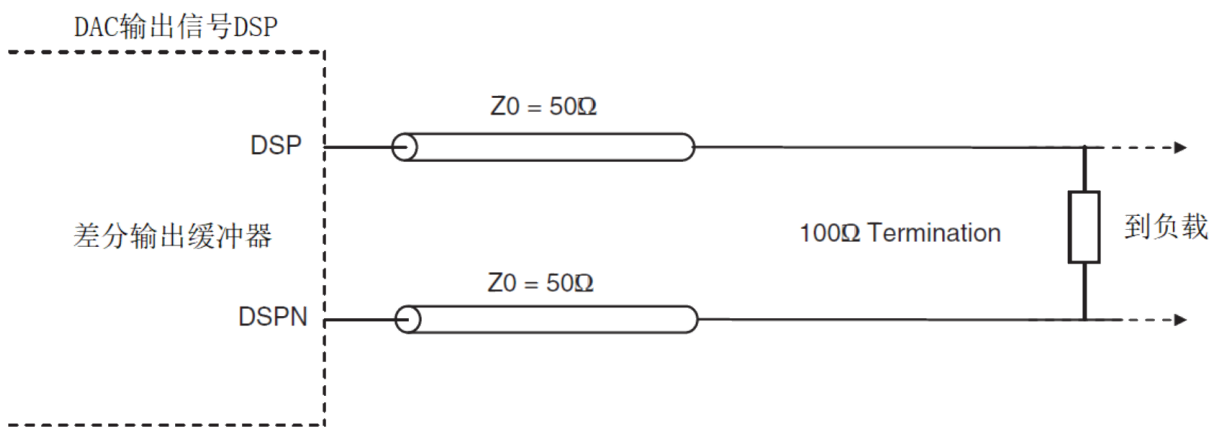


Figure 12: DSP port connection

5 控制信号配置 / Control Signal Configuration

English: The PSS and OCDS control signals use the same input buffer. - Logic "1": 200 KΩ to ground, or connected to a place at VCCD = 3.3 V, or left floating - Logic "0": 10Ω to ground

The control signals can be driven by an FPGA: - Logic "1" > VIH or VCCD = 3.3 V - Logic "0" < VIL or equal to 0 V

中文： PSS 和 OCDS 控制信号使用同样的输入缓冲器。 - Logic "1"：200 KΩ 接地，或者连接到 VCCD =3.3V 的地方，或者保持悬空 - Logic "0"：10Ω 接地

控制信号可以由 FPGA 驱动： - 逻辑"1" > VIH 或者 VCCD = 3.3V - 逻辑"0" < VIL 或者等于 0V

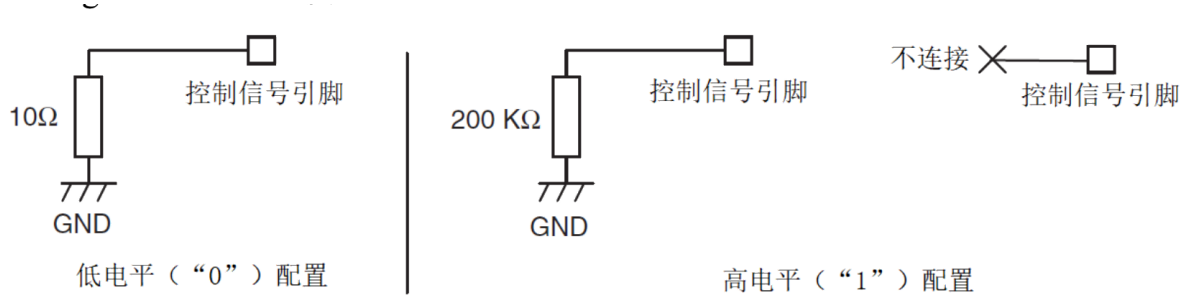


Figure 13: Control signal configuration



Figure 14: Control signals configured through FPGA

6 TVF 控制信号 / TVF Control Signal

English: TVF is a 3.3 V CMOS output signal, which can be captured by an FPGA. To change the VOL/VOH values, pull-up/pull-down resistors or a potentiometer need to be used.

中文： TVF 是 3.3V 的 CMOS 输出信号，FPGA 可以捕获该信号。为了改变 VOL/VOH 的值，需要使用上拉/下拉电阻或电位器。



Figure 15: Control signals configured through FPGA

7 电源及解耦电容 / Power Supplies and Decoupling Capacitors

English: The DAC needs 3 different supplies: VCCA5 = 5 V (for the analog core), VCCA3 = 3.3 V (for the analog section), and VCCD = 3.3 V (for the digital section).

When configuring supply-to-ground decoupling, the capacitors need to be as close to the chip as possible, using 100 pF in parallel with 10 nF capacitors. The minimum number of decoupling capacitors needed can be calculated from the number of adjacent pins.

For the VCCA5 supply, 4 pairs of 100 pF in parallel with 10 nF capacitors are needed; VCCA3 needs 4 pairs of the above capacitors, and VCCD needs 10 pairs of the above capacitors.

Each supply rail needs decoupling capacitors set as close as possible; one possible value is 100 nF in parallel with 22 uF capacitors (the best capacitance value depends on the voltage regulator).

中文： DAC 需要 3 种不同的电源：VCCA5=5V（用于模拟核）、VCCA3=3.3V（用于模拟部分）和 VCCD=3.3V（用于数字部分）。

当配置电源到地解耦电源时，电容需要尽可能地靠近芯片，使用 100pF 并联 10nF 的电容器。可以通过临近的 Pin 脚数量来计算所需要的最少解耦电容数量。

对 VCCA5 电源而言，需要 4 对 100pF 并联 10nF 的电容器，VCCA3 需要 4 对上述电容，VCCD 需要 10 对上述电容。

每一路供电电源都需要尽可能近的设置解耦电容，一个可能的值是 100nF 和 22uF 并联的电容器（最佳电容值取决于稳压器）。

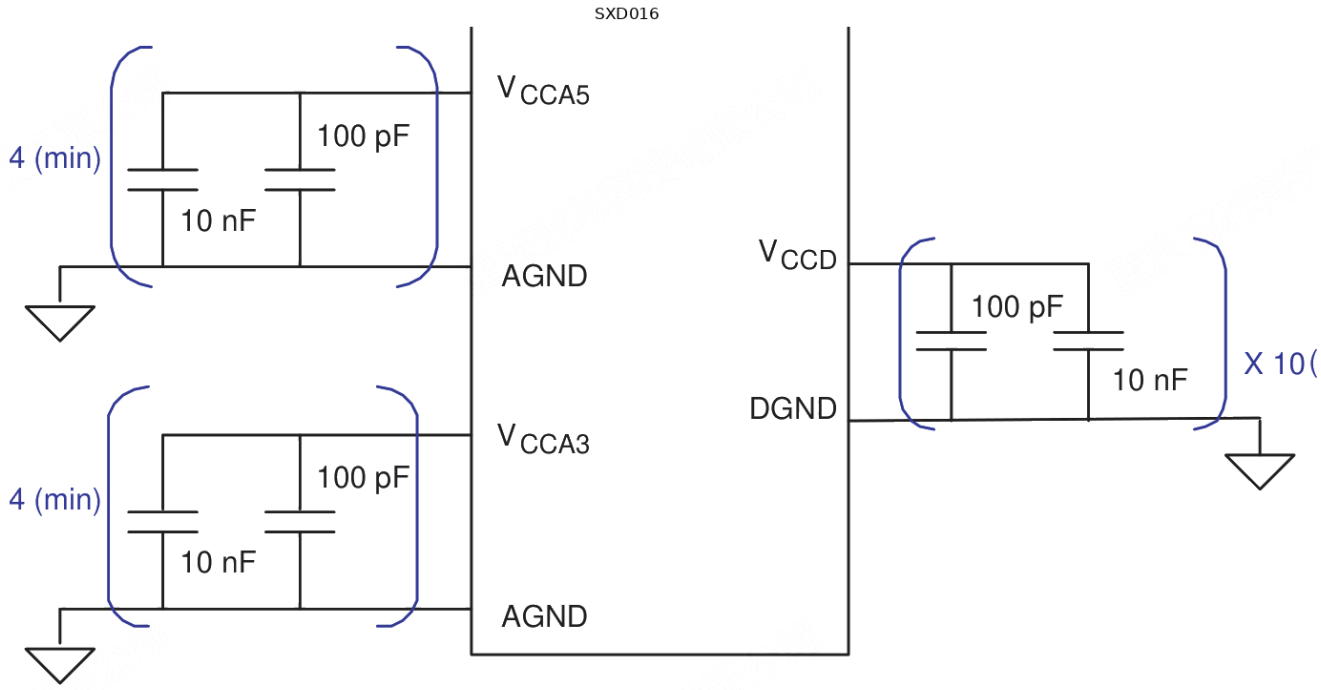


Figure 16: Decoupling capacitor configuration

8 上电/断电要求 / Power-Up/Power-Down Requirements

English: During power-up of this circuit's supplies VCCA3 and VCCD, the maximum voltage difference between the two supplies is required to be ⩽1.2 V, as shown in Figure 17. To meet this requirement, the following supply methods are recommended for VCCA3 and VCCD: - Use the same LDO to power up VCCA3 and VCCD simultaneously, with the two supplies isolated from each other by ferrite beads; - Use two LDOs of the same model to supply VCCA3 and VCCD independently. The two LDOs have the same power-up time setting (i.e., soft start), the same enable signal, and the same input supply.

If VCCA3 and VCCD do not use the above supply methods, the maximum voltage difference between the two supplies is still required to be ⩽1.2 V.

There is no specific requirement for power-down of this circuit.

Note: the power-up time of supplies VCCD and VCCA3 needs to be controlled to <40 ms.

中文： 本电路电源 VCCA3 和 VCCD 在上电过程中，要求两个电源间最大电压差 ⩽1.2V，如图 19 所示。为满足此要求，VCCA3 和 VCCD 供电建议采用以下方式： - 使用同一个 LDO 对 VCCA3 和 VCCD 同时上电，两个电源间利用磁珠相互隔离； - 使用两个同型号 LDO 各自对 VCCA3 和 VCCD 专用独立供电。这两个 LDO 上电时间设置（即软启动）相同，使能信号相同，输入电源相同。

如果 VCCA3 和 VCCD 未采用以上供电方式，则要求两个电源间最大电压差 ⩽1.2V。

本电路断电没有特定要求。

注意：电源 VCCD 和 VCCA3 上电时间需控制在 <40ms。

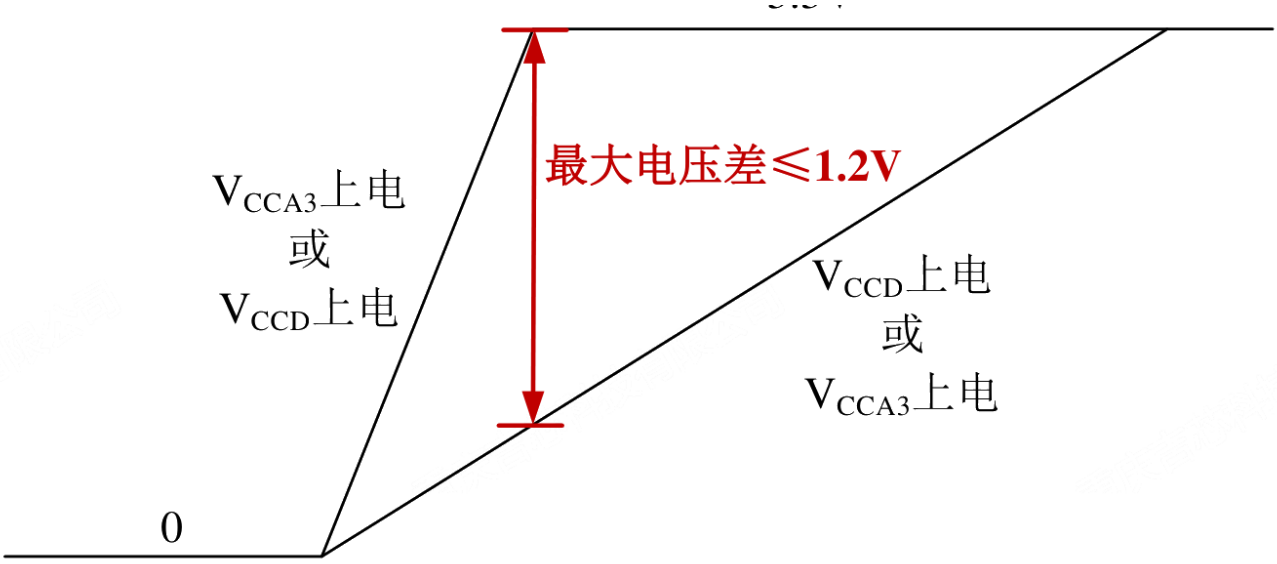


Figure 17: Power-up timing requirements

单元模块及工作原理 / Functional Blocks and Operating Principles

1 几种输出模式的说明 / Output Modes

a. 非归零（NRZ）输出模式 / Non-Return-to-Zero (NRZ) Output Mode

English: This mode works in the first Nyquist zone, and its overall attenuation is smaller than that of the return-to-zero (RTZ) mode. However, due to the sin(x)/x gain roll-off, working in the second Nyquist zone is not recommended.

中文： 这种模式工作在第一 Nyquist 区，总体衰减比归零（RTZ）模式小。但由于 sin(x)/x 的增益滚降，不建议在第二 Nyquist 区工作。

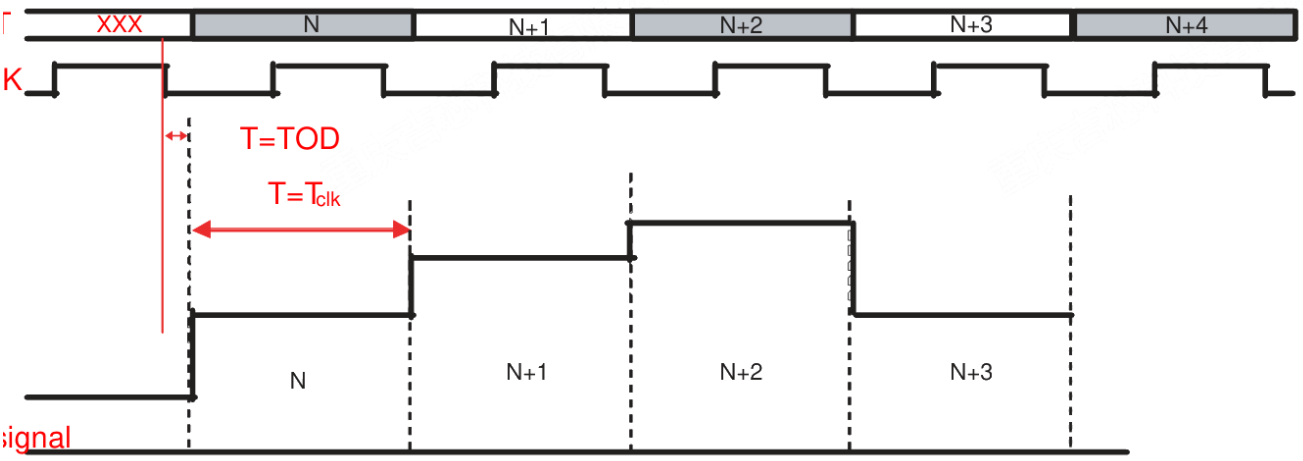


Figure 18: NRZ mode timing diagram

b. 窄归零（NRTZ）输出模式 / Narrow Return-to-Zero (NRTZ) Output Mode

English: This mode has the following advantages: - Optimizes the fundamental power in the first Nyquist zone and the beginning of the second Nyquist zone. - Improves dynamic performance. - Improves the noise floor performance. - Is a compromise between the NRZ and RTZ modes.

中文： 这种模式有以下一些优点： - 优化了第一 Nyquist 区和第二 Nyquist 区开始部分基波功率。 - 提升了动态性能。 - 改善了噪底性能。 - 是 NRZ 和 RTZ 两种模式之间的折中。

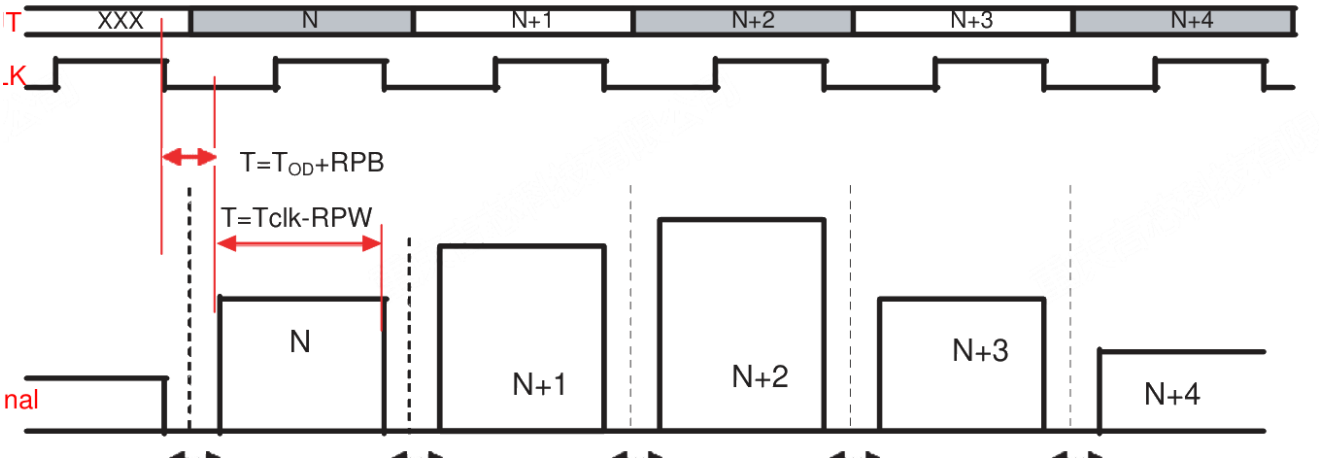


Figure 19: NRTZ mode timing diagram

c. 归零（RTZ）输出模式 / Return-to-Zero (RTZ) Output Mode

English: In return-to-zero mode, the circuit can work in the second Nyquist zone, but the disadvantage is that the attenuation is larger than in the first Nyquist zone. Its advantages are as follows: - Sinc function roll-off. - Improved dynamic performance.

中文： 归零模式下，电路可以工作在第二 Nyquist 区工作，但缺点是衰减比第一 Nyquist 区大。优点如下： - Sinc 函数滚降。 - 改善动态性能。

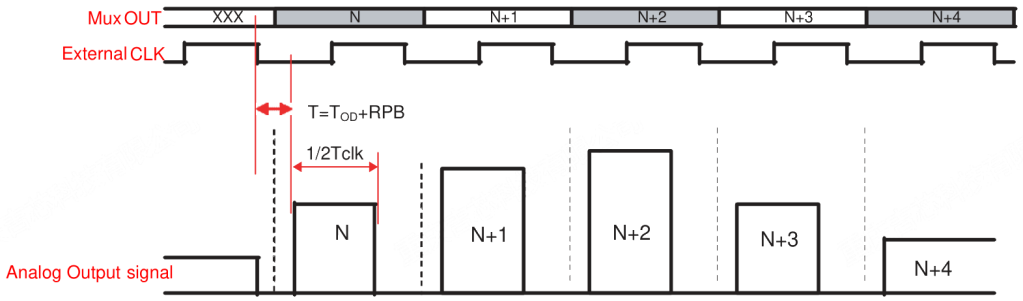


Figure 20: RTZ mode timing diagram

d. 混频（RF）模式 / Mixing (RF) Mode

English: The advantage of RF mode is that it can output relatively high-frequency signals, and its attenuation in the second Nyquist zone is smaller than that of RTZ mode. Unlike NRZ and RTZ modes, RF mode has large attenuation near DC and 2N*fCLK, but very small attenuation at fout = fCLK. Its advantages

are as follows: - Suitable for working in the second and third Nyquist zones. - Extrapolating the dynamic envelope curve, the spectrum at fCLK does not deteriorate abruptly.

中文： RF 模式的优点是可以输出比较高的频率信号，在第二 Nyquist 区衰减比 RTZ 模式小。和 NRZ 及 RTZ 模式不同，RF 模式在 DC 和 2N*fCLK 附近衰减很大，但在 fout=fCLK 处衰减很小。优点如下： - 适合工作于第二和第三 Nyquist 区。 - 外推动态包络曲线，fCLK 处频谱不会陡然变差。

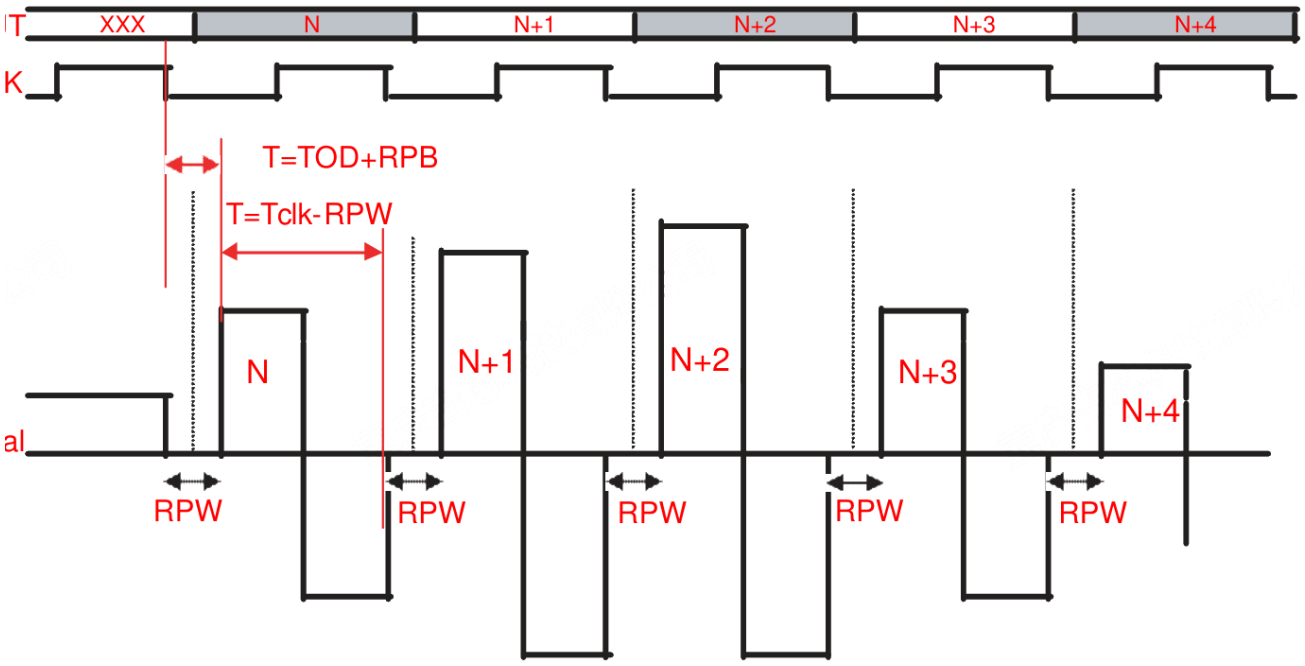


Figure 21: RF mode timing diagram

2 相移选择功能（PSS)/ Phase Shift Select Function (PSS)

English: This circuit can adjust the phase relationship between the input sampling clock (CLK) and the DSP output clock. The DSP clock output phase can be adjusted within a range of 3.5 input clock (CLK) cycles, in steps of 0.5 input clock (CLK) cycles. The three-bit SPI control code word PSS[2:0] can be used for the phase selection function.

By changing these three bits between 0 and 1, the DSP clock delay can be changed, thereby synchronizing the DAC input data and the sampling clock (the DSP clock can be provided to the FPGA for generating the DAC input data). These three control bits can be controlled through the pins PSS[2:0], or through SPI control. Which control method is effective depends on the SPI control bit ECDC.

To ensure synchronization between the sampling clock and the input data, the TVF signal can be monitored to determine how many steps the DSP clock needs to be delayed.

Note: in 4:1 MUX mode, all 8 settings are meaningful; in 2:1 MUX mode, only the first four settings are meaningful, and the last four settings produce the same result.

中文： 本电路可以调整输入采样时钟（CLK）和 DSP 输出时钟之间的相位关系。DSP 时钟输出相位可以在 3.5 个输入时钟（CLK）周期范围内进行调节，每步 0.5 个输入时钟（CLK）周期。三位 SPI 控制码字 PSS[2:0] 可用于相位选择功能。

通过改变此三位 0 或 1 可以改变 DSP 时钟延迟，从而可以同步 DAC 输入数据和采样时钟（DSP 时钟可提供给 FPGA 用于产生 DAC 输入数据）。这三位控制位可以通过引脚 PSS[2:0] 控制，也可以通过 SPI 控制。哪种控制方式有效取决于 SPI 控制位 ECDC 位。

为了确保采样时钟与输入数据间同步，可以通过监控 TVF 信号确定 DSP 时钟需要延迟多少步。

注：在 4:1 MUX 模式，8 个设置均有意义；在 2:1 MUX 模式，只有前四个设置有意义，后面四个设置产生相同的结果。

表 1 / Table 1: PSS[2:0] 码值表 / PSS[2:0] code values

符号 / Symbol	数值 / Value	含义 / Meaning
PSS[2:0]	000	DSP 输出没有延迟 / No DSP output delay
	001	DSP 输出延迟 0.5 个主时钟周期 / DSP output delayed by 0.5 master clock cycles
	010	DSP 输出延迟 1 个主时钟周期 / 1 master clock cycle
	011	DSP 输出延迟 1.5 个主时钟周期 / 1.5 master clock cycles
	100	DSP 输出延迟 2.0 个主时钟周期 / 2.0 master clock cycles
	101	DSP 输出延迟 2.5 个主时钟周期 / 2.5 master clock cycles
	110	DSP 输出延迟 3.0 个主时钟周期 / 3.0 master clock cycles
	111	DSP 输出延迟 3.5 个主时钟周期 / 3.5 master clock cycles

表 PSS[2:0]码值表

符号	数值	含义
PSS[2:0]	000	DSP输出没有延迟
	001	DSP输出延迟0.5个主时钟周期
	010	DSP输出延迟1个主时钟周期
	011	DSP输出延迟1.5个主时钟周期
	100	DSP输出延迟2.0个主时钟周期
	101	DSP输出延迟2.5个主时钟周期
	110	DSP输出延迟3.0个主时钟周期
	111	DSP输出延迟3.5个主时钟周期

采样时钟与输入数据间同步，可以通过监控 TVF 信号确定 DSP

Figure 22: PSS timing diagram (4:1 MUX, OCDS = 0)

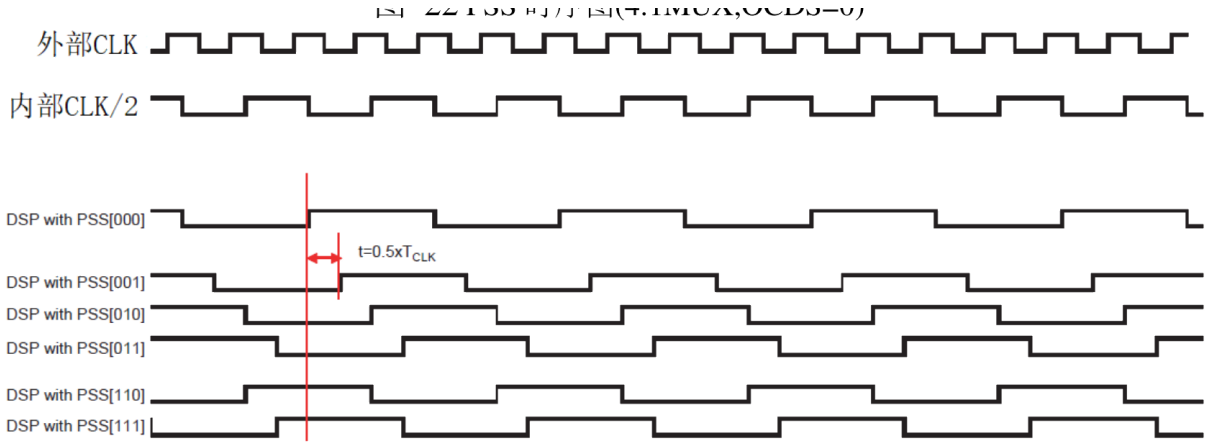


Figure 23: PSS timing diagram (2:1 MUX, OCDS = 0)

3 输出时钟分频选择功能（OCDS)/ Output Clock Divide Select Function (OCDS)

English: This circuit can set the internal divide factor of the DSP output clock to 1 or 2. The DSP output clock frequency equals fCLK/(2NX*M), where N is the MUX ratio (2 or 4), M is the IUCM ratio (1, 2, or 4), and X is the output clock divide select factor (OCDS) (1 or 2). The X value can be controlled through the OCDS bit in SPI, or through the OCDS pin. Which method is effective depends on the ECDC bit in SPI.

When the frequency required by the FPGA receiving the DSP clock is low enough, using the OCDS function allows the FPGA to not need to divide the DSP clock, thereby avoiding the phase uncertainty of FPGA division. In this case, the phase of the FPGA internal clock is the phase of the DSP clock. When a system uses multiple DACs and multiple FPGAs, after synchronizing all DACs, the OCDS function can more easily ensure a deterministic phase relationship among all FPGAs.

中文： 本电路可以设置 DSP 输出时钟内部分频因子为 1 或 2。DSP 输出时钟频率等于 fCLK/(2NX*M)，其中 N 为 MUX 比值（2 或 4)，M 为 IUCM 比值（1、2 或 4)，X 为输出时钟分频选择因子（OCDS)(1 或 2)。X 值可以通过 SPI 中 OCDS 位控制，也可以通过 OCDS 引脚控制。具体哪种方式有效取决于 SPI 中 ECDC 位。

当 FPGA 接收 DSP 时钟要求频率足够低时，使用 OCDS 功能可以让 FPGA 不需要对 DSP 时钟进行分频，从而避免了 FPGA 分频相位的不确定性。这种情况下 FPGA 内部时钟的相位就是 DSP 时钟的相位。当一个系统使用多个 DAC 和多个 FPGA 时，在同步所有 DAC 后，OCDS 功能可以更容易确保所有 FPGA 之间确定的相位关系。

表 2 / Table 2: OCDS 码值表 / OCDS code values

符号 / Symbol	数值 / Value	含义 / Meaning
OCDS	0	DSP 时钟频率 = fCLK/(2NM) / DSP clock frequency = fCLK/(2NM)
	1	DSP 时钟频率 = fCLK/(2NM2) / DSP clock frequency = fCLK/(2NM2)

表 2 OCDS 码值表

符号	数值	含义
OCDS	0	DSP时钟频率=f_{CLK}/(2*N*M)
	1	DSP时钟频率=f_{CLK}/(2*N*M*2)

Figure 24: OCDS timing diagram (4:1 MUX, IUCM = 1)

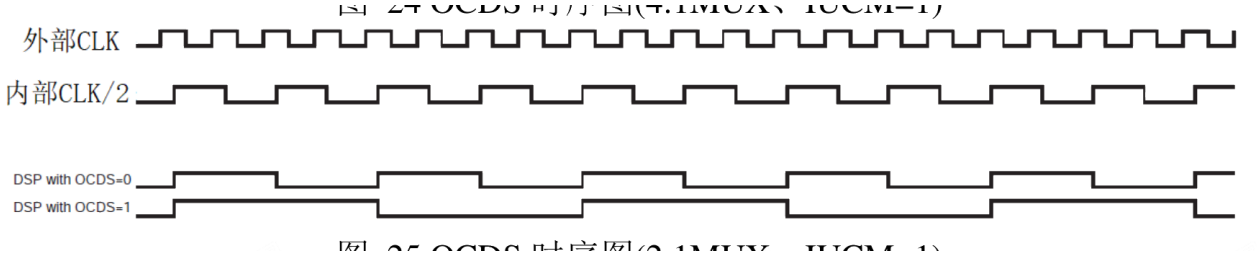


Figure 25: OCDS timing diagram (2:1 MUX, IUCM = 1)

4 输入下分频模式（IUCM)/ Input Down-Divide Mode (IUCM)

English: Three input down-divide modes of this circuit are available; this function can reduce the input data rate to 1/2 or 1/4 of the data rate required by the sampling clock. These modes can be applied in both 4:1 MUX and 2:1 MUX modes.

The working principle of this function is to apply a divide select factor (1, 2, or 4) between the DAC core clock section and the MUX clock section. The three operating modes can be selected through SPI: - IUCM1: the MUX uses the same clock as the DAC core section (default mode); - IUCM2: the MUX uses the DAC core section clock divided by two; - IUCM4: the MUX uses the DAC core section clock divided by four.

In IUCM1 mode, if the DAC conversion rate is fCLK, then in 4:1 MUX mode the input data rate is fCLK/4, and the DSP output clock frequency is fCLK/(2N*X), where N is the MUX ratio (2 or 4) and X is the OCDS ratio (1 or 2).

In IUCM2 mode, if the DAC conversion rate is fCLK, then in 4:1 MUX mode the input data rate is fCLK/8, and the DSP output clock frequency is fCLK/(2NX2), where N is the MUX ratio (2 or 4) and X is the OCDS ratio (1 or 2). This means that in input down-divide mode, the DAC can process data at 1/2 of the nominal data rate, but the sampling frequency is still fCLK.

中文： 本电路三种输入下分频模式可以得到，此功能可以降低输入数据率到采样时钟所需数据率的 1/2 或 1/4。这些模式在 4:1 MUX 和 2:1 MUX 模式均可以应用。

此功能工作原理就是在 DAC 内核时钟部分和 MUX 时钟部分之间应用一个分频选择因子（1、2 或 4）。通过 SPI 可以选择这三种工作模式： - IUCM1：MUX 使用与 DAC 内核部分相同时钟（默认模式）； - IUCM2：MUX 使用 DAC 内核部分时钟二分频后时钟； - IUCM4：MUX 使用 DAC 内核部分时钟四分频后时钟。

在 IUCM1 模式，如果 DAC 转换速率为 fCLK，那么在 4:1 MUX 模式输入数据率为 fCLK/4，DSP 输出时钟频率为 fCLK/(2N*X)，其中 N 为 MUX 比值（2 或 4），X 为 OCDS 比值（1 或 2）。

在 IUCM2 模式，如果 DAC 转换速率为 fCLK，那么在 4:1 MUX 模式输入数据率为 fCLK/8，DSP 输出时钟频率为 fCLK/(2NX2)，其中 N 为 MUX 比值（2 或 4），X 为 OCDS 比值（1 或 2）。这意味着在输入下分频模式，DAC 可以处理 1/2 标称数据率的数据，但是采样频率仍然是 fCLK。

表 3 / Table 3: IUCM 码值表 / IUCM code values

名称 / Name	值 / Value	描述 / Description	默认设置 / Default
IUCM<1:0>	00 or 01	IUCM1	00 (IUCM1)
	10	IUCM2	

名称 / Name	值 / Value	描述 / Description	默认设置 / Default
	11	IUCM4	

5 FPGA 与 DAC 的同步：IDC_P, IDC_N, TVF 功能 / FPGA-to-DAC Synchronization: IDC_P, IDC_N, TVF Functions

English: - IDC_P, IDC_N: input data check function (LVDS signals). - TVF: timing violation flag.

The IDC_P and IDC_N signals are LVDS signals; this pair of signals is synchronized with the other data bits and toggles every data cycle. This pair of signals should be generated by the FPGA, so that the DAC can check in real time whether the timing between the FPGA and the DAC is synchronized. Whether they are synchronized can be characterized by the TVF flag. The IDC signal routing should be consistent with the other data signals (same layout rules and same length). When not used, the IDC signals should be set to an LVDS low or high level.

The TVF signal is a 3.3 V output signal, which can characterize whether the DAC and FPGA are synchronized. When the TVF signal is 1, it is recommended to adopt either of the following measures: - Move the DSP output clock timing (through the PSS function). When TVF is 1, in 4:1 MUX mode, increase the PSS setting by 4; in 2:1 MUX mode, increase the PSS setting by 2. - Move the phase of the clock generated by the FPGA PLL, thereby changing the input data phase.

中文： - IDC_P, IDC_N：输入数据检查功能（LVDS 信号）。 - TVF：时序违反标志。

IDC_P, IDC_N 信号是 LVDS 信号，这对信号与其它数据位同步，并且每个数据周期都翻转。这对信号应由 FPGA 产生，从而 DAC 可以实时检查 FPGA 与 DAC 之间时序是否同步。是否同步信息可以通过 TVF 标志表征。IDC 信号布线方式应该与其它数据信号保持一致（相同版图规则和相同长度）。当不使用时，IDC 信号应设置为 LVDS 低或高电平。

TVF 信号是一个 3.3V 输出信号，可以表征 DAC 与 FPGA 是否同步。当 TVF 信号为 1 时，建议采用以下任一种措施： - 移动 DSP 输出时钟时序（可以通过 PSS 功能）。当 TVF 为 1 时，在 4:1 MUX 模式，PSS 设置增加 4；在 2:1 MUX 模式，PSS 设置增加 2。 - 移动 FPGA PLL 产生时钟相位，从而改变输入数据相位。

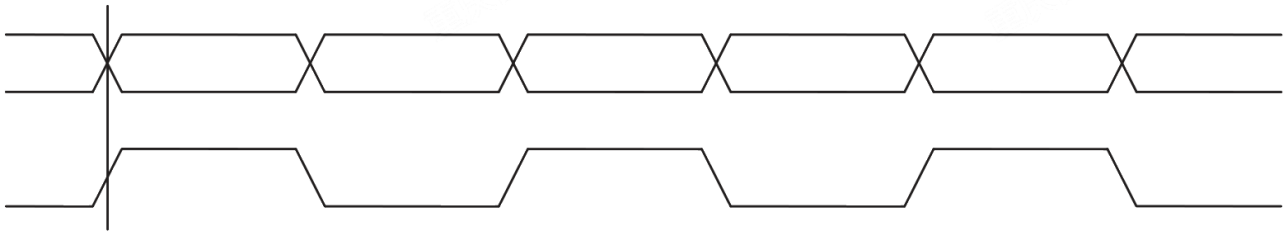


Figure 26: Timing diagram between IDC and input data

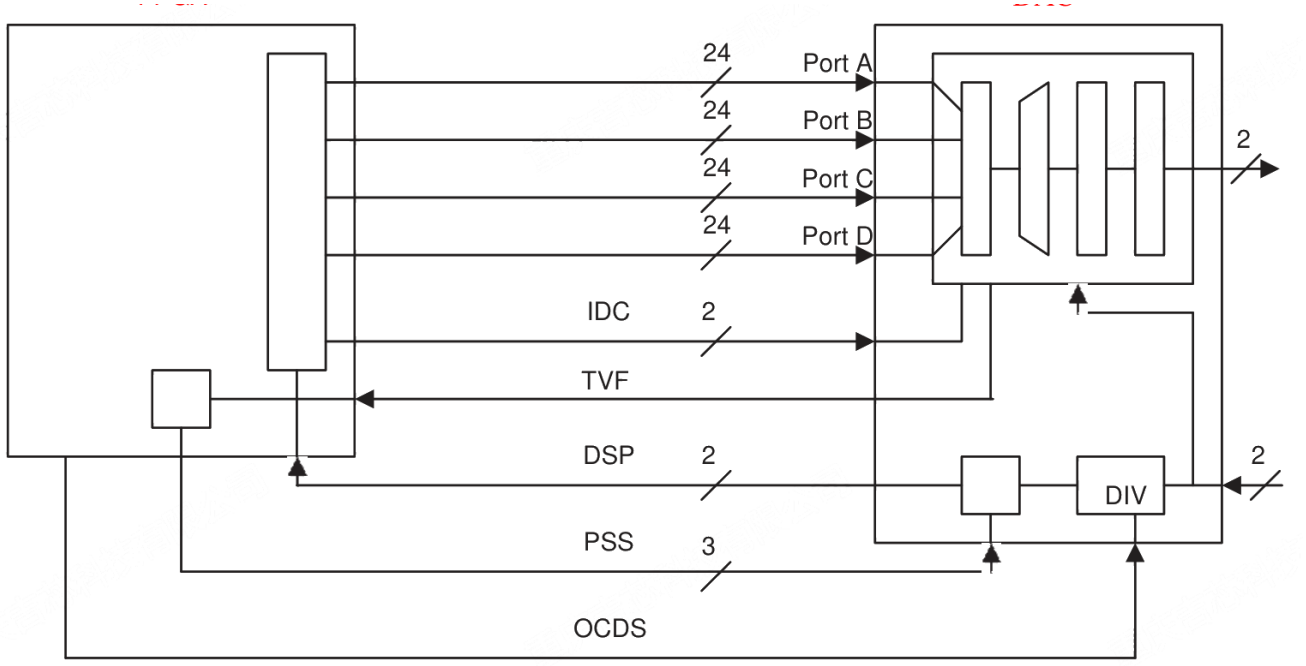


Figure 27: Logic diagram between FPGA and DAC

表 4 / Table 4: TVF 信号码值表 / TVF signal code values

符号 / Symbol	数值 / Value	含义 / Meaning
TVF	0	时序同步正常 / Timing synchronization normal
	1	检测到数据建立时间或保持时间违法 / Data setup time or hold time violation detected

6 DSP 输出时钟 / DSP Output Clock

English: The DSP output clock (DSP, DSPN) is an LVDS signal, which can be used to synchronize the FPGA in generating digital code words for the DAC. The DSP clock frequency is a fraction of the sampling clock frequency; the divide ratio depends on the OCDS and IUCM settings.

fDSP = fCLK/(2NXM) fDataRate = fCLK/(NM)

where N is the MUX ratio (2 or 4), X is the output clock divide factor (OCDS) (1 or 2), and M is the IUCM value (1, 2, or 4).

中文： DSP 输出时钟（DSP、DSPN）是 LVDS 信号，可用于同步 FPGA 产生数字码字给 DAC。DSP 时钟频率是采样时钟频率的分数，分频比取决于 OCDS 和 IUCM 设置。

fDSP=fCLK/(2NXM) fDataRate=fCLK/(NM)

其中 N 为 MUX 比值（2 或 4）、X 是输出时钟分频因子（OCDS)(1 或 2)、M 是 IUCM 值（1、2 或 4）。

7 多芯片同步 / Multi-Chip Synchronization

English: After any of the following configuration changes, the state machine inside the DAC must be reset: - After power-up; - Any change in the OCDS, MUX, or IUCM values; - Changes in parameters such as the master clock amplitude or frequency.

To achieve multi-chip synchronization, a SYNC synchronization operation needs to be generated.

When a pulse signal is applied to the SYNC/SYNCN input, the DSP clock signal stops for a determinable period of time, and then the DSP clock restarts.

The SYNC signal is an LVDS signal, active high. It can be used to synchronize multiple DACs. In OCDS = 1, IUCM = 1 mode, the width of the SYNC pulse is at least three master clock cycles, and the width of the SYNC pulse must be an integer number of clock cycles.

中文： 在以下配置改变后，DAC 内部的状态机必须复位： - 在上电后； - OCDS、MUX、IUCM 值任一个发生变化； - 主时钟幅度、频率等参数发生变化。

为了实现多芯片同步，需要产生一个 SYNC 同步操作。

当一个脉冲信号应用到 SYNC/SYNCN 输入后，DSP 时钟信号会停止一段可确定的时间，然后 DSP 时钟重启。

SYNC 信号是一个 LVDS 信号，高电平有效。它可以用于同步多个 DAC。在 OCDS=1、IUCM=1 模式下，SYNC 脉冲的宽度至少三个主时钟周期，并且 SYNC 脉冲的宽度必须是时钟周期的整数。

8 增益调节功能 / Gain Adjustment Function

English: This function is used to adjust the output gain of the DAC, and can be adjusted through the GAIN register in SPI. Nominal adjustment range: output voltage × (1 ± 15%).

中文： 这个功能用于调节 DAC 的输出增益，可以通过 SPI 中 GAIN 寄存器进行调节。标称调节范围：输出电压*（1±15%）。

9 SPI 功能描述 / SPI Function Description

a. SPI 时序描述 / SPI Timing Description

English: This SPI has only a write function and no read function, and contains four signals: - reset_n: asynchronous reset, active low; - sclk: serial clock input; - sld_n: serial enable input; - sdata: serial data input.

This SPI has 16 different register addresses, and each register address can store 12 bits of data. The SPI input format sends the 4-bit register address first, then the 12-bit data; both address and data are MSB first.

The SPI write steps are fully synchronized with the rising edge of the sclk clock, as shown in the figure below.

sld_n and sdata are sampled on each rising edge of sclk. When there is no write operation, sld_n must be set to 1. A write operation starts at the first clock cycle when sld_n = 0. Before the write operation is complete, sld_n must remain 0.

During the first 4 clock cycles with sld_n = 0, the 4-bit register address (from MSB (a[3]) to LSB (a[0])) is sent; during the following 12 clock cycles with sld_n = 0, the 12-bit data (from MSB (d[11]) to LSB (d[0])) is sent.

A complete write operation requires sld_n = 0 to be held for 16 clock cycles.

Before starting a new write operation, sld_n = 1 must be held for at least one clock cycle to request the end of the previous write operation. Before the write operation is complete, sld_n = 1 in any clock cycle will interrupt the write operation, and no data will be transferred to the internal registers. After the parallel data has been transferred to the internal registers, additional sld_n = 0 clock cycles have no effect on the write operation.

The 12-bit register data must be sent together; even if the meaningful data bits of an internal register are fewer than 12 bits, the unused bits will be ignored. See the register section for the positions and meanings of the internal register data bits.

The combination of the reset_n and sld_n signals can set the chip to its default values: - reset_n high: no effect; - reset_n low, sld_n low: program the internal registers to their default values.

中文： 此 SPI 只有写功能，无读功能，包含四个信号： - reset_n：异步复位，低电平有效； - sclk：串行时钟输入； - sld_n：串行使能输入； - sdata：串行数据输入。

此 SPI 有 16 个不同寄存器地址，每个寄存器地址可存贮 12 位数据。SPI 输入格式先发送 4 位寄存器地址，然后发送 12 位数据，地址和数据都是 MSB 在前。

SPI 写步骤与 sclk 时钟上升沿完全同步，见下图。

在 sclk 的每个上升沿对 sld_n 和 sdata 进行采样。当无写操作时，sld_n 必须置为 1。一个写操作开始于 sld_n=0 时第一个时钟周期。在写操作完成前，sld_n 必须一直为 0。

在 sld_n=0 时前 4 个时钟周期，4 位寄存器地址（MSB (a[3]) 到 LSB (a[0])) 被发送；在 sld_n=0 时后 12 个时钟周期，12 位数据（MSB (d[11]) 到 LSB (d[0])) 被发送。

一个完整的写操作需要 sld_n=0 保持 16 个时钟周期。

在开始一个新写操作前，sld_n=1 至少保持一个时钟周期用于请求结束上一个写操作。在写操作完成前，任何时钟周期 sld_n=1 都会中断写操作，没有数据会被传输到内部寄存器。当并行数据已经传输到内部寄存器后，附加的 sld_n=0 时钟周期不会对写操作产生影响。

12 位寄存器数据必须一起发送，即使内部寄存器有意义数据位不足 12 位，无用位会被忽略。内部寄存器数据位位置和意义见寄存器部分。

reset_n 和 sld_n 信号组合使用可以设置芯片到默认值。 - reset_n 为高：没有影响； - reset_n 为低、sld_n 为低：编程内部寄存器到默认值。

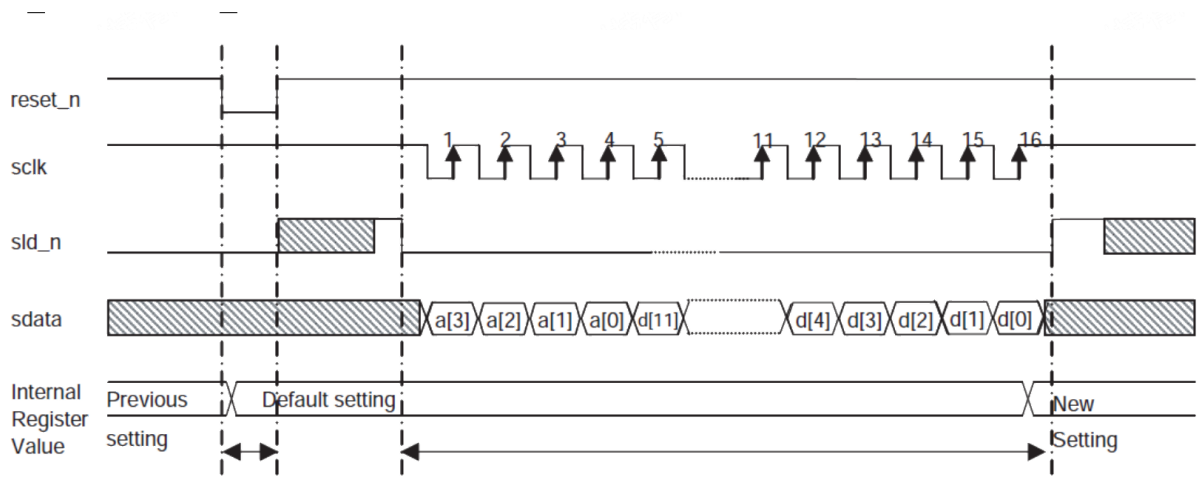


Figure 28: SPI timing diagram

表 5 / Table 5: SPI 相关时序表 / SPI timing

参数 / Parameter	描述 / Description	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
Tsclk	Sclk 时钟周期 / Sclk clock period	1			µs
Twsclk	Sclk 高低电平时间 / Sclk high/low level time	0.5			µs
Tssld_n	在 sclk 上升沿前 sld_n 建立时间要求 / sld_n setup time before sclk rising edge	4			µs
Thsld_n	在 sclk 上升沿后 sld_n 保持时间要求 / sld_n hold time after sclk rising edge	2			µs
Tssdata	在 sclk 上升沿前 sdata 建立时间要求 / sdata setup time before sclk rising edge	4			ns
Thsdata	在 sclk 上升沿后 sdata 保持时间要求 / sdata hold time after sclk rising edge	2			ns
Twlreset	reset_n 最小低电平脉冲宽度要求 / reset_n minimum low pulse width	5			ns
Tdreset	reset_n 边沿与 sclk 上升沿之间最小延迟 / Minimum delay between reset_n edge and sclk rising edge	5			µs

b. SPI 地址和数据描述 / SPI Address and Data Description

English: When sld_n goes low, the SPI is enabled. The maximum operating frequency of sclk is 1 MHz.

中文： 当 sld_n 变为低电平时，SPI 被使能。sclk 最大工作频率为 1MHz。

寄存器 / Registers

寄存器地址总表 / Register Address Map

地址 / Address	名称 / Name	描述 / Description	默认设置 / Default
0000	状态寄存器 / Status register	MUX ratio 选择；输出模式选择；IUCM ratio 选择；外部控制 DSP 时钟（ECDC）；重整形脉冲宽度（RPW）调整；重整形脉冲起点（RPB）调整 / MUX ratio select; output mode select; IUCM ratio select; external DSP clock control (ECDC); reshaping pulse width (RPW) adjustment; reshaping pulse start point (RPB) adjustment	0x922
0001	增益寄存器 / Gain register	增益调整寄存器 / Gain adjustment register	0x200
0010		不可用 / Not available	
0011		不可用 / Not available	
0100		不可用 / Not available	
0101	DSP 寄存器 / DSP register	PSS, OCDS 控制 / PSS, OCDS control	0x080
0110		不可用 / Not available	
0111		不可用 / Not available	
1000 to 1111		不可用 / Not available	

1. 状态寄存器（地址 0000)/ Status Register (Address 0000)

Bit layout (D11 → D0): RPW<2:0> (D11–D9), RPB<2:0> (D8–D6), ECDC (D5), IUCM<1:0> (D4, D3), MODE<1:0> (D2, D1), MUX (D0). Default value: 0x922.

名称 / Name	位 / Bits	值 / Value	描述 / Description	默认值 / Default	备注 / Note
MUX	D0	0	4:1 MUX 模式 / 4:1 MUX mode	0	(1)
		1	2:1 MUX 模式 / 2:1 MUX mode		
MODE<1:0>	D2, D1	00	非归零（NRZ）模式 / NRZ mode	01	(1)
		01	窄归零（NRTZ）模式 / NRTZ mode		
		10	归零（RTZ）模式 / RTZ mode		
		11	混频（RF）模式 / RF mode		
IUCM<1:0>	D3, D4	00	IUCM1	00	(1)
		01	IUCM1		
		10	IUCM2		
		11	IUCM4		
ECDC	D5	0	OCDS 和 PSS 由 DSP 寄存器（地址 0101）控制 / OCDS and PSS controlled by the DSP register (address 0101)	1	(1)(2)
		1	OCDS 和 PSS 外部控制 / OCDS and PSS externally controlled		

名称 / Name	位 / Bits	值 / Value	描述 / Description	默认值 / Default	备注 / Note
RPB<2:0>	D6, D7, D8	000	RPB2 = 38 ps	100	(3)
		001	RPB2 = 38 ps		
		010	RPB0 = 12 ps		
		011	RPB1 = 25 ps		
		100	RPB2 = 38 ps		
		101	RPB3 = 51 ps		
		110	RPB4 = 64 ps		
		111	RPB2 = 38 ps		
RPW<2:0>	D9, D10, D11	000	RPW2: 66 ps (NRTZ 模式）/ 68 ps (RF 模式)	100	(4)
		001	RPW2: 66 ps (NRTZ) / 68 ps (RF)		
		010	RPW0: 43 ps (NRTZ) / 52 ps (RF)		
		011	RPW1: 49 ps (NRTZ) / 60 ps (RF)		
		100	RPW2: 66 ps (NRTZ) / 68 ps (RF)		
		101	RPW3: 78 ps (NRTZ) / 86 ps (RF)		(5)
		110	RPW4: 66 ps (NRTZ) / 76 ps (RF)		
		111	RPW2: 66 ps (NRTZ) / 68 ps (RF)		

English: Notes: 1. In the default mode: 4:1 MUX, NRTZ output, IUCM1, PSS and OCDS externally controlled. The default mode can be set by power-on reset or by a reset_n low-level pulse while sld_n is low. 2. ECDC: when ECDC = 1, the DSP clock timing is externally controlled by pins PSS<2:0> and OCDS; when ECDC = 0, this function is controlled by the register at SPI address 0101; 3. The RPB settings can be applied to the NRTZ, RTZ, and RF output modes. The RPB values are design values. 4. The RPW settings can be applied to the NRTZ and RF output modes. The RPW values are typical values measured on one circuit. 5. From a design standpoint, when RPW > Tclk/2, the RPW value becomes Tclk – RPW. When fCLK = 6 GHz, it affects the largest RPW value (100 ps), which becomes 166.6-100 = 66.6 ps. When fCLK exceeds 5 GHz, the largest RPW value is affected (at this time RPW > Tclk/2).

中文： 注： 1. 默认模式时 4:1 MUX, NRTZ 输出，IUCM1、PSS 和 OCDS 外部控制。默认模式可以通过上电复位或当 sld_n 为低时 reset_n 低电平脉冲设置。 2. ECDC：当 ECDC=1 时，DSP 时钟时序由引脚 PSS<2:0> 和 OCDS 外部控制；当 ECDC=0 时，此功能由 SPI 地址为 0101 的寄存器控制； 3. RPB 设置可以应用于 NRTZ、RTZ 和 RF 输出模式。RPB 值是设计值。 4. RPW 设置可以应用于 NRTZ 和 RF 输出模式。RPW 值是对一只电路测量的典型值。 5. 从设计来看，当 RPW> Tclk/2 时，PRW 值就变为 Tclk – RPW。当 fCLK=6GHz 时，它影响最大的 RPW 值（100ps）变为 166.6-100=66.6ps。当 fCLK 超过 5GHz 时，最大的 RPW 值就会受到影响（此时 PRW> Tclk/2）。

2. 增益寄存器（地址 0001)/ Gain Register (Address 0001)

Bit layout (D11 → D0): GA<9:0> occupies the low 10 bits. Default value: 0x200.

3. DSP 寄存器（地址 0101)/ DSP Register (Address 0101)

Bit layout (D11 → D0): PSS<2:0> and OCDS. Default value: 0x080.

电源地间保护 / Power-to-Ground Protection

English: To improve the antistatic capability of the device, the following ESD protection circuits exist between the power pins inside the device. During power-up and normal use, avoid these ESD protection devices conducting in the forward direction for extended periods; the forward conduction value is approximately 1.15 V.

中文： 为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，上电及正常使用中应避免这些 ESD 保护管长时间正向导通，正向导通值约为 1.15V。

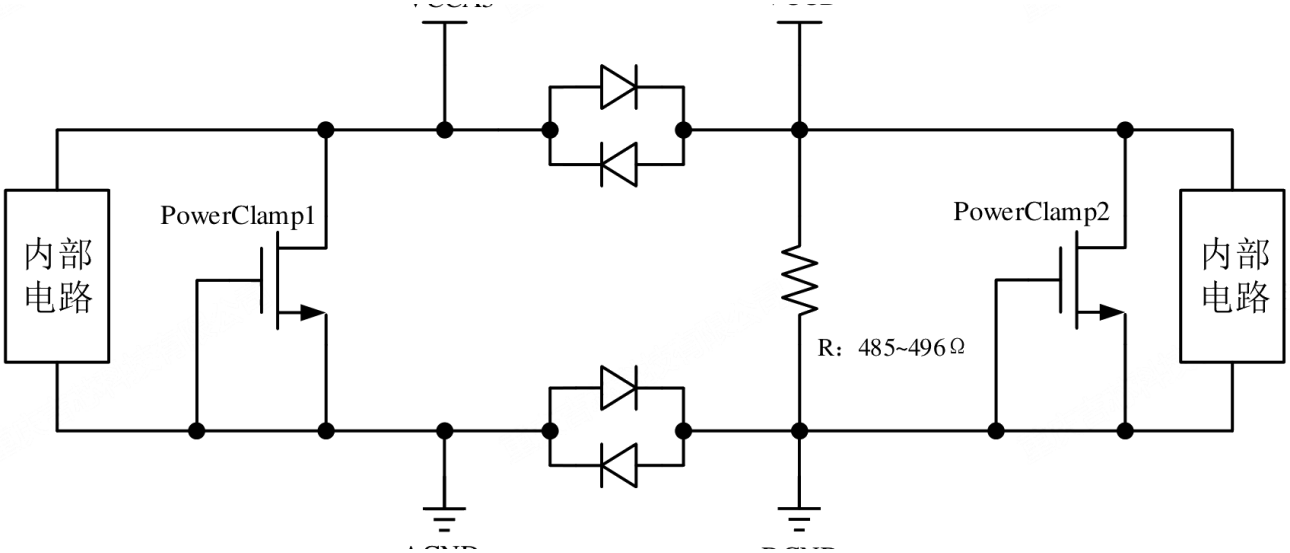


Figure 29: ESD protection circuits between internal power supplies

注意事项 / Precautions

1、产品安装注意事项 / Product Installation Notes

English: 1) Pay attention to the device orientation when soldering to avoid soldering it incorrectly. 2) Instruments and meters used for circuit debugging must have good common grounding. PCB design must maintain good grounding and power-supply decoupling. 3) Take care not to reverse the power supply or short the input/output terminals to the power supply, which can easily cause circuit damage.

中文： 1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2、产品使用注意事项 / Product Usage Notes

English: 1) It is recommended to control the ambient temperature in actual use (TA < 90°C) and pay attention to heat dissipation. 2) Power-up/power-down requirements: during power-up of this circuit's

analog supply VCCA3 and digital supply VCCD, the maximum voltage difference between the two supplies is required to be ⩽1.2 V, as shown in Figure 30. To meet this requirement, the following supply methods are recommended for VCCA3 and VCCD: - Use the same LDO to power up VCCA3 and VCCD simultaneously, with the two supplies isolated from each other by ferrite beads; - Use two LDOs of the same model to supply VCCA3 and VCCD independently. The two LDOs have the same power-up time setting (i.e., soft start), the same enable signal, and the same input supply. If VCCA3 and VCCD do not use the above supply methods, the maximum voltage difference between the two supplies is still required to be ⩽1.2 V. There is no specific requirement for power-down of this circuit. Note: the power-up time of supplies VCCD and VCCA3 needs to be controlled to <40 ms. 3) ESD precautions: the ESD protection capability of this device is 500 V human body model. Under ESD voltages exceeding this, the device is prone to ESD damage, resulting in abnormal device output. To avoid ESD damage, pay attention to the following when using this device: 1) Wear an ESD wrist strap during operation. 2) When connecting RF cables to the device output ports (OUT, OUTN), first discharge the RF cables; then, when connecting the device to the RF cables, keep the device unpowered, and power it up after the connection is successful. 3) When connecting RF cables to the device output ports (OUT, OUTN), it is recommended to simultaneously blow the device output ports (OUT, OUTN) and the RF cable connection ports with an ESD ion fan. 4) When the device output ports (OUT, OUTN) are connected to RF devices (e.g., an upconverter), keep both unpowered, and power up after the connection is successful. 5) Hot-plugging is prohibited. 6) When the device output ports (OUT, OUTN) are connected via RF cables to instruments such as a spectrum analyzer for testing, check and confirm that instruments such as the spectrum analyzer are well grounded. 7) When the unit containing this device is transported, fit protective caps on the device output ports (OUT, OUTN).

中文： 1) 建议实际使用时控制环境温度（TA<90°C），并注意散热。 2) 上电/断电要求：本电路模拟电源 VCCA3 和数字电源 VCCD 在上电过程中，要求两个电源间最大电压差 ⩽1.2V，如图 2 所示。为满足此要求，VCCA3 和 VCCD 供电推荐采用以下方式： - 使用同一个 LDO 对 VCCA3 和 VCCD 同时上电，两个电源间利用磁珠相互隔离； - 使用两个同型号 LDO 各自对 VCCA3 和 VCCD 专用独立供电。这两个 LDO 上电时间设置（即软启动）相同，使能信号相同，输入电源相同。 如果 VCCA3 和 VCCD 未采用以上供电方式，则要求两个电源间最大电压差 ⩽1.2V。本电路断电没有特定要求。注意：电源 VCCD 和 VCCA3 上电时间需控制在 <40ms。 3) 抗静电注意事项：该器件静电防护能力为人体模型 500V，该器件在超过该静电电压条件下，会容易发生静电损伤，导致器件输出异常。为避免发生静电损伤，该器件使用时需要注意以下事项： 1) 操作时佩戴静电手腕。 2) 器件输出端口（OUT、OUTN）连接射频线缆时，首先需要对射频线缆放电，然后器件连接射频线缆时器件先不上电，连接成功后再上电。 3) 推荐在器件输出端口（OUT、OUTN）连接射频线缆时，同时用除静电离子风机吹器件输出端口（OUT、OUTN）和射频线缆连接端口。 4) 器件输出端口（OUT、OUTN）与射频器件（例如上变频器）连接时，相互先不上电，连接成功后才上电。 5) 禁止热插拔。 6) 器件输出端口（OUT、OUTN）通过射频线缆与频谱分析仪等仪器连接进行测试时，检查确认频谱分析等仪器接地情况良好。 7) 该器件所在单机转运时，器件输出端口（OUT、OUTN）加保护帽。

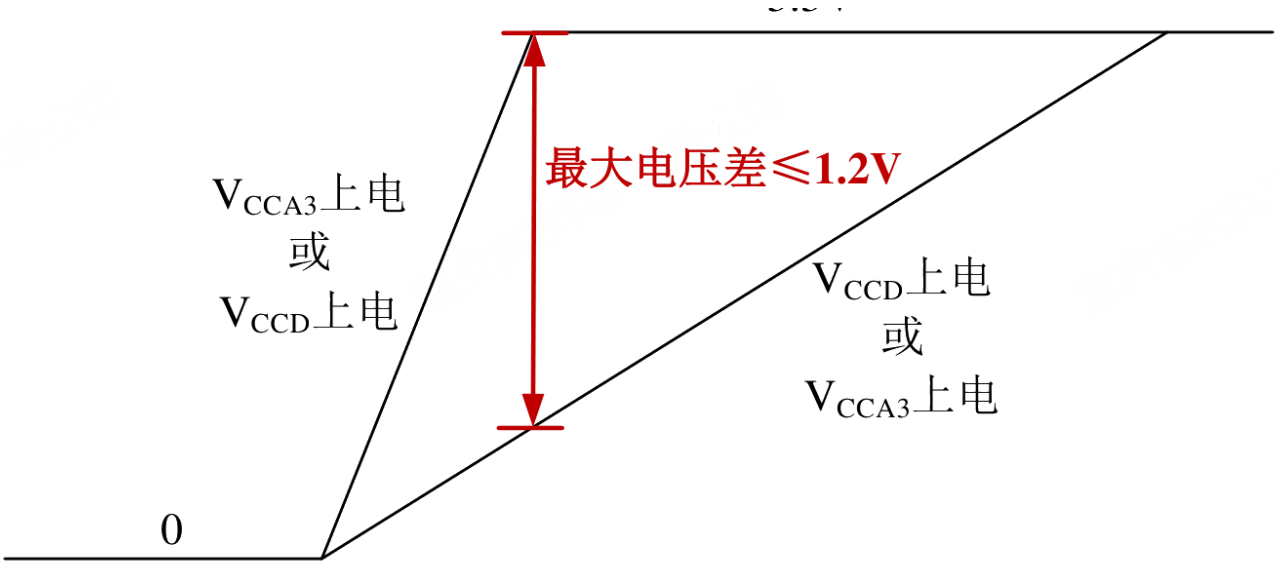


Figure 30: Power-up timing requirements

3、产品防护注意事项 / Product Protection Notes

English: 1) Temperature, humidity, and environment requirements for finished-product warehouse storage: temperature 10°C~25°C, relative humidity 25%~70%, electrostatic discharge sensitivity Class 1B (500~999 V). All terminals of this circuit have ESD protection structures; however, large-energy electrical pulses may still damage the circuit, so ESD protection should be observed during testing, handling, and storage. 2) Product storage period: counted from the inspection-lot identification code date; when the storage period of warehoused products exceeds 36 months, the products should be stored in a special cabinet for expired products, and the products must pass re-inspection before use. 3) It is recommended to use the product within 4 hours after unpacking; if exposed to air for more than 4 hours, it is recommended to perform high-temperature baking at 150°C for 8 h, then vacuum-package it and place it in a drying cabinet. 4) Avoid dropping the product during use to avoid mechanical stress damage. 5) Exceeding the absolute maximum ratings may cause permanent damage to the device. The maximum ratings do not indicate that the device can work normally under those conditions or under any other conditions beyond those shown in this product manual. Long-term operation at the absolute maximum ratings will affect the reliability of the device. 6) Plastic-packaged circuits easily absorb moisture and delaminate; keep the surrounding environment dry during use, and store under vacuum packaging at room temperature in a dry environment.

中文： 1) 成品库贮存的温湿度和环境要求：温度 10°C～25°C，相对湿度 25%～70%、静电放电敏感度 1B 等级（500~999V）。该电路所有引出端均有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 2) 产品贮存期：从检验批识别代码日期算起，入库产品贮存期超过 36 个月时产品应归入超期产品专柜存放，产品须复检合格后方能使用。 3) 建议拆封后 4 小时内使用，如在空气中暴露超过 4 小时，建议进行 150°C，8h 的高温烘焙后抽真空包装，放置于干燥柜中存放。 4) 在使用过程中应避免跌落以免造成机械应力损伤。 5) 超出绝对最大额定值可能会导致器件永久性损坏。额定最大值不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。长期在绝对最大额定值条件下工作会影响器件的可靠性。 6) 塑封电路易吸潮导致分层，使用时应注意保持周围环境干燥，存储时应真空包装储存于常温、干燥环境下。

4、电装说明 / Assembly Instructions

English: The SXD016 uses a 196-pin ball grid array plastic package (PBGA196). Surface mounting uses a conductive-adhesive bonding process, bonding uses gold-wire ball bonding, and injection molding uses a compression molding process; it is a non-hermetic package.

Assembly requirements: 1) The moisture sensitivity level of this product is MSL3. The allowable exposure time to the external environment after the product is removed from the moisture-proof bag, dry-stored, or baked until before reflow soldering is: ≤30°C/60%RH, 168 h; 2) If the device storage conditions cannot be controlled or traced, strictly perform baking at 125°C for 8 h before assembly; 3) If the assembly environment temperature and humidity cannot be guaranteed at ≤30°C/60%RH, complete soldering within 12 h after baking; 4) After baking, the product is very prone to generating static electricity; all operations require attention to ESD protection; 5) When leaded reflow soldering (Sn63Pb37) is used for board-level assembly, the recommended peak temperature range is 210°C~220°C; the maximum peak temperature is recommended not to exceed 235°C; dwell time within ±5°C of the peak temperature ≤20 s; time above the liquidus line 60~90 s; ramp-up rate 2~4°C/s; ramp-down rate ≤2°C~6°C ; 6) When lead-free reflow soldering (SAC305) is used for board-level assembly, the recommended peak temperature range is 230°C~245°C; the maximum peak temperature is recommended not to exceed 260°C; dwell time within ±5°C of the peak temperature ≤20 s; time above the liquidus line 60~90 s; ramp-up rate 2~4°C/s; ramp-down rate ≤2°C~6°C; 7) If a mixed assembly process requires a higher temperature, ensure that the device body temperature does not exceed 260°C at most. (The device body temperature measurement point is located on the top surface of the device during reflow soldering.) 8) This product uses leaded solder balls, with material Sn63Pb37.

中文： SXD016 采用 196 引脚球栅阵列塑料封装（PBGA196）。贴片采用导电胶粘接工艺，键合采用金丝球焊，注塑采用压缩模塑工艺，为非气密性封装。

电装要求： 1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； 3) 若电装环境温湿度无法保证 ≤30°C/60RH%，请在烘烤后 12h 内完成焊接； 4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~220°C，最大峰值温度不建议超过 235°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s。升温速率 2~4°C/s，降温速率 ≤2°C~6°C； 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度 ±5°C 以内停留时间 ≤20s，液相线以上停留时间 60~90s。升温速率 2~4°C/s，降温速率 ≤2°C~6°C； 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C。（器件本体温度测量点位于回流焊时器件上表面）； 8) 本产品采用有铅焊球，材料为 Sn63Pb37。

5、热阻 / Thermal Resistance

表 6 / Table 6: 封装热阻 / Package thermal resistance

项目 / Item	实测值 / Measured Value
Rth(J-C)（结到壳的热阻）/ Rth(J-C) (junction-to-case)	14°C/W

常见故障及处理办法 / Common Faults and Troubleshooting

English: 1. Abnormal output signal spectrum. When the output signal spectrum is abnormal, the following check items can usually be checked one by one: 1) Check whether the input data interface timing is appropriate: change PSS[2:0] from all 0 to all 1, and judge whether the input interface timing is appropriate by observing the TVF output value. 2) Whether the FPGA output data [A0..A11], [A0N..A11N], [B0..B11], [B0N..B11N], [C0..C11], [C0N..C11N], [D0..D11], [D0N..D11N] correspond correctly one-to-one with the DAC input data pins [A0..A11], [A0N..A11N], [B0..B11], [B0N..B11N], [C0..C11], [C0N..C11N], [D0..D11], [D0N..D11N]. 3) Check whether the device output pins OUT and OUTN are normal: test whether the differential resistance between the output pins OUT and OUTN is the nominal value of 100Ω.

中文： 1.输出信号频谱异常。当输出信号频谱异常时，通常可以按照下面的检查项目逐项检查： 1) 检查输入数据接口时序是否合适：从全 0 到全 1 改变 PSS[2:0]，通过观察 TVF 输出值，判断输入接口时序是否合适。 2) FPGA 输出数据 [A0..A11]、[A0N..A11N]、[B0..B11]、[B0N..B11N]、[C0..C11]、[C0N..C11N]、[D0..D11]、[D0N..D11N] 与 DAC 输入数据引脚 [A0..A11]、[A0N..A11N]、[B0..B11]、[B0N..B11N]、[C0..C11]、[C0N..C11N]、[D0..D11]、[D0N..D11N] 是否正确一一对应。 3) 检查该器件输出引脚 OUT、OUTN 是否正常：测试输出引脚 OUT、OUTN 之间差分电阻是否为标称值 100Ω。

电路薄弱点 / Circuit Weak Points

English: The following weak points of this circuit were found during design and manufacture, test screening, application, and other processes: 1) The ESD capability between output port OUT and output port OUTN, and of the temperature-measurement diode port diode, is relatively weak: human body model (HBM) exploratory test passed 1000 V (the detailed specification specifies 500 V), and machine model (MM) exploratory test did not pass 50 V. 2) With power applied, between output port OUT and output port OUTN it is easily damaged by cable hot-plugging: in the EMC immunity test, the electrical fast transient (EFT) exploratory test was less than 200 V. 3) There is an anti-parallel diode between the analog supply VCCA3 and the digital supply VCCD; during power-up, an excessive voltage between the two supplies may cause the diode to burn out. 4) This circuit's analog supply VCCA3 and digital supply VCCD have requirements on power-up time, and there is a possibility of cold-start failure.

中文： 该电路在设计与制造、测试筛选、应用等过程中发现存在以下薄弱点： 1) 输出端口 OUT 与输出端口 OUTN 之间、测温二极管端口 diode 抗静电能力较弱：人体静电模型（HBM）摸底通过 1000V（详细规范规定 500V）、机器静电模型（MM）摸底未通过 50V。 2) 带电情况下输出端口 OUT 与输出端口 OUTN 之间易受电缆热插拔损伤：电磁兼容抗扰度试验中电快速脉冲群（EFT）摸底小于 200V。 3) 模拟电源 VCCA3 和数字电源 VCCD 之间存在反向并联二极管，在上电过程中两个电源间电压过大可能会导致二极管烧毁。 4) 该电路模拟电源 VCCA3 和数字电源 VCCD 对上电时间存在要求，存在冷启动失败可能性。

使用过程要求 / Usage Requirements

一、禁止和要求项 / Prohibitions and Requirements

English: 1.1 Hot-plugging of output ports OUT/OUTN is prohibited. Hot-plugging of output ports OUT/OUTN is prohibited; for example, it is prohibited to unscrew the SMA connector of DAC1's output from the spectrum analyzer while powered, and then screw the SMA connector of DAC2's output onto the spectrum

analyzer while powered. It is recommended that DAC1 and DAC2 be connected to or disconnected from the spectrum analyzer while unpowered.

1.2 Excessively slow supply power-up is prohibited. The power-up time of supplies VCCD and VCCA3 needs to be controlled to <40 ms, and the maximum voltage difference between the two supplies is required to be ≤1.2 V. (The power-up requirements and recommended supply methods are the same as in the product usage notes above; the original repeats the power-up figure in this section, labeled "图2 上电时序要求" in the original.)

中文： 1.1 禁止输出端口 OUT/OUTN 热插拔。 禁止输出端口 OUT/OUTN 热插拔，例如禁止在加电条件下将 DAC1 输出的 SMA 头从频谱仪拧下来，然后将 DAC2 输出的 SMA 头在加电条件下拧到频谱仪上，建议 DAC1、DAC2 在断电条件下与频谱仪连接或断开。

1.2 禁止电源上电时间过慢。 电源 VCCD 和 VCCA3 上电时间需控制在 <40ms，要求两个电源间最大电压差 ≤1.2V。（上电要求与推荐供电方式同产品使用注意事项，此处从略；原件本节重复给出上电时序图，图题编号为"图2"。）

二、建议项 / Recommendations

English: Before and after assembly, and during debugging, if the impedance between the output ports OUT/OUTN can be tested, it is recommended to test the output impedance between the output ports OUT/OUTN.

中文： 在装配前后、调试过程中，如果可以测试输出端口 OUT/OUTN 间阻抗，建议测试输出端口 OUT/OUTN 间输出阻抗。

三、注意项 / Notes

English: 3.1 ESD precautions — the same as item 3) of the product usage notes above, except: item 2) here reads "then, when connecting the device to the RF cables, keep the device unpowered, and power it up after the connection is successful" without the initial discharge step listed separately : 1) Wear an ESD wrist strap during operation. 2) When connecting RF cables to the device output ports (OUT, OUTN), keep the device unpowered when connecting, and power it up after the connection is successful. 3) It is recommended to simultaneously blow the device output ports (OUT, OUTN) and the RF cable connection ports with an ESD ion fan. 4) When connected to RF devices, keep both unpowered, and power up after the connection is successful. 5) When connected via RF cables to instruments such as a spectrum analyzer for testing, check that the instruments are well grounded.

3.2 Harsh electromagnetic environment and ground loop notes. At test/debugging and final-assembly/integration sites, pay attention to whether the chassis ground of the board or unit containing the DAC, of the other equipment connected to it, and of the measurement equipment, together with the shield ground of their interconnection cables, forms a ground loop with the debugging bench and room protective ground; especially when there is high-power motor equipment in the room, be sure to break the ground loop.

中文： 3.1 静电防护注意事项——同产品使用注意事项 3)，此处条目为：1) 操作时佩戴静电手腕。2) 器件输出端口（OUT、OUTN）连接射频线缆时，器件先不上电，连接成功后再上电。3) 推荐同时用除静电离子风机吹器件输出端口（OUT、OUTN）和射频线缆连接端口。4) 与射频器件连接时，相互先不上电，连接成功后才上电。5) 通过射频线缆与频谱分析仪等仪器连接测试时，检查确认频谱分析等仪器接地情况良好。

3.2 恶劣电磁环境和地环路注意事项。 在测试调试和总装联调现场，注意 DAC 所在单板或单机，与其相连的其它设备和测量设备，每个设备的机壳地与其互连线的屏蔽地，是否与调试台、房间保护地形成了地环路，特别是此房间内有大功率电机设备时，务必要断开地环路。

联系方式 / Contact Information

Shenzhen Shenxin Technology Co., Ltd. / 深圳市深信科技有限公司

Contact / 联系人：Felix Lai Email / 邮箱：felix@shenxinic.com Phone / 电话：+852 51367095 Website / 网站：shenxinic.com

---

附加说明 / Additional Notes

English: 1. First release date of this manual: February 2022. 2. Product status: ☒ In production (this product model is currently in production; formal products can be provided) / ☐ Pre-release (this product model has not yet entered formal production; samples can be provided). 3. Description of replacement of foreign products: 3.1 Outline dimension comparison — see Appendix Table 1: the length and width are consistent, and the height differs slightly, so replacement can be achieved. 3.2 Standard comparison: 3.2.1 absolute maximum ratings comparison — see Appendix Table 2; 3.2.2 recommended operating conditions comparison — see Appendix Table 3; 3.2.3 electrical characteristics comparison — see Appendix Table 4.

中文： 1. 本说明书首次发布日期：2022 年 2 月。 2. 本产品状态：☒生产（该产品型号目前已在生产，可以提供正式产品）☐预发布（该产品型号尚未投入正式生产，可以提供样品） 3. 替代国外产品情况说明： 3.1 外形尺寸对比：见附表 1，长宽一致、高度略有差异，可实现替换。 3.2 标准对比：3.2.1 绝对最大额定值对比见附表 2；3.2.2 推荐工作条件对比见附表 3；3.2.3 电特性对比见附表 4。

附表 1 / Appendix Table 1: 实测器件尺寸对比表 / Measured device dimension comparison

型号 / Model	样品（L×W×H)/ Sample (L×W×H)	对比结果 / Comparison Result
SXD016	15mm x 15mm x 1.70mm	长宽一致、高度略有差异 / Length and width consistent, height slightly different
国外产品 / Foreign product	15mm x 15mm x 1.78mm	

附表 2 / Appendix Table 2: 绝对最大额定值对比 / Absolute maximum ratings comparison

参数 / Parameter	采购规范要求 / Procurement Specification	国外产品手册 / Foreign Product Datasheet	比对结果 / Result
VCCA5	6.0V	6.0V	一致 / Consistent
VCCA3	4.0V	4.0V	一致 / Consistent
VCCD	4.0V	4.0V	一致 / Consistent
贮存温度 / Storage temperature	-65°C～150°C	无 / None	

参数 / Parameter	采购规范要求 / Procurement Specification	国外产品手册 / Foreign Product Datasheet	比对结果 / Result
结温 / Junction temperature	150°C	170°C	有差异 / Different
引线耐焊接温度（10s)/ Lead soldering temperature (10 s)	300°C	无 / None	

English: From the maximum-ratings comparison, except for the junction temperature, all other maximum ratings of the device are consistent with the foreign product datasheet.

中文： 通过最大额定值对比可知，器件除结温外，其余最大额定值与国外产品手册一致。

附表 3 / Appendix Table 3: 推荐工作条件对比 / Recommended operating conditions comparison

参数 / Parameter	采购规范要求 / Procurement Specification	国外产品手册 / Foreign Product Datasheet	比对结果 / Result
VCCA5	5V	5V	一致 / Consistent
VCCA3	3.3V	3.3V	一致 / Consistent
VCCD	3.3V	3.3V	一致 / Consistent
LVDS 数字输入低电压 / LVDS digital input low voltage	1.075V	1.075V	一致 / Consistent
LVDS 数字输入高电压 / LVDS digital input high voltage	1.425V	1.425V	一致 / Consistent
数字输入差分摆幅 / Digital input differential swing	350mVp	350mVp	一致 / Consistent
时钟输入差分摆幅 / Clock input differential swing	1.4Vpp	1.4Vpp	一致 / Consistent
时钟输入功率（差分模式）/ Clock input power (differential mode)	4dBm	4dBm	一致 / Consistent
工作温度范围 / Operating temperature range	-55°C≤TC≤125°C	-55°C≤TC, Tj≤125°C	有差异 / Different

English: From the recommended-operating-conditions comparison, except for the operating temperature range, the procurement specification requirements are consistent with the foreign product datasheet.

中文： 通过推荐工作条件对比可知，器件除工作温度范围外，采购规范要求与国外产品手册一致。

附表 4 / Appendix Table 4: 电特性对比 / Electrical characteristics comparison

English: From Appendix Table 4, there are certain differences between the device procurement specification requirements and the requirements of the foreign product datasheet.

中文： 从附表 4 中可看出，器件采购规范要求与国外产品器件手册的要求存在一定差异。

参数 / Parameter	符号 / Symbol	条件 / Conditions	采购规范要求最小 / Spec Min	采购规范要求最大 / Spec Max	国外产品手册最小 / Foreign Min	国外产品手册最大 / Foreign Max	单位 / Unit	对比结果 / Result
分辨率 / Resolution	RES		12	12	12	12	Bits	一致 / Consistent
5V 模拟电源电流 / 5V analog supply current	ICCA5	4:1 MUX 模式	—	120	—	115	mA	有差异 / Different
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3	4:1 MUX 模式	—	210	—	240	mA	有差异 / Different
3.3V 数字电源电流 / 3.3V digital supply current	ICCD	4:1 MUX 模式	—	510	—	490	mA	有差异 / Different
功耗 / Power consumption	PW	4:1 MUX 模式	—	3	—	3	W	一致 / Consistent
5V 模拟电源电流 / 5V analog supply current	ICCA5	2:1 MUX 模式	—	120	—	115	mA	有差异 / Different
3.3V 模拟电源电流 / 3.3V analog supply current	ICCA3	2:1 MUX 模式	—	200	—	240	mA	有差异 / Different
3.3V 数字电源电流 / 3.3V digital supply current	ICCD	2:1 MUX 模式	—	450	—	430	mA	有差异 / Different
功耗 / Power consumption	PW	2:1 MUX 模式	—	2.8	—	2.8	W	一致 / Consistent
数字差分输入电压 / Digital differential input voltage	VID		100	500	100	500	mVp	一致 / Consistent
数字差分输入电阻 / Digital differential input resistance	RILVDS		80	130	80	120	Ω	有差异 / Different
时钟输入共模电压 / Clock input common-mode voltage	VICLKCM		2.4	2.6	2.4	2.6	V	一致 / Consistent
时钟差分输入电阻 / Clock differential input resistance	RICLK		80	130	80	120	Ω	有差异 / Different
时钟差分输出电压 / Clock differential output voltage	VOD		240	450	240	450	mVp	一致 / Consistent
时钟输出共模电压 / Clock output common-mode voltage	VOCLKCM		1.125	1.375	1.125	1.375	V	一致 / Consistent
模拟输出内部差分电阻 / Analog output internal differential resistance	ROUT		90	120	90	110	Ω	有差异 / Different
sdata, sld_n, sclk, reset_n 低电平输入电流 / low-level input current	IIL		-120	-10	-120	-10	uA	一致 / Consistent
sdata, sld_n, sclk, reset_n 高电平输入电流 / high-level input current	IIH		10	120	10	120	uA	一致 / Consistent
OCDS, PSS 低电平输入电流 / input low-level current	IIL		-150	-50	-150	-50	uA	一致 / Consistent
OCDS, PSS 高电平输入电流 / input high-level current	IIH		50	150	50	150	uA	一致 / Consistent
微分非线性 / Differential nonlinearity	EDL		-3	+3	-0.8	+0.8	LSB	有差异 / Different
积分非线性 / Integral nonlinearity	EL		-5	+5	-2.5	+2.5	LSB	有差异 / Different
DAC 输出电压 / DAC output voltage	VOUT	GA<9:0>=0x200	0.88	1.08	0.92	1.08	Vpp	有差异 / Different
DAC 输出电压调节步进电压 / DAC output voltage adjustment step	VADJ		-5	+5	-5	+5	mV	一致 / Consistent
DAC 输出电压电源敏感度 / DAC output voltage supply sensitivity	VSEN		-5	+5	—	+5	%	一致 / Consistent
无杂散动态范围 / SFDR		非归零模式 / NRZ: fCLK=6.4GSPS, fout=64MHz, 0dBFS, 4:1 MUX	60	—	—	—	dBc	
无杂散动态范围 / SFDR		非归零模式 / NRZ: fCLK=6.4GSPS, fout=3.136GHz, 0dBFS, 4:1 MUX	40	—	—	—	dBc	
无杂散动态范围 / SFDR		窄归零模式 / NRTZ: fCLK=6.4GSPS, fout=3.136GHz, 0dBFS, 4:1 MUX	45	—	—	—	dBc	
无杂散动态范围 / SFDR		窄归零模式 / NRTZ: fCLK=6.4GSPS, fout=6.336GHz, 0dBFS, 4:1 MUX	45	—	—	—	dBc	
无杂散动态范围 / SFDR		归零模式 / RTZ: fCLK=6.4GSPS, fout=6.336GHz, 0dBFS, 4:1 MUX	47	—	—	—	dBc	
无杂散动态范围 / SFDR		混频模式 / RF: fCLK=6.4GSPS, fout=6.336GHz, 0dBFS, 4:1 MUX	46	—	—	—	dBc	
无杂散动态范围 / SFDR		混频模式 / RF: fCLK=6.4GSPS, fout=9.536GHz, 0dBFS, 4:1 MUX	45	—	—	—	dBc	
无杂散动态范围 / SFDR		混频模式 / RF: fCLK=6.4GSPS, fout=12.736GHz, 0dBFS, 4:1 MUX	40	—	—	—	dBc	
最大工作时钟频率 / Maximum operating clock frequency	fCLK	4:1 MUX 模式	6.4	—	6	—	GSPS	有差异 / Different
最大工作时钟频率 / Maximum operating clock frequency	fCLK	2:1 MUX 模式	3.2	—	3.2	—	GSPS	一致 / Consistent
最大输入数据率 / Maximum input data rate	fDATA	4:1 MUX 模式	1600	—	1500	—	MSPS	有差异 / Different
最大输入数据率 / Maximum input data rate	fDATA	2:1 MUX 模式	1600	—	1600	—	MSPS	一致 / Consistent