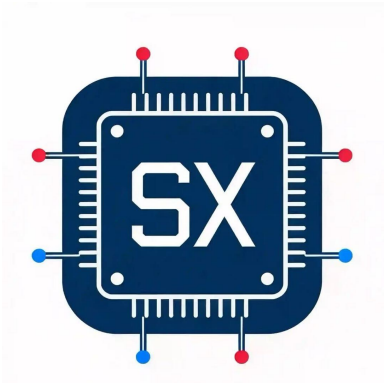


SXD034

Dual-Channel 16-Bit, 250 MSPS D/A Converter

双通道 16 位 250MSPS D/A 转换器

16-bit | 2 channels | 250 MSPS | QFN72 | Parallel CMOS
16 位 | 双通道 | 250MSPS | QFN72 | 并行 CMOS

对标 / Cross Reference: AD9747 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

Shenzhen Shenxin Technology Co., Ltd. · 深圳市深信科技有限公司

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SXD034 Dual-Channel 16-Bit 250MSPS D/A Converter — Product Manual (Bilingual)

SXD034 型双通道 16 位 250MSPS D/A 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深信科技 **V.20260722**

对标 / Cross Reference: AD9747 — pin-to-pin compatible alternative

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版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20260722	2026.07	/	/	首次发布 / Initial release

产品用途及应用范围 / Applications and Scope

English: Wireless base stations: W-CDMA, CDMA2000; broadband communications: LMDS/MMDS; instruments and meters; RF signal generators, arbitrary waveform generators.

中文： 无线基站：W-CDMA，CDMA2000；宽带通信：LMDS/MMDS；仪表仪器；射频信号产生器，任意波形发生器。

标准 / Standards

English: Detailed specification and approval number: Q/GC 0226-2026 — Detailed Specification for Semiconductor Integrated Circuit SXD034 Dual-Channel 16-Bit 250MSPS D/A Converter. Quality grade / quality assurance requirement: enterprise standard.

中文： 详细规范及确认号：Q/GC 0226-2026 《半导体集成电路 SXD034 型双通道 16 位 250MSPS D/A 转换器详细规范》；质量等级/质量保证要求：企标。

产品特点 / Features

English: - Analog supply voltage: 3.3V/1.8V - Digital supply voltage: 3.3V/1.8V - Maximum sample rate: 250MSPS - Spurious-free dynamic range (SFDR): ⩾72 dBc @ fOUT=20MHz, fDAC=250MSPS (typical 86dBc) - Differential nonlinearity error (DNL): ±2.6LSB - Integral nonlinearity error (INL): ±5.5LSB - Power consumption: ⩽355mW (typical 312mW) - Full-scale output current: 20mA - Circuit interface: 3.3V LVCMOS - ESD rating: Class 1C, HBM model: 1000V - Weight: 0.23g±0.05g - Moisture sensitivity level and package: MSL3, QFN72

中文： - 模拟电源电压：3.3V/1.8V - 数字电源电压：3.3V/1.8V - 最高采样率：250MSPS - 无杂散动态范围：⩾72 dBc@fOUT=20MHz，fDAC=250MSPS（典型值 86dBc） - 微分线性误差：±2.6LSB - 积分线性误差：±5.5LSB - 功耗：⩽355mW(典型值 312mW) - 满度输出电流：20mA - 电路接口：3.3V LVCMOS - ESD 等级：1C 级，HBM 模型：1000V - 重量：0.23g±0.05g - 湿敏等级和封装形式：MSL3，QFN72

产品描述 / Product Description

English: The SXD034 is a high-dynamic-range, dual-channel, 16-bit, 250MSPS digital-to-analog converter fabricated in a standard CMOS process, with a segmented current-steering architecture and a programmable full-scale output current of 8.6~31.7mA. The product has features specific to direct up-conversion applications, such as gain and offset compensation, which allow it to interface seamlessly with analog quadrature modulators.

This product is packaged in a 72-pin quad flat no-lead plastic package (QFN72) with outline dimensions of 10.0mm (L) × 10.0mm (W) × 0.85mm (H).

The functional block diagram of this product is shown in Figure 1.

中文： SXD034 是一款高动态范围的双通道 16 位 250MSPS 数模转换器，采用标准 CMOS 工艺制造，架构为分段电流舵结构，具有 8.6~31.7mA 可编程满度输出电流。该产品具有针对直接上变频应用的特定功能，比如增益和失调补偿，它们可以和模拟正交调制器无缝连接。

该产品采用 72 脚无引线塑料载体封装 (QFN72)，外形尺寸为长 10.0mm×宽 10.0mm×高 0.85mm。

该产品功能框图如图 1 所示。

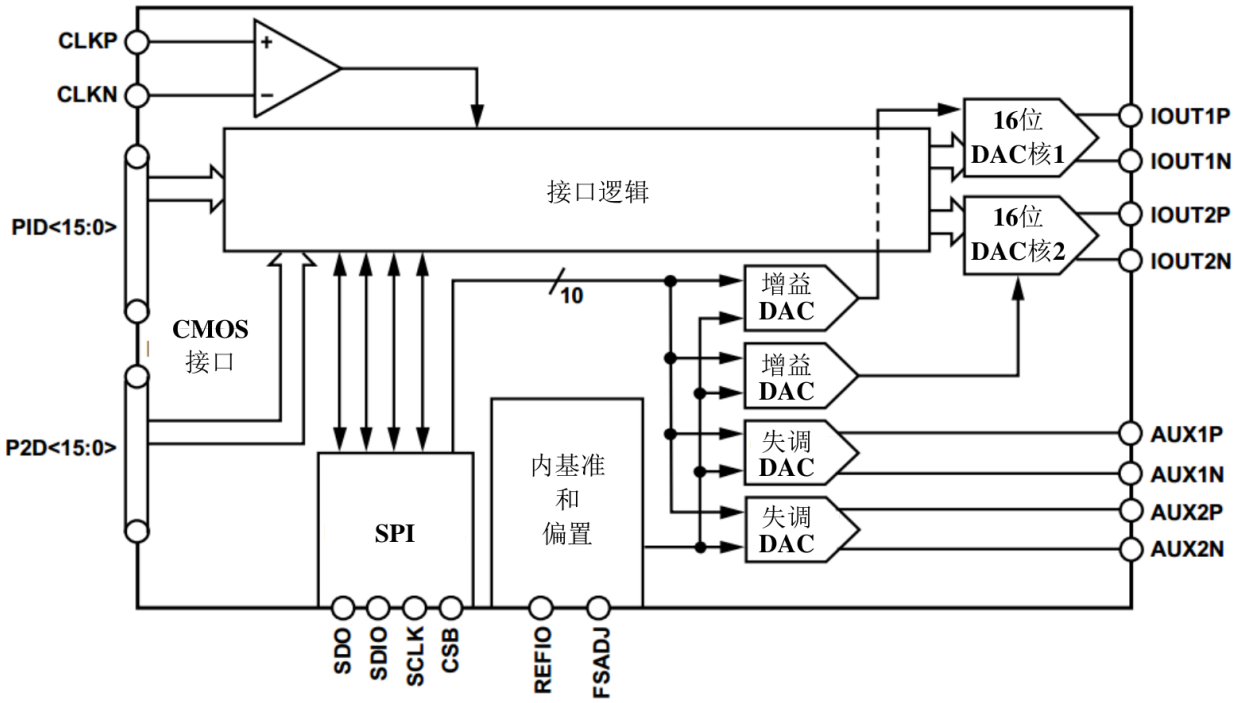


Figure 1: Functional block diagram

产品外形图和实物图片 / Package Outline and Product Photos

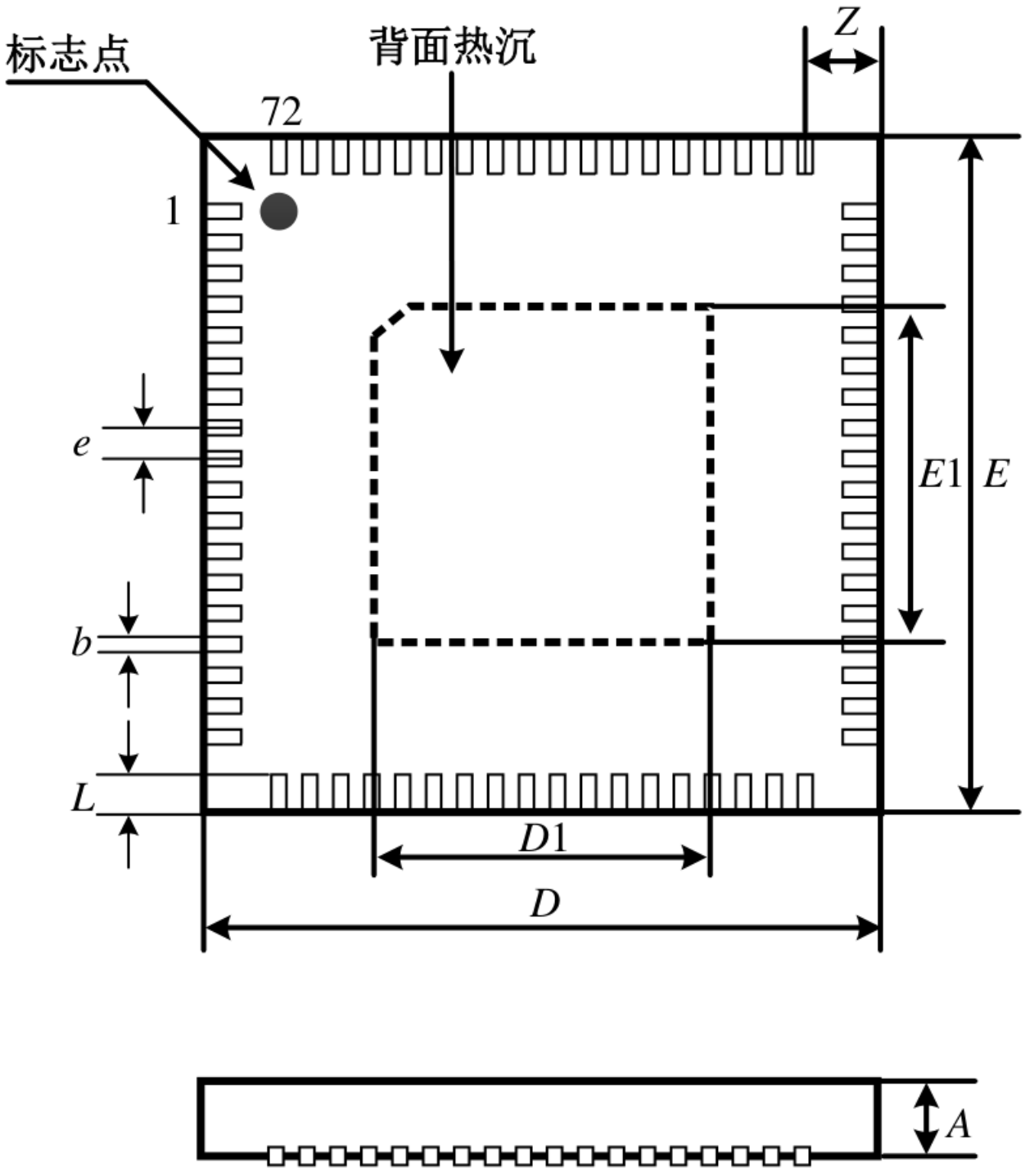


Figure 2: Package outline dimensions drawing

单位为毫米 / Units in mm

尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max	尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max
A	0.60	0.85 [a]	1.10	Z	—	0.75 [a]	1.30 [b]
D	9.90	10.00 [a]	10.10	b	0.20	0.25 [a]	0.30

尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max	尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max
D1	4.50	4.70 [a]	4.90	e	—	0.50	—
E	9.90	10.00 [a]	10.10	L	0.30	0.40 [a]	0.50
E1	4.50	4.70 [a]	4.90				

[a] 实际公称值，推荐用户参考该尺寸设计使用；/ a: Actual nominal value; users are advised to design with reference to this dimension.

注：推荐焊盘设计详见电装说明。/ Note: see the assembly instructions for recommended pad layout.

引出端排列（俯视图）/ Pin Arrangement (Top View)

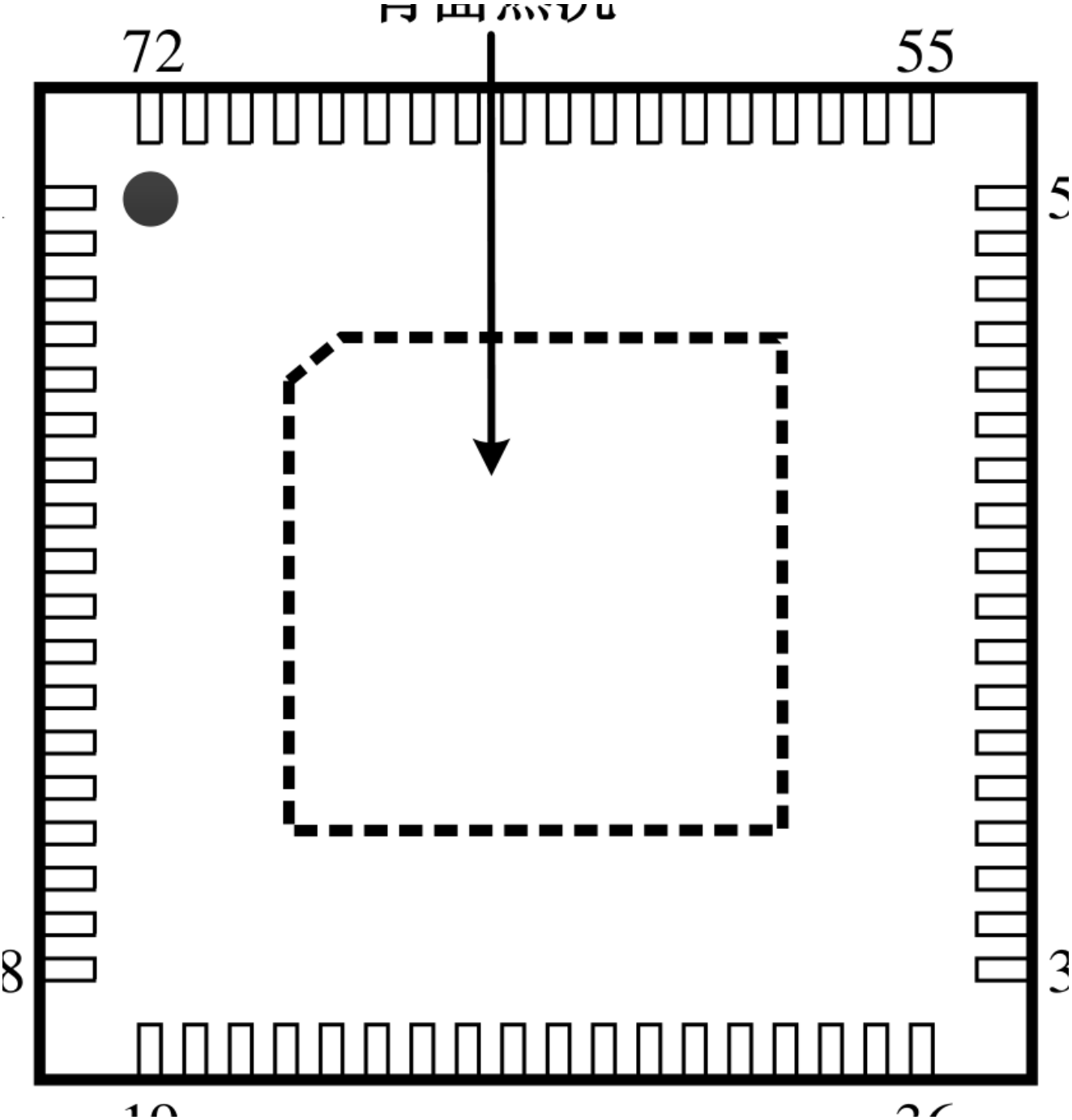


Figure 3: Pin arrangement (top view)

引出端功能符号表 / Pin Function Table

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
1	CVDD18	1.8V 时钟电源 / 1.8V clock supply	/	37	P2D9	通道 2 输入数据第 9 位 / Channel 2 input data bit 9	I

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
2	CVSS	0V 时钟地 / 0V clock ground	/	38	P2D8	通道 2 输入数据第 8 位 / Channel 2 input data bit 8	I
3	CLKP	DAC 差分时钟输入正端 / DAC differential clock input, positive	I	39	P2D7	通道 2 输入数据第 7 位 / Channel 2 input data bit 7	I
4	CLKN	DAC 差分时钟输入负端 / DAC differential clock input, negative	I	40	P2D6	通道 2 输入数据第 6 位 / Channel 2 input data bit 6	I
5	CVSS	0V 时钟地 / 0V clock ground	/	41	P2D5	通道 2 输入数据第 5 位 / Channel 2 input data bit 5	I
6	CVDD18	1.8V 时钟电源 / 1.8V clock supply	/	42	P2D4	通道 2 输入数据第 4 位 / Channel 2 input data bit 4	I
7	DVSS	0V 数字地 / 0V digital ground	/	43	P2D3	通道 2 输入数据第 3 位 / Channel 2 input data bit 3	I
8	DVDD18	1.8V 数字核心电源 / 1.8V digital core supply	/	44	P2D2	通道 2 输入数据第 2 位 / Channel 2 input data bit 2	I
9	P1D15	通道 1 输入数据第 15 位 / Channel 1 input data bit 15	I	45	P2D1	通道 2 输入数据第 1 位 / Channel 2 input data bit 1	I
10	P1D14	通道 1 输入数据第 14 位 / Channel 1 input data bit 14	I	46	P2D0	通道 2 输入数据第 0 位 / Channel 2 input data bit 0	I
11	P1D13	通道 1 输入数据第 13 位 / Channel 1 input data bit 13	I	47	DVDD18	1.8V 数字核心电源 / 1.8V digital core supply	/
12	P1D12	通道 1 输入数据第 12 位 / Channel 1 input data bit 12	I	48	DVSS	0V 数字地 / 0V digital ground	/
13	P1D11	通道 1 输入数据第 11 位 / Channel 1 input data bit 11	I	49	SDO	SPI 数据输出 / SPI data output	O
14	P1D10	通道 1 输入数据第 10 位 / Channel 1 input data bit 10	I	50	SDIO	SPI 数据输入和可选数据输出 / SPI data input and optional data output	I/O
15	P1D9	通道 1 输入数据第 9 位 / Channel 1 input data bit 9	I	51	SCLK	SPI 时钟输入 / SPI clock input	I
16	P1D8	通道 1 输入数据第 8 位 / Channel 1 input data bit 8	I	52	CSB	SPI 片选输入 / SPI chip-select input	I
17	P1D7	通道 1 输入数据第 7 位 / Channel 1 input data bit 7	I	53	RESET	硬复位 / Hardware reset	I
18	P1D6	通道 1 输入数据第 6 位 / Channel 1 input data bit 6	I	54	FSADJ	满度输出电流调节 / Full-scale output current adjust	I
19	P1D5	通道 1 输入数据第 5 位 / Channel 1 input data bit 5	I	55	REFIO	基准输入输出 / Reference input/ output	I/O
20	P1D4	通道 1 输入数据第 4 位 / Channel 1 input data bit 4	I	56	AVDD33	3.3V 模拟电源 / 3.3V analog supply	/
21	P1D3	通道 1 输入数据第 3 位 / Channel 1 input data bit 3	I	57	AVDD33	3.3V 模拟电源 / 3.3V analog supply	/
22	P1D2		I	58	AVSS	0V 模拟地 / 0V analog ground	/

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
		通道 1 输入数据第 2 位 / Channel 1 input data bit 2					
23	P1D1	通道 1 输入数据第 1 位 / Channel 1 input data bit 1	I	59	IOUT2P	DAC2 电流输出正端 / DAC2 current output, positive	O
24	P1D0	通道 1 输入数据第 0 位 / Channel 1 input data bit 0	I	60	IOUT2N	DAC2 电流输出负端 / DAC2 current output, negative	O
25	DCO	数据时钟输出 / Data clock output	O	61	AVSS	0V 模拟地 / 0V analog ground	/
26	DNC [a]	悬空引脚 / Do-not-connect pin	/	62	AUX2P	辅助 DAC2 默认电流输出端 / Auxiliary DAC2 default current output	O
27	DVDD33	3.3V 数字 IO 电源 / 3.3V digital I/O supply	/	63	AUX2N	辅助 DAC2 可选电流输出端 / Auxiliary DAC2 optional current output	O
28	DVSS	0V 数字地 / 0V digital ground	/	64	AVSS	0V 模拟地 / 0V analog ground	/
29	IQSEL	单通道模式 IQ 帧信号 / Single-port mode IQ frame signal	I	65	AUX1N	辅助 DAC1 可选电流输出端 / Auxiliary DAC1 optional current output	O
30	DNC [a]	悬空引脚 / Do-not-connect pin	/	66	AUX1P	辅助 DAC1 默认电流输出端 / Auxiliary DAC1 default current output	O
31	P2D15	通道 2 输入数据第 15 位 / Channel 2 input data bit 15	I	67	AVSS	0V 模拟地 / 0V analog ground	/
32	P2D14	通道 2 输入数据第 14 位 / Channel 2 input data bit 14	I	68	IOUT1N	DAC1 电流输出负端 / DAC1 current output, negative	O
33	P2D13	通道 2 输入数据第 13 位 / Channel 2 input data bit 13	I	69	IOUT1P	DAC1 电流输出正端 / DAC1 current output, positive	O
34	P2D12	通道 2 输入数据第 12 位 / Channel 2 input data bit 12	I	70	AVSS	0V 模拟地 / 0V analog ground	/
35	P2D11	通道 2 输入数据第 11 位 / Channel 2 input data bit 11	I	71	AVDD33	3.3V 模拟电源 / 3.3V analog supply	/
36	P2D10	通道 2 输入数据第 10 位 / Channel 2 input data bit 10	I	72	AVDD33	3.3V 模拟电源 / 3.3V analog supply	/
—	EAPD	背面热沉（需接地）/ Exposed pad (must be grounded)	/				

[a] 使用时不能连接该引脚 / a: This pin must not be connected in use.

推荐工作条件 / Recommended Operating Conditions

English: - CVDD18: 1.70V~1.90V - DVDD18: 1.70V~1.90V - AVDD33: 3.13V~3.47V - DVDD33: 3.13V~3.47V - Operating ambient temperature TA: -40°C ~ 85°C

Note: See the cross-reference notes in the Additional Notes for the comparison with the foreign product.

中文： - CVDD18：1.70V~1.90V - DVDD18：1.70V~1.90V - AVDD33：3.13V~3.47V - DVDD33：3.13V~3.47V - 工作环境温度 TA：-40°C ~ 85°C

注：请查看附件说明中替代国外产品情况说明。

绝对最大额定值 / Absolute Maximum Ratings

English: - Supply voltages: CVDD18: -0.3V ~ 1.98V; DVDD18: -0.3V ~ 1.98V; AVDD33: -0.3V ~ 3.6V; DVDD33: -0.3V ~ 3.6V - AVSS: -0.3V~0.3V - DVSS: -0.3V~0.3V - CVSS: -0.3V~0.3V - Reference input/output pin voltage: −0.3V~AVDD33+0.3V - DAC1 current output pin voltage: −0.3V~AVDD33+0.3V - DAC2 current output pin voltage: −0.3V~AVDD33+0.3V - Auxiliary DAC1 current output pin voltage: −0.3V~AVDD33+0.3V - Auxiliary DAC2 current output pin voltage: −0.3V~AVDD33+0.3V - Input data pin voltage: −0.3V~DVDD33+0.3V - Clock input pin voltage: −0.3V~CVDD18+0.3V - Reset pin and 4-wire SPI pin voltage: −0.3V~DVDD33+0.3V - Storage temperature (Tstg): -65°C~150°C - Lead soldering temperature (Th) (10s): 260°C

中文： - 电源电压：CVDD18：-0.3V ~ 1.98V；DVDD18：-0.3V ~ 1.98V；AVDD33：-0.3V ~ 3.6V；DVDD33：-0.3V ~ 3.6V - AVSS：-0.3V~0.3V - DVSS：-0.3V~0.3V - CVSS：-0.3V~0.3V - 基准输入输出引脚电压：−0.3V~AVDD33+0.3V - DAC1 电流输出引脚电压：−0.3V~AVDD33+0.3V - DAC2 电流输出引脚电压：−0.3V~AVDD33+0.3V - 辅助 DAC1 电流输出引脚电压：−0.3V~AVDD33+0.3V - 辅助 DAC2 电流输出引脚电压：−0.3V~AVDD33+0.3V - 输入数据引脚电压：−0.3V~DVDD33+0.3V - 时钟输入引脚电压：−0.3V~CVDD18+0.3V - 复位引脚、四线 SPI 引脚电压：−0.3V~DVDD33+0.3V - 贮存温度（Tstg）：-65°C~150°C - 引线耐焊接温度（Th）（10s）：260°C

性能指标 / Performance Specifications

Conditions / 条件（除另有规定外 / unless otherwise specified）: AVDD33=DVDD33=3.3V, DVDD18=CVDD18=1.8V, IFS=20mA, -40°C≤TA≤85°C.

特性 / Parameter	符号 / Symbol	条件 / Conditions	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
分辨率 / Resolution	RES	—		16		Bit
微分误差 / Differential nonlinearity error	EDL	—	-6.0	±2.6	6.0	LSB
积分误差 / Integral nonlinearity error	EL	—	-9.0	±5.5	9.0	LSB
失调误差 [a] / Offset error [a]	EO	—	-0.050	0.0004	0.050	%FSR
增益误差 / Gain error	EG	—	-8.0	-1.0	8.0	%FSR
增益失配 [a] / Gain mismatch [a]	EGMIS	—	-2.5	-0.06	2.5	%FSR
电流输出范围 / Current output range	IFS	—	8.0	—	32.0	mA
输出顺从电压范围 [a] / Output compliance voltage range [a]	VOC	—	-1.0	—	1.0	V
辅助 DAC 满度输出电流 [a] / Auxiliary DAC full-scale output current [a]	IFSAUX	—	-2.2	—	2.2	mA
	VOCAUXSI	—	0.8	—	1.6	V

特性 / Parameter	符号 / Symbol	条件 / Conditions	最小 / Min	典型 / Typ	最大 / Max	单位 / Unit
辅助 DAC 输出顺从电压范围（电流沉模式）[a] / Auxiliary DAC output compliance voltage range (current-sink mode) [a]						
辅助 DAC 输出顺从电压范围（电流源模式）[a] / Auxiliary DAC output compliance voltage range (current-source mode) [a]	VOCAUXSO	—	0	—	1.6	V
基准输出电压 / Reference output voltage	VREFO	—	1.15	1.20	1.25	V
基准外部电压输入范围 [a] / External reference voltage input range [a]	VREFIR	—	1.15	—	1.30	V
基准输入输出电阻 [a] / Reference input/output resistance [a]	RREF	—	4	5	6	kΩ
3.3V 模拟电源电流 [a] / 3.3V analog supply current [a]	IAVDD33	—	—	56	60	mA
3.3V 数字电源电流 [a] / 3.3V digital supply current [a]	IDVDD33	—	—	13	15	mA
1.8V 模拟电源电流 [a] / 1.8V analog supply current [a]	IAVDD18	—	—	18	22	mA
1.8V 数字电源电流 [a] / 1.8V digital supply current [a]	IDVDD18	—	—	29	36	mA
功耗 / Power consumption	PW	fDAC=250MSPS, fOUT = 20MHz	—	312	355	mW
DAC 输出禁能功耗 [a] / DAC output-disabled power [a]	PDACPD	—	—	85	180	mW
全芯片休眠功耗 [a] / Full-chip sleep power [a]	PPD	—	—	1.3	10	mW
无杂散动态范围 / Spurious-free dynamic range	SFDR	fDAC=250MSPS, fOUT = 20MHz	72	86	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	fDAC=250MSPS, fOUT = 180MHz [a]	55	66	—	dBc
互调失真 [a] / Intermodulation distortion [a]	IMD	fDAC=250MSPS, fOUT = 20MHz	76	87	—	dBc
串扰 [a] / Crosstalk [a]	XT	fDAC=250MSPS, fOUT = 20MHz	70	94	—	dBc
输入时钟差分峰峰值电压 [a] / Input clock differential peak-to-peak voltage [a]	VDPPCLK	fDAC=250MSPS, fOUT = 20MHz	400	800	1600	mV
输入时钟共模电压 [a] / Input clock common-mode voltage [a]	VCMCLK	fDAC=250MSPS, fOUT = 20MHz	300	400	500	mV
采样速率 / Sample rate	fDAC	—	—	—	250	MSPS
输入时钟频率 [a] / Input clock frequency [a]	fCLK	—	—	—	250	MHz
SPI 时钟频率 [a] / SPI clock frequency [a]	fSCLK	—	—	—	40	MHz
SPI 时钟脉冲高电平宽度 [a] / SPI clock pulse high width [a]	tPWH	—	10	—	—	ns
SPI 时钟脉冲低电平宽度 [a] / SPI clock pulse low width [a]	tPWL	—	10	—	—	ns

注：典型值为常温测试数据。/ Note: typical values are room-temperature test data. [a]：未纳入考核，仅供用户参考使用。/ a: Not subject to acceptance testing; provided for user reference only.

主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

English: 1. Differential and integral nonlinearity error curves. 2. Output signal spectrum at 180MHz analog output.

中文： 1、微分误差和积分误差曲线。2、模拟输出 180MHz 条件下输出信号频谱。

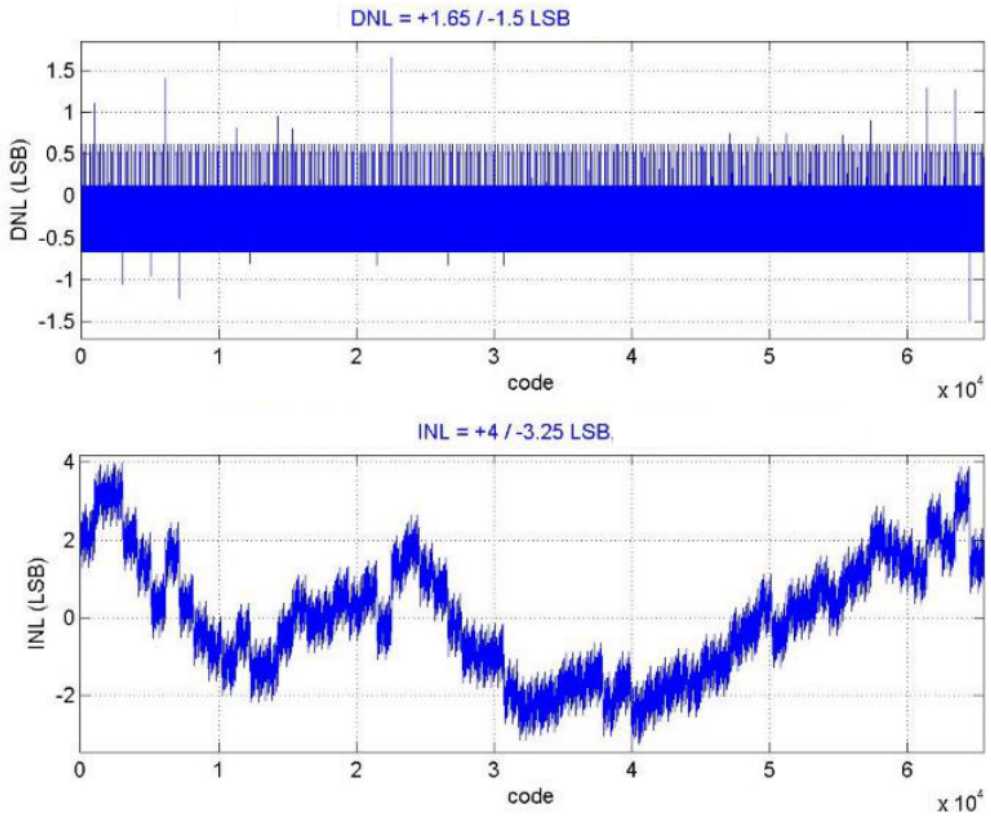


图4 微分误差和积分误差曲线，T_A=25℃

80MHz 条件下输出信号频谱

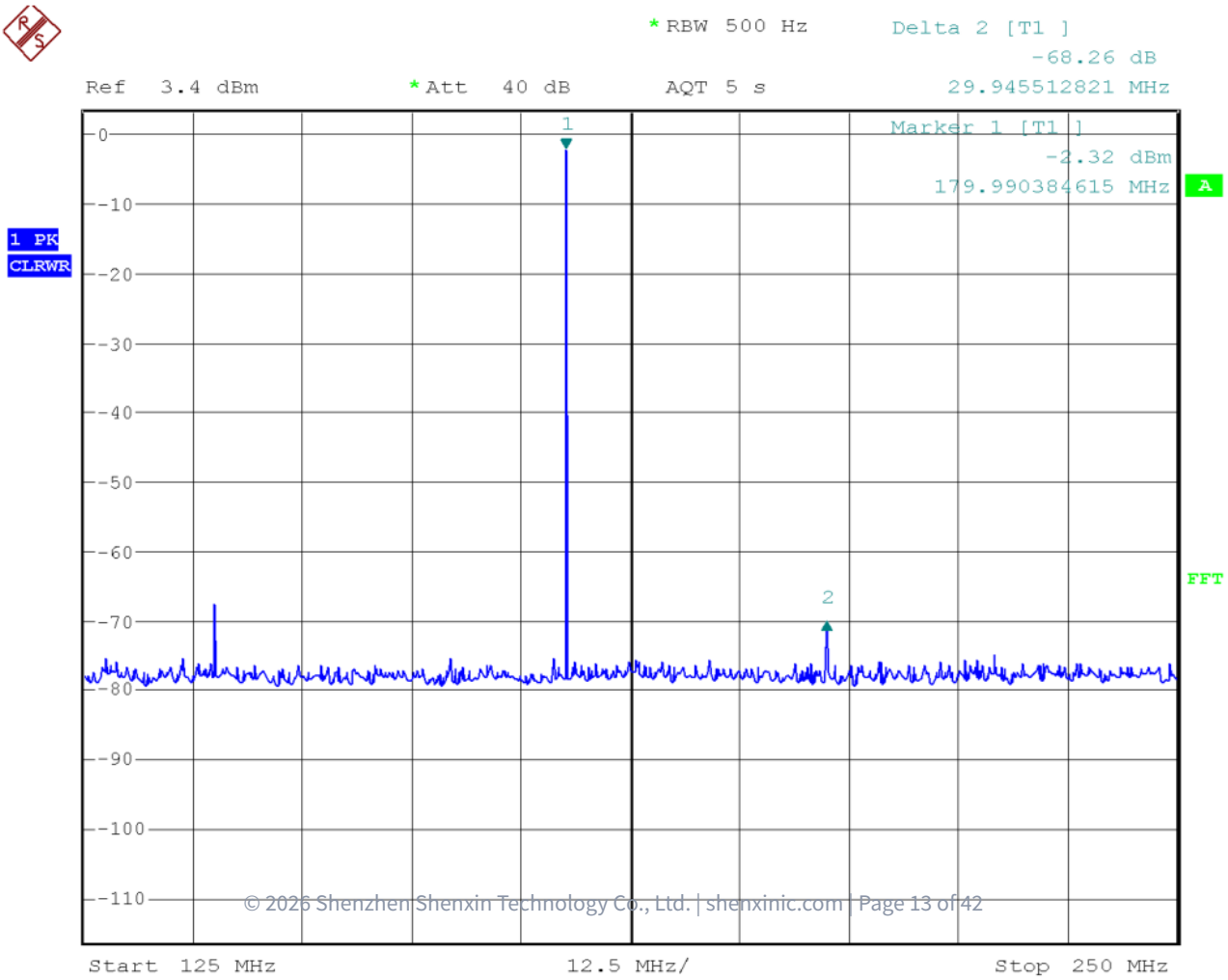


Figure 4: Differential and integral nonlinearity error curves, TA=25°C

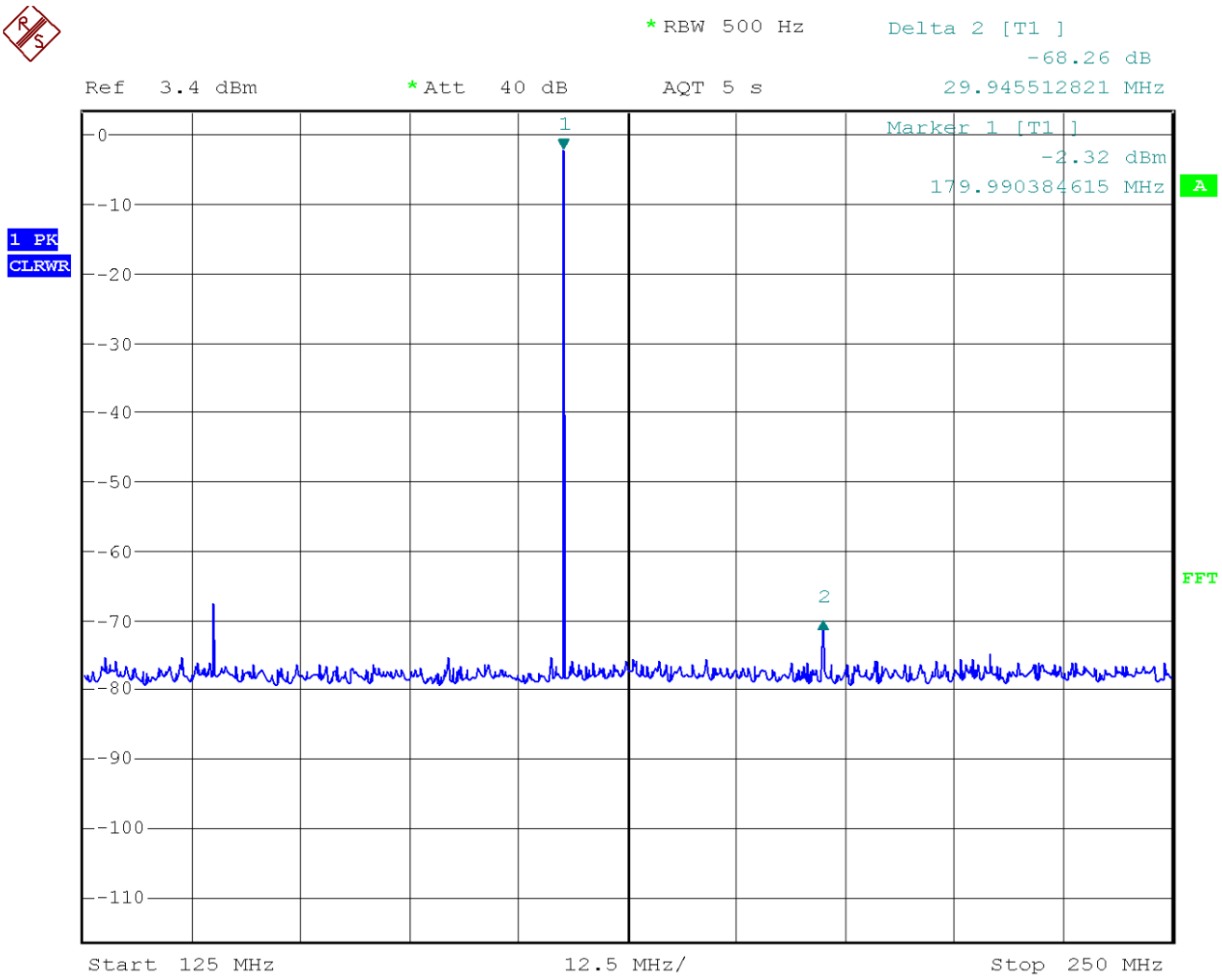


Figure 5: Output signal spectrum at fCLK=250MHz, fOUT=180MHz, TA=25°C

典型应用线路图 / Typical Application Circuit

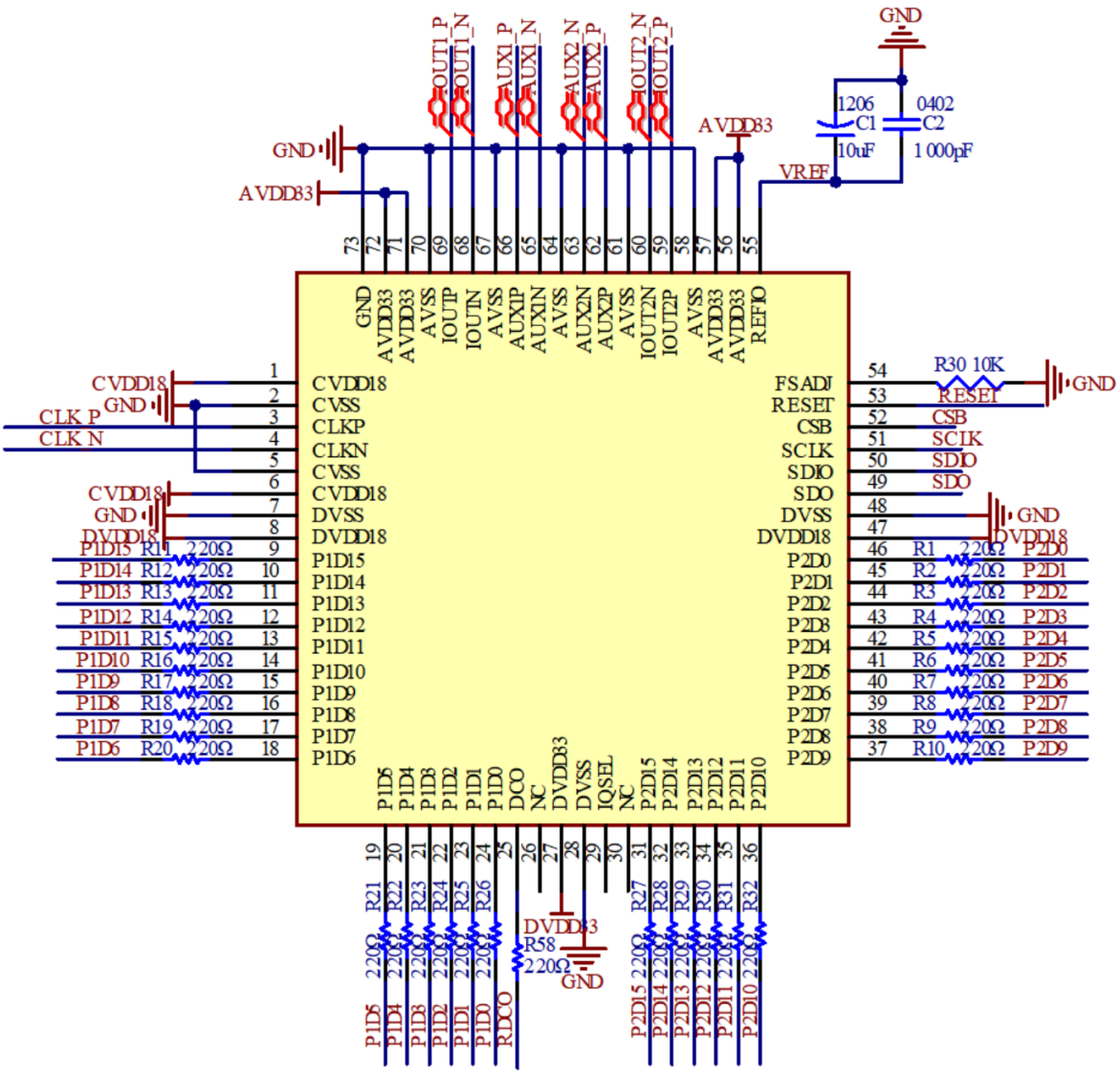


Figure 6: Typical peripheral circuit diagram

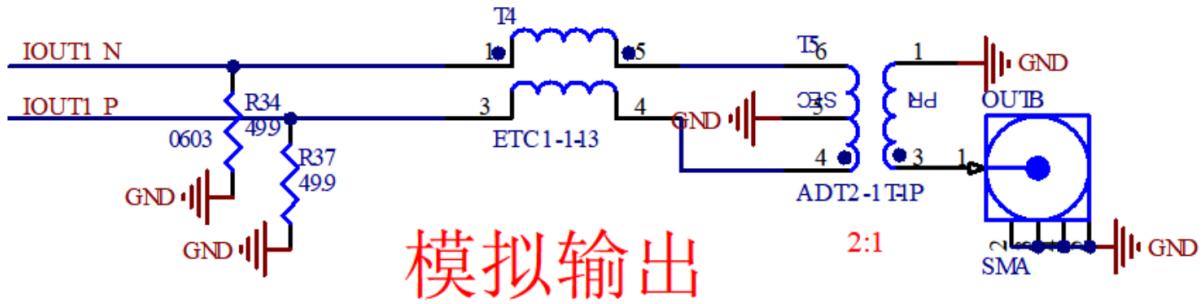


Figure 7: Analog front-end circuit

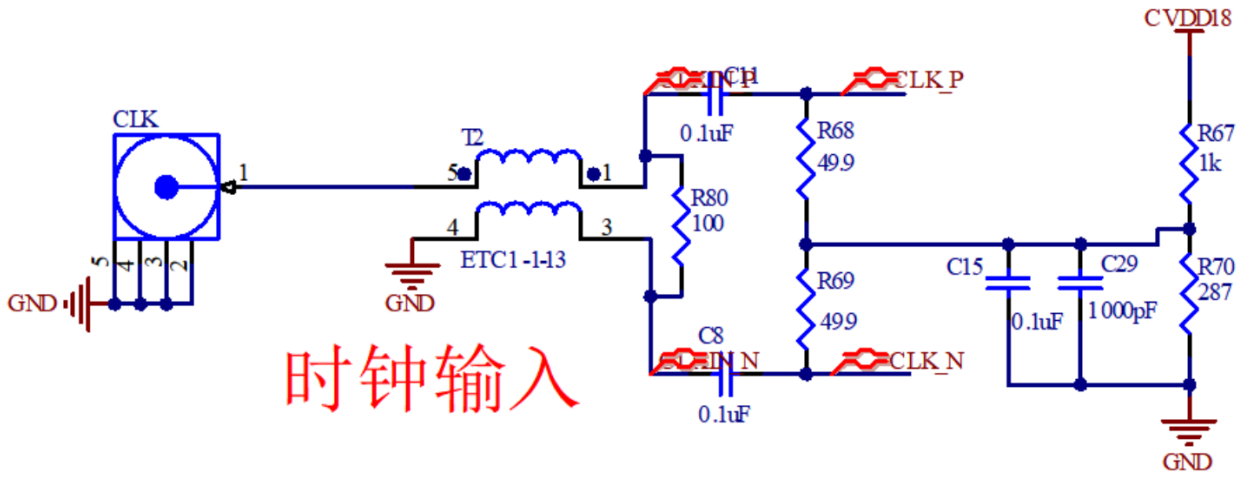


Figure 8: Clock front-end circuit

单元模块及工作原理 / Functional Blocks and Operating Principles

1、SPI 接口 / 1. SPI Interface

English: The SXD034 uses an SPI interface that connects easily to many industry-standard microcontrollers and microprocessors. This serial I/O port is compatible with most synchronous transfer formats, including Motorola SPI and Inter SSR protocols. The interface allows read/write access to all registers that configure the SXD034. Single- or multi-byte transfers are supported, in either MSB-first or LSB-first transfer format. The SXD034 serial interface port can be configured as a single bidirectional pin I/O (SDIO) or as two unidirectional input/output pins (SDIO/SDO).

中文： SXD034 采用了 SPI 接口，可轻松地与许多工业标准的微控制器和微处理器连接。该串行 I/O 端口与大多数同步传输格式兼容，包括 Motorola SPI 和 Inter SSR 协议。该接口允许读/写访问所有设置 SXD034 的寄存器。支持单或多字节传输，支持先 MSB（MSB-first）或先 LSB（LSB-first）传输格式。SXD034 串行接口端口可设置为一个双向管脚 I/O（SDIO）或两个单向的输入/输出管脚（SDIO/SDO）。

1.1 串行接口通常工作情况 / 1.1 Normal Serial Interface Operation

English: A SXD034 communication cycle has two phases. Phase 1 is the instruction cycle, used to write an instruction byte into the SXD034. The instruction byte provides the SXD034 serial controller with information for Phase 2 of the communication cycle (the data transfer cycle). The Phase 1 instruction byte defines whether the upcoming data transfer is a read or a write, how many bytes of data are to be transferred, and the starting register address corresponding to the data transfer of the first byte. A logic high followed by a logic low on the CSB pin resets the SPI port to its initial state and defines the start of the instruction cycle. From this point, the next 8 SCLK rising edges define the 8 bits of the instruction byte of the current communication cycle.

The remaining SCLK edges are used for Phase 2 of the communication cycle. Phase 2 implements the actual data transfer between the serial controller and the system controller. Phase 2 of the communication cycle can transfer 1, 2, 3, or 4 data bytes, the number being determined by the instruction

byte. A multi-byte transfer is the preferred approach. Single-byte transfers are typically used only when accessing a single byte or when CPU overhead must be reduced.

All serial data transferred into/out of the device is synchronized to the SCLK pin signal: input data is always latched on the rising edge of SCLK, and output data is valid after the falling edge of SCLK. Once the last bit of each transfer byte has been written, the entire register contents change immediately.

Whenever synchronization is lost, the current I/O operation can be terminated asynchronously simply by driving CSB high. Register data that has not been written when the I/O operation terminates will be lost. Driving CSB low resets the serial controller and starts a new communication cycle.

Table 1 shows the contents of the instruction byte.

中文： SXD034 的一个通信周期有两个阶段。阶段 1 是指令周期，用来写入一个指令字节到 SXD034。指令字节提供了 SXD034 串口控制器在通信周期的阶段 2（数据传输周期）的信息。阶段 1 的指令字节定义了即将到来的数据传递是读或是写，有多少字节的数据传输，以及第一个字节的数据传输所对应的起始寄存器地址。CSB 引脚逻辑高后跟一个逻辑低将 SPI 端口复位到初始状态并且定义了指令周期的起始状态。从此时开始，接下来的 8 个 SCLK 上升沿定义当前通信周期的指令字节的 8 位数据。

余下的 SCLK 边沿用于通信周期的阶段 2。阶段 2 实现串口控制器和系统控制器间实际的数据传输。通信周期的阶段 2 可以传输 1、2、3 或 4 个数据字节，具体字节数由指令字节决定。采用一个多字节传输是首选方案。单字节传输通常只需要在存取一个字节或者要减小 CPU 开销时采用。

传送入/出器件的所有串口数据与 SCLK 引脚信号同步，输入数据总是在 SCLK 的上升沿锁存，输出数据则在 SCLK 的下降沿之后有效。每个传输字节一旦写完最后一位整个寄存器内容将立即改变。

任何时候同步丢失，只要将 CSB 置于高电平就能够异步终止当前 I/O 操作。IO 操作终止后任何为写入的寄存器数据将丢失。将 CSB 置低将复位串口控制器并启动新的通信周期。

表 1 展示了指令字节所包含的内容。

表1 短指令字节描述表 / Table 1. Short Instruction Byte Description

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
读/写 / Read/Write	A6	A5	A4	A3	A2	A1	A0

English: R/W, bit 7 of the instruction byte, determines whether the data transfer following the instruction byte is a read or a write operation. Logic 1 indicates a read operation. Logic 0 indicates a write operation.

N1 and N2, bits 6 and 5 of the instruction byte, determine how many bytes are to be transferred during the data transfer cycle, decoded as shown in Table 2.

中文： R/W，指令字节的 bit7，决定了指令字节后的数据传输是读操作还是写操作。逻辑 1 表示读操作。逻辑 0 表示写操作。

N1，N2，指令字节的 bit6 和 bit5，决定了在数据传输周期有多少字节需要传输，解码如表 2 所示。

表2 字节传输计数表 / Table 2. Byte Transfer Count

N1	N2	描述 / Description
0	0	传输 1 个字节 / Transfer 1 byte
0	1	传输 2 个字节 / Transfer 2 bytes
1	0	传输 3 个字节 / Transfer 3 bytes
1	1	传输 4 个字节 / Transfer 4 bytes

English: A4, A3, A2, A1, A0, bits 4, 3, 2, 1, 0 of the instruction byte, determine which register is accessed by the data-transfer portion of the communication cycle. For a multi-byte transfer, whether this address denotes the starting byte address or the ending byte address depends on the current data transfer mode. For MSB-first mode, the address specified by the current operation cycle is the ending address, i.e., the address of the most significant data; the remaining addresses of the multi-byte data transfer are generated by the serial controller decrementing from the specified address. For LSB-first mode, the address specified by the current operation cycle is the starting address, i.e., the address of the least significant data; the remaining addresses of the multi-byte data transfer are generated by the serial controller incrementing from the specified address.

The serial port supports MSB-first and LSB-first data formats. This function is controlled by LSBFIRST (Reg0x00, Bit6). The default is MSB first (LSBFIRST = 0).

When LSBFIRST = 0 (MSB first), instruction and data bytes must be written in order from MSB to LSB. In MSB-first format, a multi-byte data transfer starts with the instruction byte, which contains the register address information of the most significant byte. Subsequent data bytes must follow the order from high address to low address. In MSB-first mode, the serial port's internal byte address generator decrements successively, providing the register address for each data byte of the multi-byte communication cycle.

When LSBFIRST = 1 (LSB first), instruction and data bytes must be written in order from the least significant bit to the most significant bit. In LSB-first format, a multi-byte data transfer starts with the instruction byte, which contains the register address information of the least significant byte, followed by multiple data bytes. In LSB-first mode, the serial port's internal byte address generator increments successively, providing the register address for each data byte of the multi-byte communication cycle.

When the serial port attribute configuration needs to be changed, a single-byte transfer is recommended to avoid possible unpredictable device behavior.

中文： A4，A3，A2，A1，A0，指令字节的 bit4，bit3，bit2，bit1，bit0，决定了通信周期的数据传输部分存取的是哪个寄存器。对于多字节传输，该地址表示起始字节地址还是终止地址取决于当前数据传输的模式。对于 MSB-first 模式，当前操作周期指定的地址是终止地址或者高有效位数据地址，多字节数据传输的其余地址由串口控制器从指定地址处递减产生。对于 LSB-first 模式，当前操作周期指定的地址是起始地址或者低有效位数据地址，多字节数据传输的其余地址由串口控制器从指定地址处递增产生。

串口支持 MSB-first 和 LSB-first 数据格式。该功能受 LSBFIRST（Reg0x00, Bit6）控制。默认为 MSB first（LSBFIRST＝0）。

当 LSBFIRST＝0（MSB first）时，指令和数据字节必须按从 MSB 到 LSB 的顺序写入。在 MSB-first 格式时，多字节数据传输开始于指令字节，该指令字节包含了最高位字节的寄存器地址信息。接下来的数据字节需要遵循从高地址到低地址的顺序。在 MSB-first 模式下，串行端口内部字节地址发生器会逐次递减，为多字节通信周期的每个数据字节提供寄存器地址。

当 LSBFIRST＝1（LSB first）时，指令和数据字节必须按从最低位到最高位的顺序写入。在 LSB-first 格式时，多字节数据传输开始于指令字节，该指令字节包含了最低位字节的寄存器地址信息，接着是多个数据字节。在 LSB-first 模式下，串行端口内部字节地址发生器会逐次增加，为多字节通信周期的每个数据字节提供寄存器地址。

当需要改变串口属性配置时，建议使用单字节传输方式，以避免可能出现的无法预料的器件行为。

1.2 SPI 端口描述 / 1.2 SPI Port Description

English: CSB – Chip select signal Active low, starts an input and defines a communication cycle. It allows multiple devices to use the same serial channel. The chip-select signal should remain low throughout the communication cycle. Driving the CSB pin high at any time can terminate an incomplete data transfer. When this port input is high, the SDO and SDIO ports become high-impedance.

SCLK – Serial clock SCLK is used to synchronize data to and from the SXD034 and to run the internal state machine. The maximum operating frequency of SCLK is 40MHz. Data is written on the rising edge of SCLK. Data is read out on the falling edge.

SDIO – Serial data I/O port Data is always written into the device through this port. In addition, this port can also be used as a bidirectional data line. This port is configured by SDIO_DIR (Reg0x00, Bit7). The default value is 0, which configures SDIO as a unidirectional port.

SDO – Serial data output For protocols with independent transmit and receive data lines, data is read out from this port. Register bit SDIO_DIR (Reg0x00, Bit7) configures this port. If this bit is set to 1, SDO is placed in a high-impedance state and cannot output data.

中文： CSB－片选信号 低有效开始输入及定义一个通信周期。允许多个器件使用相同的串行通道。在整个通信周期内片选信号应该保持为低。任何时候将 CSB 引脚置高可以终止未完成的数据传输。当该端口输入为高时，端口 SDO 和 SDIO 变为高阻态。

SCLK-串行时钟 SCLK 用来同步到 SXD034 和源于 SXD034 的数据，以及运行内部状态机。SCLK 的最大工作频率为 40MHz。数据写入是在 SCLK 的上升沿。数据读出是在下降沿。

SDIO－串行数据 I/O 端口 数据总是从该端口写入器件。另外，该端口还可以用作双向数据线。由 SDIO_DIR（Reg0x00, Bit7）对该端口配置。默认值为 0，SDIO 配置成单向端口。

SDO－串行数据输出 对于独立发射和接收数据线的协议，数据从该端口读出。寄存器位 SDIO_DIR（Reg0x00, Bit7）对该端口进行配置。如果该位被置为 1，SDO 被置为高阻态，不能输出数据。

1.3 SPI 寄存器映射表 / 1.3 SPI Register Map

表3 SPI 寄存器映射表 / Table 3. SPI Register Map

寄存器 / Register	地址 / Address	默认值 / Default	第7位 / Bit 7	第6位 / Bit 6	第5位 / Bit 5	第4位 / Bit 4	第3位 / Bit 3	第2位 / Bit 2	第1位 / Bit 1	第0位 / Bit 0
SPI 控制 / SPI control	0x00	0x00	SDIODIR	LSBFIRST	SWRESET					
	0x02	0x00	DATTYPE	ONEPORT			INVDCO			

寄存器 / Register	地址 / Address	默认值 / Default	第7位 / Bit 7	第6位 / Bit 6	第5位 / Bit 5	第4位 / Bit 4	第3位 / Bit 3	第2位 / Bit 2	第1位 / Bit 1	第0位 / Bit 0
数据控制 / Data control										
断电 / Power-down	0x03	0x00	PD_DCO		PD_AUX2	PD_AUX1	PD_BIAS	PD_CLK	PD_DAC2	PD_DAC1
DAC 模式选择 / DAC mode select	0x0A	0x00					DAC1MOD [1:0]		DAC2MOD [1:0]	
DAC1 增益 LSB / DAC1 gain LSB	0x0B	0xF9	DAC1FSC[7:0]							
DAC1 增益 MSB / DAC1 gain MSB	0x0C	0x01							DAC1FSC[9:8]	
辅助 DAC1 LSB / Auxiliary DAC1 LSB	0x0D	0x00	AUXDAC1[7:0]							
辅助 DAC1 MSB / Auxiliary DAC1 MSB	0x0E	0x00	AUX1PIN	AUX1DIR					AUXDAC1[9:8]	
DAC2 增益 LSB / DAC2 gain LSB	0x0F	0xF9	DAC2FSC[7:0]							
DAC2 增益 MSB / DAC2 gain MSB	0x10	0x01							DAC2FSC[9:8]	
辅助 DAC2 LSB / Auxiliary DAC2 LSB	0x11	0x00	AUXDAC2[7:0]							
辅助 DAC2	0x12	0x00	AUX2PIN	AUX2DIR					AUXDAC2[9:8]	

寄存器 / Register	地址 / Address	默认值 / Default	第7位 / Bit 7	第6位 / Bit 6	第5位 / Bit 5	第4位 / Bit 4	第3位 / Bit 3	第2位 / Bit 2	第1位 / Bit 1	第0位 / Bit 0
MSB / Auxiliary DAC2 MSB										

English: The SPI register table is described in detail in Table 4: unless otherwise stated, for all defined bits, reading these registers returns the previously written value.

中文： SPI 寄存器表具体描述如表 4：除非另有说明，对所有定义位，读取这些寄存器将返回之前写入的值。

表4 SPI 寄存器描述 / Table 4. SPI Register Description

寄存器 / Register	地址 / Address	位 / Bit	名字 / Name	描述 / Description
SPI 控制 / SPI control	0x00	7	SDIODIR	0=SPI 工作于四线模式，SDIO 仅作为输入。/ 0 = SPI operates in 4-wire mode, SDIO is input only. 1=SPI 工作于三线模式，SDIO 作为双向输入/输出。/ 1 = SPI operates in 3-wire mode, SDIO is a bidirectional input/output.
SPI 控制 / SPI control	0x00	6	LSBFIRST	0=LSBFIRST 功能关闭，SPI 串行数据模式为 MSB 到 LSB。/ 0 = LSBFIRST function off, SPI serial data mode is MSB to LSB. 1=LSBFIRST 功能开启，SPI 串行数据模式为 LSB 到 MSB。/ 1 = LSBFIRST function on, SPI serial data mode is LSB to MSB.
SPI 控制 / SPI control	0x00	5	SWRESET	0=在软复位之后继续普通工作。/ 0 = Continue normal operation after soft reset. 1=软复位；向所有寄存器载入默认值(除了寄存器 0x00)。/ 1 = Soft reset; load defaults into all registers (except register 0x00).
数据控制 / Data control	0x02	7	DATTYPE	0=DAC 输入数据为二进制格式的 2 的补码。/ 0 = DAC input data is in binary two's-complement format. 1=DAC 输入数据为二进制格式的无符号数。/ 1 = DAC input data is an unsigned number in binary format.
数据控制 / Data control	0x02	6	ONEPORT	0=普通的双端口输入模式。/ 0 = Normal dual-port input mode. 1=可选的单端口输入模式，只在端口 1 接收交织的数据。/ 1 = Optional single-port input mode; interleaved data is received at port 1 only.
数据控制 / Data control	0x02	4	INVDCO	1=数据输出时钟反相。/ 1 = Data output clock inverted.
断电 / Power-down	0x03	7	PD_DCO	1=数据输出时钟断电。/ 1 = Data output clock powered down.
断电 / Power-down	0x03	5	PD_AUX2	1=辅助 DAC2 断电。/ 1 = Auxiliary DAC2 powered down.
断电 / Power-down	0x03	4	PD_AUX1	1=辅助 DAC1 断电。/ 1 = Auxiliary DAC1 powered down.
断电 / Power-down	0x03	3	PD_BIAS	1=基准电路断电。/ 1 = Reference circuit powered down.
断电 / Power-down	0x03	2	PD_CLK	1=时钟输入电路断电。/ 1 = Clock input circuit powered down.
断电 / Power-down	0x03	1	PD_DAC2	1=DAC2 断电。/ 1 = DAC2 powered down.
断电 / Power-down	0x03	0	PD_DAC1	1=DAC1 断电。/ 1 = DAC1 powered down.

寄存器 / Register	地址 / Address	位 / Bit	名字 / Name	描述 / Description
DAC 模式选择 / DAC mode select	0x0A	3:2	DAC1MOD[1:0]	00=DAC1 工作于普通模式。/ 00 = DAC1 operates in normal mode. 01=DAC1 工作于混频模式。/ 01 = DAC1 operates in mix mode. 10=DAC1 工作于归零模式。/ 10 = DAC1 operates in return-to-zero mode.
DAC 模式选择 / DAC mode select	0x0A	1:0	DAC2MOD[1:0]	00=DAC2 工作于普通模式。/ 00 = DAC2 operates in normal mode. 01=DAC2 工作于混频模式。/ 01 = DAC2 operates in mix mode. 10=DAC2 工作于归零模式。/ 10 = DAC2 operates in return-to-zero mode.
DAC1 增益 / DAC1 gain	0x0B	7:0	DAC1FSC[7:0]	DAC1 满度输出电流 10 位调节码字。/ DAC1 full-scale output current 10-bit adjustment code. （与 0x0C 的 DAC1FSC[9:8] 合并 / combined with DAC1FSC[9:8] in 0x0C）
DAC1 增益 / DAC1 gain	0x0C	1:0	DAC1FSC[9:8]	0x03FF=设置满度输出电流为最大值 31.66mA。/ 0x03FF = set full-scale output current to the maximum, 31.66mA. 0x01F9=设置满度输出电流为名义值 20mA。/ 0x01F9 = set full-scale output current to the nominal value, 20mA. 0x0000=设置满度输出电流为最小值 8.64mA。/ 0x0000 = set full-scale output current to the minimum, 8.64mA.
辅助 DAC1 / Auxiliary DAC1	0x0D	7:0	AUXDAC1[7:0]	辅助 DAC1 输出电流 10 位调节码字。/ Auxiliary DAC1 output current 10-bit adjustment code. （与 0x0E 的 AUXDAC1[9:8] 合并 / combined with AUXDAC1[9:8] in 0x0E）
辅助 DAC1 / Auxiliary DAC1	0x0E	1:0	AUXDAC1[9:8]	0x03FF=设置输出电流为 2.0mA。/ 0x03FF = set output current to 2.0mA. 0x0200=设置输出电流为 1.0mA。/ 0x0200 = set output current to 1.0mA. 0x0000=设置输出电流为 0.0mA。/ 0x0000 = set output current to 0.0mA.
辅助 DAC1 / Auxiliary DAC1	0x0E	7	AUX1PIN	1=AUX1P 引脚有效。/ 1 = AUX1P pin active. 0=AUX1N 引脚有效。/ 0 = AUX1N pin active.
辅助 DAC1 / Auxiliary DAC1	0x0E	6	AUX1DIR	0=配置辅助 DAC1 为电流源。/ 0 = Configure auxiliary DAC1 as a current source. 1=配置辅助 DAC1 为电流沉。/ 1 = Configure auxiliary DAC1 as a current sink.
DAC2 增益 / DAC2 gain	0x0F	7:0	DAC2FSC[7:0]	DAC2 满度输出电流 10 位调节码字。/ DAC2 full-scale output current 10-bit adjustment code. （与 0x10 的 DAC2FSC[9:8] 合并 / combined with DAC2FSC[9:8] in 0x10）
DAC2 增益 / DAC2 gain	0x10	1:0	DAC2FSC[9:8]	0x03FF=设置满度输出电流为最大值 31.66mA。/ 0x03FF = set full-scale output current to the maximum, 31.66mA. 0x01F9=设置满度输出电流为名义值 20mA。/ 0x01F9 = set full-scale output current to the nominal value, 20mA. 0x0000=设置满度输出电流为最小值 8.64mA。。/ 0x0000 = set full-scale output current to the minimum, 8.64mA..
辅助 DAC2 / Auxiliary DAC2	0x11	7:0	AUXDAC2[7:0]	辅助 DAC2 输出电流 10 位调节码字。/ Auxiliary DAC2 output current 10-bit adjustment code. （与 0x12 的 AUXDAC2[9:8] 合并 / combined with AUXDAC2[9:8] in 0x12）
辅助 DAC2 / Auxiliary DAC2	0x12	1:0	AUXDAC2[9:8]	0x03FF=设置输出电流为 2.0mA。/ 0x03FF = set output current to 2.0mA. 0x0200=设置输出电流为 1.0mA。/ 0x0200 = set output current to 1.0mA. 0x0000=设置输出电流为 0.0mA。/ 0x0000 = set output current to 0.0mA.
辅助 DAC2 / Auxiliary DAC2	0x12	7	AUX2PIN	1=AUX2P 引脚有效。/ 1 = AUX2P pin active. 0=AUX2N 引脚有效。/ 0 = AUX2N pin active.
辅助 DAC2 / Auxiliary DAC2	0x12	6	AUX2DIR	0=配置辅助 DAC2 为电流源。/ 0 = Configure auxiliary DAC2 as a current source. 1=配置辅助 DAC2 为电流沉。/ 1 = Configure auxiliary DAC2 as a current sink.

2、数据输入 / 2. Data Input

English: The SXD034 can optionally operate in two data input modes: dual-port mode and single-port mode. When operating in the default dual-port mode (ONEPORT=0), each DAC receives data from its designated port. When operating in single-port mode (ONEPORT=1), both DACs receive data from port 1. In single-port mode, the data of DAC1 and DAC2 is interleaved, and the IQSEL input signal routes the data correctly to the DACs. In single-port mode: when the IQSEL signal is high, port 1 data is input to DAC1; when the IQSEL signal is low, port 1 data is input to DAC2. In dual-port mode, the IQSEL signal can be ignored.

In dual-port mode, the input data rate must be the sample rate (up to 250MSPS); in single-port mode, the input data rate must be twice the sample rate. Since the maximum input data rate is 250MSPS, in single-port mode the maximum DAC clock rate is 125MHz.

In both dual-port and single-port modes, the data clock output (DCO) signal used to drive the FPGA operates at the DAC sample rate. It can be inverted via the INVDCO bit.

中文： SXD034 可以选择性地工作在两种数据输入模式：双端口模式和单端口模式。当工作在默认的双端口模式时(ONEPORT=0)，每个 DAC 从指定的端口接收数据。当工作在单端口模式时 (ONEPORT=1)，两个 DAC 都从端口 1 接收数据。在单端口模式下，DAC1 和 DAC2 的数据是交织的，IQSEL 输入信号将数据正确地导向 DAC。在单端口模式下：当 IQSEL 信号为高，端口 1 的数据输入到 DAC1；当 IQSEL 信号为低，端口 1 的数据输入到 DAC2。在双端口模式下，IQSEL 信号可以忽略。

在双端口模式下，输入数据率必须为采样率（最高 250MSPS）在单端口模式下，输入数据率必须为两倍的采样率。由于输入数据率最高为 250MSPS，所以单端口模式下，DAC 时钟最高速率为 125MHz。

在双端口模式和单端口模式下，用于激励 FPGA 的数据时钟输出(DCO)信号都工作于 DAC 采样速率。它可以通过 INVDCO 位来反相。

2.1 输入数据时序 / 2.1 Input Data Timing

English: For most DACs, the signal-to-noise ratio (SNR) is a function of the positional relationship between the clock edges and the data transition edges. The SXD034 operates with rising-edge triggering, so it exhibits high SNR sensitivity when an input data transition edge approaches the rising clock edge.

The minimum setup time and hold time define, in each data cycle, a timing window within which data can be sampled correctly. The user must carefully lay out the data and clock delivered to the chip so that they stay away from the minimum setup time and minimum hold time.

中文： 对于大多数 DAC 来说，信噪比(SNR)都是时钟边沿和数据变化沿位置关系的函数。SXD034 采用上升沿触发工作方式，所以当输入数据变化沿接近时钟上升沿时表现出大的 SNR 敏感性。

最小的建立时间和保持时间在每一个数据周期确定了一个数据可以被正确采样的时序窗口。用户必须对送到芯片的数据和时钟进行仔细布局，使其远离最小建立时间和最小保持时间。

2.2 双端口模式时序 / 2.2 Dual-Port Mode Timing

English: Figure 9 is the timing illustration for dual-port mode. Data delivered to DAC1 is labeled Ix, and data delivered to DAC2 is labeled Qx. Setup and hold times are referenced to the positive edge of the DAC

clock. The timing of data arriving at the input pins must satisfy the minimum setup and hold times. Note that there is a fixed delay from DCO to the DAC clock, which can also be used to verify timing.

中文： 图 9 为双端口模式的时序说明图。送到 DAC1 的数据标注为 Ix，送到 DAC2 的数据标注为 Qx。建立和保持时间以 DAC 时钟的正边沿为基准。数据达到输入引脚的时序必须满足最小的建立和保持时间。注意 DCO 到 DAC 时钟有一个固定延迟，也可以用它来确认时序。

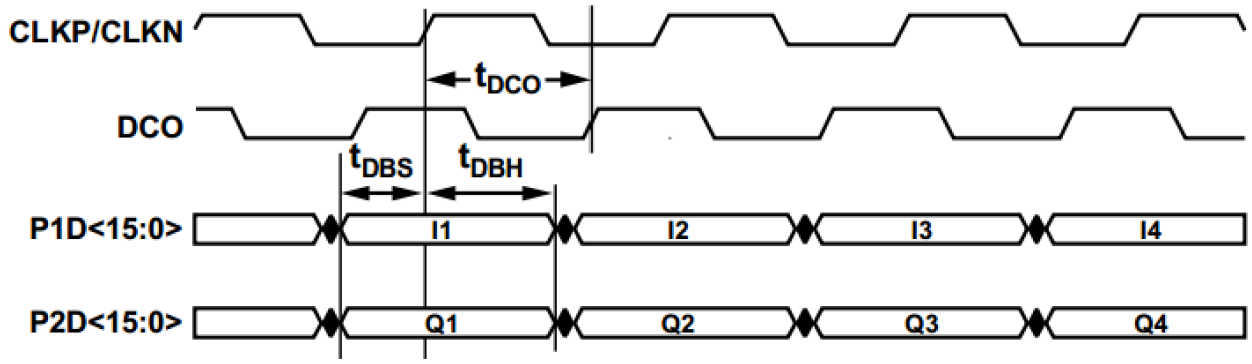


Figure 9: Dual-port mode timing diagram

2.3 单端口模式时序 / 2.3 Single-Port Mode Timing

English: Figure 10 is the timing illustration for single-port mode. In single-port mode, the data of both DACs comes from port 1. Ix and Qx data appear interleaved at port 1. The IQSEL signal accompanying the input data routes the Ix and Qx signals to the two DACs respectively. When the IQSEL signal is high, data is input to DAC1; when the IQSEL signal is low, data is input to DAC2. The IQSEL signal must be aligned in timing with the input data.

中文： 图 10 为双端口模式的时序说明图。在单端口模式下，两个 DAC 的数据都来自于端口 1。Ix 和 Qx 数据交织出现在端口 1。伴随输入数据的 IQSEL 信号将 Ix 和 Qx 信号分别导向两个 DAC。当 IQSEL 信号为高，数据输入到 DAC1；当 IQSEL 信号为低，数据输入到 DAC2。IQSEL 信号必须和输入数据在时序上对齐。

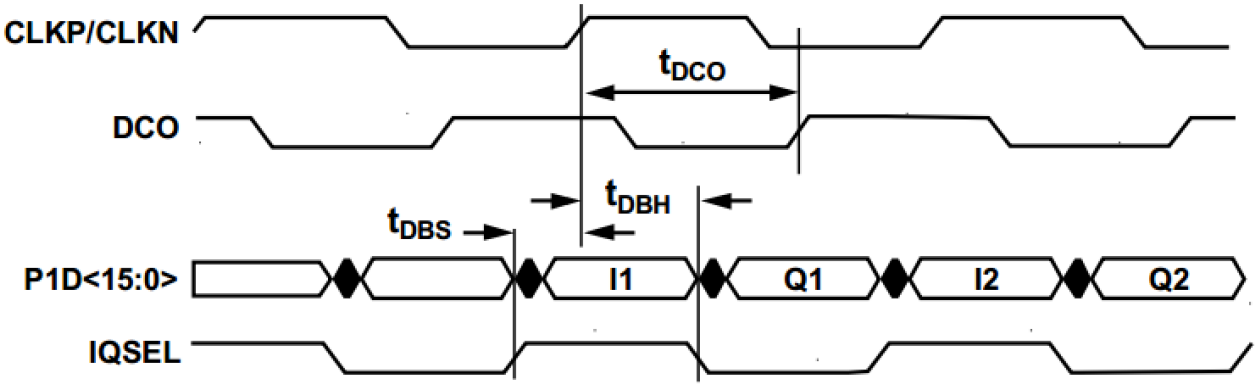


Figure 10: Single-port mode timing diagram

2.4 SPI 端口、Reset 和 Pin 模式 / 2.4 SPI Port, Reset and Pin Mode

English: Generally, after the SXD034 powers up, a high pulse must be applied to the RESET pin to ensure that all control registers are in their default state. Once the RESET pin goes low, the SPI port is activated.

The SXD034 supports Pin mode operation, which allows certain functions to be selected through pins rather than the SPI port. As long as the RESET pin is high, the device remains in Pin mode. In Pin mode, the functions of the four SPI port pins are as shown in Table 5.

中文： 一般来说，当 SXD034 上电后，需要给 RESET 引脚施加一个高脉冲以确保所有的控制寄存器处于默认状态。一旦 RESET 引脚变低，SPI 端口会被激活。

SXD034 支持 Pin 模式工作，它允许通过引脚而不是 SPI 端口来选择某些功能。只要 RESET 引脚为高，器件就始终处于 Pin 模式。在 Pin 模式下，四个 SPI 端口引脚的功能如表 5 所示。

表5 SPI 寄存器映射表 / Table 5. SPI Register Map

Pin 名称 / Pin Name	Pin 模式功能描述 / Pin-Mode Function Description
SCLK	等效于 ONEPORT，寄存器 0x02[6]，该位的值（1/0）等于引脚状态（高/低）。/ Equivalent to ONEPORT, register 0x02[6]; the value of this bit (1/0) equals the pin state (high/low).
SDIO	等效于 DATTYPE，寄存器 0x02[7]，该位的值（1/0）等于引脚状态（高/低）。/ Equivalent to DATTYPE, register 0x02[7]; the value of this bit (1/0) equals the pin state (high/low).
CSB	使能混频模式。当 CSB 为高，寄存器 0x0A 为 0x05，将 DAC1 和 DAC2 同时配置成混频模式。/ Enables mix mode. When CSB is high, register 0x0A is 0x05, configuring DAC1 and DAC2 into mix mode simultaneously.
SDO	使能全芯片断电。如果 SDO 为高，寄存器 0x03 为 0xFF。/ Enables full-chip power-down. If SDO is high, register 0x03 is 0xFF.

3、驱动 DACCLK 输入 / 3. Driving the DACCLK Input

English: The clock input requires a low-jitter drive signal. It is a PMOS input differential pair powered from a 1.8V supply. For a 400mV common-mode voltage, each input pin voltage can safely swing to 800mVp-p. Although these input levels are not directly LVDS-compatible, the clock can be driven by a DC-offset AC-coupled LVDS signal, as shown in Figure 11.

中文： 时钟输入要求一个低抖动的驱动信号。它是一个由 1.8V 电源供电的 PMOS 输入差分对。对于 400mV 共模电压，每个输入管脚电压可安全地摆到 800mVp-p。虽然这些输入电平不是直接 LVDS 兼容，时钟可由一个直流偏移交流耦合的 LVDS 信号驱动，如图 11 所示。

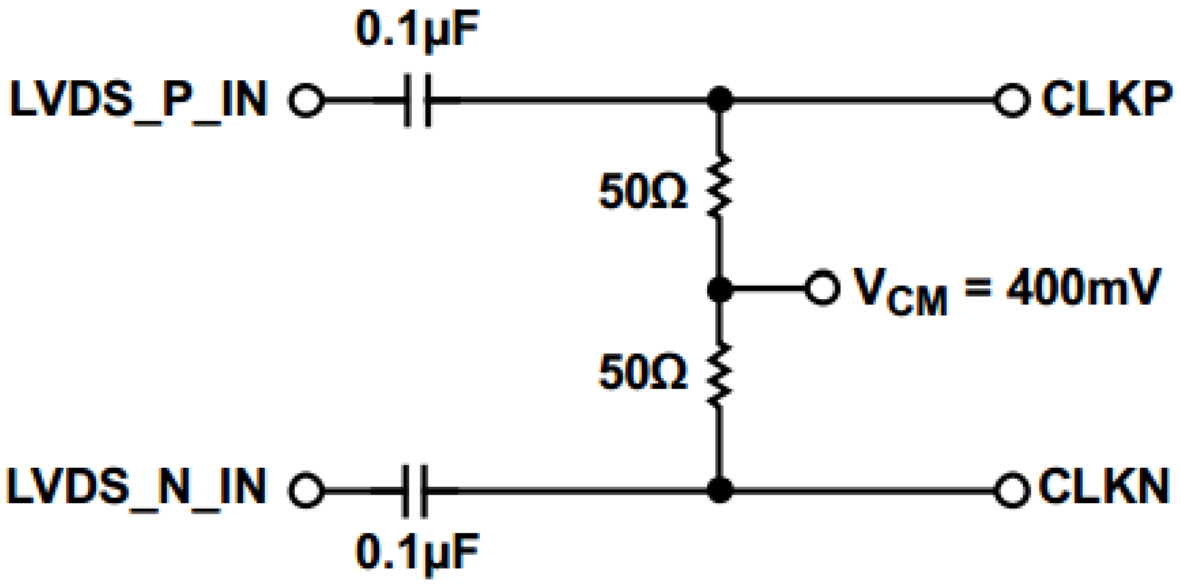


Figure 11: LVDS DAC clock drive circuit

English: At lower sample rates, a CMOS or TTL clock is also acceptable. It can be implemented through transformer coupling and clamping, as shown in Figure 12.

中文： 在更低的采样率时，CMOS 或者 TTL 时钟也是可以接受的。可以通过变压器耦合和箝位实现，如图 12 所示。

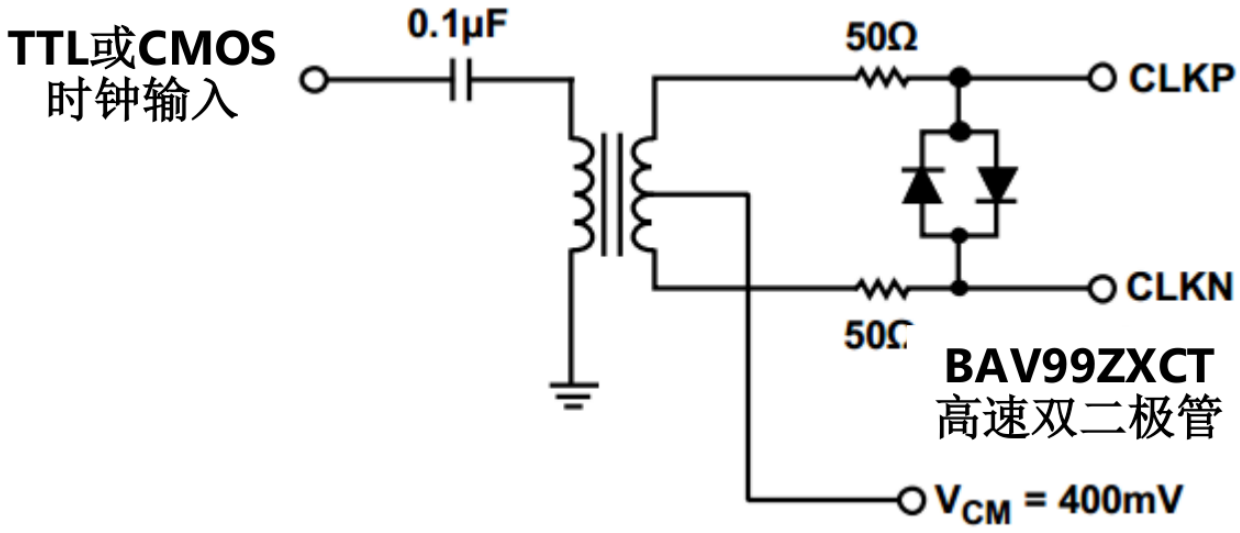


Figure 12: TTL or CMOS DAC clock drive circuit

English: If a sine-wave clock source is available, it can be coupled directly to the DAC clock input through a transformer. As shown in Figure 13.

中文： 如果有正弦波时钟源，可以将其直接通过变压器耦合至 DAC 时钟输入端。如图 13 所示。

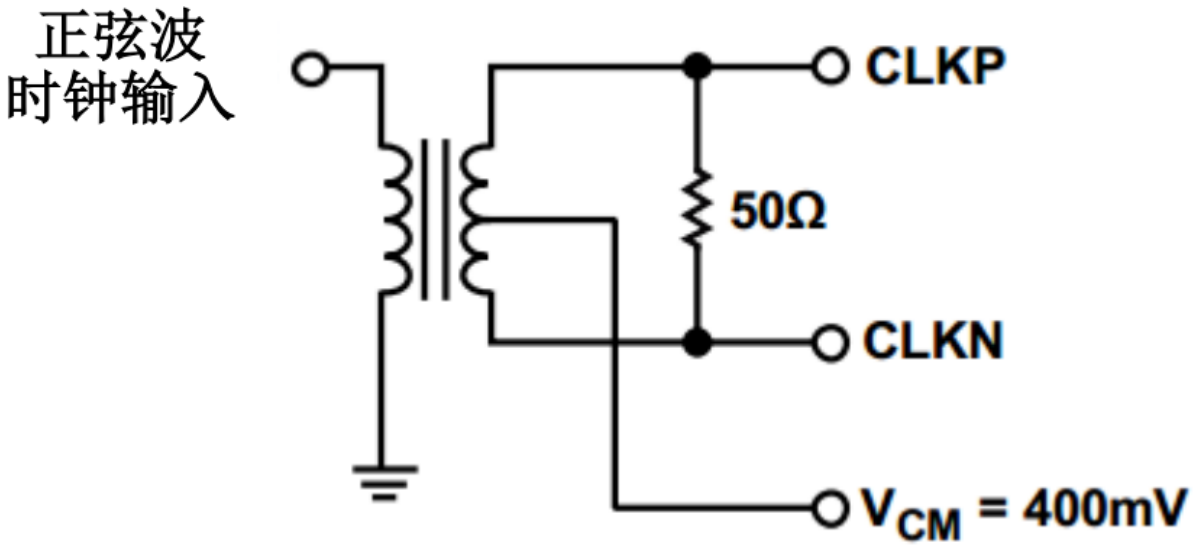


Figure 13: Sine-wave DAC clock drive circuit

English: The 400mV common-mode voltage can be obtained by simply dividing CVDD18 with a resistor network. As shown in Figure 14.

For any clock bias circuit, CVDD18 and CVSS must be used, because noise coupled onto the clock from other supplies will be amplified by the DAC input signal, degrading DAC performance.

中文： 400mV 的共模电压可以通过对 CVDD18 进行简单的电阻网络分压得到。如图 14 所示。

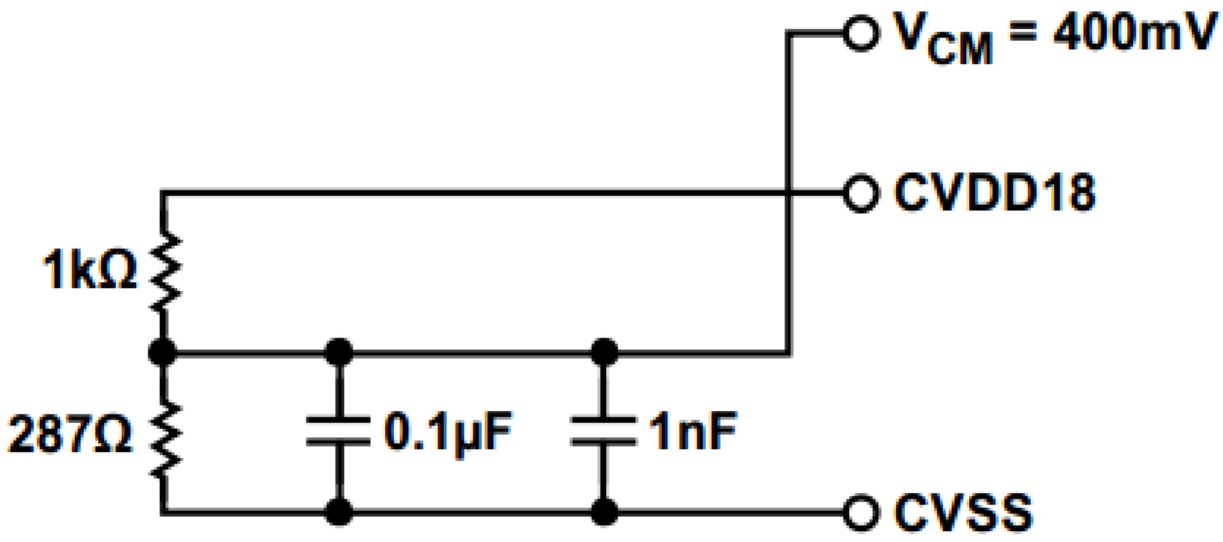


Figure 14: Common-mode voltage generation

中文（续）： 对任何时钟偏置电路都必须使用 CVDD18 和 CVSS，因为从其他电源耦合到时钟上的噪声会被 DAC 输入信号放大，从而降低 DAC 性能。

English (continued): For any clock bias circuit, CVDD18 and CVSS must be used, because noise coupled onto the clock from other supplies will be amplified by the DAC input signal, thereby degrading DAC performance.

4、满度电流产生 / 4. Full-Scale Current Generation

English: The full-scale currents of DAC1 and DAC2 are a function of the current flowing through the external resistor (connected to FSADJ, pin 54). This external resistor is 10kΩ. The internal amplifier sets its current to 120μA by making the voltage across the resistor equal to the bandgap reference voltage of 1.2V.

The REFIO pin (pin 55) must be bypassed to ground through a 0.1μF capacitor. The bandgap voltage on this pin can be used by other external circuits. The typical output impedance is 5kΩ. If needed, an external reference voltage can also be connected to REFIO to overdrive the internal reference.

The gains of DAC1 and DAC2 can be adjusted independently via the DAC1FSC[9:0] and DAC2FSC[9:0] bits. Under the default value 0x01F9, the full-scale current IFS is 20mA. The full-scale current range is from 8.6mA (0x0000) to 31.7mA (0x3FF):

IFS = (1.2V / 10000) × (72 + ((3/16) × DACnFSC))

中文： DAC1 和 DAC2 的满度电流是流经外部电阻（连接到 FSADJ，第 54 脚）电流的函数。此外部电阻为 10kΩ。内部放大器通过使电阻上的电压为带隙基准电压 1.2V 来设置其电流为 120μA。

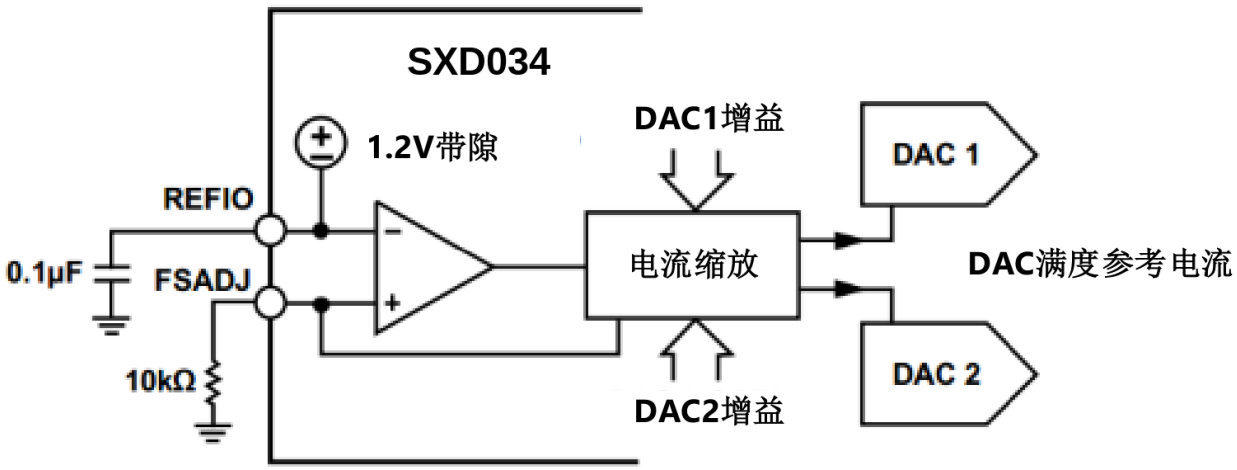


Figure 15: Reference circuit

中文（续）： REFIO 脚（第 55 脚）必须通过一个 0.1μF 电容旁路到地。这个脚上的带隙电压可以用于其他外部电路。典型输出阻抗为 5kΩ。如果有需要，还可以连接一个外部基准参考电压到 REFIO 以过驱动内部基准参考。

DAC1 和 DAC2 的增益可以通过 DAC1FSC[9:0]和 DAC2FSC[9:0]位进行独立地调节。默认值 0x01F9 的条件下，满度电流 IFS 为 20mA。满度电流范围从 8.6mA(0x0000)到 31.7mA(0x3FF)：

IFS = (1.2V / 10000) × (72 + ((3/16) × DACnFSC)) [原文公式：IFS = 1.2V/10000 × (72 + (3/16 × DACnFSC))]

5、模拟工作模式 / 5. Analog Operating Modes

English: The SXD034 can operate in 3 modes: normal mode, return-to-zero mode, and mix mode. Normal mode is suitable for operation in the first Nyquist zone, with maximum signal power; return-to-zero mode is suitable for operation in the second Nyquist zone, with minimum roll-off; mix mode is suitable for

operation in the second/third Nyquist zone, with maximum signal power. Different operating modes can be implemented by modifying Bit[3:0] of register 0x0A via SPI.

The output signal envelopes in the different modes are shown in Figure 16.

中文： SXD034 可以工作于 3 种模式：正常模式，归零模式和混频模式。其中正常模式适合工作在第一 Nyquist 区，信号功率最大，归零模式适合工作在第二 Nyquist 区，滚降最小，混频模式适合工作在第二/三 Nyquist 区，信号功率最大。可以通过 SPI 对寄存器 0x0A 的 Bit[3:0]修改实现不同的工作模式。

不同模式下，输出信号的包络如图 16 所示。

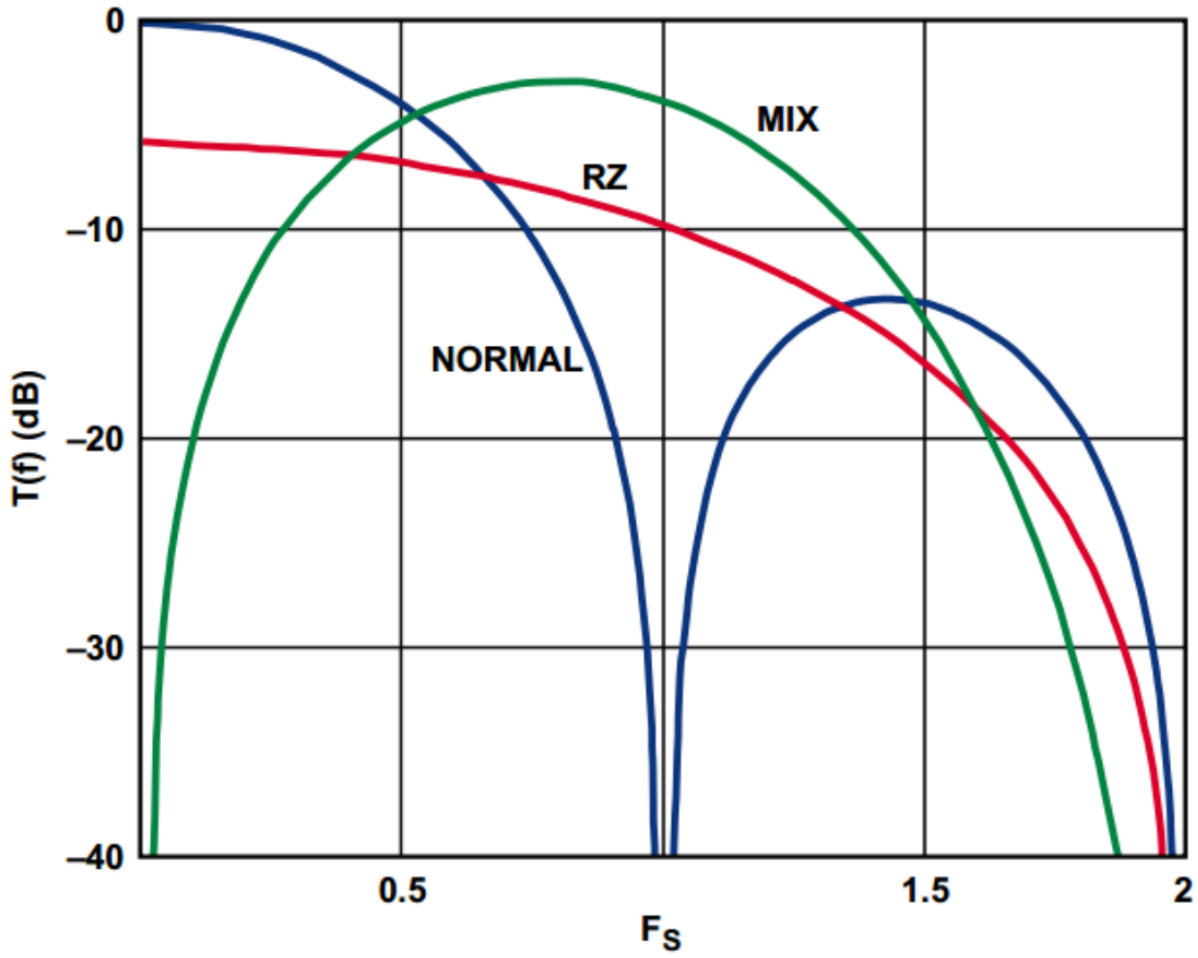


Figure 16: Output signal envelopes in different analog operating modes

6、辅助 DAC / 6. Auxiliary DAC

English: Figure 17 is the functional block diagram of the SXD034 auxiliary DAC. The auxiliary DAC is a current-output device with two output pins, AUXP and AUXN. The active pin can be configured as a current source or a current sink with a full-scale current of 2mA. When configured as a current source, the compliance voltage range is 0V to 1.6V; when configured as a current sink, the compliance voltage range is reduced to 0.8V to 1.6V. Only one of AXUP or AUXN can be active at the same time; the inactive pin is always in a high-impedance state (greater than 100kΩ).

In single-sideband transmitter applications, the input reference DC offset current of the quadrature modulator and the output offset voltage of the DAC cause local-oscillator feedthrough at the modulator

output, degrading system performance. The auxiliary DAC can eliminate the DC offset and the local-oscillator feedthrough. The circuit configuration for implementing DC offset correction with the auxiliary DAC depends on the interface between the DAC and the modulator.

中文： 图 17 是 SXD034 辅助 DAC 的功能框图。辅助 DAC 是有两个输出引脚 AUXP 和 AUXN 的电流输出器件。激活的引脚可以被配置成满度电流为 2mA 的电流源或者电流沉。当配置成电流源，顺从电压范围为 0V 到 1.6V；当配置成电流沉，顺从电压范围减小到 0.8V 到 1.6V。在同一时间只能激活 AXUP 或 AUXN 中的一个，未被激活的引脚始终处于高阻态（大于 100kΩ）。

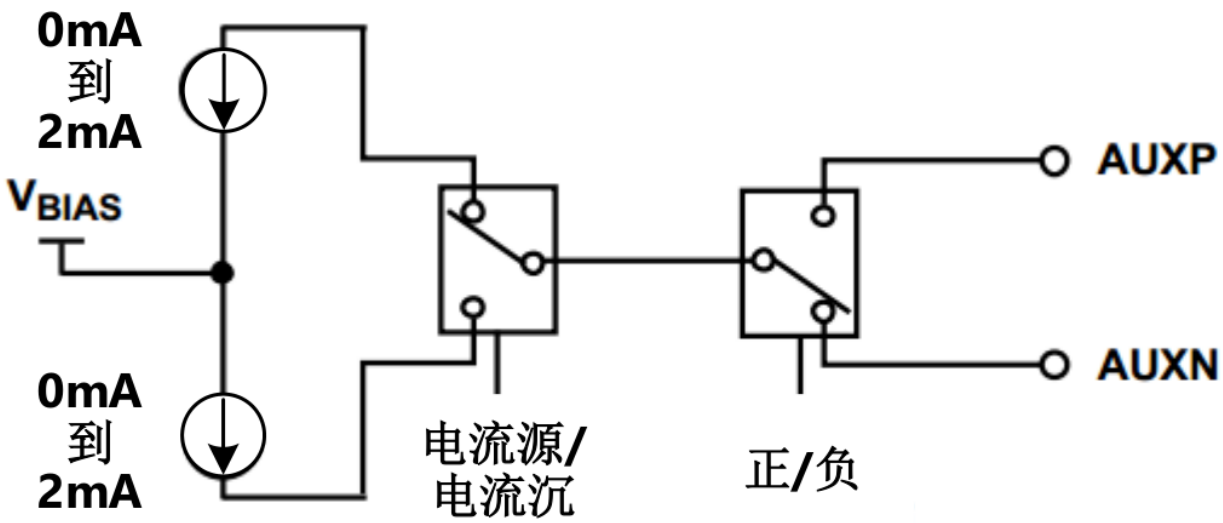


Figure 17: Auxiliary DAC functional block diagram

中文（续）： 在单边带发射机应用中，正交调制器的输入参考直流失调电流和 DAC 的输出失调电压会导致调制器输出的本振馈通，从而降低系统性能。辅助 DAC 可以消除直流失调以及本振馈通。采用辅助 DAC 实现直流失调校正的电路配置取决于 DAC 和调制器的接口。

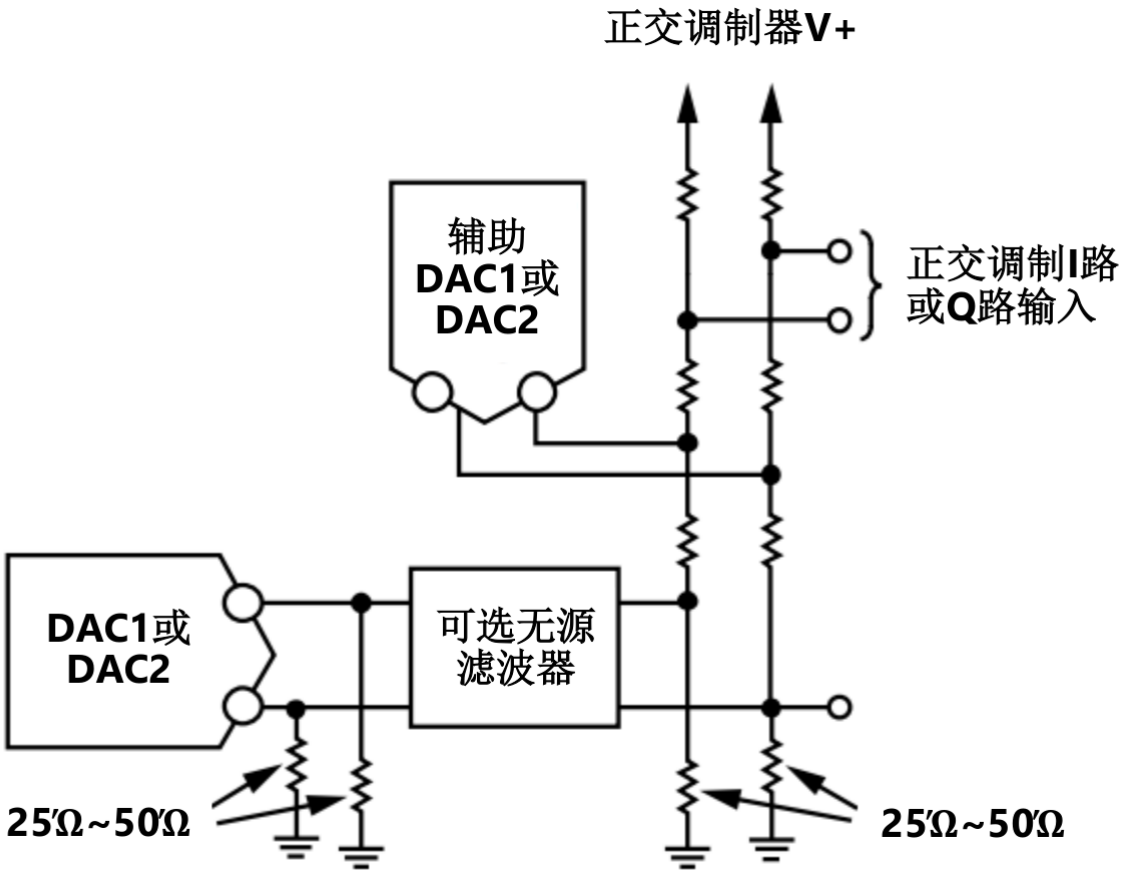


Figure 18: DC-coupling the DAC to a quadrature modulator using passive DC level shifting

寄存器 / Registers

1、默认值 / 1. Default Values

English: After reset, the key registers are loaded with default values. The default values of the registers are given in the memory map register table.

中文： 复位后，关键寄存器加载默认值。寄存器的默认值在存储器映射寄存器表中。

2、SPI 软复位 / 2. SPI Soft Reset

English: After a soft reset command is issued, 10ms is required before recovery. When used in application settings, ensure sufficient delay is programmed into the firmware for the soft reset before starting operation.

中文： 发出软复位指令后，需要 10ms 才能恢复。当用于应用设置时，确保在开始运行之前软复位编程到固件中有足够的延迟。

3、内存映射寄存器表 / 3. Memory Map Register Table

表6 SPI 寄存器 / Table 6. SPI Registers

寄存器 / Register	地址 / Address	默认值 / Default	位 / Bit	名字 / Name	描述 / Description
SPI 控制 / SPI control	0x00	0x00	7	SDIODIR	0=SPI 工作于四线模式，SDIO 仅作为输入。/ 0 = SPI operates in 4-wire mode, SDIO is input only. 1=SPI 工作于三线模式，SDIO 作为双向输入/输出。/ 1 = SPI operates in 3-wire mode, SDIO is a bidirectional input/output.
SPI 控制 / SPI control	0x00	0x00	6	LSBFIRST	0=LSBFIRST 功能关闭，SPI 串行数据模式为 MSB 到 LSB。/ 0 = LSBFIRST function off, SPI serial data mode is MSB to LSB. 1=LSBFIRST 功能开启，SPI 串行数据模式为 LSB 到 MSB。/ 1 = LSBFIRST function on, SPI serial data mode is LSB to MSB.
SPI 控制 / SPI control	0x00	0x00	5	SWRESET	0=在软复位之后继续普通工作。/ 0 = Continue normal operation after soft reset. 1=软复位；向所有寄存器载入默认值(除了寄存器 0x00)。/ 1 = Soft reset; load defaults into all registers (except register 0x00).
数据控制 / Data control	0x02	0x00	7	DATTYPE	0=DAC 输入数据为二进制格式的 2 的补码。/ 0 = DAC input data is in binary two's-complement format. 1=DAC 输入数据为二进制格式的无符号数。/ 1 = DAC input data is an unsigned number in binary format.
数据控制 / Data control	0x02	0x00	6	ONEPORT	0=普通的双端口输入模式。/ 0 = Normal dual-port input mode. 1=可选的单端口输入模式，只在端口 1 接收交织的数据。/ 1 = Optional single-port input mode; interleaved data is received at port 1 only.
数据控制 / Data control	0x02	0x00	4	INVDCO	1=数据输出时钟反相。/ 1 = Data output clock inverted.
断电 / Power-down	0x03	0x00	7	PD_DCO	1=数据输出时钟断电。/ 1 = Data output clock powered down.
断电 / Power-down	0x03	0x00	5	PD_AUX2	1=辅助 DAC2 断电。/ 1 = Auxiliary DAC2 powered down.
断电 / Power-down	0x03	0x00	4	PD_AUX1	1=辅助 DAC1 断电。/ 1 = Auxiliary DAC1 powered down.
断电 / Power-down	0x03	0x00	3	PD_BIAS	1=基准电路断电。/ 1 = Reference circuit powered down.
断电 / Power-down	0x03	0x00	2	PD_CLK	1=时钟输入电路断电。/ 1 = Clock input circuit powered down.
断电 / Power-down	0x03	0x00	1	PD_DAC2	1=DAC2 断电。/ 1 = DAC2 powered down.
断电 / Power-down	0x03	0x00	0	PD_DAC1	1=DAC1 断电。/ 1 = DAC1 powered down.
DAC 模式选择 / DAC mode select	0x0A	0x00	3:2	DAC1MOD[1:0]	00=DAC1 工作于普通模式。/ 00 = DAC1 operates in normal mode. 01=DAC1 工作于混频模式。/ 01 = DAC1 operates in mix mode. 10=DAC1 工作于归零模式。/ 10 = DAC1 operates in return-to-zero mode.
	0x0A	0x00	1:0	DAC2MOD[1:0]	

寄存器 / Register	地址 / Address	默认值 / Default	位 / Bit	名字 / Name	描述 / Description
DAC 模式选择 / DAC mode select					00=DAC2 工作于普通模式。/ 00 = DAC2 operates in normal mode. 01=DAC2 工作于混频模式。/ 01 = DAC2 operates in mix mode. 10=DAC2 工作于归零模式。/ 10 = DAC2 operates in return-to-zero mode.
DAC1 增益 / DAC1 gain	0x0B	0xF9	7:0	DAC1FSC[7:0]	DAC1 满度输出电流 10 位调节码字。/ DAC1 full-scale output current 10-bit adjustment code. （与 0x0C 合并 / combined with 0x0C）
DAC1 增益 / DAC1 gain	0x0C	0x01	1:0	DAC1FSC[9:8]	0x03FF=设置满度输出电流为最大值 31.66mA。/ 0x03FF = set full-scale output current to the maximum, 31.66mA. 0x01F9=设置满度输出电流为名义值 20mA。/ 0x01F9 = set full-scale output current to the nominal value, 20mA. 0x0000=设置满度输出电流为最小值 8.64mA。/ 0x0000 = set full-scale output current to the minimum, 8.64mA.
辅助 DAC1 / Auxiliary DAC1	0x0D	0x00	7:0	AUXDAC1[7:0]	辅助 DAC1 输出电流 10 位调节码字。/ Auxiliary DAC1 output current 10-bit adjustment code. （与 0x0E 合并 / combined with 0x0E）
辅助 DAC1 / Auxiliary DAC1	0x0E	0x00	1:0	AUXDAC1[9:8]	0x03FF=设置输出电流为 2.0mA。/ 0x03FF = set output current to 2.0mA. 0x0200=设置输出电流为 1.0mA。/ 0x0200 = set output current to 1.0mA. 0x0000=设置输出电流为 0.0mA。/ 0x0000 = set output current to 0.0mA.
辅助 DAC1 / Auxiliary DAC1	0x0E	0x00	7	AUX1PIN	1=AUX1P 引脚有效。/ 1 = AUX1P pin active. 0=AUX1N 引脚有效。/ 0 = AUX1N pin active.
辅助 DAC1 / Auxiliary DAC1	0x0E	0x00	6	AUX1DIR	0=配置辅助 DAC1 为电流源。/ 0 = Configure auxiliary DAC1 as a current source. 1=配置辅助 DAC1 为电流沉。/ 1 = Configure auxiliary DAC1 as a current sink.
DAC2 增益 / DAC2 gain	0x0F	0xF9	7:0	DAC2FSC[7:0]	DAC2 满度输出电流 10 位调节码字。/ DAC2 full-scale output current 10-bit adjustment code. （与 0x10 合并 / combined with 0x10）
DAC2 增益 / DAC2 gain	0x10	0x01	1:0	DAC2FSC[9:8]	0x03FF=设置满度输出电流为最大值 31.66mA。/ 0x03FF = set full-scale output current to the maximum, 31.66mA. 0x01F9=设置满度输出电流为名义值 20mA。/ 0x01F9 = set full-scale output current to the nominal value, 20mA. 0x0000=设置满度输出电流为最小值 8.64mA。。/ 0x0000 = set full-scale output current to the minimum, 8.64mA..
辅助 DAC2 / Auxiliary DAC2	0x11	0x00	7:0	AUXDAC2[7:0]	辅助 DAC2 输出电流 10 位调节码字。/ Auxiliary DAC2 output current 10-bit adjustment code. （与 0x12 合并 / combined with 0x12）
辅助 DAC2 / Auxiliary DAC2	0x12	0x00	1:0	AUXDAC2[9:8]	0x03FF=设置输出电流为 2.0mA。/ 0x03FF = set output current to 2.0mA. 0x0200=设置输出电流为 1.0mA。/ 0x0200 = set output current to 1.0mA. 0x0000=设置输出电流为 0.0mA。/ 0x0000 = set output current to 0.0mA.
辅助 DAC2 / Auxiliary DAC2	0x12	0x00	7	AUX2PIN	1=AUX2P 引脚有效。/ 1 = AUX2P pin active. 0=AUX2N 引脚有效。/ 0 = AUX2N pin active.
辅助 DAC2 / Auxiliary DAC2	0x12	0x00	6	AUX2DIR	0=配置辅助 DAC2 为电流源。/ 0 = Configure auxiliary DAC2 as a current source. 1=配置辅助 DAC2 为电流沉。/ 1 = Configure auxiliary DAC2 as a current sink.

电源地间保护 / Power-to-Ground Protection

English: None.

中文： 无。

注意事项 / Precautions

1、产品安装注意事项 / 1. Product Installation Precautions

English: 1) Pay attention to device orientation during soldering to avoid soldering it in the wrong orientation. 2) Instruments and meters used for debugging the circuit must share a good common ground. PCB design must maintain good grounding and power-supply decoupling. 3) Take care not to reverse the power supply or short the input/output pins to the power supply, which can easily damage the circuit.

中文： 1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2、产品使用注意事项 / 2. Product Usage Precautions

English: 1) It is recommended to reset the circuit first after power-up before use. 2) Pay attention to the ambient temperature in actual use, and ensure heat dissipation. 3) For the supply voltage range, refer to the Recommended Operating Conditions section. 4) Do not use the product beyond its maximum limit conditions, otherwise irreversible damage to the circuit will result. 5) The heat sink (exposed pad) is analog ground; the DNC pins are recommended to be left floating. 6) Use a multilayer PCB with independent power and ground planes. Route high-frequency signal lines directly over the ground plane. On the board, keep digital signal lines as far as possible from sensitive analog input lines, analog output lines, reference input lines, common-mode input lines, and clock input lines, as the actual layout permits. Use symmetrical routing for analog output lines and clock input lines as far as possible to reduce the influence of second-harmonic distortion and thereby improve the dynamic performance of the DAC. Use digital signal lines that are as short as possible and length-matched to reduce transmission delay and the effects of mismatch caused by signal skew. 7) The product requires 4 independent supply inputs: analog supply input (AVDD33), clock supply input (CVDD18), 3.3V digital supply input (DVDD33), and 1.8V digital supply input (DVDD18). Each supply terminal requires a 0.1μF and a 10μF decoupling capacitor placed close by to its corresponding ground plane, followed by a ferrite-bead connection to reduce power-supply noise coupling; all supplies must be decoupled with a tantalum or electrolytic capacitor at the point where they enter the PCB. The inductance of the ferrite bead and the decoupling capacitors can form a π-type filter network to further improve supply performance. 8) The grounding and power-supply decoupling methods seriously affect the product's performance. Unwanted digital signals affect the dynamic performance of the D/A converter through coupling at the input, reference, supply, and ground terminals. In high-speed, high-frequency signal applications, the requirements for proper grounding and power-supply decoupling are very strict. These techniques can reduce the effects of EMI and internal coupling on the product, thereby achieving better dynamic performance. 9) Reference voltage filtering: for accurate conversion, the reference voltage input must be bypassed with a capacitor; the capacitor must be close to the device and the lead resistance minimized.

中文： 1) 推荐上电后首先对电路进行复位，再进行使用。 2) 建议实际使用时关注环境温度，并注意散热。 3) 供电电压范围参考推荐工作条件部分。 4) 不能超过产品最大限定条件使，否者将会对电路造成不可逆的损坏。 5) 热沉为模拟地，DNC 引脚建议悬空。 6) 采用多层布线的 PCB 板，采用独立的电源层和地层。将高频信号线直接布在地层之上。在板上根据实际情况尽量将数字信号线远离敏感的模拟输入线、模拟输出线、基准输入线、共模输入线以及时钟输入线。模拟输出线和时钟输入线尽量采用对称设计来减小二次谐波失真的影响，从而提高 DAC 的动态性能。对数字信号线采用尽可能短以及等长匹配的设计来来减小传输延迟以及由于信号歪斜导致的不匹配带来的影响。 7) 产品需要 4 组独立的电源输入。分别为模拟电源输入（AVDD33），时钟电源输入（CVDD18），3.3V 数字电源输入（DVDD33）和 1.8V 数字电源输入（DVDD18）。对每一组电源端都需要就近接一个 0.1μF 和 10μF 的去耦电容到各自对应的地平面，然后，用磁珠连接来减少电源噪声耦合的影响，对所有电源都要在接入 PCB 板的那一点用钽电容或电解电容来去耦。磁珠的电感和去耦电容可以形成一个 π 型滤波网络进一步提高电源性能。 8) 接地和电源去耦的方式会严重的影响产品的性能。不想要的数字信号会通过输入、基准、电源和接地端的耦合来影响 D/A 转换器的动态性能。高速、高频信号应用中对适当接地和电源去耦的要求非常严格。这些技术可以减小 EMI 和内部耦合对产品的影响，从而获得更好的动态性能。 9) 基准电压滤波：为了精确转换，基准电压输入处必须用电容旁路，电容必须靠近器件并尽量减少引线电阻。

3、产品防护注意事项 / 3. Product Protection Precautions

English: 1) Temperature and humidity and environmental requirements for finished-product warehouse storage: temperature 10°C～25°C, relative humidity 25%～70%; electrostatic discharge sensitivity Class 1B (500~999V). All pins of this circuit have ESD protection structures; however, high-energy electrical pulses can still damage the circuit, so ESD protection should be observed during testing, handling, and storage. 2) Product storage period: counted from the date of the inspection-lot identification code; when warehoused products have been stored for more than 36 months, they shall be moved to the over-age product cabinet, and the products must pass re-inspection before use. 3) It is recommended to use the product within 4 hours after unpacking; if exposed to air for more than 4 hours, high-temperature baking at 150°C for 8h is recommended, followed by vacuum packaging and storage in a dry cabinet. 4) Avoid dropping the product during use, to prevent mechanical stress damage. 5) Exceeding the absolute maximum ratings may cause permanent damage to the device. The maximum ratings do not imply that the device can operate normally under these conditions or under any other conditions beyond those shown in this product manual. Long-term operation at the absolute maximum ratings will affect device reliability. 6) Plastic-packaged circuits readily absorb moisture, causing delamination; keep the surrounding environment dry during use, and store vacuum-packed at room temperature in a dry environment.

中文： 1) 成品库贮存的温湿度和环境要求：温度 10°C～25°C，相对湿度 25%～70%、静电放电敏感度 1B 等级（500~999V）。该电路所有引出端均有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 2) 产品贮存期:从检验批识别代码日期算起，入库产品贮存期超过 36 个月时产品应归入超期产品专柜存放，产品须复检合格后方能使用。 3) 建议拆封后 4 小时内使用，如在空气中暴露超过 4 小时，建议进行 150°C，8h 的高温烘焙后抽真空包装，放置于干燥柜中存放。 4) 在使用过程中应避免跌落以免造成机械应力损伤。 5) 超出绝对最大额定值可能会导致器件永久性损坏。额定最大值不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。长期在绝对最大额定值条件下工作会影响器件的可靠性。 6) 塑封电路易吸潮导致分层，使用时应注意保持周围环境干燥，存储时应真空包装储存于常温、干燥环境下。

4、电装说明 / 4. Assembly Instructions

English: 1) The moisture sensitivity level of this product is MSL3. The allowable exposure time to the external environment from removal from the moisture-proof bag, dry storage, or baking until reflow soldering is: ≤30°C/60RH%, 168h. 2) If device storage conditions cannot be controlled or traced, bake strictly at 125°C for 8h before assembly. 3) If the assembly environment temperature/humidity cannot be guaranteed at ≤30°C/60RH%, complete soldering within 12h after baking. 4) After baking, the product readily generates static electricity; observe ESD protection in all operations. 5) For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C~235°C; the maximum peak temperature should not exceed 235°C; time within ±5°C of the peak temperature ≤20s; time above liquidus 60~90s; ramp-up rate 2~4°C/s; ramp-down rate 2°C/s ~6°C/s. 6) For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C~245°C; the maximum peak temperature should not exceed 260°C; time within ±5°C of the peak temperature ≤20s; time above liquidus 60~90s; ramp-up rate 2~4°C/s; ramp-down rate 2°C/s ~6°C/s. 7) If a mixed assembly process requires elevated temperature, ensure the device body temperature does not exceed 260°C at its maximum. (The device body temperature measurement point is at the top surface of the device during reflow soldering.) 8) The solder terminal surface finish of this product is nickel-palladium-gold, with gold content less than 3%; no gold embrittlement will occur, and tinning is not required. 9) If forced tinning is required, perform tinning in accordance with the national aerospace industry standard QJ3267, Technical Requirements for Tinning of Electronic Components. Note that the device must be dried before tinning; the tinning set temperature must not exceed 300°C; the heating time per side of the four pin sides must be less than 5s; the heat-sink surface heating time must be less than 30s; and tinning must be performed no more than 1 time.

中文： 1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h。 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤。 3) 若电装环境温湿度无法保证≤30°C/60RH%，请在烘烤后 12h 内完成焊接。 4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护。 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s。升温速率 2~4°C/s，降温速率 2°C/s ~6°C/s。 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s。升温速率 2~4°C/s，降温速率 2°C/s ~6°C/s。 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C。（器件本体温度测量点位于回流焊时器件上表面）。 8) 本产品焊接端表面处理方式为镍钯金，但含量小于 3%，不会出现金脆现象，不需要搪锡。 9) 若有强制搪锡需求，按《国家航天行业标准 QJ3267 电子元器件搪锡工艺技术要求》标准进行搪锡。应注意搪锡前器件需烘干，搪锡设置温度不超过 300°C，四边引脚每边受热时间小于 5s，热沉表面受热时间小于 30s，搪锡次数不超过 1 次。

5、热阻 / 5. Thermal Resistance

表7 封装热阻 / Table 7. Package Thermal Resistance

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)	20.55 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2, natural-convection thermal test environmental requirements and test method for integrated circuits

项目 / Item	实测值 / Measured Value	依据标准及方法 / Standard and Method
Rthjt(结到器件顶面的热阻) / Rthjt (junction-to-package-top thermal resistance)	2.811 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14, two-interface separation method for one-dimensional heat-transfer paths
Rthj-bottom（结到器件底面的热阻） / Rthj-bottom (junction-to-package-bottom thermal resistance)	2.657 K/W	JESD51-14 拐点理论器件内部结构分层得到 / JESD51-14, obtained by inflection-point-theory layering of the device internal structure

常见故障及处理办法 / Common Faults and Troubleshooting

English: 1. No output signal: check whether there is a clock input at the clock pins; check that the power and ground signal connections are correct; ensure the input voltage and reference voltage are accurate; 2. Output data jitter: check the external circuit and connections; ensure the reference voltage is stable. 3. Unstable device operation: check the power supply; ensure the supply voltage is stable.

中文： 1、 无输出信号：检查时钟引出端是否有时钟输入，检查电源、地信号连接是否正常，保证输入电压、基准电压准确； 2、 输出数据抖动：检查外部电路和连接，保证基准电压稳定。 3、 器件工作不稳定：检查电源，保证电源电压稳定。

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附加说明 / Additional Notes

English: 1. First release date of this manual: July 2026. 2. Product status: ☑ Production (this model is currently in production; formal products are available) ☐ Pre-release (this model has not yet entered formal production; samples are available) 3. Cross-reference notes vs. the foreign product:

中文： 1. 本说明书首次发布日期：2026 年 7 月。 2. 本产品状态：☑生产 （该产品型号目前已在生产，可以提供正式产品） ☐预发布（该产品型号尚未投入正式生产，可以提供样品） 3. 替代国外产品情况说明：

1）绝对最大额定值对比 / 1) Absolute Maximum Ratings Comparison

附表1 绝对最大额定值对比 / Appendix Table 1. Absolute Maximum Ratings Comparison

参数 / Parameter	SXD034 规范要求 / SXD034 Specification	进口器件 / Imported Device	比对结果 / Comparison Result
CVDD18	-0.3V ~ 1.98V	-0.3V ~ 1.98V	一致 / Consistent
DVDD18	-0.3V ~ 1.98V	-0.3V ~ 1.98V	一致 / Consistent

参数 / Parameter	SXD034 规范要求 / SXD034 Specification	进口器件 / Imported Device	比对结果 / Comparison Result
AVDD33	-0.3V ~ 3.6V	-0.3V ~ 3.6V	一致 / Consistent
DVDD33	-0.3V ~ 3.6V	-0.3V ~ 3.6V	一致 / Consistent
AVSS	-0.3V ~ 0.3V	-0.3V ~ 0.3V	一致 / Consistent
DVSS	-0.3V ~ 0.3V	-0.3V ~ 0.3V	一致 / Consistent
CVSS	-0.3V ~ 0.3V	-0.3V ~ 0.3V	一致 / Consistent
基准输入输出引脚电压 / Reference input/output pin voltage	-0.3V ~ AVDD33+0.3V	-0.3V ~ AVDD33+0.3V	一致 / Consistent
DAC1 电流输出引脚电压 / DAC1 current output pin voltage	-0.3V ~ AVDD33+0.3V	-0.3V ~ AVDD33+0.3V	一致 / Consistent
DAC2 电流输出引脚电压 / DAC2 current output pin voltage	-0.3V ~ AVDD33+0.3V	-0.3V ~ AVDD33+0.3V	一致 / Consistent
辅助 DAC1 电流输出引脚电压 / Auxiliary DAC1 current output pin voltage	-0.3V ~ AVDD33+0.3V	-0.3V ~ AVDD33+0.3V	一致 / Consistent
辅助 DAC2 电流输出引脚电压 / Auxiliary DAC2 current output pin voltage	-0.3V ~ AVDD33+0.3V	-0.3V ~ AVDD33+0.3V	一致 / Consistent
输入数据引脚电压 / Input data pin voltage	-0.3V ~ DVDD33+0.3V	-0.3V ~ DVDD33+0.3V	一致 / Consistent
时钟输入引脚电压 / Clock input pin voltage	-0.3V ~ CVDD18+0.3V	-0.3V ~ CVDD18+0.3V	一致 / Consistent
复位引脚、四线 SPI 引脚电压 / Reset pin and 4-wire SPI pin voltage	-0.3V ~ DVDD33+0.3V	-0.3V ~ DVDD33+0.3V	一致 / Consistent
贮存温度（Tstg）/ Storage temperature (Tstg)	-65°C~150°C	-65°C~150°C	一致 / Consistent
结温（TJ）/ Junction temperature (TJ)	125°C	125°C	一致 / Consistent
引线耐焊接温度（Th）（10s）/ Lead soldering temperature (Th) (10s)	260°C	——	——
热阻(Rth) / Thermal resistance (Rth)	25°C/W	25°C/W	一致 / Consistent

2）推荐工作条件对比 / 2) Recommended Operating Conditions Comparison

附表2 推荐工作条件对比 / Appendix Table 2. Recommended Operating Conditions Comparison

参数 / Parameter	SXD034 规范要求 / SXD034 Specification	进口器件 / Imported Device	比对结果 / Comparison Result
CVDD18	1.70V~1.90V	1.70V~1.90V	一致 / Consistent
DVDD18	1.70V~1.90V	1.7V~1.9V	一致 / Consistent
AVDD33	3.13V~3.47V	3.13V~3.47V	一致 / Consistent
DVDD33	3.13V~3.47V	3.13V~3.47V	一致 / Consistent
工作环境温度（TA）/ Operating ambient temperature (TA)	-40°C～+85°C	-40~85°C	一致 / Consistent

3）性能指标对比 / 3) Performance Specifications Comparison

附表3 主要性能指标对比 / Appendix Table 3. Main Performance Specifications Comparison

Conditions / 条件（除另有规定外 / unless otherwise specified）: AVDD33=DVDD33=3.3V, DVDD18=CVDD18=1.8V, IFS=20mA, -40°C≤TA≤85°C. Columns: 国内产品 / Domestic product (SXD034): 最小 / Min, 典型 / Typ, 最大 / Max; 国外产品 / Foreign product (进口器件 / imported device): 最小 / Min, 典型 / Typ, 最大 / Max.

特性 / Parameter	符号 / Symbol	条件 / Conditions	SXD034 最小 / Min	SXD034 典型 / Typ	SXD034 最大 / Max	进口器件 最小 / Min	进口器件 典型 / Typ	进口器件 最大 / Max	单位 / Unit	对比结果 / Comparison
产品型号 / Model			SXD034			进口器件 / Imported device				一致 / Consistent
分辨率 / Resolution	RES	—		16			16		Bit	一致 / Consistent
微分误差 / Differential nonlinearity error	EDL	—	-6.0	-2.6	6.0	—	±2.0	—	LSB	略大 / Slightly larger
积分误差 / Integral nonlinearity error	EL	—	-9.0	-5.5	9.0	—	±4.0	—	LSB	略大 / Slightly larger
失调误差 / Offset error	EO	—	-0.050	0.0004	0.050	—	±0.001	—	%FSR	小 / Smaller
增益误差 / Gain error	EG	—	-8.0	-1.0	8.0	—	±2.0	—	%FSR	小 / Smaller
增益失配 / Gain mismatch	EGMIS	—	-2.5	-0.06	2.5	—	±2.0	—	%FSR	小 / Smaller
电流输出范围 / Current output range	IFS	—	8.0	—	32.0	8.6	—	31.7	mA	略大 / Slightly larger
输出顺从电压范围 / Output compliance voltage range	VOC	—	-1.0	—	1.0	-1.0	—	1.0	V	一致 / Consistent
辅助 DAC 满度输出电流 / Auxiliary DAC full-scale output current	IFSAUX	—	-2.2	—	2.2	-2.0		2.0	mA	略大 / Slightly larger
辅助 DAC 输出顺从电压范围（电流沉模式） / Auxiliary DAC output compliance voltage range	VOCAUXSI	—	0.8	—	1.6	0.8	—	1.6	V	一致 / Consistent

特性 / Parameter	符号 / Symbol	条件 / Conditions	SXD034 最小 / Min	SXD034 典型 / Typ	SXD034 最大 / Max	进口器件 最小 / Min	进口器件 典型 / Typ	进口器件 最大 / Max	单位 / Unit	对比结果 / Comparison
(current-sink mode)										
辅助 DAC 输出顺从电压范围（电流源模式） / Auxiliary DAC output compliance voltage range (current-source mode)	VOCAUXSO	—	0	—	1.6	0	—	1.6	V	一致 / Consistent
基准输出电压 / Reference output voltage	VREFO	—	1.15	1.20	1.25	—	1.20	—	V	一致 / Consistent
基准外部电压输入范围 / External reference voltage input range	VREFIR	—	1.15	—	1.30	1.15	—	1.30	V	一致 / Consistent
基准输入输出电阻 / Reference input/output resistance	RREF	—	4	5	6	—	5	—	kΩ	一致 / Consistent
3.3V 模拟电源电流 / 3.3V analog supply current	IAVDD33	—	—	56	60	—	56	60	mA	一致 / Consistent
3.3V 数字电源电流 / 3.3V digital supply current	IDVDD33	—	—	13	15	—	12	16	mA	一致 / Consistent
1.8V 模拟电源电流 / 1.8V analog supply current	IAVDD18	—	—	18	22	—	18	22	mA	一致 / Consistent
1.8V 数字电源电流 / 1.8V digital supply current	IDVDD18	—	—	29	36	—	32	36	mA	一致 / Consistent
功耗 / Power consumption	PW	fDAC=250MSPS, fOUT = 20MHz	—	312	365	—	310	355	mW	略大 / Slightly larger
DAC 输出禁能功耗 / DAC output-disabled power	PDACPD	—	—	85	180	—	125	—	mW	小 / Smaller
全芯片休眠功耗 / Full-chip sleep power	PPD	—	—	1.3	10	—	3	—	mW	小 / Smaller
	SFDR		72	86	—	—	82	—	dBc	

特性 / Parameter	符号 / Symbol	条件 / Conditions	SXD034 最小 / Min	SXD034 典型 / Typ	SXD034 最大 / Max	进口器件 最小 / Min	进口器件 典型 / Typ	进口器件 最大 / Max	单位 / Unit	对比结果 / Comparison
无杂散动态范围 / Spurious-free dynamic range		fDAC=250MSPS, fOUT = 20MHz								略大 / Slightly larger
无杂散动态范围 / Spurious-free dynamic range	SFDR	fDAC=250MSPS, fOUT = 180MHz	55	66	—	—	66	—	dBc	一致 / Consistent
互调失真 / Intermodulation distortion	IMD	fDAC=250MSPS, fOUT = 20MHz	76	87	—	—	86	—	dBc	略大 / Slightly larger
串扰 / Crosstalk	XT	fDAC=250MSPS, fOUT = 20MHz	70	94	—	—	80	—	dBc	大 / Larger
输入时钟差分峰峰值电压 / Input clock differential peak-to-peak voltage	VDPPCLK	fDAC=250MSPS, fOUT = 20MHz	400	800	1600	400	800	1600	mV	一致 / Consistent
输入时钟共模电压 / Input clock common-mode voltage	VCMCLK	fDAC=250MSPS, fOUT = 20MHz	300	400	500	300	400	500	mV	一致 / Consistent
采样速率 / Sample rate	fDAC	—	—	—	250	—	—	—	MSPS	—
输入时钟频率 / Input clock frequency	fCLK	—	—	—	250	—	—	250	MHz	一致 / Consistent
SPI 时钟频率 / SPI clock frequency	fSCLK	—	—	—	40	—	—	40	MHz	一致 / Consistent
SPI 时钟脉冲高电平宽度 / SPI clock pulse high width	tPWH	—	10	—	—	10	—	—	ns	一致 / Consistent
SPI 时钟脉冲低电平宽度 / SPI clock pulse low width	tPWL	—	10	—	—	10	—	—	ns	一致 / Consistent

注：SXD034、进口器件典型值均为常温实测值，SXD034 极限值为规范要求，进口器件极限值为数据手册值。/ Note: the typical values of both the SXD034 and the imported device are room-temperature measured values; the SXD034 limit values are specification requirements, and the imported device limit values are datasheet values.

4）其它指标对比 / 4) Other Parameter Comparison

附表4 其它指标对比 / Appendix Table 4. Other Parameter Comparison

参数 / Parameter	SXD034	进口器件 / Imported Device	比对结果 / Comparison Result
封装形式 / Package	QFN72	LFCSP72（QFN72）	一致 / Consistent
质量等级 / Quality grade	企业标准 / Enterprise standard	工业级 / Industrial grade	不一致 / Not consistent
尺寸 / Dimensions	10mm10mm0.85mm	10mm10mm0.85mm	一致 / Consistent
替代建议 / Cross-reference recommendation	□直接替代 / □Direct replacement □有效替代 / □Effective alternative □功能替代 / □Functional alternative		

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