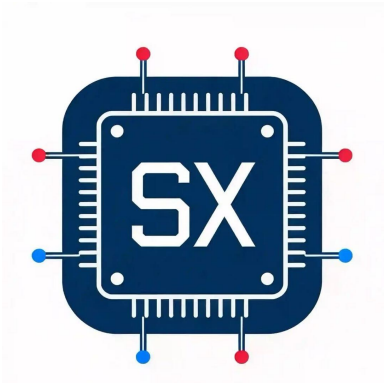


SXD052

Dual-Channel 16-Bit, 11 GSPS RF D/A Converter

双通道 16 位 11GSPS RF D/A 转换器

16-bit | 2 channels | 11 GSPS | BGA144 | JESD204B

16位 | 双通道 | 11GSPS | BGA144 | JESD204B

对标 / Cross Reference: AD9174 — pin-to-pin compatible alternative

Product Datasheet / 产品数据手册

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SXD052 Dual-Channel 16-Bit 11GSPS RF D/A Converter — Product Manual (Bilingual)

SXD052 型双通道 16 位 11GSPS RF D/A 转换器产品说明书、使用手册（中英对照）

Shenzhen Shenxin Technology Co., Ltd. / 深信科技 **V1.20260730**

对标 / Cross Reference: AD9174 — pin-to-pin compatible alternative

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版本修订记录 / Revision History

版本号 / Version	发布日期 / Release Date	更改章节 / Changed Section	更改说明 / Change Description	备注 / Remarks
V1.20260730	20260730	——	首次发布 / Initial release	

产品用途及应用范围 / Applications and Scope

English: Wireless communications infrastructure; multiband base-station radios; microwave / E-band backhaul systems; instrumentation and automated test equipment (ATE).

中文： 无线通信基础设施；多频段基站无线电；微波/E 频段回程系统；仪器仪表、自动测试设备（ATE）。

标准 / Standards

English: Detailed specification and approval number: Q/GC 0238-2026 — Detailed Specification for Semiconductor Integrated Circuit SXD052 Dual-Channel 16-Bit 11GSPS RF D/A Converter. Quality grade: enterprise standard.

中文： 详细规范及确认号：Q/GC 0238-2026 《半导体集成电路 SXD052 型双通道 16 位 11GSPS RF D/A 转换器详细规范》；质量等级：企标。

产品特点 / Features

English: - Supply voltages include: 0.975V and 1.8V - Resolution: 16bit - Conversion rate: 11000MSPS - SFDR: typical 74dBc @ fin = 100MHz; typical 60dBc @ fin = 3700MHz - IMD3: typical 74dBc @ fin = 1840MHz; typical 76dBc @ fin = 3700MHz - Power consumption: typical 2W @ dual-link mode, Mode 1 (L=2, M=4, NP=16, N=16), fDAC=11000MSPS, fout=2000MHz - Flexible 8-lane, 15.4Gbps JESD204B interface, supporting multichip synchronization — Subclass 1 - Analog output range: 14.4mA~24mA - ESD rating: Class 1B, HBM model: 500V - Circuit interface: JESD204B - Product weight: 0.622g±0.09g - Supports single-band and multiband applications - Selectable interpolation filters - 1×, 2×, 3×, 4×, 6× and 8× configurable channel datapath interpolation - 1×, 2×, 4×, 6×, 8× and 12× configurable main datapath interpolation - Integrated high-performance, low-noise PLL clock multiplier - Package: BGA144

中文： - 电源电压包括：0.975V 和 1.8V - 分辨率：16bit - 转换速率：11000MSPS - SFDR：典型 74dBc @ fin = 100MHz；典型 60dBc @ fin = 3700MHz - IMD3：典型 74dBc @ fin = 1840MHz；典型 76dBc @ fin = 3700MHz - 功耗：典型 2W @双链路模式，模式 1（L=2，M=4，NP=16, N=16），fDAC=11000MSPS，fout=2000MHz - 灵活的 8 线，15.4Gbps JESD204B 接口，支持多芯片同步-Subclass 1 - 模拟输出范围：14.4mA~24mA - ESD 等级：1B 级，HBM 模型：500V - 电路接口：JESD204B - 产品重量：0.622g±0.09g - 支持单频段和多频段应用 -

可选择内插滤波器 - 1×、2×、3×、4×、6×和 8×可配置通道数据路径插值 - 1×、2×、4×、6×、8×和 12×可配置主通道数据路径插值 - 集成高性能、低噪声 PLL 时钟倍频器 - 封装形式：BGA144

产品描述 / Product Description

English: The SXD052 dual-channel 16-bit 11GSPS RF-DAC is a high-speed, high-precision digital-to-analog converter, a monolithic integrated circuit fabricated in a CMOS process, applicable to communications, instrumentation and other fields. It also has DDS functionality, with a maximum conversion rate of up to 12GSPS. Each RF-DAC has three bypassable complex datapaths and a main datapath. With an 8-lane JESD204B serial input data interface, a high-performance on-chip PLL clock multiplier and digital signal processing functions, it is suitable for single-band and multiband direct-to-RF wireless applications.

To accommodate different input signal bandwidth requirements, the sub-channel datapath offers selectable 1x, 2x, 3x, 4x, 6x and 8x configurable data-channel interpolation, and the main datapath offers selectable 1x, 2x, 4x, 6x, 8x and 12x configurable data-channel interpolation. An integrated NCO enables DDS functionality or complex modulation of the input signal. In ultra-wide data-rate mode, the channelizer and main datapath are bypassed and the device operates as a single-channel 16-bit DAC providing data rates up to 6.16GSPS. The full-scale output current of the circuit is adjustable. The operating mode, interpolation factor and other configuration of the circuit can all be set via SPI. An on-chip transmit-enable function is also integrated, enabling additional power saving and downstream circuit protection.

The functional block diagram of this product is shown in Figure 1.

中文： SXD052 型双通道 16 位 11GSPS RF-DAC 是一款高速高精度数模转换器，采用 CMOS 工艺制造的单片集成电路，可应用于通信、仪器等领域。同时具有 DDS 功能，最高转换率可达到 12GSPS。每个 RF-DAC 具有 3 个可旁路复数数据路径和主数据路径。采用 8 线 JESD204B 串行线输入数据接口、高性能片内 PLL 时钟倍频器和数字信号处理功能，适合单频段和多频段直接至射频（RF）无线应用。

为适应不同输入信号带宽的需求，子通道数据路径可选择 1x、2x、3x、4x、6x 和 8x 可配置数据通道插值，主数据路径可选择 1x、2x、4x、6x、8x 和 12x 可配置数据通道插值。集成了 NCO，可实现 DDS 功能或对输入信号进行复调制。在超宽数据速率模式，旁路通道选择器和主数据路径，作为单通道 16 位 DAC 提供高达 6.16GSPS 的数据速率。电路满幅输出电流可调节。电路的工作模式，内插倍数等配置都可通过 SPI 进行设置。同时片上集成发送使能功能，可实现额外省电和下游电路保护。

该产品功能框图如图 1 所示。

该产品功能框图如图 1 所示。

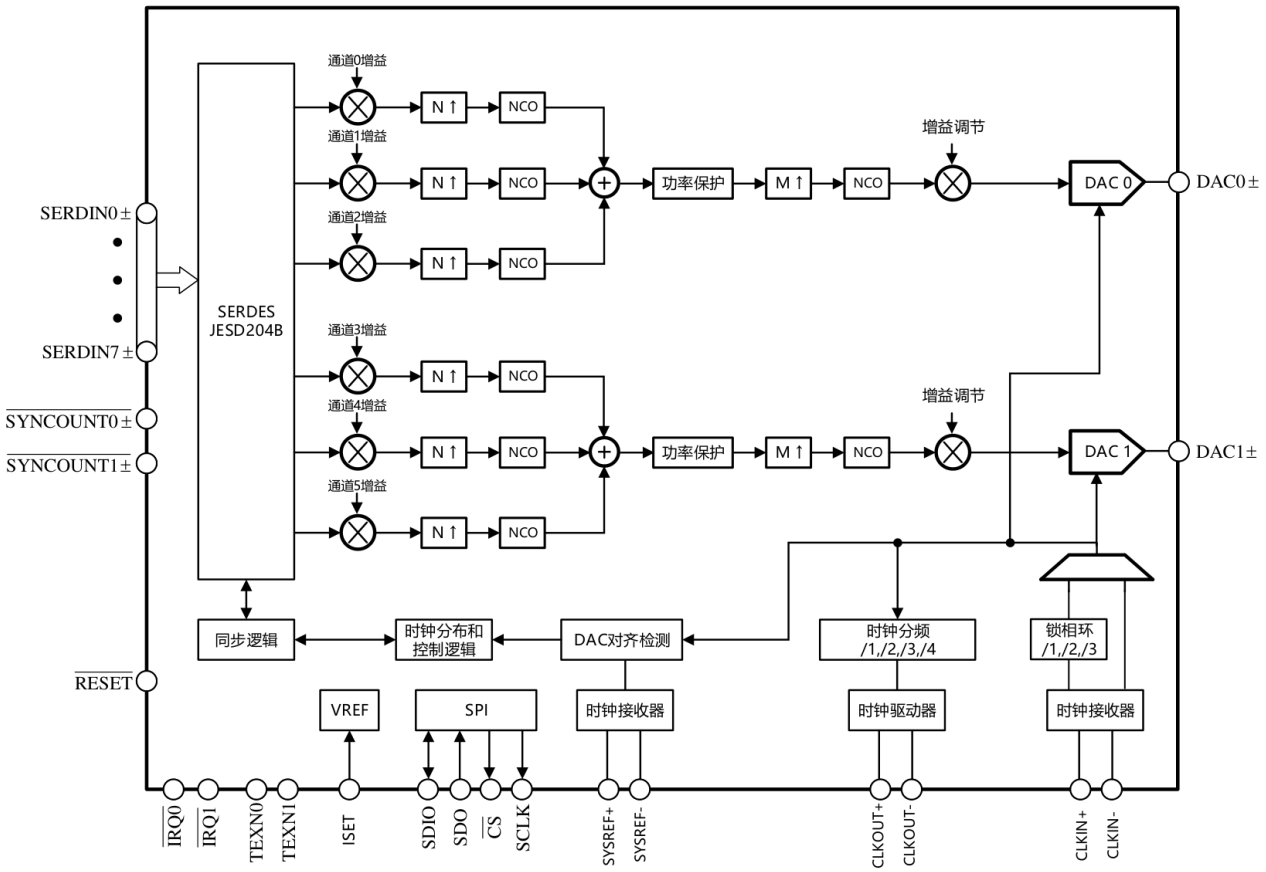


Figure 1: Functional block diagram

产品外形图 / Package Outline

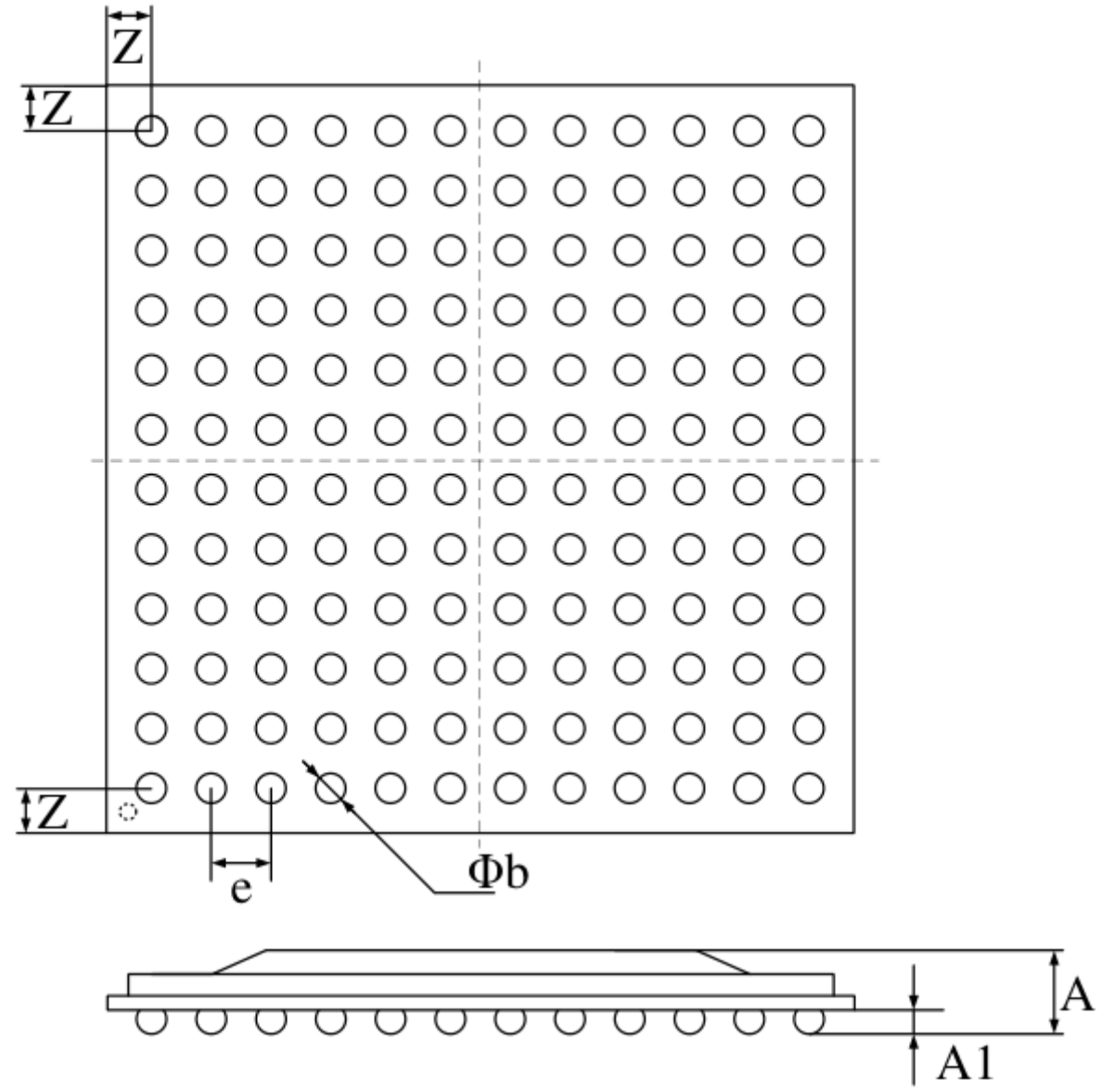

Z
Z
Z
e
Φb
A
A1
D
E

Figure 2: Package outline dimensions

单位为毫米 / Units in mm

尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max	尺寸符号 / Dimension	数值 / Value — 最小 / Min	数值 / Value — 公称 / Nom	数值 / Value — 最大 / Max
A	1.66	1.87	2.08	E	9.80	10.0 [a]	10.20
A1	0.30	0.35 [a]	0.40	Φb	0.40	0.45 [a]	0.50
D	9.80	10.00 [a]	10.20	e	—	0.80 [a]	—
Z	—	0.60 [a]	0.90				

[a] 外壳实际公称值，推荐用户参考该尺寸设计使用；/ Actual nominal package values; users are advised to design with reference to these dimensions.

注：推荐焊盘设计详见电装说明。/ Note: see the assembly instructions for recommended pad layout.

引出端排列（俯视图）/ Pin Arrangement (Top View)

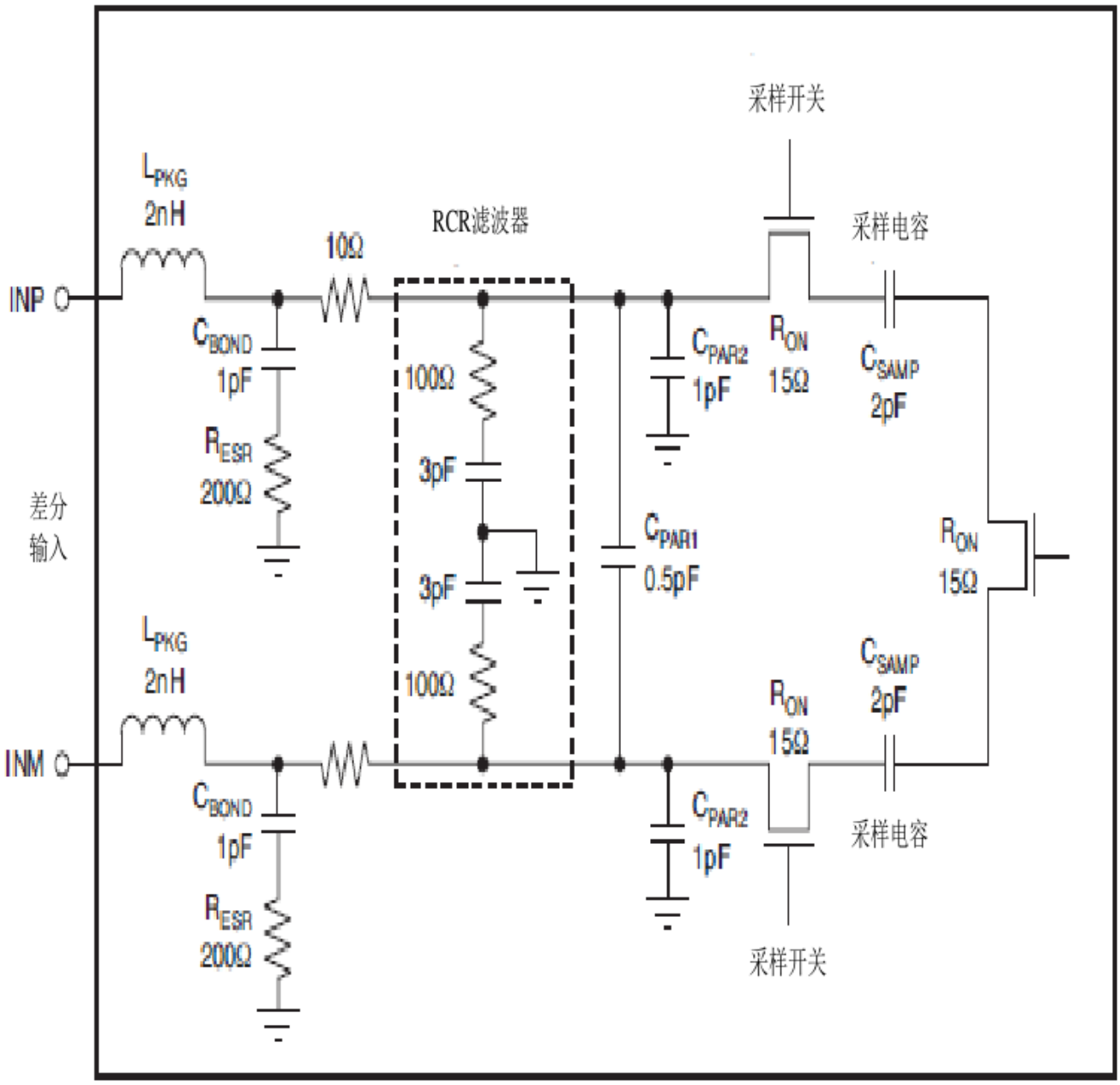


Figure 3: Pin arrangement (top view)

引出端功能符号表 / Pin Function Table

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
A1	GND	地 / Ground	/	G1	GND	地 / Ground	/
A2	SERDIN7+	SERDES Lane7 输入正端 / SERDES Lane 7 input, positive	I	G2	GND	地 / Ground	/

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
A3	SERDIN6+	SERDES Lane6 输入正端 / SERDES Lane 6 input, positive	I	G3	GND	地 / Ground	/
A4	SERDIN5+	SERDES Lane5 输入正端 / SERDES Lane 5 input, positive	I	G4	GND	地 / Ground	/
A5	SERDIN4+	SERDES Lane4 输入正端 / SERDES Lane 4 input, positive	I	G5	GND	地 / Ground	/
A6	GND	地 / Ground	/	G6	GND	地 / Ground	/
A7	GND	地 / Ground	/	G7	GND	地 / Ground	/
A8	SERDIN3+	SERDES Lane3 输入正端 / SERDES Lane 3 input, positive	I	G8	GND	地 / Ground	/
A9	SERDIN2+	SERDES Lane2 输入正端 / SERDES Lane 2 input, positive	I	G9	GND	地 / Ground	/
A10	SERDIN1+	SERDES Lane1 输入正端 / SERDES Lane 1 input, positive	I	G10	GND	地 / Ground	/
A11	SERDIN0+	SERDES Lane0 输入正端 / SERDES Lane 0 input, positive	I	G11	GND	地 / Ground	/
A12	GND	地 / Ground	/	G12	GND	地 / Ground	/
B1	GND	地 / Ground	/	H1	SYSREF+	系统参考时钟正端 / System reference clock, positive	I
B2	SERDIN7–	SERDES Lane7 输入负端 / SERDES Lane 7 input, negative	I	H2	SYSREF–	系统参考时钟负端 / System reference clock, negative	I
B3	SERDIN6–	SERDES Lane6 输入负端 / SERDES Lane 6 input, negative	I	H3	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
B4	SERDIN5–	SERDES Lane5 输入负端 / SERDES Lane 5 input, negative	I	H4	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
B5	SERDIN4–	SERDES Lane4 输入负端 / SERDES Lane 4 input, negative	I	H5	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
B6	GND	地 / Ground	/	H6	FILT_FINE	片上 DAC_PLL 精细环路滤波器输入 / On-chip DAC PLL fine loop-filter input	I/O
B7	GND	地 / Ground	/	H7	FILT_COARSE	片上 DAC_PLL 粗略环路滤波器输入 / On-chip DAC PLL coarse loop-filter input	I/O

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
B8	SERDIN3–	SERDES Lane3 输入负端 / SERDES Lane 3 input, negative	I	H8	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
B9	SERDIN2–	SERDES Lane2 输入负端 / SERDES Lane 2 input, negative	I	H9	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
B10	SERDIN1–	SERDES Lane1 输入负端 / SERDES Lane 1 input, negative	I	H10	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
B11	SERDIN0–	SERDES Lane0 输入负端 / SERDES Lane 0 input, negative	I	H11	GND	地 / Ground	/
B12	GND	地 / Ground	/	H12	CLKIN–	时钟输入负端 / Clock input, negative	I
C1	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	J1	GND	地 / Ground	/
C2	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	J2	DNC	悬空[a] / Do not connect[a]	/
C3	GND	地 / Ground	/	J3	GND	地 / Ground	/
C4	GND	地 / Ground	/	J4	GND	地 / Ground	/
C5	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	J5	GND	地 / Ground	/
C6	DVDD1.8	1.8V 数字和 I/O 电源 / 1.8V digital and I/O supply	/	J6	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
C7	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	J7	FILT_BYP	片上 DAC_PLL 的 LDO 旁路脚 / On-chip DAC PLL LDO bypass pin	I/O
C8	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	J8	GND	地 / Ground	/
C9	GND	地 / Ground	/	J9	GND	地 / Ground	/
C10	GND	地 / Ground	/	J10	GND	地 / Ground	/
C11	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	J11	GND	地 / Ground	/
C12	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	J12	CLKIN+	时钟输入正端 / Clock input, positive	I
D1	SYNCOUT1+	同步输出信号 1 正端 / Sync output signal 1, positive	O	K1	CLKOUT+	时钟输出正端 / Clock output, positive	O
D2	SYNCOUT1-	同步输出信号 1 负端 / Sync output signal 1, negative	O	K2	GND	地 / Ground	/
D3	DVDD1.8	1.8V 数字和 I/O 电源 / 1.8V digital and I/O supply	/	K3	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
D4	TXEN1	DAC1 的传输使能 / DAC1 transmit enable	I	K4	DNC	悬空[a] / Do not connect[a]	/

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
D5	GND	地 / Ground	/	K5	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
D6	SVDD1.0	1.0V SERDES 电源 / 1.0V SERDES supply	/	K6	FILT_VCM	片上 DAC_PLL 的 VCO 共模输入 / On-chip DAC PLL VCO common-mode input	I/O
D7	GND	地 / Ground	/	K7	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
D8	TXEN0	DAC0 的传输使能 / DAC0 transmit enable	I	K8	GND	地 / Ground	/
D9	IRQ0	中断请求 0 / Interrupt request 0	O	K9	GND	地 / Ground	/
D10	DVDD1.8	1.8V 数字和 I/O 电源 / 1.8V digital and I/O supply	/	K10	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
D11	SYNCOUT0-	同步输出信号 0 负端 / Sync output signal 0, negative	O	K11	GND	地 / Ground	/
D12	SYNCOUT0+	同步输出信号 0 正端 / Sync output signal 0, positive	O	K12	GND	地 / Ground	/
E1	DNC	悬空[a] / Do not connect[a]	/	L1	CLKOUT-	时钟输出负端 / Clock output, negative	O
E2	DNC	悬空[a] / Do not connect[a]	/	L2	GND	地 / Ground	/
E3	DVDD1.8	1.8V 数字和 I/O 电源 / 1.8V digital and I/O supply	/	L3	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
E4	SDO	SPI 数据输出端 / SPI data output	O	L4	GND	地 / Ground	/
E5	SCLK	SPI 时钟 / SPI clock	I	L5	GND	地 / Ground	/
E6	CS	SPI 片选信号 / SPI chip select	I	L6	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
E7	SDIO	SPI 数据输入/输出端 / SPI data input/output	I/O	L7	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
E8	RESET	复位端 / Reset	I	L8	GND	地 / Ground	/
E9	IRQ1	中断请求 1 / Interrupt request 1	O	L9	GND	地 / Ground	/
E10	DVDD1.8	1.8V 数字和 I/O 电源 / 1.8V digital and I/O supply	/	L10	AVDD1.8	1.8V 模拟电源 / 1.8V analog supply	/
E11	DNC	悬空[a] / Do not connect[a]	/	L11	GND	地 / Ground	/
E12	DNC	悬空[a] / Do not connect[a]	/	L12	ISET	基准电流产生端 / Reference-current setting pin	O
F1	GND	地 / Ground	/	M1	GND	地 / Ground	/
F2	GND	地 / Ground	/	M2	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
F3	GND	地 / Ground	/	M3	GND	地 / Ground	/
F4	DAVDD1.0	1.0V 数字到模拟电源 / 1.0V digital-to-analog supply	/	M4	DAC1+	DAC1 电流输出正端 / DAC1 current output, positive	O

引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O	引出端号 / Pin No.	符号 / Symbol	名称 / Name	I/O
F5	DVDD1.0	1.0V 数字电源 / 1.0V digital supply	/	M5	DAC1–	DAC1 电流输出负端 / DAC1 current output, negative	O
F6	DVDD1.0	1.0V 数字电源 / 1.0V digital supply	/	M6	GND	地 / Ground	/
F7	DVDD1.0	1.0V 数字电源 / 1.0V digital supply	/	M7	GND	地 / Ground	/
F8	DVDD1.0	1.0V 数字电源 / 1.0V digital supply	/	M8	DAC0-	DAC0 电流输出负端 / DAC0 current output, negative	O
F9	DAVDD1.0	1.0V 数字到模拟电源 / 1.0V digital-to-analog supply	/	M9	DAC0+	DAC0 电流输出正端 / DAC0 current output, positive	O
F10	GND	地 / Ground	/	M10	GND	地 / Ground	/
F11	GND	地 / Ground	/	M11	AVDD1.0	1.0V 模拟和时钟电源 / 1.0V analog and clock supply	/
F12	GND	地 / Ground	/	M12	GND	地 / Ground	/

[a] 使用时悬空，不要连接此脚。/ Leave floating in use; do not connect this pin.

推荐工作条件 / Recommended Operating Conditions

English: - 1.8V analog supply (VAVDD1.8): 1.71V ~ 1.89V - 1.0V analog and clock supply (VAVDD1.0): 0.95V ~ 1.00V - 1.0V digital supply (VDVDD1.0): 0.95V ~ 1.00V - 1.0V digital-to-analog supply (VDAVDD1.0): 0.95V ~ 1.00V - 1.0V SERDES supply (VSVDD1.0): 0.95V ~ 1.00V - 1.8V digital and I/O supply (VDVDD1.8): 1.71V ~ 1.89V - Operating ambient temperature (TC): -40°C ~ 85°C

Note: this product has high power consumption; pay attention to the ambient temperature in actual use and take care with heat dissipation.

中文： - 1.8V 模拟电源（VAVDD1.8）： 1.71 V～1.89 V - 1.0V 模拟和时钟电源（VAVDD1.0）： 0.95V～1.00 V - 1.0V 数字电源（VDVDD1.0）： 0.95V～1.00 V - 1.0V 数字到模拟的电源（VDAVDD1.0）： 0.95V～1.00 V - 1.0V SERDES 电源（VSVDD1.0）： 0.95V～1.00 V - 1.8V 数字和 I/O 电源（VDVDD1.8）： 1.71 V～1.89V - 工作环境温度（TC）： -40°C~85°C

注：本产品功耗较高，建议实际使用时关注环境温度，并注意散热。

绝对最大额定值 / Absolute Maximum Ratings

English: - 1.8V analog supply (VAVDD1.8): -0.3V ~ +2.2V - 1.0V analog and clock supply (VAVDD1.0): -0.2V ~ +1.02V - 1.0V digital supply (VDVDD1.0): -0.2V ~ +1.02V - 1.0V digital-to-analog supply (VDAVDD1.0): -0.2V ~ +1.02V - 1.0V SERDES supply (VSVDD1.0): -0.2V ~ +1.02V - 1.8V digital and I/O supply (VDVDD1.8): -0.3V ~ +2.2V - Storage temperature (Tstg): -65°C ~ 150°C - Lead soldering temperature (Th) (10s): 260°C

中文： - 1.8V 模拟电源（VAVDD1.8）： -0.3 V～+2.2 V - 1.0V 模拟和时钟电源（VAVDD1.0）： -0.2 V～+1.02V - 1.0V 数字电源（VDVDD1.0）： -0.2 V～+1.02V - 1.0V 数字到模拟的电源（VDAVDD1.0）： -0.2 V～+1.02V - 1.0V

SERDES 电源（VSVDD1.0）： -0.2 V～+1.02V - 1.8V 数字和 I/O 电源（VDVDD1.8）： -0.3 V～+2.2V - 贮存温度（Tstg）： -65°C~150°C - 引线耐焊接温度（Th）（10s）： 260°C

性能指标 / Performance Specifications

Conditions / 条件（除另有规定外 / unless otherwise specified）: VAVDD1.0 = 0.975V, VAVDD1.8 = 1.8V, VDVDD1.0 = VDAVDD1.0 = 0.975V, VDVDD1.8 = 1.8V, VSVDD1.0 = 0.975V, GND = 0V, -40°C ⩽ TC ⩽ 85°C.

参数 / Parameter	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
分辨率 / Resolution	RES			16		bits
微分非线性误差 / Differential nonlinearity error	DNL		-18	-13/6	18	LSB
积分非线性误差 / Integral nonlinearity error	INL		-30	-15/12	23	LSB
增益误差 / Gain error	EG		-20	-7.3	20	%
最小满量程输出电流 / Minimum full-scale output current	IFSMIN	RSET=5kΩ	13	14.4	18	mA
最大满量程输出电流 / Maximum full-scale output current	IFSMAX	RSET=5kΩ	20	24.0	29	mA
DAC 输出差分阻抗 [a] / DAC output differential impedance [a]	ZDIFF_DAC	TC=25°C	80	106	120	Ω
最小时钟输入功率 [a] / Minimum clock input power [a]	PCLKIMIN		3	—	—	dBm
最大时钟输入功率 [a] / Maximum clock input power [a]	PCLKIMAX	器件上差分电阻 Rload=100Ω, TC=25°C / Differential resistor on device Rload=100Ω, TC=25°C	—	—	9	dBm
时钟输入差分阻抗 [a] / Clock input differential impedance [a]	ZDIFF_CLKI	TC=25°C	80	106	120	Ω
时钟输入共模电压 / Clock input common-mode voltage	VCM_CLKI	交流耦合 / AC-coupled	0.4	0.477	0.6	V
时钟输出差分阻抗 [a] / Clock output differential impedance [a]	ZDIFF_CLKO	TC=25°C	70	86	110	Ω
时钟输出共模电压 / Clock output	VCM_CLKO	交流耦合 / AC-coupled	0.4	0.492	0.6	V

参数 / Parameter	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
common-mode voltage						
内部基准电压 / Internal reference voltage	VREFO		0.4	0.501	0.6	V
AVDD1.0 电源电流 / AVDD1.0 supply current	IAVDD1.0		—	625	1100	mA
AVDD1.8 电源电流 / AVDD1.8 supply current	IAVDD1.8		—	78	140	mA
DVDD1.0 电源电流[b] / DVDD1.0 supply current[b]	IDVDD1.0	双链路模式，模式 1（L=2，M=4，NP=16, N=16），fDAC=11000MSPS，fout=2000MHz / Dual-link mode, Mode 1 (L=2, M=4, NP=16, N=16), fDAC=11000MSPS, fout=2000MHz	—	952	2000	mA
DVDD1.8 电源电流 / DVDD1.8 supply current	IDVDD1.8	同上 / Same as above	—	36	60	mA
SVDD1.0 电源电流 / SVDD1.0 supply current	ISVDD1.0	同上 / Same as above	—	275	600	mA
总功耗 / Total power consumption	PW		—	1.95	4	W
最大输出转换率 / Maximum output conversion rate	fDACmax	16 位分辨率，带插值，VDDX[c]=0.975V / 16-bit resolution, with interpolation, VDDX[c]=0.975V	11	—	—	GSPS
最大 SCLK 时钟速率 / Maximum SCLK clock rate	fWSCLK	SPI 写操作 / SPI write operation	80	—	—	MHz
SCLK 时钟高电平 / SCLK clock high level	tWPWH	SPI 写操作，SCLK=20MHz / SPI write, SCLK=20MHz	5.03	—	—	ns
SCLK 时钟低电平 / SCLK clock low level	tWPWL	SPI 写操作，SCLK=20MHz / SPI write, SCLK=20MHz	1.6	—	—	ns
SDIO 到 SCLK 建立时间 / SDIO-to-SCLK setup time	tWDS	SPI 写操作 / SPI write	1.154	—	—	ns
SCLK 到 SDIO 保持时间 / SCLK-to-SDIO hold time	tWDH	SPI 写操作 / SPI write	0.577	—	—	ns
$\overline{CS}$ 到 SCLK 建立时间 / $\overline{CS}$-to-SCLK setup time	tWS	SPI 写操作 / SPI write	1.036	—	—	ns
SCLK 到 $\overline{CS}$ 保持时间 / SCLK-to-$\overline{CS}$ hold time	tWH	SPI 写操作 / SPI write	-5.3	—	—	ps
SCLK 时钟速率 / SCLK clock rate	fRSCLK	SPI 读操作 / SPI read	—	—	48.58	MHz
	tRPWH	SPI 读操作 / SPI read	5.03	—	—	ns

参数 / Parameter	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
SCLK 时钟高电平 / SCLK clock high level						
SCLK 时钟低电平 / SCLK clock low level	tRPWL	SPI 读操作 / SPI read	1.6	—	—	ns
SDIO 到 SCLK 建立时间 / SDIO-to-SCLK setup time	tRDS	SPI 读操作 / SPI read	1.158	—	—	ns
SCLK 到 SDIO 保持时间 / SCLK-to-SDIO hold time	tRDH	SPI 读操作 / SPI read	0.537	—	—	ns
$\overline{CS}$ 到 SCLK 建立时间 / $\overline{CS}$-to-SCLK setup time	tRS	SPI 读操作 / SPI read	1.036	—	—	ns
输入高电平 / Input high level	VIH	输入引脚（SDIO、SCLK、$\overline{CS}$、$\overline{RESET}$、TXEN0、TXEN1）/ Input pins (SDIO, SCLK, $\overline{CS}$, $\overline{RESET}$, TXEN0, TXEN1)	1.48	—	—	V
输入低电平 / Input low level	VIL	同上 / Same as above	—	—	0.425	V
输入高电平电流 / Input high-level current	IIH	同上 / Same as above	-1	0.003	1	uA
输入低电平电流 / Input low-level current	IIL	同上 / Same as above	-1	0.001	1	uA
输出高电平 / Output high level	VOH	输出引脚（SDIO，SDO），4mA 负载 / Output pins (SDIO, SDO), 4mA load	1.52	—	—	V
输出低电平 / Output low level	VOL	同上 / Same as above	—	—	0.175	V
输出高电平电流 / Output high-level current	IOH	输出引脚（SDIO，SDO）/ Output pins (SDIO, SDO)	4	—	—	mA
输出低电平电流 / Output low-level current	IOL	输出引脚（SDIO，SDO）/ Output pins (SDIO, SDO)	4	—	—	mA
中断输出高电平 / Interrupt output high level	VOH,IRQ	中断输出引脚（$\overline{IRQ0}$、$\overline{IRQ1}$）/ Interrupt output pins ($\overline{IRQ0}$, $\overline{IRQ1}$)	1.71	—	—	V
中断输出低电平 / Interrupt output low level	VOL,IRQ	同上 / Same as above	—	—	0.075	V
SYSREF± 输入差分阻抗 / SYSREF± input differential impedance	ZDIFF_SYS		80	106	120	Ω
SYNCOUT 输出差分电压 / SYNCOUT output differential voltage	VOD		320	365	460	mV
	VOS		1.06	1.13	1.3	V

参数 / Parameter	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
SYNCOUT 输出偏移电压 / SYNCOUT output offset voltage						
SYNCOUT 输出高电平 / SYNCOUT output high level	VOH,SYNCOUT		1.66	1.80	—	V
SYNCOUT 输出低电平 / SYNCOUT output low level	VOL,SYNCOUT		—	0.002	0.045	V
最大通道 NCO 时钟速率 [a] / Maximum channel NCO clock rate [a]	fCNCO	TC=25°C	1540	—	—	MHz
最大主 NCO 时钟速率 [a] / Maximum main NCO clock rate [a]	fMNCO	TC=25°C	11	—	—	GHz
无杂散动态范围 / Spurious-free dynamic range	SFDR	-7dBFS，随机化开启，fDAC=11000MSPS，模式 1（L=2，M=4，NP=16, N=16），VDDX [c]=0.975V; fout=100MHz / -7dBFS, randomization on, fDAC=11000MSPS, Mode 1, VDDX [c]=0.975V; fout=100MHz	60	72	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	同上；fout=2000MHz / Same; fout=2000MHz	55	66	—	dBc
无杂散动态范围 / Spurious-free dynamic range	SFDR	同上；fout=3700MHz / Same; fout=3700MHz	50	61	—	dBc
非谐波无杂散动态范围 [ad] / Non-harmonic SFDR [ad]	SFDRNH	-7dBFS，随机化开启，fDAC=11000MSPS，模式 1（L=2，M=4，NP=16, N=16），VDDX [c]=0.975V; fout=100MHz	70	82	—	dBc
非谐波无杂散动态范围 [ad] / Non-harmonic SFDR [ad]	SFDRNH	同上；fout=2000MHz / Same; fout=2000MHz	65	77	—	dBc
非谐波无杂散动态范围 [ad] / Non-harmonic SFDR [ad]	SFDRNH	同上；fout=3700MHz / Same; fout=3700MHz	60	71	—	dBc
双音互调失真 / Two-tone intermodulation distortion	IMD3	TC=25°C；-7dBFS/单音，fDAC=11000MSPS，模式 1（L=2，M=4，NP=16, N=16），VDDX [c]=0.975V; 1MHz 间距，fout=2000MHz / TC=25°C; -7dBFS/tone, fDAC=11000MSPS, Mode 1, VDDX [c]=0.975V; 1MHz spacing, fout=2000MHz	65	78	—	dBc
双音互调失真 / Two-tone intermodulation distortion	IMD3	同上；1MHz 间距，fout=3700MHz / Same; 1MHz spacing, fout=3700MHz	60	74	—	dBc
噪声频谱密度 [a] / Noise spectral density [a]	NSD	0dBFS/单音，在距离 fOUT 10% 上测量，随机化开启，fDAC=11000 MSPS，fout=2000MHz，VDDX [c]=0.975V，TC=25°C / 0dBFS/tone, measured at 10% offset from fOUT, randomization on,	140	153	—	dBc/Hz

参数 / Parameter	符号 / Symbol	条件 / Conditions	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
		fDAC=11000 MSPS, fout=2000MHz, VDDX [c]=0.975V, TC=25°C				
输出隔离度 [a] / Output isolation [a]	ISO	fDAC=11000 MSPS，fOUT=2000MHz，模式 1（L=2，M=4，NP=16, N=16），VDDX [c]=0.975V，TC=25°C	60	75	—	dB
JESD204B Lane 最大速率 [a] / JESD204B lane maximum rate [a]	fSDATA	TC=25°C	15.4	—	—	Gbps
最小时钟输出频率 / Minimum clock output frequency	fCLKOMIN		—	—	727.5	MHz
最大时钟输出频率 / Maximum clock output frequency	fCLKOMAX		3000	—	—	MHz
最小锁相环频率范围 [a] / Minimum PLL frequency range [a]	fVCOMIN	VCO 输出分频 1，TC=25°C / VCO output divide 1, TC=25°C	—	—	8.6	GHz
最大锁相环频率范围 [a] / Maximum PLL frequency range [a]	fVCOMAX	VCO 输出分频 1，TC=25°C / VCO output divide 1, TC=25°C	11	—	—	GHz

[a] 每检验批，A 组检验抽样方案常温取 3（0），筛选、B 组、C 组、D 组检验不测试此参数；/ Per inspection lot: Group A inspection sampling at room temperature takes 3 (0); screening and Groups B, C, D inspections do not test this parameter. [b] DVDD1.0 电源电流包含 DAVDD1.0 电源电流；/ The DVDD1.0 supply current includes the DAVDD1.0 supply current. [c] VDDX 表示 VAVDD1.0、VDVDD1.0、VDAVDD1.0、VSVDD1.0；/ VDDX denotes VAVDD1.0, VDVDD1.0, VDAVDD1.0, VSVDD1.0. [d] 计算 SFDR 时，先去掉前 7 次谐波。/ When calculating SFDR, the first seven harmonics are removed first.

注：典型值为常温 Tc=25°C测试数据。/ Note: typical values are room-temperature (Tc=25°C) test data.

主要特性曲线图（电特性测试图）/ Typical Characteristic Curves (Electrical Test Plots)

English: 1.1 Spectrum at -7dBFS, randomization on, fDAC=11000MSPS, Mode 1 (L=2, M=4, NP=16, N=16), fout=100MHz. 1.2 Spectrum at fout=2000MHz under the same conditions. 1.3 Spectrum at fout=3700MHz under the same conditions. 2.1 IMD3 plot, -7dBFS/tone, fDAC=11000MSPS, Mode 1 (L=2, M=4, NP=16, N=16), 1MHz spacing, fout=3700MHz. 3.1 NSD plot, 0dBFS/tone, measured at 10% offset from fOUT, randomization on, fDAC=11000 MSPS, fout=2150MHz. 4. Differential and integral nonlinearity error plots. 5. SFDR vs. output frequency. 6. IMD3 vs. output frequency. 7. IMD3 vs. output frequency. 8. Phase Noise vs. output frequency.

中文： 1.1 -7dBFS，随机化开启，fDAC=11000MSPS，模式 1（L=2，M=4，NP=16, N=16），fout=100MHz 条件下频谱图。1.2 同条件 fout=2000MHz 频谱图。1.3 同条件 fout=3700MHz 频谱图。2.1 IMD3 图-7dBFS/单音，fDAC=11000MSPS，模式 1（L=2，M=4，NP=16, N=16），1MHz 间距，fout=3700MHz。3.1 NSD 图

0dBFS/单音，在距离 fOUT 10%上测量，随机化开启，fDAC=11000 MSPS，fout=2150MHz。4、微分非线性误差和积分非线性误差图。5、SFDR 随输出频率变化曲线图。6、IMD3 随输出频率变化曲线图。7、IMD3 随输出频率变化曲线图。8、Phase Noise 随输出频率变化曲线。

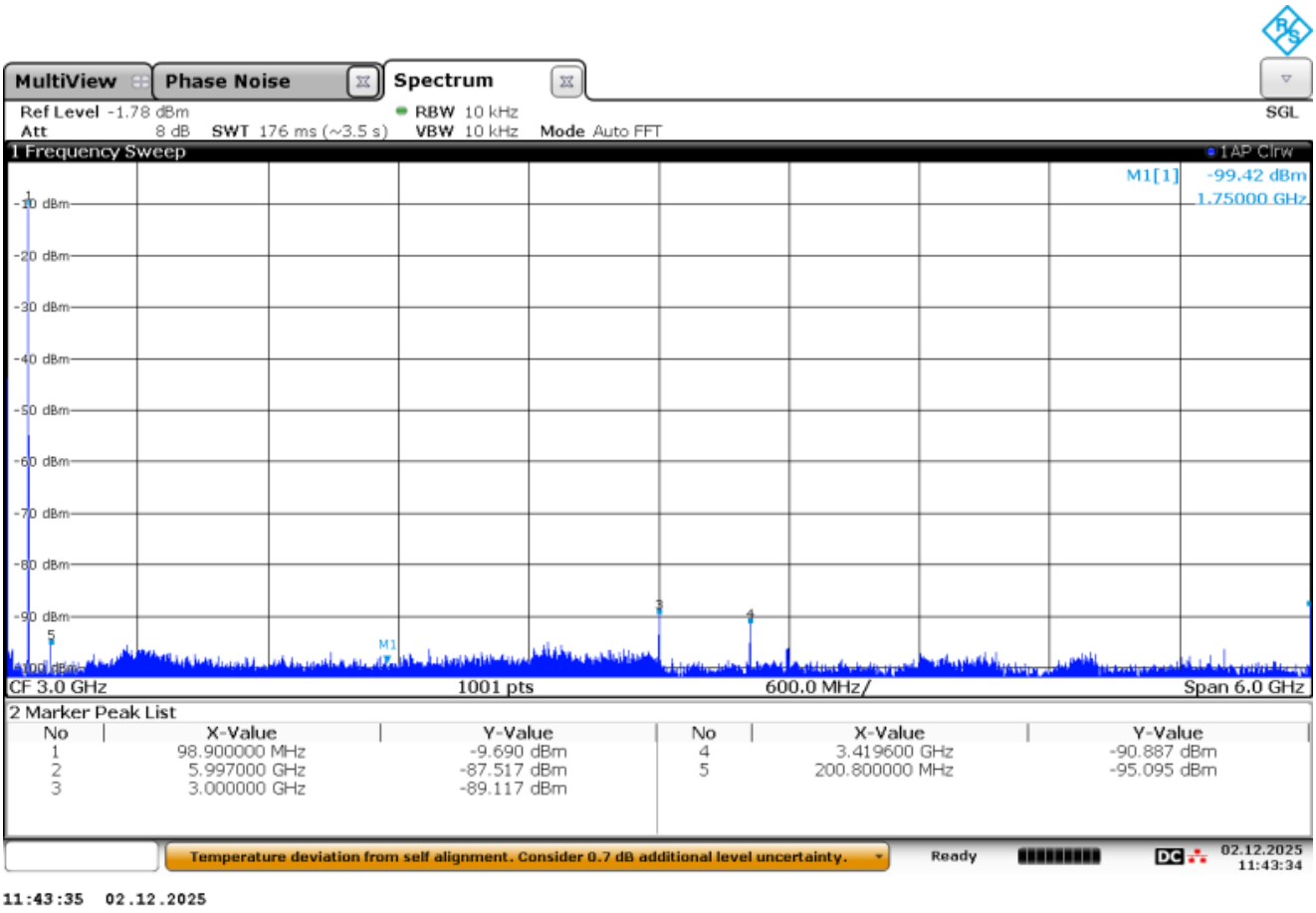


Figure 4: Spectrum, -7dBFS, randomization on, fDAC=11000MSPS, Mode 1 (L=2, M=4, NP=16, N=16), fout=100MHz

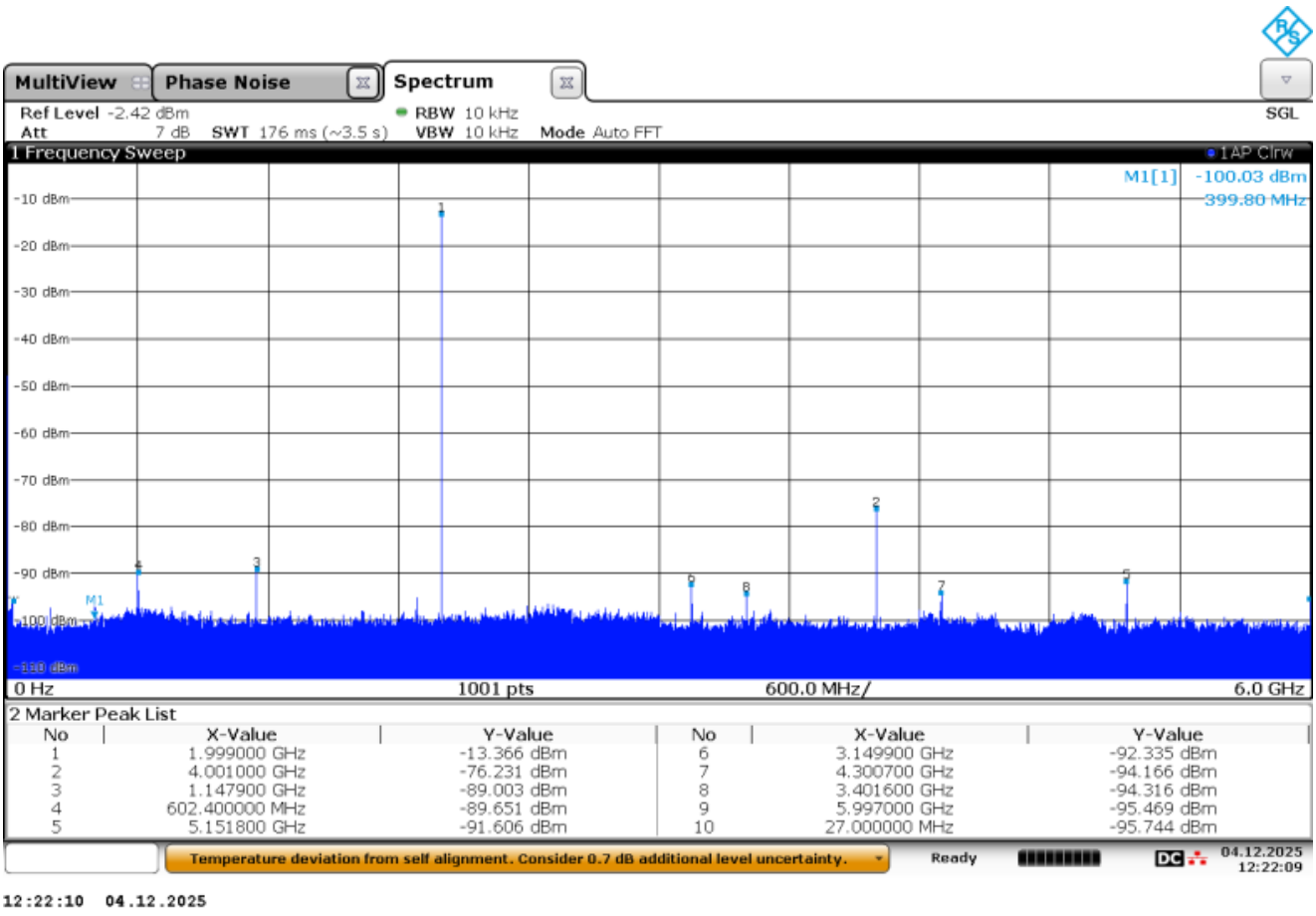


Figure 5: Spectrum, -7dBFS, randomization on, fDAC=11000MSPS, Mode 1 (L=2, M=4, NP=16, N=16), fout=2000MHz

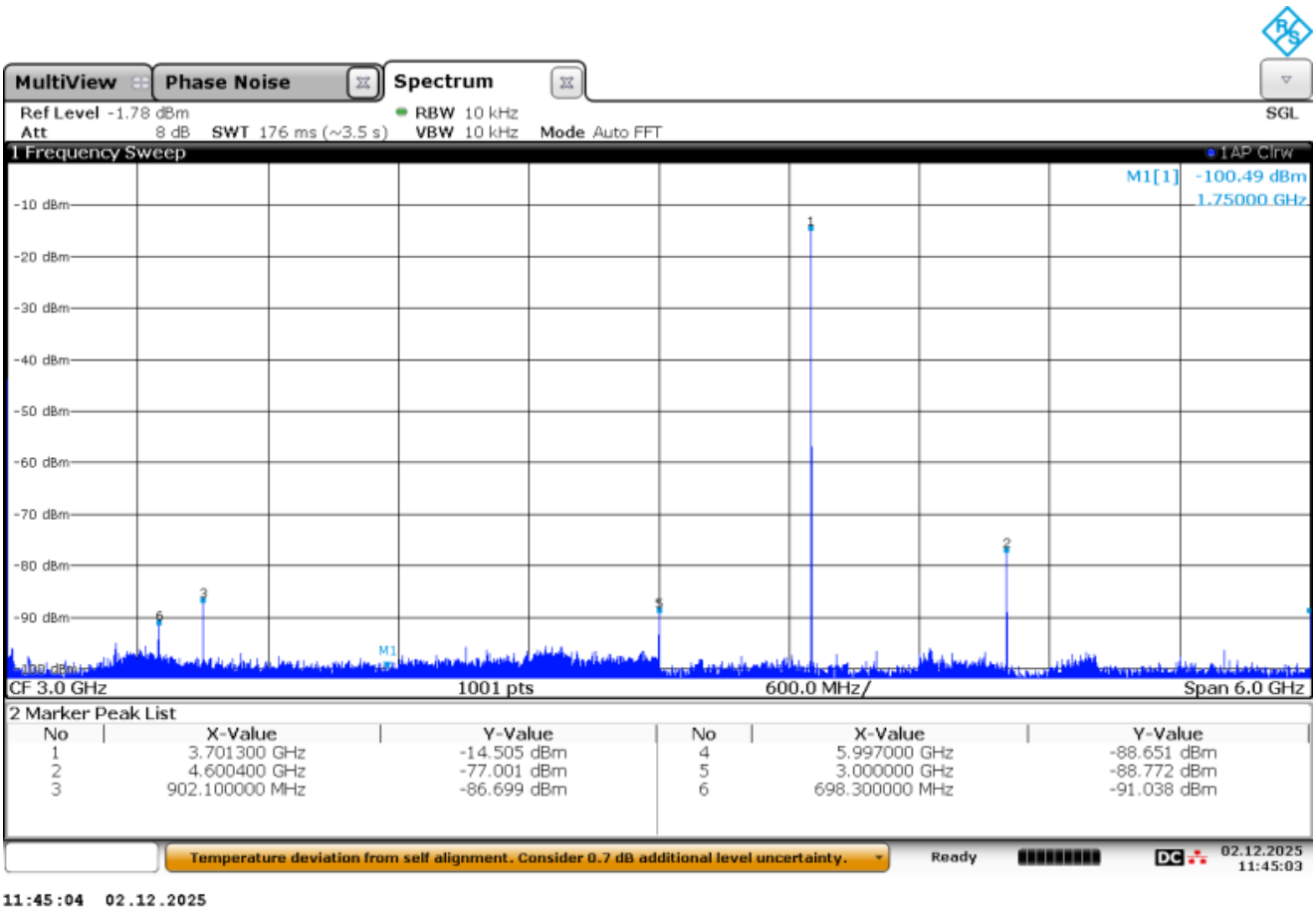


Figure 6: Spectrum, -7dBFS, randomization on, fDAC=11000MSPS, Mode 1 (L=2, M=4, NP=16, N=16), fout=3700MHz

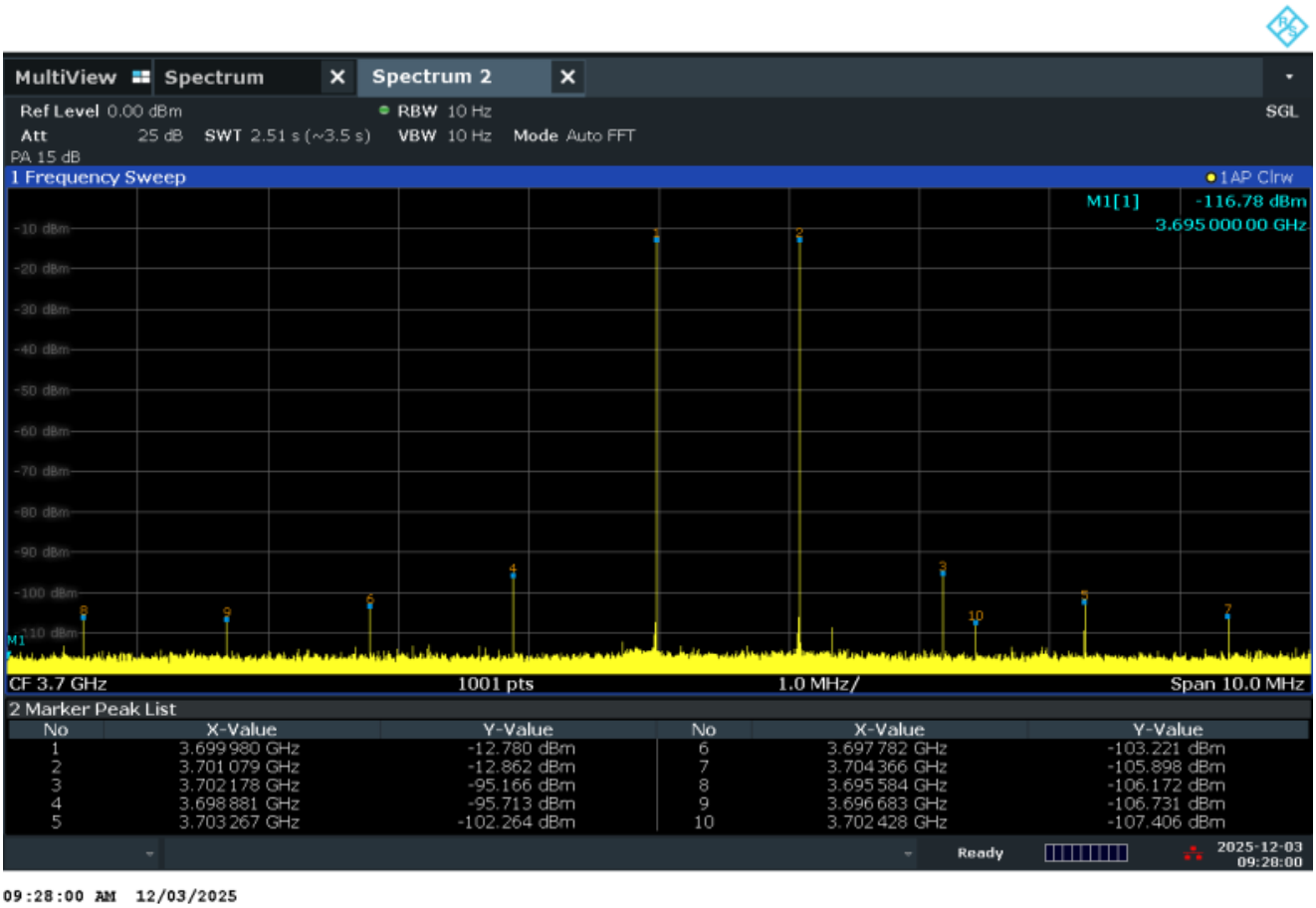


Figure 7: IMD3 at fout=3700MHz, -7dBFS/tone, fDAC=11000MSPS, Mode 1 (L=2, M=4, NP=16, N=16), 1MHz spacing

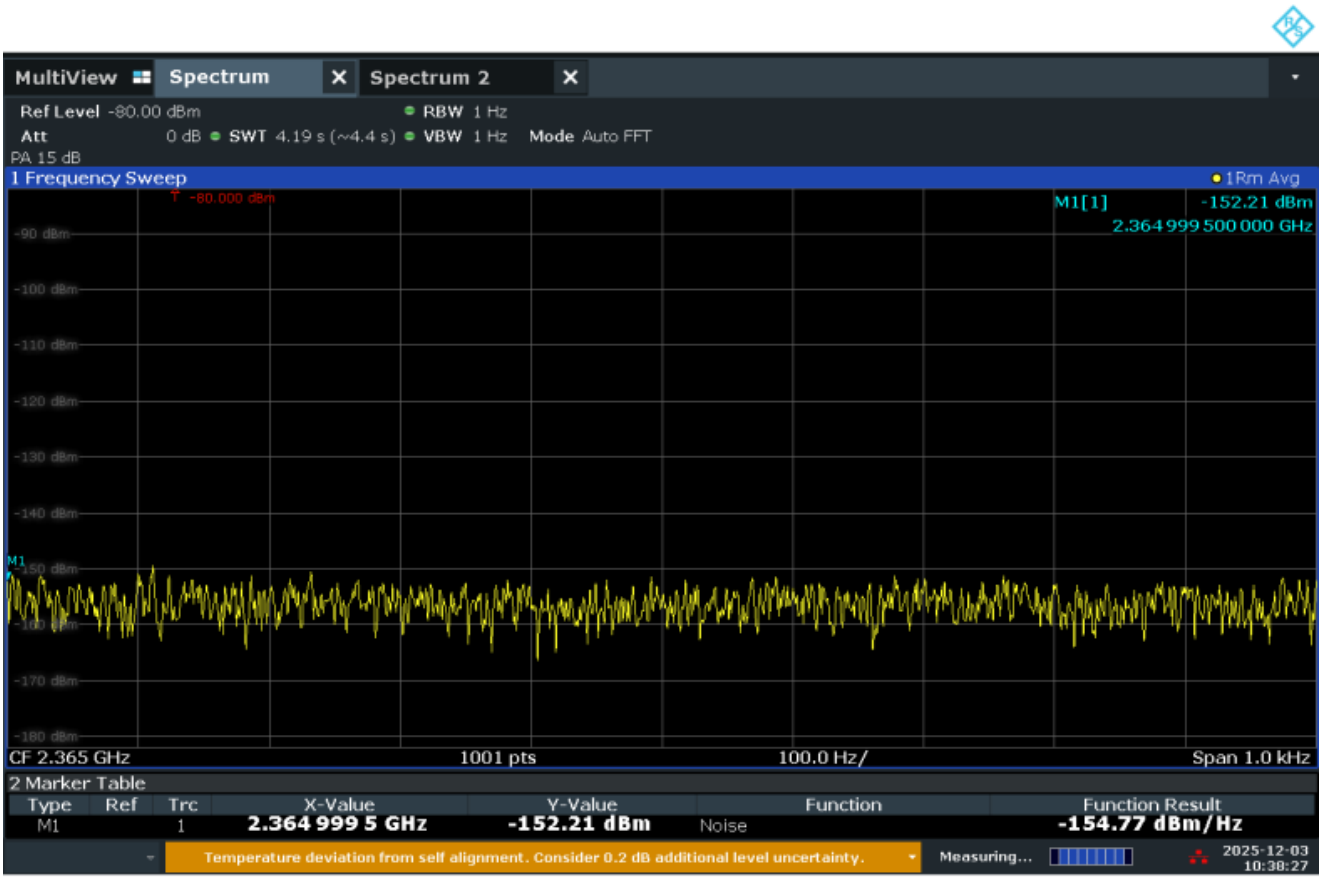


Figure 8: NSD at fout=2150MHz, 0dBFS/tone, measured at 10% offset from fOUT, randomization on, fDAC=11000 MSPS

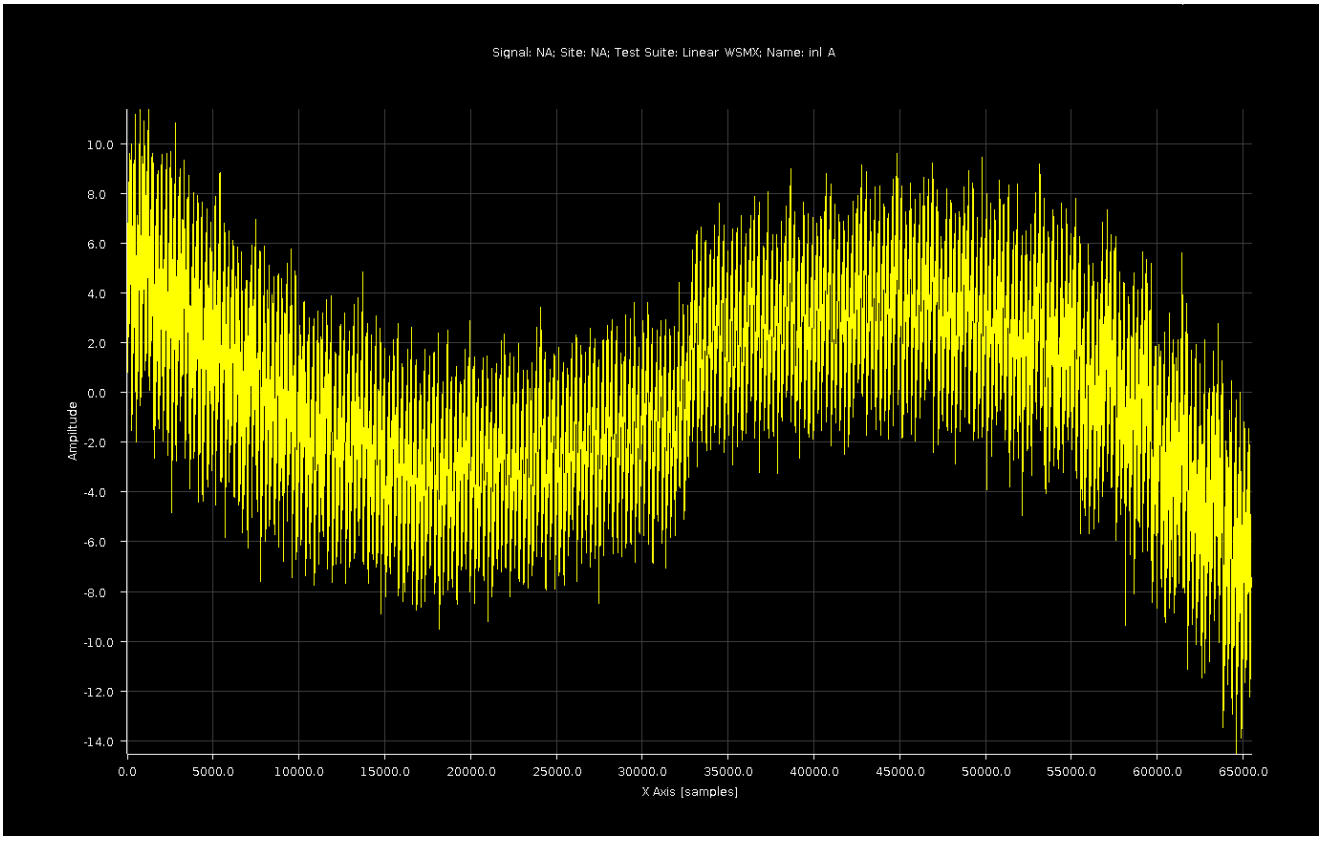


Figure 9: MODE10 1x1x fDAC=2.5GHz, shuffle on (DNL/INL plot)

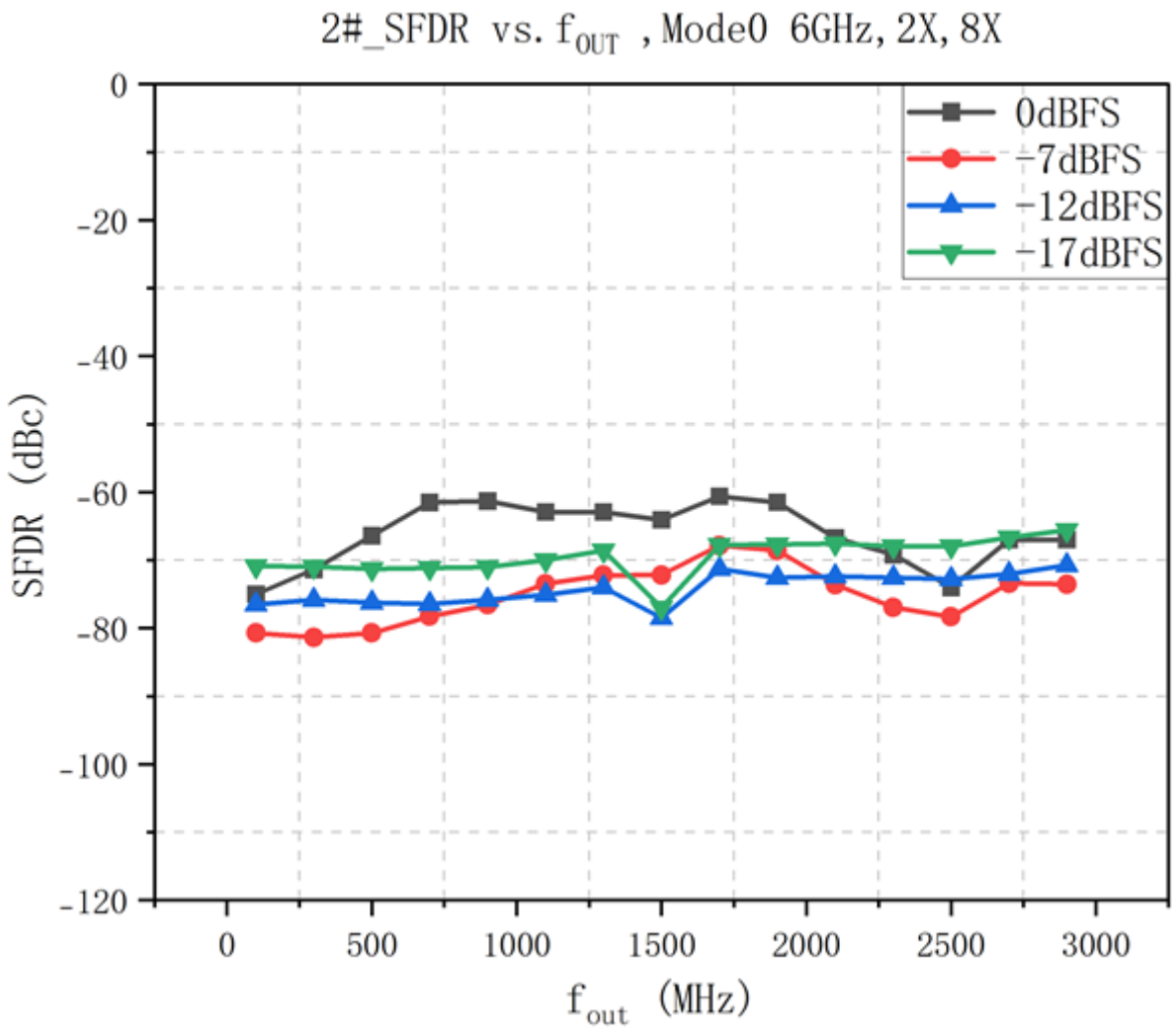


Figure 10: SFDR vs. output frequency, MODE0, 2X8X, 6GHz

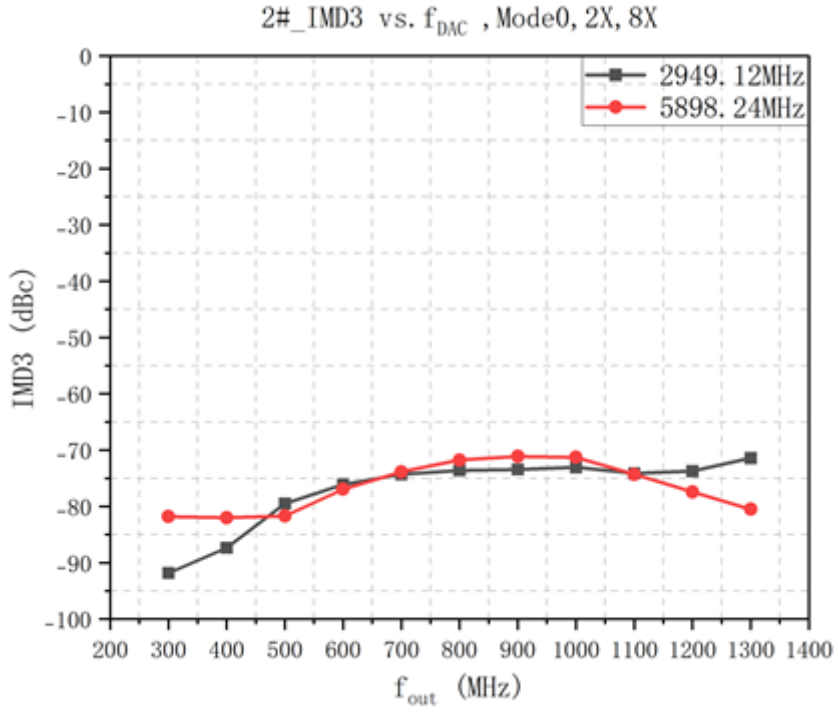


Figure 11: IMD3 vs. output frequency, MODE0, 2X8X, 2949.12MHz and 5898.24MHz

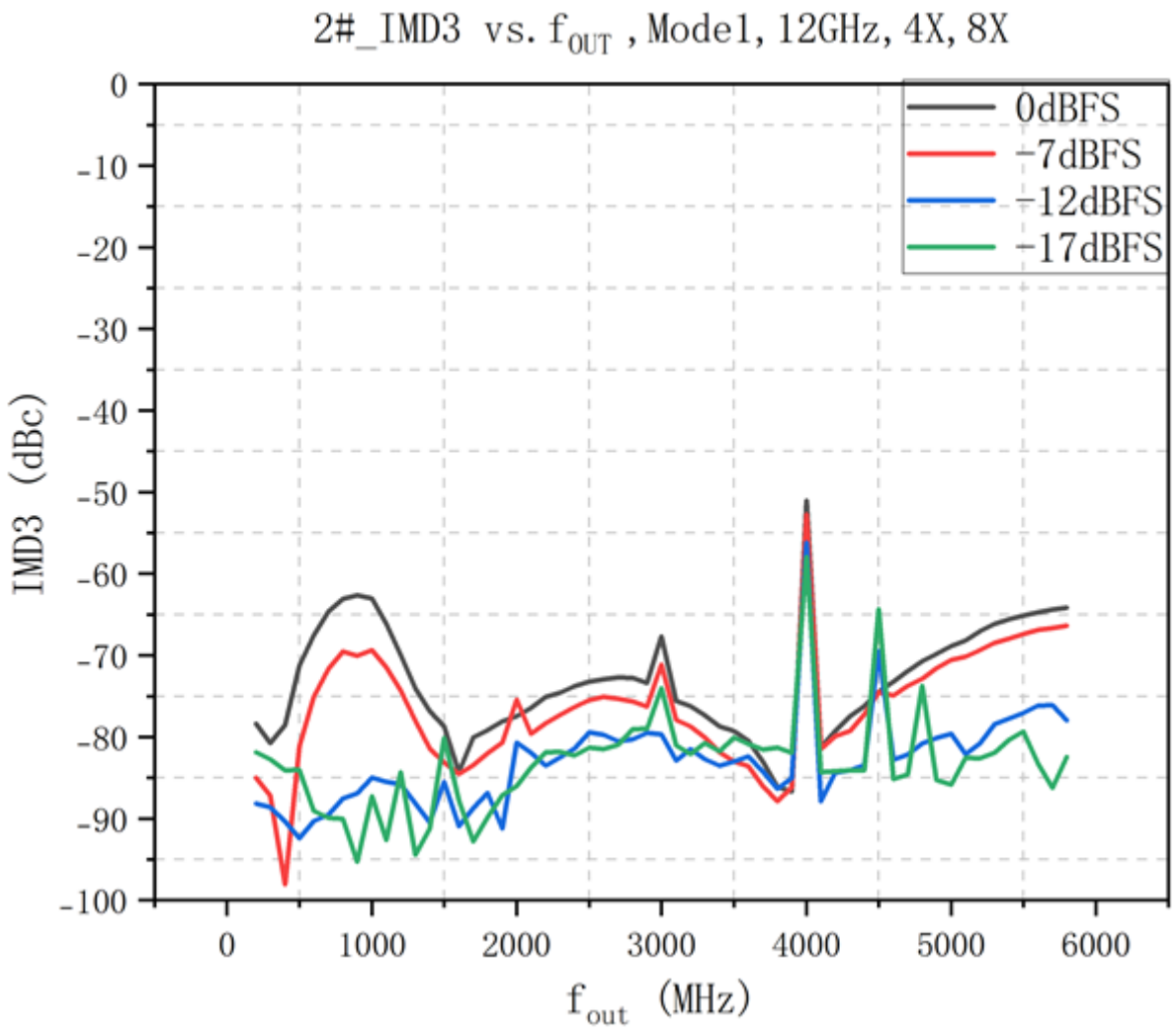


Figure 12: IMD3 vs. output frequency, MODE1, 4X8X, 12GHz

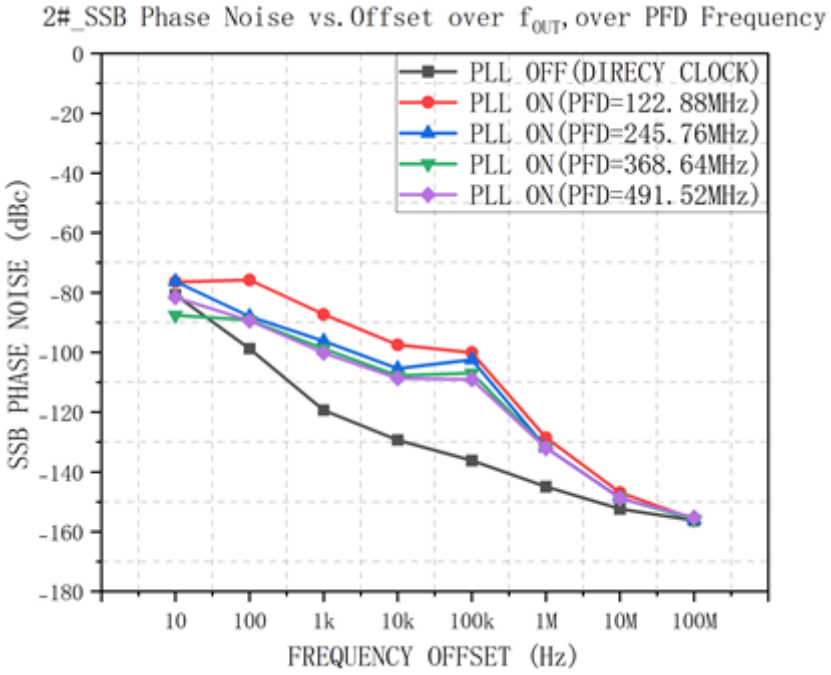


Figure 13: Phase Noise vs. output frequency, fDAC = 12GHz, fOUT=1.8GHz, PLL On, PLL Reference Clock = 500MHz

典型应用线路图 / Typical Application Circuit

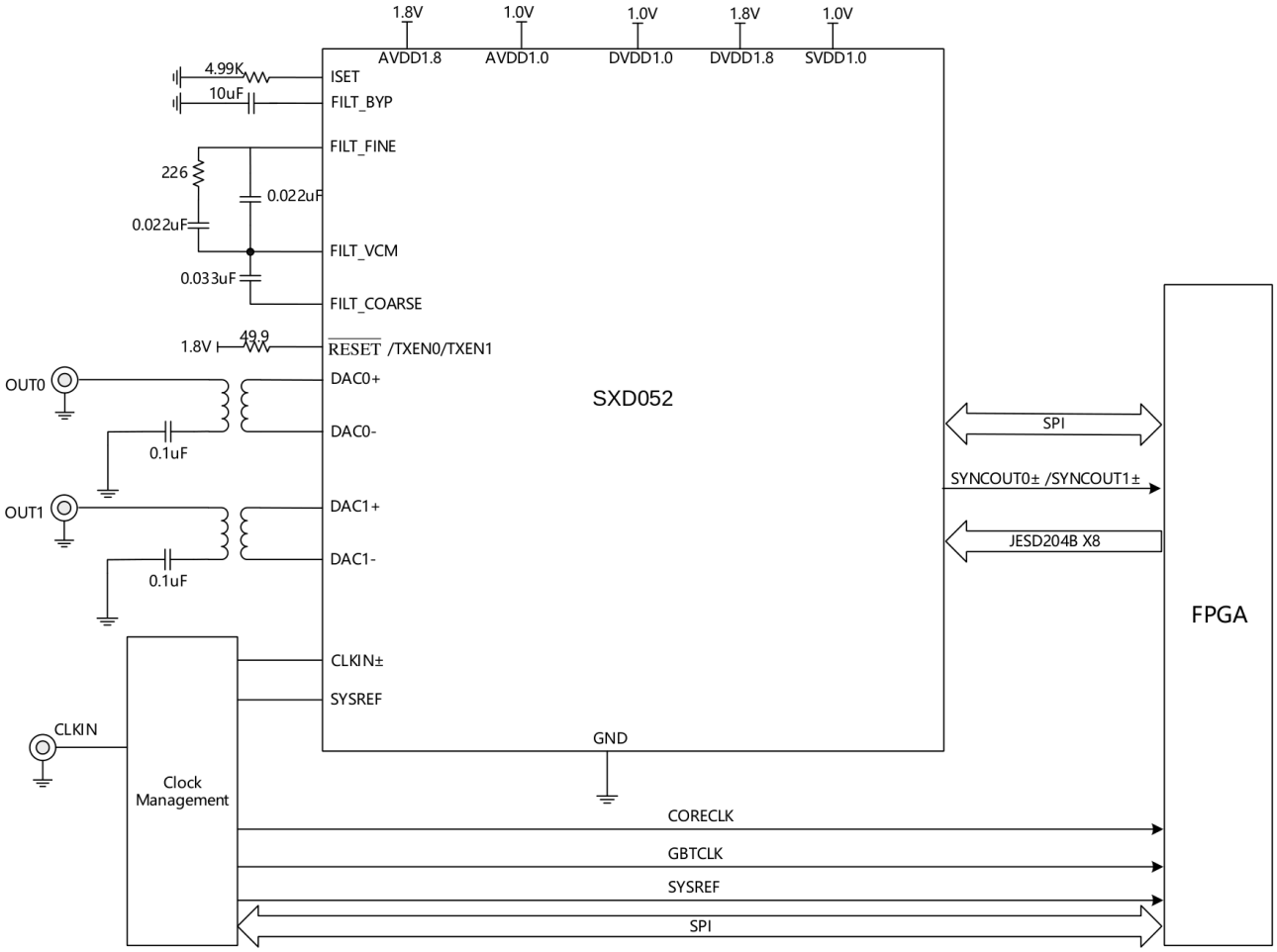


Figure 14: SXD052 typical peripheral circuit

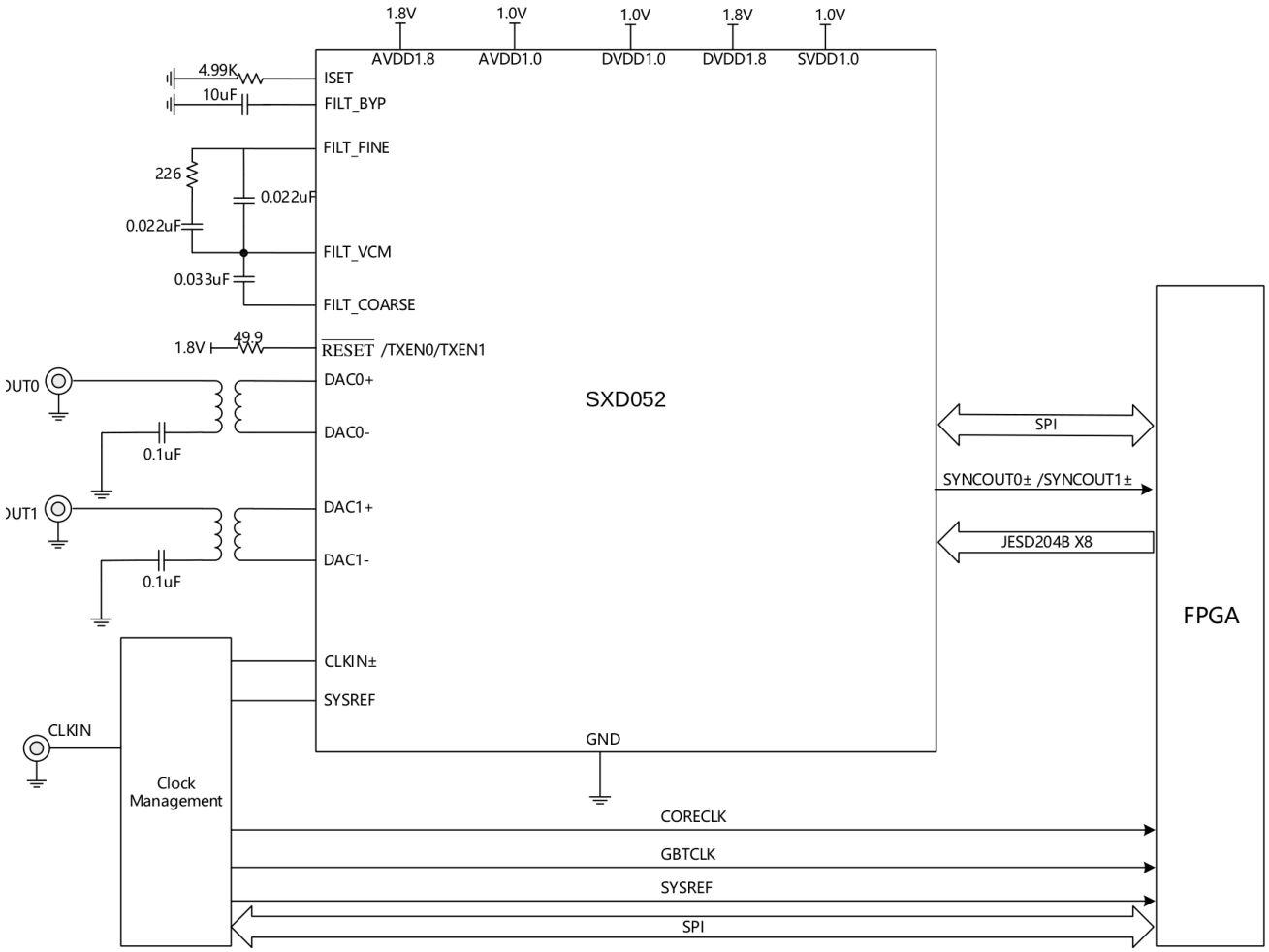


Figure 15: JESD204B interface circuit

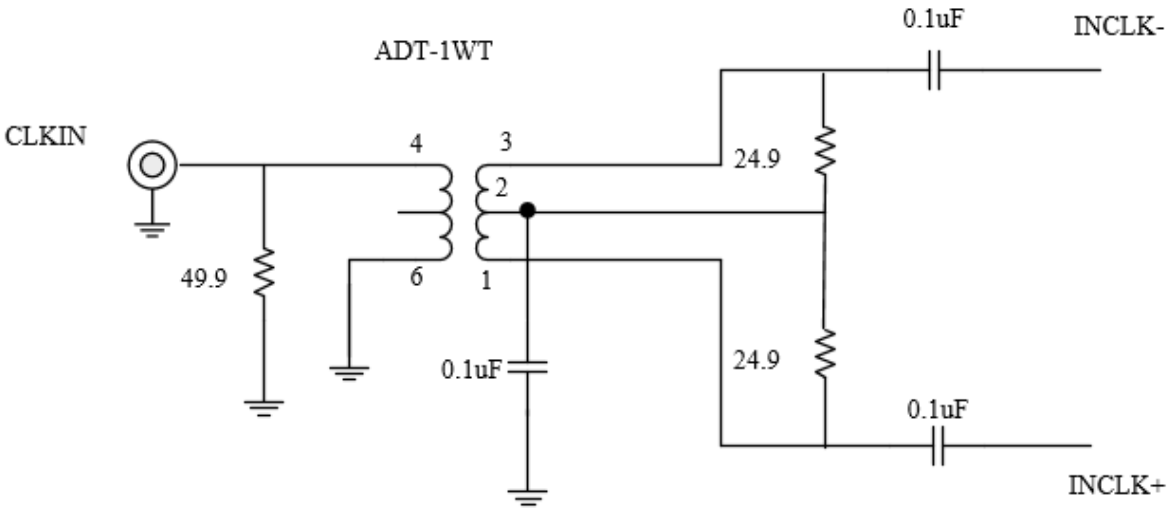


Figure 16: Clock front-end circuit

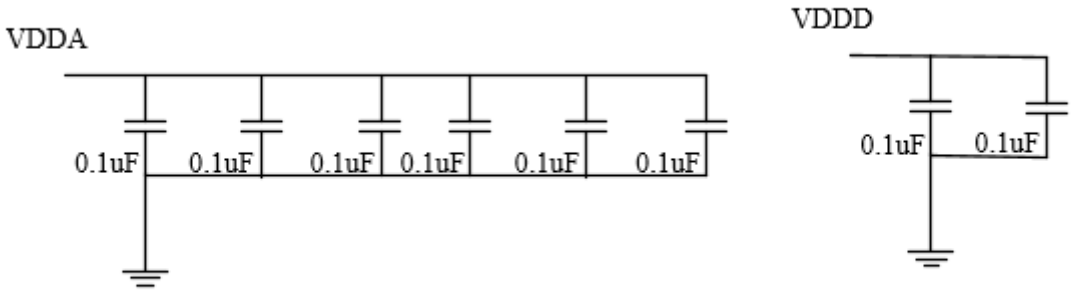


Figure 17: Power supply filtering

单元模块及工作原理 / Functional Blocks and Operating Principles

1、工作原理 / 1. Theory of Operation

English: The SXD052 is a 16-bit dual-channel RF DAC with a high-speed JESD204B SERDES interface, compliant with Subclass 0 and Subclass 1 operation requirements. Figure 1 shows the functional block diagram of the SXD052. Each DAC core has three individually bypassable channels, each channel supporting complex data-rate inputs up to 1.575 GSPS. The JESD204B interface can be configured for single-link or dual-link operation, in which each of the eight high-speed serial ports can transfer data to the channel datapaths — called channelizers — at up to 15.4 Gbps. Compared with LVDS or CMOS interfaces, the SERDES interface simplifies the device pin count, board layout and input clock requirements.

As required by the JESD204B specification, the local clock of the SERDES interface comes from the device clock (CLKIN± pins). The device clock can serve as the reference for the on-chip PLL to provide the DAC clock, or the PLL can be bypassed and the DAC clock provided directly by a high-fidelity external clock source. The SERDES interface can be configured to run with 1, 2, 3, 4 or 8 lanes in each link mode, depending on the required input data rate. In dual-link operation, each link can use up to four lanes.

The digital datapath of the SXD052 includes bypassable (1×) interpolation blocks in the channel datapaths and the main datapath. Depending on the mode required, the channel datapath also offers 2×, 3×, 4×, 6× and 8× interpolation options, and the main datapath offers 2×, 4×, 6×, 8× and 12× interpolation options. See Table 1 for the various supported processing modes and the associated interpolation options.

When 1× interpolation (bypass) is not selected, each channel digital datapath allows the user to independently control each channel's gain stage and NCO module. The NCO module has a 48-bit modulus NCO option, enabling digital frequency translation of signals with almost unlimited precision. At the end of the three channelizer datapaths, a summing node combines the three channelizers at up to 1.575 GSPS and sends the result as input to the respective main DAC datapath for further digital processing.

Each main DAC datapath contains: an optional power-amplifier (PA) protection module, a main datapath interpolation module, a main NCO with optional modulus capability, and a ramp-up/ramp-down gain module provided by the PA protection module. There is also an optional calibration single-tone feature, and four modulator-switch modes as part of the main NCO module.

Each NCO can independently operate in direct digital synthesis (DDS) mode. By providing digital data from the SERDES interface, each NCO tone frequency can be assigned individually, or collectively assigned to all NCOs using an SPI-programmable register. Frequencies can be controlled individually.

The SXD052 also has an FFH function, allowing fast hopping among 31 additional NCOs, each NCO operating at 32-bit precision. Multiple operating modes exist, and coherence or phase continuity can be maintained between frequency hops. Assuming each frequency tuning word (FTW) is preloaded, only a single SPI write is needed to hop to the next frequency.

The SXD052 also supports multichip synchronization, which both synchronizes multiple DACs and establishes a constant, deterministic latency (latency-locked) path for the DACs. The latency of each DAC remains constant, and the latency spread among linked DACs is within a few DAC clock cycles. The external alignment signal (SYSREF±) makes the SXD052 compliant with the JESD204B Subclass 1 standard. Several methods of handling the SYSREF± signal can be used in a system.

An SPI port can configure the various functional blocks and monitor their status. The various functional blocks and the data interface must be set up in a predetermined order for proper operation (see the Start-Up Sequence section). A simple SPI initialization routine that configures the JESD204B link is included in the SXD052-FMC-EBZ evaluation board package. This manual describes the various modules of the SXD052 in detail, including descriptions of the JESD204B interface, control parameters, and the various registers used to configure and monitor the device. The recommended start-up routine reliably configures the data link.

中文： SXD052 是一款 16 位双通道射频 DAC，具有高速 JESD204B SERDES 接口，符合 Subclass0 和 Subclass1 操作要求。图 1 显示了 SXD052 的功能框图。每个 DAC 核都有三个可单独旁路的信道，每个信道支持高达 1.575 GSPS 的复数数据速率输入。JESD204B 接口可配置为单链路或双链路工作，其中 8 个高速串行端口当中的每一个都能以最大 15.4Gbps 的速率传输数据到通道数据路径，称之为信道化。与 LVDS 或 CMOS 接口相比，SERDES 接口简化了对器件的引脚数量、电路板布局和输入时钟的要求。

按照 JESD204B 规范的要求，SERDES 接口的本地时钟来自器件时钟（CLKIN±引脚）。器件时钟可以作为片上 PLL 的基准，以提供 DAC 时钟；或者可以将该 PLL 旁路，DAC 时钟直接由高保真的外部时钟源提供。SERDES 接口可以配置为在每种链路模式的 1、2、3、4 或 8 lane 下运行，取决于所需的输入数据速率。在双链路运行下，每个链路最多可以使用四个 lane。

SXD052 的数字数据路径包括通道数据路径和主数据路径中的可旁路（1×）插值块。根据所需模式，通道数据路径还有 2×、3×、4×、6×和 8×插值选项，主数据路径也有 2×、4×、6×、8×和 12×插值选项。关于各种可支持的处理模式，以及相关的插值选项，请参见表 1。

不选择 1×插值（旁路），每个通道的数字数据路径允许用户独立控制每个通道的增益级和 NCO 模块。NCO 模块有一个 48 位的模量 NCO 选项，可以实现几乎无限精度的信号的数字移频。在三个信道器数据路径的末端，有一个求和节点，将三个信道器以最大 1.575 GSPS 的速率组合在一起，作为输入发送到各自的主 DAC 数据路径，做进一步的数字处理。

每个主 DAC 数据路径包含：一个可选的功率放大器（PA）保护模块，一个主数据路径插值模块，一个具有可选模量特征的主 NCO，以及一个由 PA 保护模块提供的 ramp-up/ramp-down 增益模块。此外，还有一个可选的校准单音特征，以及作为主 NCO 模块一部分的四个调制器开关模式。

每个 NCO 可以独立地在直接数字合成（DDS）模式下运行。通过提供来自 SERDES 接口的数字数据，可以单独分配每个 NCO 单音频率，或者使用一个 SPI 可编程寄存器集体分配给所有 NCO。频率可以单独控制。

SXD052 还具有 FFH 功能，从而可以在 31 个额外的 NCO 之间快速跳转，每个 NCO 运行在 32 位的精度下。存在着多种运行模式，在跳频之间可以保持相干性或相位连续性。假设每个频率调整字(FTW)都已预装，那么只需一次 SPI 写入就可以跳到下一个频率。

SXD052 还能进行多芯片同步，既能使多个 DAC 同步，又能为 DAC 建立一个恒定和确定性的延迟（延迟锁定）路径。每个 DAC 的延迟值保持恒定，建立好链路的 DACs 之间的延迟值范围在几个 DAC 时钟周期内。外部对齐信号（SYSREF±）使 SXD052 符合 JESD204B Subclass1 标准。有几种处理 SYSREF±信号的方法可在系统中使用。

一个 SPI 端口可以配置各种功能模块并监测其状态。各种功能模块和数据接口必须按照预定的顺序设置，以便正常运行（见启动顺序部分）。简单的 SPI 初始化例程配置 JESD204B 链路，包含在 SXD052-FMC-EBZ 评估板封装中。本产品手册详细描述了 SXD052 的各种模块。提供了 JESD204B 接口、控制参数以及用于配置和监控器件的各种寄存器的说明。推荐的启动例程可靠地配置了数据链路。

表 1 JESD204B 支持的工作模式和插值组合 / Table 1. Supported JESD204B Operating Modes and Interpolation Combinations

应用 / Application	链路模式 / Link Mode	JESD204B 模式 / Mode	链路通道 / Lanes per Link	DAC 通道数 / DAC Channels	最大通道数据速率 (MSPS)[1] / Max Channel Data Rate (MSPS)[1]	通道内插值 / Channel Interpolation	主数据路径插值 / Main Datapath Interpolation	最大 DAC 速率 (GSPS)[2] / Max DAC Rate (GSPS)[2]	最大瞬时带宽 (MHz)[3] / Max Instantaneous BW (MHz)[3]
信道器模式（所有复数）375MHz (N = 16 位) — 单通道 / Channelizer mode (all complex), 375MHz (N = 16 bits) — Single channel	单 / Single	0	1	1	385	2×	8×	6.16	308
同上 / Same	双 / Dual	0	1	1	385	4×, 6×	6×, 8×	12	308
信道器模式 375MHz — 双通道 / Channelizer 375MHz —	单 / Single	1	2	2	385	4×, 6×	6×, 8×	12	616

应用 / Application	链路模式 / Link Mode	JESD204B 模式 / Mode	链路通道 / Lanes per Link	DAC 通道数 / DAC Channels	最大通道数据速率 (MSPS)[1] / Max Channel Data Rate (MSPS)[1]	通道内插值 / Channel Interpolation	主数据路径插值 / Main Datapath Interpolation	最大 DAC 速率 (GSPS)[2] / Max DAC Rate (GSPS)[2]	最大瞬时带宽 (MHz)[3] / Max Instantaneous BW (MHz)[3]
Dual channel									
信道器模式 375MHz — 三通道 / Channelizer 375MHz — Three channels	单 / Single	2	3	3	385	4×, 6×	6×, 8×	12	924
信道器模式 500MHz (N = 12 位) — 单通道 / Channelizer 500MHz (N = 12 bits) — Single channel	单 / Single	5	1	1	513	2×	6×	6.16	410.4
同上 / Same	双 / Dual	5	1	1	513	3×	6×, 8×	12	410.4
信道器模式 500MHz — 双通道 / Channelizer 500MHz — Dual channel	单/双 / Single/Dual	6	2	2	513	3×	6×, 8×	12	
信道器模式 750MHz (N = 16 位) — 单通道 / Channelizer 750MHz (N = 16 bits) — Single channel	单 / Single	3	2	1	770	1×	8×	6.16	616
同上 / Same	双 / Dual	3	2	1	770	2×, 3×	6×, 8×	12	616
信道器模式 750MHz — 双通道 / Channelizer 750MHz — Dual channel	单 / Single	4	4	2	770	2×, 3×	6×, 8×	12	616

应用 / Application	链路模式 / Link Mode	JESD204B 模式 / Mode	链路通道 / Lanes per Link	DAC 通道数 / DAC Channels	最大通道数据速率 (MSPS)[1] / Max Channel Data Rate (MSPS)[1]	通道内插值 / Channel Interpolation	主数据路径插值 / Main Datapath Interpolation	最大 DAC 速率 (GSPS)[2] / Max DAC Rate (GSPS)[2]	最大瞬时带宽 (MHz)[3] / Max Instantaneous BW (MHz)[3]
同上 / Same	双 / Dual	4	4	2	385	4×	8×	12	308
信道器模式 187MHz (N = 16 位) — 双通道 / Channelizer 187MHz (N = 16 bits) — Dual channel	单/双 / Single/Dual	7	1	2	192.5	8×	6×, 8×	12	154
带宽模式（复数或实数）3000MHz (N=16 位) — 复数 / Bandwidth mode (complex or real), 3000MHz (N=16 bits) — Complex	单 / Single	10, 11	8	1	3080	1×	2×, 4×	12	2464
带宽模式 3000MHz — 实数，双 DAC / Bandwidth 3000MHz — Real, dual DAC	单 / Single	10, 11	8	1	3080	1×	1×	3.08	1540
带宽模式 3000MHz — 实数，单 DAC / Bandwidth 3000MHz — Real, single DAC	单 / Single	18, 19	4	1	3080	1×	1×	3.08	1540
带宽模式 1500MHz (N=16 位) — 复数，双 DAC / Bandwidth	单/双 / Single/Dual	8, 9	4	2 [4]	1540	1×	2×, 4×, 6×, 8×, 12×	12	2464 [4]

应用 / Application	链路模式 / Link Mode	JESD204B 模式 / Mode	链路通道 / Lanes per Link	DAC 通道数 / DAC Channels	最大通道数据速率 (MSPS)[1] / Max Channel Data Rate (MSPS)[1]	通道内插值 / Channel Interpolation	主数据路径插值 / Main Datapath Interpolation	最大 DAC 速率 (GSPS)[2] / Max DAC Rate (GSPS)[2]	最大瞬时带宽 (MHz)[3] / Max Instantaneous BW (MHz)[3]
1500MHz (N=16 bits) — Complex, dual DAC									
带宽模式 4000MHz (N=12 位) — 复数 / Bandwidth 4000MHz (N=12 bits) — Complex	单 / Single	12	8	1	4100	1×	2× [5]	8.2	3280
带宽模式 4000MHz — 实数，双 DAC / Bandwidth 4000MHz — Real, dual DAC	单 / Single	12	8	1	4100	1×	1×	4.1	2050
带宽模式 2000MHz (N=12 位) — 复数，双 DAC / Bandwidth 2000MHz (N=12 bits) — Complex, dual DAC	单/双 / Single/ Dual	22	4	2 [4]	2050	1×	4×, 6×	12	3280 [4]
带宽模式 6000MHz (N=16 位) — 实数，单 DAC / Bandwidth 6000MHz (N=16 bits) — Real, single DAC	单 / Single	20, 21	8	1	6160	1×	1×	6.16	3080

[1] 最大数据速率是根据最大通道速率计算的。数据速率的计算公式为：通道速率=（10/8）×NP×数据速率×(M/L)，其中 NP、M 和 L 值取决于所选的模式。/ The maximum data rate is calculated from the maximum lane rate. Lane rate = (10/8) × NP × data rate × (M/L), where NP, M and L depend on the selected mode. [2] 每个模式的最大 DAC 速率取决于电压容限以及特定配置的通道速率。/ The maximum DAC rate of each mode depends on the voltage tolerance and the lane rate of the specific configuration. [3] 对于复数模式，瞬时带宽

（IBW）是指 I 和 Q 同时占据的带宽（称为 I/Q 组合带宽）。复数模式的带宽部分受插值滤波器带宽的限制。当将插值滤波器旁路时，再将 SXD052 配置为实数模式时，IBW=1/2×数据速率。/ For complex modes, instantaneous bandwidth (IBW) is the bandwidth occupied by I and Q simultaneously (the combined I/Q bandwidth). The bandwidth of complex modes is partly limited by the interpolation filter bandwidth. When the interpolation filter is bypassed and the SXD052 is configured in real mode, IBW = 1/2 × data rate. [4] 通过正确的调制器开关配置，SXD052 可配置为宽带、双通道 DAC，每个通道都包括自己的主数据路径 NCO。在这种情况下，调制器开关被配置为一个求和节点，该节点将两个数据路径的复杂数据送入一个 DAC 内核。/ With the correct modulator-switch configuration, the SXD052 can be configured as a wideband dual-channel DAC, each channel including its own main datapath NCO. In this case the modulator switch is configured as a summing node that feeds the complex data of two datapaths into one DAC core. [5] 只有当 JESD204B 被配置为 Subclass1 工作时才支持。/ Supported only when JESD204B is configured for Subclass 1 operation.

1.1 SPI 接口 / 1.1 SPI Interface

English: The SXD052 uses an SPI interface that connects easily to many industry-standard microcontrollers and microprocessors. The serial I/O port is compatible with most synchronous transfer formats, including Motorola SPI and Intel SSR protocols. The interface allows read/write access to all registers that configure the SXD052. Both MSB-first and LSB-first transfer formats are supported. The SXD052 serial interface port can be set as a 4-wire interface or a 3-wire interface, where in the 3-wire interface the input and output share a single I/O pin (SDIO). Data can be transferred one byte at a time with the address specified for each read/write operation, or transferred in multibyte mode with the address auto-incrementing at the end of each transfer cycle, so that sequential read/write operations in multibyte mode increase link throughput.

The SXD052 communication cycle has two phases. Phase 1 is the instruction cycle (writing the instruction byte to the device), aligned with the first 16 SCLK rising edges; the instruction byte provides the serial-port controller with information about the data-transfer cycle, i.e. Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or a write, and the starting register address of the next data transfer.

Applying a logic high and then a logic low on the CS pin resets the serial-port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction byte of the current I/O operation.

The remaining SCLK edges represent Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the circuit and the system controller. Phase 2 of the communication cycle is the transfer of one or more data bytes. During the transfer cycle, 8×N SCLK cycles are required to transfer N bytes. A register updates (latches) its data immediately when the last bit of each transferred byte is written. Only the FTW and the NCO phase offset take effect immediately when the frequency tuning word FTW_LOAD_REQ bit is set.

中文： SXD052 采用了 SPI 接口，可轻松的与许多工业标准的微控制器和微处理器连接。该串行 I/O 端口与大多数同步传输格式兼容，包括 Motorola SPI 和 Inter SSR 协议。该接口允许对配置 SXD052 的所有寄存器进行读/写访问。支持 MSB first 或 LSB first 传输格式。SXD052 串行接口端口可设置为 4 线接口或 3 线接口，其中 3 线接口的输入和输出共享一个单引脚 I/O（SDIO）。数据可以一次传输一个字节，同时传输每次读/写操作指定的地址，也可以以多字节模式传输，同时在每个传输周期结束时，地址自动递增，因此对多字节模式的地址进行连续读/写操作时，可以增加链路吞吐量。

SXD052 的通信周期有两个阶段。阶段 1 是指令周期（向设备写入指令字节），与前 16 个 SCLK 上升沿相吻合，该指令字节向串行端口控制器提供有关数据传输周期，即通信周期第 2 阶段的信息。第 1 阶段指令字定义了即将进行的数据传输是读还是写，以及下一步数据传输的起始寄存器地址。

CS 引脚上输入逻辑高电平，然后是逻辑低电平，可以将串口时序复位到指令周期的初始状态。从这个状态开始，接下来的 16 个上升的 SCLK 沿代表当前 I/O 操作的指令字节。

剩余的 SCLK 沿代表通信周期的第 2 阶段。第 2 阶段是电路和系统控制器之间的实际数据传输。通信周期的第 2 阶段是一个或多个数据字节的传输。在传输周期中，需要 8×N 个 SCLK 周期来传输 N 个字节。寄存器在写入每个传输字节的最后一位时立即更新（锁存）其数据。只有 FTW 和 NCO 相位偏移，需要频率调谐字 FTW_LOAD_REQ 位被设置时，寄存器才会立即改变。

1.1.1 数据格式 / 1.1.1 Data Format

English: The instruction byte contains the information shown in Table 2.

中文： 指令字节包含表 2 所示的信息。

表 2 指令字节数据格式 / Table 2. Instruction Byte Data Format

MSB				·····			LSB
I15	I14	I13	I12	·····	I2	I1	I0
R/W	A14	A13	A12	·····	A2	A1	A0

English: R/W, bit 15 of the instruction byte, determines whether a read or a write data transfer follows the instruction-word write. Logic 1 indicates a read operation; logic 0 indicates a write operation.

A14 to A0 of the instruction byte, i.e. bits I14 to I0 of the instruction word, determine the register accessed during the data-transfer phase of the communication cycle. For multibyte transfers, A[14:0] is the starting address. The remaining register addresses are generated according to the address-increment bit. If the address-increment bit is set high (Register 0x000, Bit 5 and Bit 2), a multibyte SPI write starts at A[14:0] and increments by 1 every 8 bits sent/received. If the address-increment bit is set to 0, the address decrements by 1 every 8 bits.

中文： R/W，指令字节的第 15 位，决定在指令字写入后，是读还是写数据传输。逻辑 1 表示读操作，逻辑 0 表示写操作。

指令字节的 A14 到 A0，即指令字的位 I14 到位 I0，决定了在通信周期的数据传输信息访问的寄存器。对于多字节传输，A[14:0]为起始地址。剩余的寄存器地址根据地址增量位生成。如果地址增量位被设置为高位（寄存器 0x000、位 5 和位 2），多字节的 SPI 写入从 A[14:0]开始，每发送/接收 8 个 bit，就增加 1。如果地址增量位被设置为 0，地址每 8 bit 递减 1。

1.1.2 SPI 端口描述 / 1.1.2 SPI Port Description

English: - **SCLK — Serial clock.** The serial clock pin synchronizes data into the circuit and runs the internal state machine. The maximum frequency of SCLK is 80 MHz. All data is written to registers on the rising edge of SCLK and driven out on the falling edge of SCLK. - **CSB — Chip select.** An active-low input that initiates and defines a communication cycle. It allows multiple devices to use the same serial channel. When this port input is high, the ports SDO and SDIO become high-impedance. The chip-select

signal should remain low throughout the communication cycle. - **SDIO — Serial data I/O port.** This pin is a bidirectional data port. In 4-wire mode, this pin serves as the data input and SDO as the data output. - **SDO — Serial data output.** Data is read out from this port. When the circuit operates in 3-wire mode, this port cannot output data and is set to high-impedance.

中文： - SCLK-串行时钟：串行时钟引脚将数据同步到电路，并运行内部状态机。SCLK 的最大频率为 80 MHz。所有的数据都在 SCLK 的上升沿写入寄存器，在 SCLK 的下降沿驱动输出。 - CSB－片选信号：低有效开始输入及定义一个通信周期。允许多个器件使用相同的串行通道。当该端口输入为高时，端口 SDO 和 SDIO 变为高阻态。在整个通信周期内片选信号应该保持为低。 - SDIO－串行数据 I/O 端口：该引脚是双向数据端口。在 4 线模式下，该引脚作为数据输入，SDO 作为数据输出。 - SDO－串行数据输出：数据从该端口读出。当电路工作于 3 线模式时，该端口不能进行数据输出，并被设置成高阻态。

1.1.3 SPI 的配置 / 1.1.3 SPI Configuration

English: The serial port supports both MSB-first and LSB-first data formats. This function is controlled by LSB first (Register 0x000, Bit 6 and Bit 1). The default is MSB-first format (LSB first bits = 0).

When LSB first = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. R/W followed by A[14:0] forms the instruction word, and D[7:0] is the data word.

When LSB first = 1 (LSB first), the instruction and data bits must be written from LSB to MSB. A[0:14] is followed by R/W, and then by D[0:7].

The SPI supports 3-wire or 4-wire interfaces. When the SDO active bit = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with an input pin (SDIO) and an output pin (SDO) is used. When the SDO active bit = 0, the SDO pin is not used and the SDIO pin is used for both input and output.

Holding the CS pin low supports multibyte data transfers. The first 8 SCLKs after the instruction cycle read/write from the register provided in the instruction cycle. With every additional 8 SCLK cycles, the address increments or decrements and read/write proceeds on the new register. The direction of address change can be set using ADDRINC or ADDRINC_M (Register 0x000, Bit 5 and Bit 2). When ADDRINC or ADDRINC_M is 1, the address increments over multiple cycles. When ADDRINC or ADDRINC_M is 0, the address decrements. A new write cycle can always be initiated by raising CS to a high level and then lowering it to a low level.

To prevent confusion and ensure consistency between circuits, after the address phase the chip tests the first nibble (4 bits) and ignores the second nibble. This test is performed independently of the LSB-first bit and ensures there are extra clock cycles after the soft-reset bits (Register 0x000, Bit 0 and Bit 7). The first-nibble test applies only when writing Register 0x000.

The SPI read/write operation timing is shown in Figure 18. For both read and write operations, the instruction cycle writes information triggered on clock rising edges; in a write operation the communication cycle writes input data on clock rising edges, and in a read operation the communication cycle updates output data on clock falling edges.

中文： 串行端口可以支持 MSB first 和 LSB first 数据格式。该功能由 LSB first（寄存器 0x000，位 6 和位 1）控制。默认为 MSB first（LSB first 位=0）格式。

当 LSB first =0（MSB first）时，指令和数据位必须从 MSB 写到 LSB。R/W 后面接 A[14:0]为指令字，D[7:0]为数据字。

当 LSB first =1（LSB first）时，指令和数据位必须从 LSB 写到 MSB。A[0:14]后面是 R/W，随后是 D[0:7]。

SPI 支持 3 线制或 4 线制接口。当 SDO 有效位=1（寄存器 0x000、位 4 和位 3）时，使用输入引脚（SDIO）和输出引脚（SDO）的 4 线接口。当 SDO 有效位=0 时，SDO 引脚未被使用，SDIO 引脚用于输入和输出。

将 CS 引脚保持低电平可支持多字节数据传输。指令周期后的前 8 个 SCLK 从指令周期中提供的寄存器中读/写。每增加 8 个 SCLK 周期，地址就会递增或递减，在新的寄存器上进行读/写。地址的变化方向可以使用 ADDRINC 或 ADDRINC_M（寄存器 0x000，位 5 和位 2）来设置。当 ADDRINC 或 ADDRINC_M 为 1 时，多周期地址递增。当 ADDRINC 或 ADDRINC_M 为 0 时，地址递减。一个新的写入周期总是可以通过使 CS 升到高电平，然后再降到低电平来启动。

为了防止混淆并确保电路之间的一致性，芯片在地址阶段后测试第一个半字节（4bit），忽略第二个半字节。这个测试与 LSB first 位独立完成，并确保在软复位（soft reset）位（寄存器 0x000、位 0 和位 7）之后有额外的时钟周期。第一个半字节测试仅在写入寄存器 0x000 时才适用。

SPI 读/写操作时序如图 18 所示，无论读操作还是写操作，指令周期都是时钟上升沿触发写入信息，写操作时通信周期在时钟上升沿写入输入数据，读操作时通信周期在时钟下降沿更新输出数据。

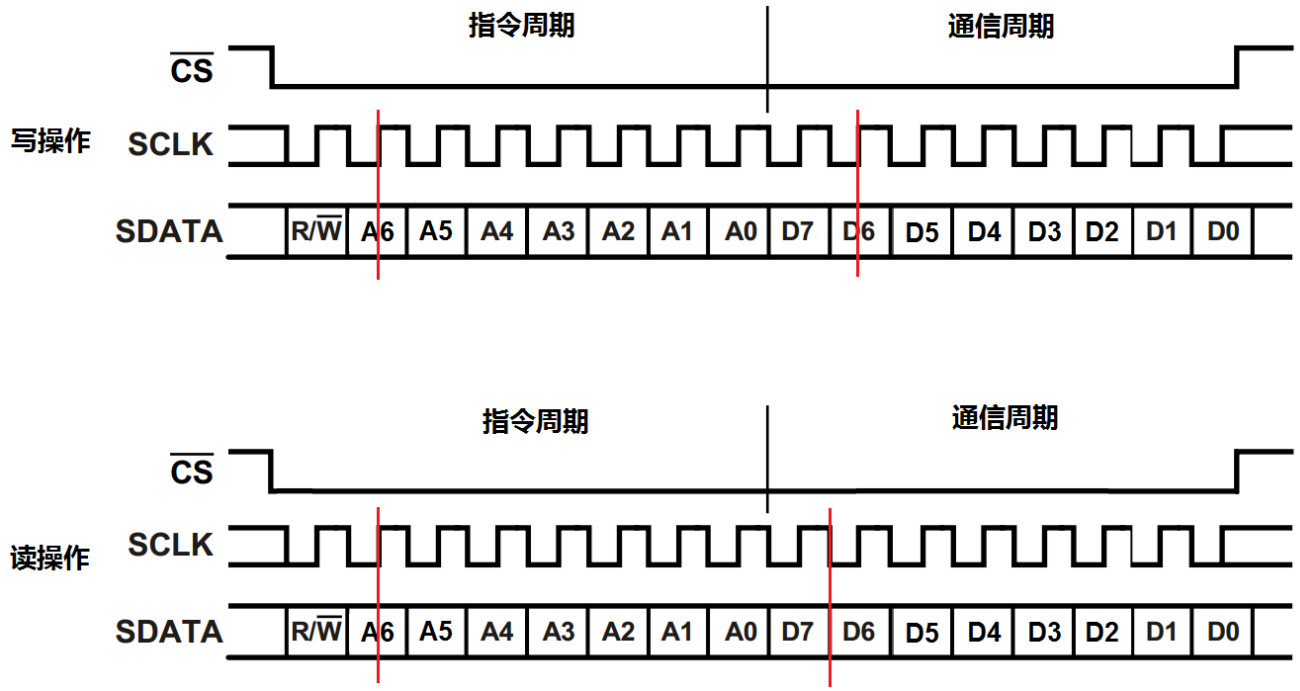


Figure 18: SPI read/write operation timing diagram

2、JESD204B 串行数据接口 / 2. JESD204B Serial Data Interface

2.1 JESD204B 概述 / 2.1 JESD204B Overview

English: The SXD052 has eight JESD204B SERDES data ports for receiving the input sample data of the device. These eight JESD204B ports can be combined into one (single-link) or two (dual-link) identical JESD204B links. Each link can feed its own datapaths with its own channelizers.

Both single-link and dual-link JESD204B modes align their respective (local) clocks to the same system reference (SYSREF±) and device clock (CLKIN±) signals. However, the SYNCOUT0̄± and SYNCOUT1̄±

signals are per JESD204B link, and in dual-link mode the two links can operate independently of each other.

The JESD204B serial interface is divided into three layers: the physical layer, the data link layer and the transport layer. Figure 19 shows the three communication layers implemented in the SXD052 serial data interface, which recover the clock and perform deserialization, descrambling and deframing before the data is sent to each digital signal processing channelizer of the device.

The communication layers are described as follows: - The physical layer establishes a reliable channel between the transmitter and the receiver. - The data link layer is responsible for splitting data into octets and descrambling the data. - The transport layer receives the descrambled JESD204B frames and converts them into DAC samples.

In the following sections, each layer is described in detail, including information on configuring each aspect of the interface.

Some JESD204B parameters (L, F, K, M, N, NP, S, HD) define how the data is packed and tell the device how to turn the serial data into samples. These parameters are described in detail in the transport layer section. The SXD052 also has a descrambler option (see the descrambler section for more information). To increase the maximum data rate achievable by the SERDES interface, the SXD052 can use a 12-bit packing mode (NP=12, N=11 or 12) for applications that do not require 16-bit data.

The SXD052 has multiple JESD204B modes, including single-link and dual-link modes, and the chip can be configured according to requirements such as the number of channels, the number of DAC cores and the link speed. See Table 3 and Table 4 for these modes and their respective JESD204B link parameters. The specific combination of channel interpolation and main datapath interpolation depends on the operating mode. Table 1 lists all link and interpolation combinations and the maximum data rate supported by each mode.

The SXD052 has two DAC cores, each with its own analog output. Each DAC core is fed by three complex channelizers. The effective number of converters of a JESD204B link is the number of non-complex channels in a given operating mode, expressed by the M parameter of the JESD204B standard. Thus M=1 denotes a single non-complex channel, M=2 denotes one complex channel, a set of two complex channels is expressed as M=4, and so on. When the total datapath interpolation is set to 1×, the complex channels are bypassed and the data input is assumed to be real. Only in this case does M=2 represent the actual number of DAC cores, with no complex data required.

For a specific JESD204B operating mode, the following relationships hold: - Total interpolation = channel interpolation × main interpolation - Data rate = DAC rate / total interpolation - Lane rate = (M/L) × NP × (10/8) × data rate

where the lane rate must be between 3 Gbps and 15.4 Gbps. M, L and NP are the JESD204B link parameters of the selected JESD204B operating mode.

Achieving and maintaining synchronization between the JESD204B transmitter and the JESD204B receiver is essential to maintaining link reliability. After the link is established, the stability and phase relationship between the different system clocks become important. If a particular clock slips relative to the common reference, the link may be lost and need to be re-established. Likewise, if a particular lane is out of sync with the other lanes within the link, the link may also be lost. To simplify the process of establishing and

re-establishing the link, the SXD052 designates an independent master synchronization signal for each JESD204B link. The SYNCOUTx± pins serve as the master flag signals for all lanes in a specific link. If the data received on the lanes is not synchronized, the SYNCOUTx± pin is deasserted, the transmitter stops sending data and begins sending synchronization characters to all lanes in that link until resynchronization between lanes is achieved.

中文： SXD052 有八个 JESD204B SERDES 数据端口，用于接收器件的输入采样数据。这八个 JESD204B 端口可以组合成一个（单链路）或两个（双链路）相同的 JESD204B 链路。每条链路都可以用自己的信道器为自己的数据路径提供数据。

单链路和双链路 JESD204B 模式都将各自的（本地）时钟与相同的系统基准（SYSREF±）和器件时钟（CLKIN±）信号对齐。然而，SYNCOUT0±和 SYNCOUT1±信号是针对各自 JESD204B 链路的，在双链路模式下，两个链路可以相互独立运行。

JESD204B 串行接口被分为三层：分别是物理层、数据链路层和传输层。图 19 显示了在 SXD052 串行数据接口中实现的三个通信层，以便在将数据发送到设备的每个数字信号处理信道器之前恢复时钟并进行反序列化、解扰和解帧。

通信层的描述如下： - 物理层在发射器和接收器之间建立了一个可靠的通道。 - 数据链路层负责将数据拆分成八位字，并对数据进行解扰。 - 传输层接收解扰的 JESD204B 帧并将其转换为 DAC 样本。

在随后的章节中，将对每一层进行详细描述，包括配置接口各个方面的信息。

一些 JESD204B 参数（L、F、K、M、N、NP、S、HD）定义了数据的打包方式，并告诉设备如何将串行数据变成样本。这些参数在传输层部分有详细描述。SXD052 还有一个解扰选项（更多信息见解扰器部分）。为了提高 SERDES 接口可实现的最大数据速率，SXD052 能够为不需要 16 位数据的应用使用 12 位打包模式（NP=12，N=11 或 12）。

SXD052 具有多种 JESD204B 模式，包括单链路和双链路模式，并可以根据通道数量、DAC 核数量和链路速度等各方面的要求，对芯片进行配置。这些模式及其各自的 JESD204B 链路参数参见表 3 和表 4。通道插值和主数据路径插值的具体组合取决于运行模式。表 1 列出了所有的链路和插值组合，以及每种模式支持的最大数据速率。

SXD052 有两个 DAC 内核，每个都有自己的模拟输出。每个 DAC 内核由三个复数信号器提供数据。JESD204B 链路的有效转换器数量为给定工作模式下的非复数通道数量，用 JESD204B 标准的 M 参数表示。因此，用 M=1 表示单个非复数通道，M=2 表示一个复数通道，一组两个复数通道用 M=4 表示，以此类推。当总数据路径插值设置为 1×时，将复数通道旁路，数据输入被假定为实数。仅在这种情况下，M=2 代表 DAC 核的实际数量，无需复数数据。

对于一个特定的 JESD204B 工作模式，存在以下关系： 总插值=通道插值×主内插值 数据速率=DAC 速率/总插值 通道速率=（M/L）×NP×（10/8）×数据速率 其中，通道速率必须在 3Gbps 和 15.4Gbps 之间。M、L 和 NP 是所选的 JESD204B 工作模式下的 JESD204B 链路参数。

在 JESD204B 发射器和 JESD204B 接收器之间实现并保持同步，对于维持链路的可靠性至关重要。链路建立后，不同系统时钟之间的稳定性和相位关系变得很重要。如果某个特定的时钟相对于共同的基准出现了滑动，链路可能会丢失，并需要重新建立。同样，如果一个特定的通道与链路内的其他通道不同步，此链路也可能会丢失。为了简化建立与重建链路的过程，SXD052 为每个 JESD204B 链路指定了一个独立的主同步信号。SYNCOUTx± 引脚被用作特定链路中所有通道的主标志信号。如果各通道接收到的数据不同步，SYNCOUTx± 引脚将被解除，发射器停止发送数据，并开始向该链路中的所有通道发送同步字符，直到实现通道间的重新同步。

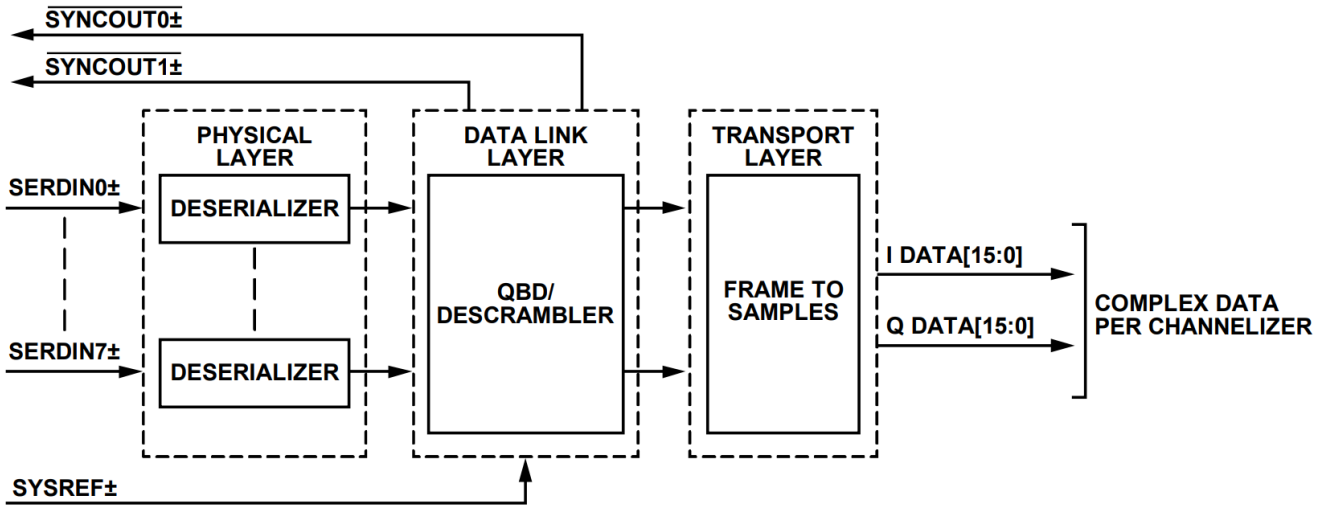


Figure 52. Functional Block Diagram of Serial Link Receiver

Figure 19: Serial link receiver functional block diagram

表 3 单链路 JESD204B 工作模式 / Table 3. Single-Link JESD204B Operating Modes

参数 / Parameter	0	1	2	3	4	5	6	7	8	9	10	11	12	18	19	20	21	22
L（通道数 / lanes）	1	2	3	2	4	1	2	1	4	4	8	8	8	4	4	8	8	4
M（转换器数量 / converters）	2	4	6	2	4	2	4	4	2	2	2	2	2	1	1	1	1	2
F（每通道每帧八位字 / octets per frame per lane）	4	4	4	2	2	3	3	8	1	2	1	2	3	1	2	1	2	3
S（每帧转换器的采样数 / samples per frame per converter）	1	1	1	1	1	1	1	1	1	2	2	4	8	2	4	4	8	4
NP（每个样本的总比特数 / total bits per sample）	16	16	16	16	16	12	12	16	16	16	16	16	12	16	16	16	16	12
N（转换器分辨率 / converter resolution）	16	16	16	16	16	12	12	16	16	16	16	16	12	16	16	16	16	12
K（每个多帧的帧数 / frames per multiframe）	32	32	32	32	32	32	32	32	32	32	32	32	32	32	32	32	32	32
HD（高密度用户数据格式 / high-density format）	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

表 4 双链路 JESD204B 工作模式 / Table 4. Dual-Link JESD204B Operating Modes

参数 / Parameter	0	1	2	3	4	5	6	7	8	9	18	19	22
L（通道数 / lanes）	1	2	3	2	4	1	2	1	4	4	4	4	4
M（转换器数量 / converters）	2	4	6	2	4	2	4	4	2	2	1	1	2
F（每通道每帧八位字 / octets per frame per lane）	4	4	4	2	2	3	3	8	1	2	1	2	3
S（每帧转换器的采样数 / samples per frame per converter）	1	1	1	1	1	1	1	1	1	2	2	4	4
NP（每个样本的总比特数 / total bits per sample）	16	16	16	16	16	12	12	16	16	16	16	16	12
N（转换器分辨率 / converter resolution）	16	16	16	16	16	12	12	16	16	16	16	16	12
K（每个多帧的帧数 / frames per multiframe）	32	32	32	32	32	32	32	32	32	32	32	32	32

参数 / Parameter	0	1	2	3	4	5	6	7	8	9	18	19	22
HD（高密度用户数据格式 / high-density format）	1	1	1	1	1	1	1	1	1	1	1	1	1

表 5 F=1 JESD204B 工作模式的每通道的数据结构[1] / Table 5. Per-Lane Data Structure for F=1 JESD204B Modes[1]

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	帧 0，八位字 0 / Frame 0, Octet 0	帧 1，八位字 0 / Frame 1, Octet 0
模式 8（L=4，M=2，S=1，NP=16，N=16）/ Mode 8	通道 0 / Lane 0	M0S0[15:8]	M0S1[15:8]
	通道 1 / Lane 1	M0S0[7:0]	M0S1[7:0]
	通道 2 / Lane 2	M1S0[15:8]	M1S1[15:8]
	通道 3 / Lane 3	M1S0[7:0]	M1S1[7:0]
模式 10（L=8，M=2，S=2，NP=16，N=16）/ Mode 10	通道 0 / Lane 0	M0S0[15:8]	M0S2[15:8]
	通道 1 / Lane 1	M0S0[7:0]	M0S2[7:0]
	通道 2 / Lane 2	M0S1[15:8]	M0S3[15:8]
	通道 3 / Lane 3	M0S1[7:0] M1S0[15:8]	M0S3[7:0] M1S2[15:8]
	通道 4 / Lane 4	M1S0[7:0] M1S1[15:8]	M1S2[7:0] M1S3[15:8]
	通道 5 / Lane 5	M1S0[7:0]	M1S3[7:0]
	通道 6 / Lane 6		
	通道 7 / Lane 7		
模式 18（L=4，M=1，S=2，NP=16，N=16）/ Mode 18	通道 0 / Lane 0	M0S0[15:8]	M0S2[15:8]
	通道 1 / Lane 1	M0S0[7:0]	M0S2[7:0]
	通道 2 / Lane 2	M0S1[15:8]	M0S3[15:8]
	通道 3 / Lane 3	M0S1[7:0]	M0S3[7:0]
模式 20（L=8，M=1，S=4，NP=16，N=16）/ Mode 20	通道 0 / Lane 0	M0S0[15:8]	M0S4[15:8]
	通道 1 / Lane 1	M0S0[7:0]	M0S4[7:0]
	通道 2 / Lane 2	M0S1[15:8]	M0S5[15:8]
	通道 3 / Lane 3	M0S1[7:0] M0S2[15:8]	M0S5[7:0] M0S6[15:8]
	通道 4 / Lane 4	M0S2[7:0] M0S3[15:8]	M0S6[7:0] M0S7[15:8]
	通道 5 / Lane 5	M0S3[7:0]	M0S7[7:0]
	通道 6 / Lane 6		
	通道 7 / Lane 7		

[1] Mx 是转换器编号，Sy 是样品编号。例如，M0S0 表示转换器 0，样本 0。/ Mx is the converter number and Sy is the sample number. For example, M0S0 denotes converter 0, sample 0.

表 6 F=2 JESD204B 工作模式的每条通道的数据结构[1] / Table 6. Per-Lane Data Structure for F=2 JESD204B Modes[1]

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	帧 0，八位字 0 / Frame 0, Octet 0	帧 0，八位字 1 / Frame 0, Octet 1	帧 1，八位字 0 / Frame 1, Octet 0	帧 1，八位字 1 / Frame 1, Octet 1 [原件表头作"八位字 2"，按序列校正并标注 / source header reads "Octet 2"; corrected per sequence]
模式 3（L=2，M=2，S=1，NP=16，N=16）/ Mode 3	通道 0 / Lane 0	M0S0[15:8]	M0S0[7:0]	M0S1[15:8]	M0S1[7:0]
	通道 1 / Lane 1	M1S0[15:8]	M1S0[7:0]	M1S1[15:8]	M1S1[7:0]
模式 4（L=4，M=4，S=1，NP=16，N=16）/ Mode 4	通道 0 / Lane 0	M0S0[15:8]	M0S0[7:0]	M0S1[15:8]	M0S1[7:0]
	通道 1 / Lane 1	M1S0[15:8]	M1S0[7:0]	M1S1[15:8]	M1S1[7:0]
	通道 2 / Lane 2	M2S0[15:8]	M2S0[7:0]	M2S1[15:8]	M2S1[7:0]
	通道 3 / Lane 3	M3S0[15:8]	M3S0[7:0]	M3S1[15:8]	M3S1[7:0]
模式 9（L=4，M=2，S=2，NP=16，N=16）/ Mode 9	通道 0 / Lane 0	M0S0[15:8]	M0S0[7:0]	M0S2[15:8]	M0S2[7:0]
	通道 1 / Lane 1	M0S1[15:8]	M0S1[7:0]	M0S3[15:8]	M0S3[7:0]
	通道 2 / Lane 2	M1S0[15:8]	M1S0[7:0]	M1S2[15:8]	M1S2[7:0]
	通道 3 / Lane 3	M1S1[15:8]	M1S1[7:0]	M1S3[15:8]	M1S3[7:0]
模式 11（L=8，M=2，S=4，NP=16，N=16）/ Mode 11	通道 0 / Lane 0	M0S0[15:8]	M0S0[7:0]	M0S4[15:8]	M0S4[7:0]
	通道 1 / Lane 1	M0S1[15:8]	M0S1[7:0]	M0S5[15:8]	M0S5[7:0]
	通道 2 / Lane 2	M0S2[15:8]	M0S2[7:0]	M0S6[15:8]	M0S6[7:0]
	通道 3 / Lane 3	M0S3[15:8]	M0S3[7:0]	M0S7[15:8]	M0S7[7:0]
	通道 4 / Lane 4	M1S0[15:8]	M1S0[7:0]	M1S4[15:8]	M1S4[7:0]
	通道 5 / Lane 5	M1S1[15:8]	M1S1[7:0]	M1S5[15:8]	M1S5[7:0]
	通道 6 / Lane 6	M1S2[15:8]	M1S2[7:0]	M1S6[15:8]	M1S6[7:0]
		M1S3[15:8]	M1S3[7:0]	M1S7[15:8]	M1S7[7:0]

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	帧 0，八位字 0 / Frame 0, Octet 0	帧 0，八位字 1 / Frame 0, Octet 1	帧 1，八位字 0 / Frame 1, Octet 0	帧 1，八位字 1 / Frame 1, Octet 1 [原件表头作"八位字 2"，按序列校正并标注 / source header reads "Octet 2"; corrected per sequence]
	通道 7 / Lane 7				
模式 19（L=4，M=1，S=4，NP=16，N=16）/ Mode 19	通道 0 / Lane 0	M0S0[15:8]	M0S0[7:0]	M0S4[15:8]	M0S4[7:0]
	通道 1 / Lane 1	M0S1[15:8]	M0S1[7:0]	M0S5[15:8]	M0S5[7:0]
	通道 2 / Lane 2	M0S2[15:8]	M0S2[7:0]	M0S6[15:8]	M0S6[7:0]
	通道 3 / Lane 3	M0S3[15:8]	M0S3[7:0]	M0S7[15:8]	M0S7[7:0]
模式 21（L=8，M=1，S=8，NP=16，N=16）/ Mode 21	通道 0 / Lane 0	M0S0[15:8]	M0S0[7:0]	M0S8[15:8]	M0S8[7:0]
	通道 1 / Lane 1	M0S1[15:8]	M0S1[7:0]	M0S9[15:8]	M0S9[7:0]
	通道 2 / Lane 2	M0S2[15:8]	M0S2[7:0]	M0S10[15:8]	M0S10[7:0]
	通道 3 / Lane 3	M0S3[15:8]	M0S3[7:0]	M0S11[15:8]	M0S11[7:0]
	通道 4 / Lane 4	M0S4[15:8]	M0S4[7:0]	M0S12[15:8]	M0S12[7:0]
	通道 5 / Lane 5	M0S5[15:8]	M0S5[7:0]	M0S13[15:8]	M0S13[7:0]
	通道 6 / Lane 6	M0S6[15:8]	M0S6[7:0]	M0S14[15:8]	M0S14[7:0]
	通道 7 / Lane 7	M0S7[15:8]	M0S7[7:0]	M0S15[15:8]	M0S15[7:0]

[1] Mx 是转换器编号，Sy 是样品编号。例如，M0S0 表示转换器 0，样本 0。/ Mx is the converter number and Sy is the sample number. For example, M0S0 denotes converter 0, sample 0.

表 7 F=3 JESD204B 工作模式的每条通道的数据结构[1] / Table 7. Per-Lane Data Structure for F=3 JESD204B Modes[1]

帧 0 / Frame 0：八位字 0（半字节 0 / 半字节 1）、八位字 1（半字节 0 / 半字节 1）、八位字 2（半字节 0 / 半字节 1），共 6 个半字节列 / six nibble columns.

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	半字节序列 / Nibble Sequence (Octet 0 N0, N1; Octet 1 N0, N1; Octet 2 N0, N1)
模式 5（L=1，M=2，S=1，NP=12，N=12）/ Mode 5	通道 0 / Lane 0	M0S0[11:8], M0S0[7:4], M0S0[3:0], M1S0[11:8], M1S0[7:4], M1S0[3:0]

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	半字节序列 / Nibble Sequence (Octet 0 N0, N1; Octet 1 N0, N1; Octet 2 N0, N1)
模式 6（L=2，M=4，S=1，NP=12，N=12）/ Mode 6	通道 0 / Lane 0	M0S0[11:8], M0S0[7:4], M0S0[3:0], M1S0[11:8], M1S0[7:4], M1S0[3:0]
	通道 1 / Lane 1	M2S0[11:8], M2S0[7:4], M2S0[3:0], M3S0[11:8], M3S0[7:4], M3S0[3:0]
模式 22（L=4，M=2，S=4，NP=12，N=12）/ Mode 22	通道 0 / Lane 0	M0S0[11:8], M0S0[7:4], M0S0[3:0], M0S1[11:8], M0S1[7:4], M0S1[3:0]
	通道 1 / Lane 1	M0S2[11:8], M0S2[7:4], M0S2[3:0], M0S3[11:8], M0S3[7:4], M0S3[3:0]
	通道 2 / Lane 2	M1S0[11:8], M1S0[7:4], M1S0[3:0], M1S1[11:8], M1S1[7:4], M1S1[3:0]
	通道 3 / Lane 3	M1S2[11:8], M1S2[7:4], M1S2[3:0], M1S3[11:8], M1S3[7:4], M1S3[3:0]
模式 12（L=8，M=2，S=8，NP=12，N=12）/ Mode 12	通道 0 / Lane 0	M0S0[11:8], M0S0[7:4], M0S0[3:0], M0S1[11:8], M0S1[7:4], M0S1[3:0]
	通道 1 / Lane 1	M0S2[11:8], M0S2[7:4], M0S2[3:0], M0S3[11:8], M0S3[7:4], M0S3[3:0]
	通道 2 / Lane 2	M0S4[11:8], M0S4[7:4], M0S4[3:0], M0S5[11:8], M0S5[7:4], M0S5[3:0]
	通道 3 / Lane 3	M0S6[11:8], M0S6[7:4], M0S6[3:0], M0S7[11:8], M0S7[7:4], M0S7[3:0]
	通道 4 / Lane 4	M1S0[11:8], M1S0[7:4], M1S0[3:0], M1S1[11:8], M1S1[7:4], M1S1[3:0]
	通道 5 / Lane 5	M1S2[11:8], M1S2[7:4], M1S2[3:0], M1S3[11:8], M1S3[7:4], M1S3[3:0]
	通道 6 / Lane 6	M1S4[11:8], M1S4[7:4], M1S4[3:0], M1S5[11:8], M1S5[7:4], M1S5[3:0]
	通道 7 / Lane 7	M1S6[11:8], M1S6[7:4], M1S6[3:0], M1S7[11:8], M1S7[7:4], M1S7[3:0]

[1] Mx 是转换器编号，Sy 是样品编号。例如，M0S0 表示转换器 0，样本 0。/ Mx is the converter number and Sy is the sample number. For example, M0S0 denotes converter 0, sample 0.

表 8 F=4 JESD204B 工作模式的每条通道的数据结构[1] / Table 8. Per-Lane Data Structure for F=4 JESD204B Modes[1]

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	帧 0 / Frame 0（八位字 0–3 / Octets 0–3）	帧 1 / Frame 1（八位字 0–3 / Octets 0–3）
模式 0（L=1，M=2，S=1，NP=16，N=16）/ Mode 0	通道 0 / Lane 0	M0S0[15:8], M0S0[7:0], M1S0[15:8], M1S0[7:0]	M0S1[15:8], M0S1[7:0], M1S1[15:8], M1S1[7:0]
模式 1（L=2，M=4，S=1，NP=16，N=16）/ Mode 1	通道 0 / Lane 0	M0S0[15:8], M0S0[7:0], M1S0[15:8], M1S0[7:0]	M0S1[15:8], M0S1[7:0], M1S1[15:8], M1S1[7:0]
	通道 1 / Lane 1	M2S0[15:8], M2S0[7:0], M3S0[15:8], M3S0[7:0]	M2S1[15:8], M2S1[7:0], M3S1[15:8], M3S1[7:0]
	通道 0 / Lane 0		

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	帧 0 / Frame 0（八位字 0–3 / Octets 0–3）	帧 1 / Frame 1（八位字 0–3 / Octets 0–3）
模式 2（L=3，M=6，S=1，NP=16，N=16）/ Mode 2		M0S0[15:8], M0S0[7:0], M1S0[15:8], M1S0[7:0]	M0S1[15:8], M0S1[7:0], M1S1[15:8], M1S1[7:0]
	通道 1 / Lane 1	M2S0[15:8], M2S0[7:0], M3S0[15:8], M3S0[7:0]	M2S1[15:8], M2S1[7:0], M3S1[15:8], M3S1[7:0]
	通道 2 / Lane 2	M4S0[15:8], M4S0[7:0], M5S0[15:8], M5S0[7:0]	M4S1[15:8], M4S1[7:0], M5S1[15:8], M5S1[7:0]

[1] Mx 是转换器编号，Sy 是样品编号。例如，M0S0 表示转换器 0，样本 0。/ Mx is the converter number and Sy is the sample number. For example, M0S0 denotes converter 0, sample 0.

表 9 F=8 JESD204B 工作模式的每条通道的数据结构[1] / Table 9. Per-Lane Data Structure for F=8 JESD204B Modes[1]

JESD204B 模式和参数 / Mode and Parameters	链路逻辑通道 / Logical Lane	帧 0 / Frame 0（八位字 0–7 / Octets 0–7）
模式 7（L=1，M=4，S=1，NP=16，N=16）/ Mode 7	通道 0 / Lane 0	M0S0[15:8], M0S0[7:0], M1S0[15:8], M1S0[7:0], M2S0[15:8], M2S0[7:0], M3S0[15:8], M3S0[7:0]

[1] Mx 是转换器编号，Sy 是样品编号。例如，M0S0 表示转换器 0，样本 0。/ Mx is the converter number and Sy is the sample number. For example, M0S0 denotes converter 0, sample 0.

2.2 物理层 / 2.2 Physical Layer

English: The physical layer of the JESD204B interface (hereafter called the deserializer) has eight identical lanes. Each lane consists of termination, an equalizer, clock and data recovery (CDR) circuitry, and a 1:40 demultiplexer functional block (see Figure 20).

Per the JESD204B specification, JESD204B data is input to the SXD052 through the SERDINx± differential input pins.

中文： JESD204B 接口的物理层（以下称为解串器），有八个相同的通道。每个通道由终端、均衡器、时钟和数据恢复（CDR）电路以及 1:40 解复用功能模块组成（见图 20）。

根据 JESD204B 规范，JESD204B 数据通过 SERDINx±差分输入引脚输入到 SXD052。

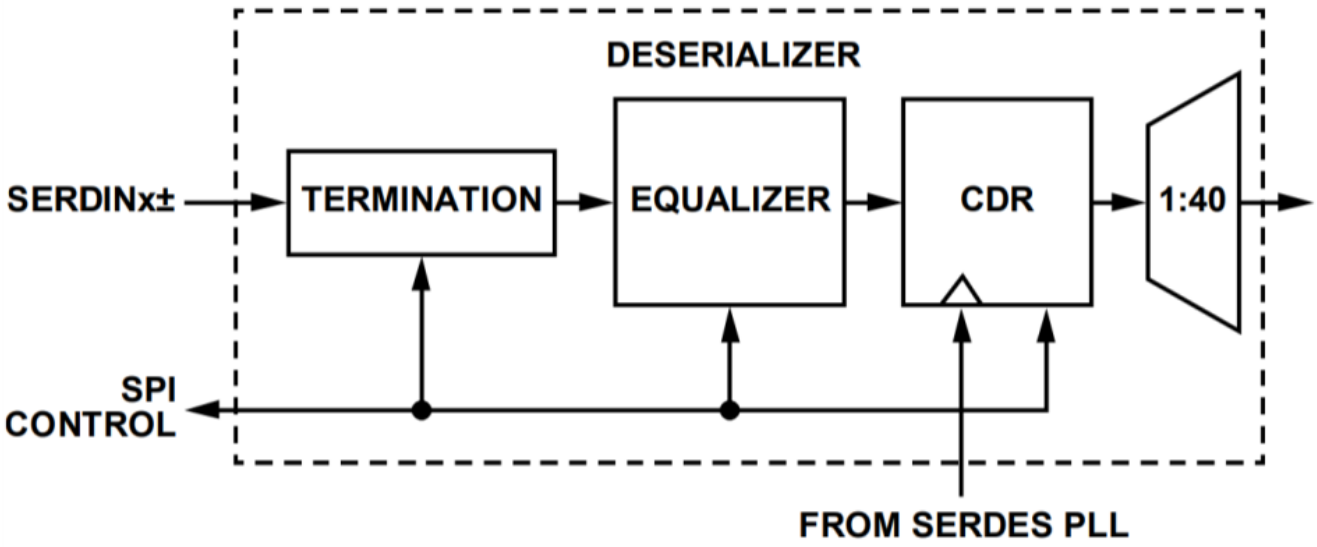


Figure 20: Deserializer block diagram

2.2.1 接口上电和输入端 / 2.2.1 Interface Power-Up and Inputs

English: Before using the JESD204B interface, Register 0x200 Bit 0 must be set to 0 to start it. In addition, the power to each unused physical lane (PHY) (SERDINx±) must be turned off. Therefore, if a physical lane is in use, set the corresponding bit representing physical lane x in Register 0x201 to 0; if not in use, set it to 1.

The SXD052 automatically calibrates the input termination to 100 Ω at DC. This calibration procedure executes automatically when the JESD204B interface block is configured and requires no additional SPI register writes.

中文： 在使用 JESD204B 接口之前，必须设置寄存器 0x200 的 Bit0=0 来启动它。此外，必须关闭未使用的（SERDINx±）每个物理通道（PHY）的电源。因此，如果正在使用物理通道，需将寄存器 0x201 中代表物理通道 x 的相应 Bit 设置为 0，如果不使用则设置为 1。

SXD052 在直流时将输入终端自动校准为 100Ω。该校准程序在配置 JESD204B 接口模块时自动执行，不需要任何额外的 SPI 寄存器写入。

2.2.2 接收器眼图模板 / 2.2.2 Receiver Eye Mask

English: The SXD052 complies with the JESD204B specification for the receiver eye mask and is able to capture mask data as shown in Figure 21. Figure 21 shows the receiver eye diagram normalized to the data-rate interval. The SXD052 also supports increased insertion-loss limits, defined in the equalization section.

中文： SXD052 兼容 JESD204B 关于接收器眼图模板的规范，能够捕获如图 21 所示的模板数据。图 21 显示了归一化为数据速率区间的接收器眼图。SXD052 还支持增加插入损耗限制，具体定义见均衡部分。

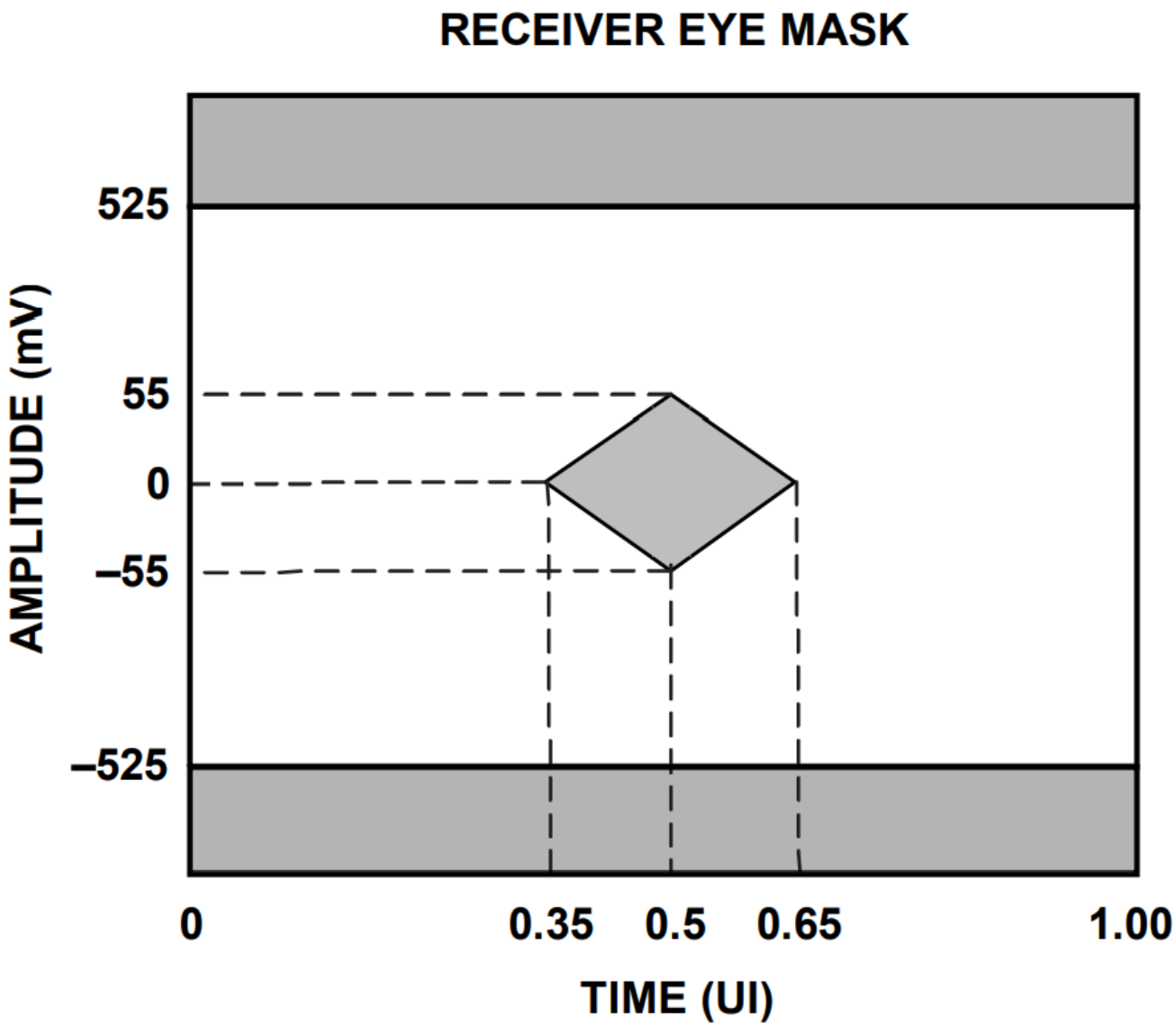


Figure 21: Receiver eye mask

2.2.3 时钟关系 / 2.2.3 Clock Relationships

English: The following clock rates are also used in the JESD204B interface. The relationship between any clocks can be derived from the following formulas: - Data rate = DAC rate / total interpolation - Lane rate = (M/L) × NP × (10/8) × data rate - Byte rate = lane rate / 10

The above relationships come from 8-bit/10-bit encoding, i.e. each byte is represented by 10 bits. - PCLK rate = byte rate / 4 = lane rate / 40

The processing clock is used by the four-byte decoder. - Frame rate = byte rate / F, where F is defined as octets/frame/lane. - PCLK factor = frame rate / PCLK rate = 4/F

where: - M is the JESD204B parameter for the number of converters per link; it is the effective number of converters seen by the JESD204B interface (not necessarily equal to the number of DAC cores). - L is the JESD204B parameter representing the lanes per link. - F is the JESD204B parameter representing the octets per frame per lane. - NP is the JESD204B parameter representing the total number of bits per sample.

中文： 在 JESD204B 接口中还使用了以下的时钟速率。任何一个时钟之间的关系都可以从以下公式中得出。 数据速率=DAC 速率/总插值 通道速率=（M/L）×NP×（10/8）×数据速率 字节速率=通道速率/10 上述关系式来自于 8 位/10 位编码方式，即每个字节由 10 位表示。 PCLK 速率=字节速率/4=通道速率/40 处理时钟用于四字节解码器。 帧率=字节速率/F 其中 F 定义为八位字/帧/通道。 PCLK 系数=帧率/PCLK 速率=4/F 其中： M 是每条链路转换器的 JESD204B 参数，它是 JESD204B 接口看到的有效转换器数量（不一定等于 DAC 核的数量）。 L 是 JESD204B 参数，代表每条链路的通道。 F 是 JESD204B 参数，代表每通道每帧的八位字。 NP 是 JESD204B 参数，代表每个样本的总位数。

2.3 SERDES PLL / 2.3 SERDES PLL

2.3.1 SERDES PLL 的功能概述 / 2.3.1 SERDES PLL Functional Overview

English: The independent SERDES PLL uses integer-N technology to implement clock synthesis. The entire SERDES PLL is integrated on chip, including the VCO and the loop filter. The SERDES PLL can provide quadrature clocks to achieve gapless coverage of a wide data-rate range (3 Gbps to 15.4 Gbps). These clocks are the inputs to the CDR block, described in the clock and data recovery section.

The reference clock of the SERDES PLL runs at frequency fREF, which equals 1/40 of the lane rate (PCLK rate). For the SERDES circuit setup and the related register writes, see the Start-Up Sequence section. The SERDES PLL block automatically adjusts to the corresponding lane-rate divider range according to the SERDES mode in use. Using the DAC clock generated by the DAC PLL or the clock directly from the CLKIN± pins, it divides the DAC clock frequency by 4 and, according to the JESD204B parameters corresponding to the mode and interpolation stored in Register 0x110 and Register 0x111, determines the divider suitable for generating the PCLK frequency (lane rate ÷ 40), as shown in Figure 22.

Confirm whether the SERDES PLL is operating by reading Register 0x281. If Bit 0 of Register 0x281 = 1, the SERDES PLL is locked.

中文： 独立的 SERDES PLL 使用整数 N 技术来实现时钟合成。整个 SERDES PLL 被集成在芯片上，包括 VCO 和环路滤波器。SERDES PLL 能够提供正交时钟，以实现无间隙的宽范围数据速率（3 Gbps 至 15.4 Gbps）。这些时钟是 CDR 模块的输入，在时钟与数据恢复部分有相关描述。

SERDES PLL 的基准时钟以频率 fREF 运行，该频率等于通道速率(PCLK 速率)的 1/40。关于 SERDES 电路的设置和相关寄存器写入，可参见启动顺序部分。SERDES PLL 模块根据正在使用的 SERDES 模式，自动调整到相应的通道速率的分频范围。它采用由 DAC PLL 产生的 DAC 时钟或直接来自 CLKIN±引脚的时钟，将 DAC 时钟频率进行 4 分频，根据寄存器 0x110 和寄存器 0x111 当中存储的模式和插值相对应的 JESD204B 参数，来确定适合产生 PCLK 频率的分频器(通道速率÷40)，如图 22 所示。

通过读取寄存器 0x281 来确认 SERDES PLL 是否工作。如果寄存器 0x281 的 Bit0=1，说明 SERDES PLL 已经锁定。

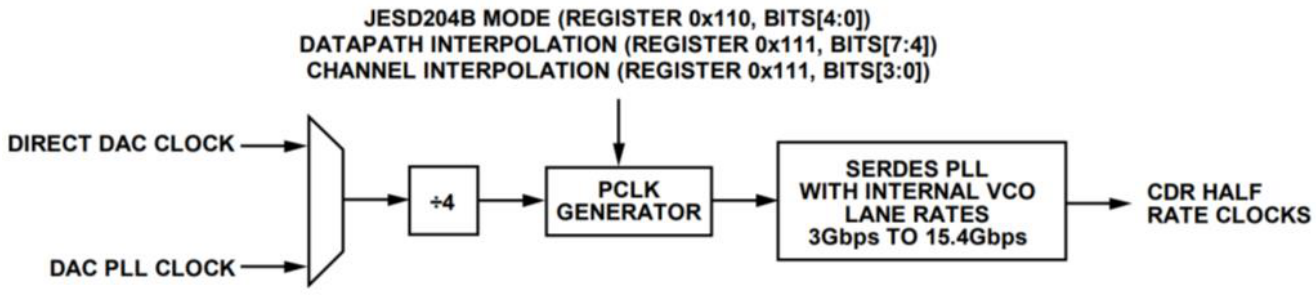


Figure 22: SERDES PLL synthesizer including VCO divider block

2.3.2 时钟和数据恢复 / 2.3.2 Clock and Data Recovery

English: The deserializer is equipped with CDR circuitry. The CDR does not recover the clock from the JESD204B serial lane; instead it recovers the clock from the SERDES PLL. The SERDES PLL in turn uses PCLK as its reference, where PCLK comes from the DAC clock. Therefore, locking the JESD204B transmitter clock to the device clock of the SXD052 is essential.

For the phase used to sample each serial lane's data, the CDR circuit synchronizes it individually. Each serial interface has this independent phase adjustment, which ensures accurate data sampling and simplifies the implementation of multiple serial interfaces on the PCB.

中文： 解串器配备了 CDR 电路。CDR 不是从 JESD204B 串行通道恢复时钟，而是从 SERDES PLL 恢复时钟。SERDES PLL 反过来使用 PCLK 作为其基准，其中 PCLK 来自 DAC 时钟。因此，将 JESD204B 发射器时钟锁定在 SXD052 的器件时钟上至关重要。

对于每个串行通道数据采样所用的相位，CDR 电路对其进行单独同步。每个串行接口都有这种独立相位调整，这确保了准确的数据采样，并简化了 PCB 上多个串行接口的实现。

2.3.3 关闭未使用的 PHY 的电源 / 2.3.3 Powering Down Unused PHYs

English: Any unused but enabled lane consumes extra power. Therefore, the power to each unused lane (SERDINx±) must be turned off by writing 1 to the corresponding bit of PHY_PD (Register 0x201).

中文： 任何未使用，但已使能的通道都会消耗额外的功率。所以，必须通过向 PHY_PD（寄存器 0x201）的相应位写入 1，来关闭每个不使用的通道（SERDINx±）的电源。

2.3.4 均衡化 / 2.3.4 Equalization

English: To compensate for signal-integrity distortion on each PHY lane caused by PCB trace length and impedance, the SXD052 adds an easy-to-use, low-power equalizer on each JESD204B lane. When operating at the maximum lane rate of 15.4 Gbps, the SXD052 equalizer can compensate up to 16 dB of insertion loss. Figure 23 shows the equalizer performance at 15.4 Gbps, close to the maximum baud rate of the SXD052. The lane must also meet the insertion-loss deviation (also called spectral ripple) requirement of the JESD204B specification (less than 1.5 dB from 50 MHz to 0.75× the baud rate).

To ensure the SXD052 can compensate the amount of insertion loss in the system, the equalizer block can be set appropriately. Table 10 shows the register settings for equalizer boost, equalizer gain and feedback control, with specific values depending on the insertion-loss level in the system. Registers 0x240 and 0x241 set the equalizer boost of the PHY lanes (2 bits control one lane). Registers 0x242 and 0x243 set the equalizer gain of the PHY lanes (2 bits control one lane). Registers 0x244 to 0x24B set the feedback control of the PHY lanes (5 bits control one lane; each register is responsible for one control).

Figures 24 and 25 provide points of reference for hardware design, showing the insertion loss of well-laid-out stripline and microstrip transmission lines at different lengths. For specific layout recommendations for JESD204B lanes, see the hardware considerations section.

中文： 为了补偿每个 PHY 通道因 PCB 线路长度和阻抗造成的信号完整性失真，SXD052 在每个 JESD204B 通道上添加了一个易于使用的低功率均衡器。SXD052 均衡器在 15.4 Gbps 的最大通道速率下工作时，可以补偿高达

16 dB 的插入损耗。图 23 显示了 15.4 Gbps 速率下的均衡器性能，接近 SXD052 的最大波特率。该通道还必须满足 JESD204B 规范的插入损耗偏差（也称为频谱纹波）要求（从 50 MHz 到 0.75 倍波特率，小于 1.5 dB）。

为确保 SXD052 能够补偿系统中的插入损耗量，可适当设置均衡器模块。表 10 展示了均衡器提升、均衡器增益和反馈控制的寄存器设置，具体数值取决于系统中的插入损耗水平。寄存器 0x240 和寄存器 0x241 用于设置 PHY 通道的均衡器提升（2Bit 控制一个）。寄存器 0x242 和寄存器 0x243 用于设置 PHY 通道的均衡器增益（2Bit 控制一个）。寄存器 0x244 至寄存器 0x24B 用于设置 PHY 通道的反馈控制（5Bit 控制一个，每个寄存器负责一个控制）。

图 24 和图 25 为硬件设计提供了参考(points of reference)，分别展示了布局良好的带状线和微带传输线，在不同长度下的插入损耗。关于 JESD204B 通道的具体布局建议，可参阅硬件考虑部分。

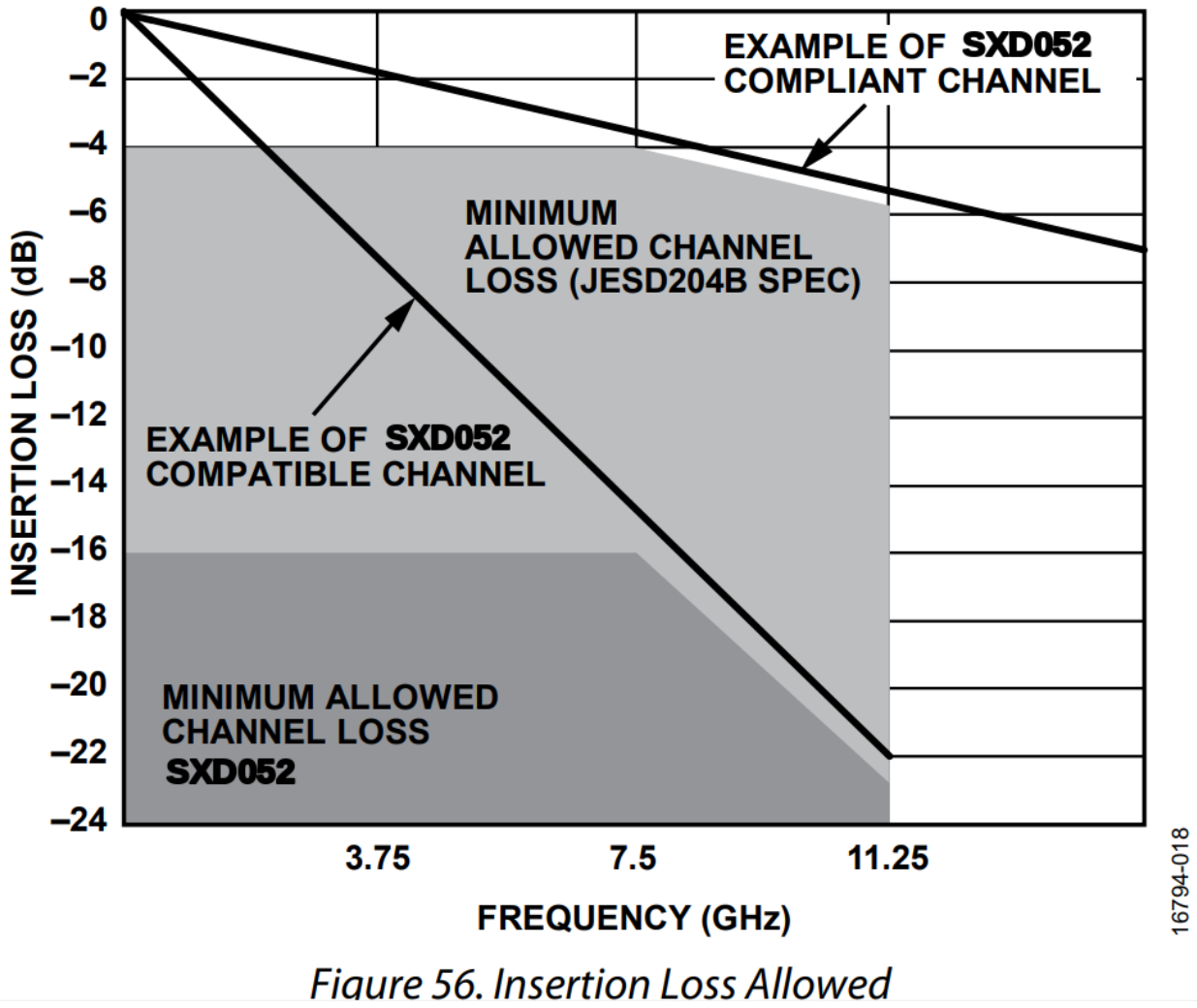


Figure 56. Insertion Loss Allowed

Figure 23: Allowable insertion loss

表 10 每个 PHY 控制的均衡器寄存器控制设置 / Table 10. Equalizer Register Control Settings per PHY

/ Item	插入损耗 / Insertion Loss ≤11dB	插入损耗 / Insertion Loss >11 dB
均衡器提升 / Equalizer boost	0x02	0x03
均衡器增益 / Equalizer gain	0x01	0x03
反馈 / Feedback	0x1F	0x1F

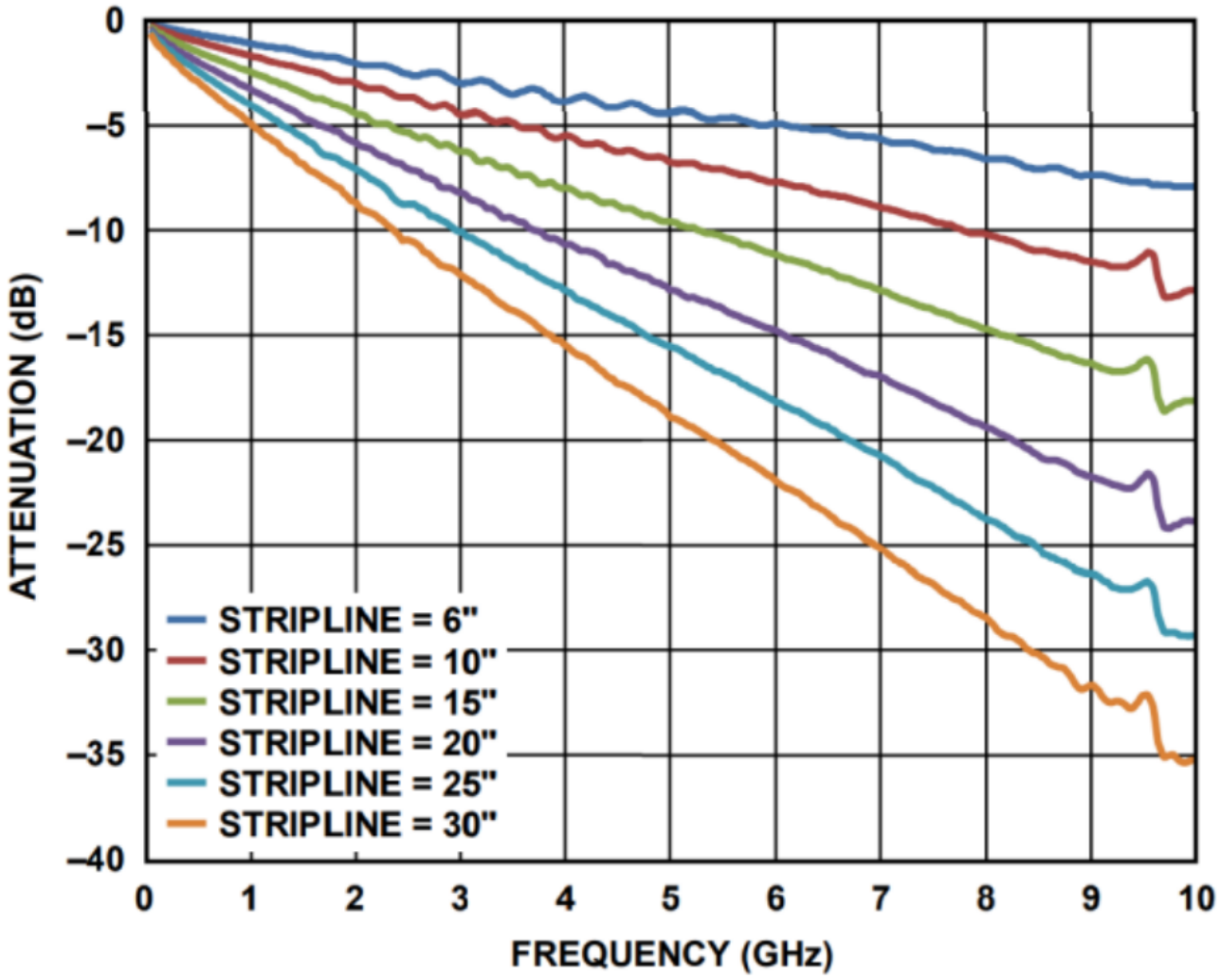


Figure 24: Insertion loss of 50Ω stripline on FR4

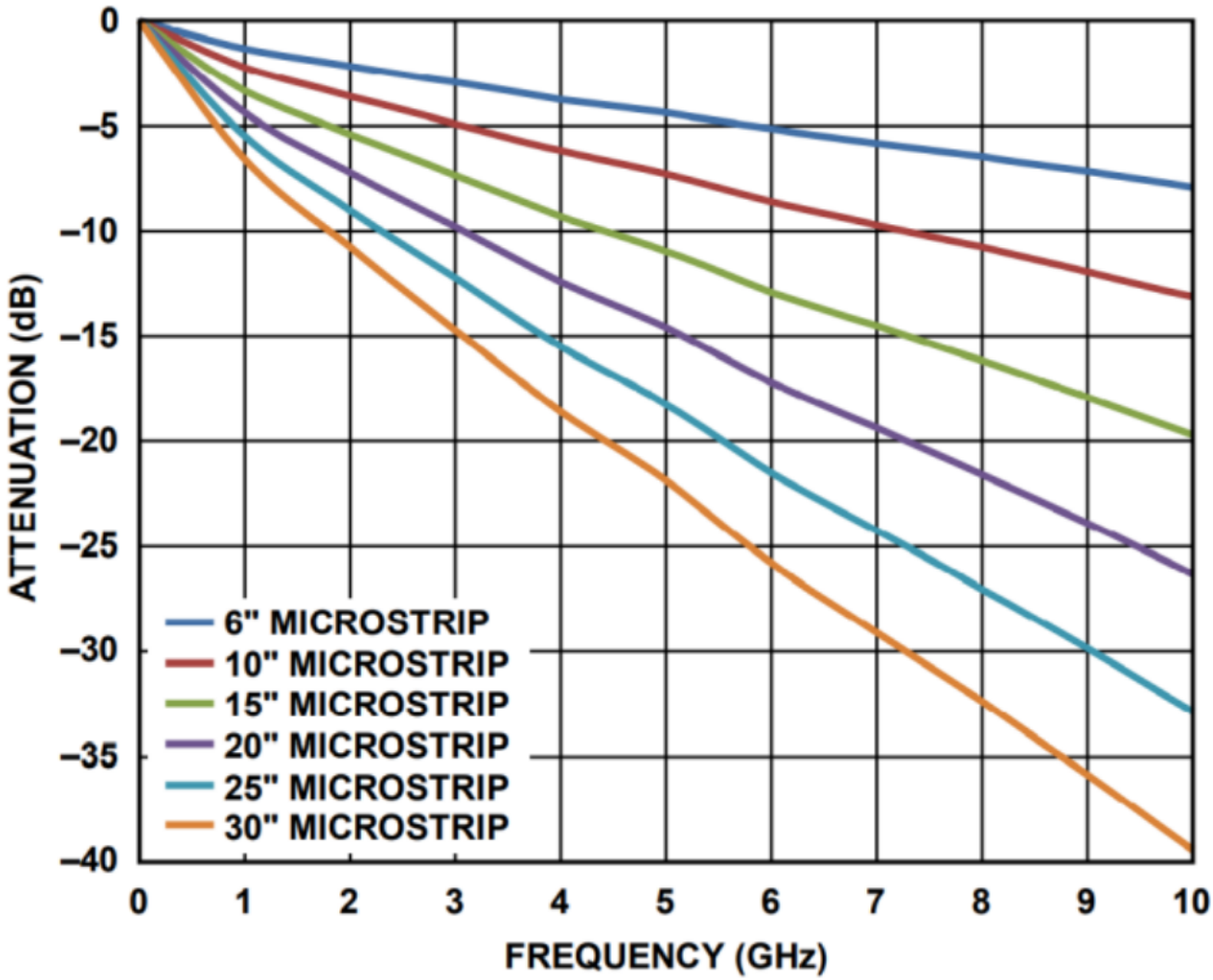


图25　FR4 上 50Ω微带的插入损耗

Figure 25: Insertion loss of 50Ω microstrip on FR4

2.4 数据链路层 / 2.4 Data Link Layer

English: After receiving the deserialized data from the PHY, the data link layer of the SXD052 JESD204B interface deframes and descrambles the data and submits the data octets to the transport layer, where they are recombined into the original data samples before entering the DAC core. The architecture of the data link layer is shown in Figure 26. The data link layer consists of a per-lane synchronization FIFO, a crossbar multiplexer switch, a deframer and a descrambler.

The SXD052 can be set to receive data from a single-link or dual-link high-speed JESD204B serial data interface. When operating in dual-link mode, the data link layer abstracts the interface to the user as two independent JESD204B links, each link occupying up to four lanes. In either mode, all eight lanes of the JESD204B interface can handle link-layer communication such as code group synchronization (CGS), frame alignment and frame synchronization.

The SXD052 decodes 8-bit/10-bit control characters, which mark frame edges and help maintain alignment between serial lanes. Each SXD052 serial interface link can issue a synchronization request by

setting its SYNCOUTx± signal low. The synchronization protocol follows Section 4.9 of the JESD204B standard. When a stream of four consecutive /K/ symbols is received, the SXD052 sets the SYNCOUTx± signal high on the next internal LMFC rising edge, deactivating the synchronization request. The SXD052 then waits for the transmitter to send the initial lane alignment sequence (ILAS). During ILAS, as described in the JESD204B serial link establishment section, all lanes are aligned using /A/-to-/R/ character transitions. The elastic buffer holds data of lanes that arrive earlier until a new lane alignment character arrives. At that time, the buffers of all lanes are released and all lanes complete alignment (see Figure 27).

中文： 接收到来自 PHY 的反序列化数据后，SXD052 JESD204B 接口的数据链路层对该数据进行解帧和解扰，并将数据八位字提交给传输层，在数据进入 DAC 核之前，重新组合成原始数据样本。数据链路层的架构如图 26 所示。数据链路层由每个通道的同步 FIFO、纵横多路式开关、解帧器和解扰器组成。

SXD052 可被设置为从单链路或双链路高速 JESD204B 串行数据接口接收数据。在双链路模式下工作时，数据链路层将接口抽象为两个独立的 JESD204B 链路给用户，每个链路最多占据四个通道。在任一模式下，JESD204B 接口的八个通道都能处理链路层通信，如码组同步（CGS）、帧对齐和帧同步。

SXD052 对 8 位/10 位控制字符进行解码，这些字符标志着帧的边缘，有助于保持串行通道之间的对齐。每个 SXD052 串行接口链路可以通过将其 SYNCOUTx± 信号设置为低电平来发出同步请求。同步协议遵循 JESD204B 标准的第 4.9 节。当收到四个连续的/K/符号流时，SXD052 在下一个内部 LMFC 上升沿将 SYNCOUTx± 信号设置为高电平，从而停用同步请求。然后，SXD052 等待发射器发出初始通道对齐序列（ILAS）。在 ILAS 期间，如 JESD204B 串行链路建立部分所述，所有通道都使用/A/到/R/字符转换进行对齐。弹性缓冲器对先一步到达的通道数据进行保持，直到新的通道对齐字符到达。在这时，释放所有通道的缓冲器，所有通道完成对齐（见图 27）。

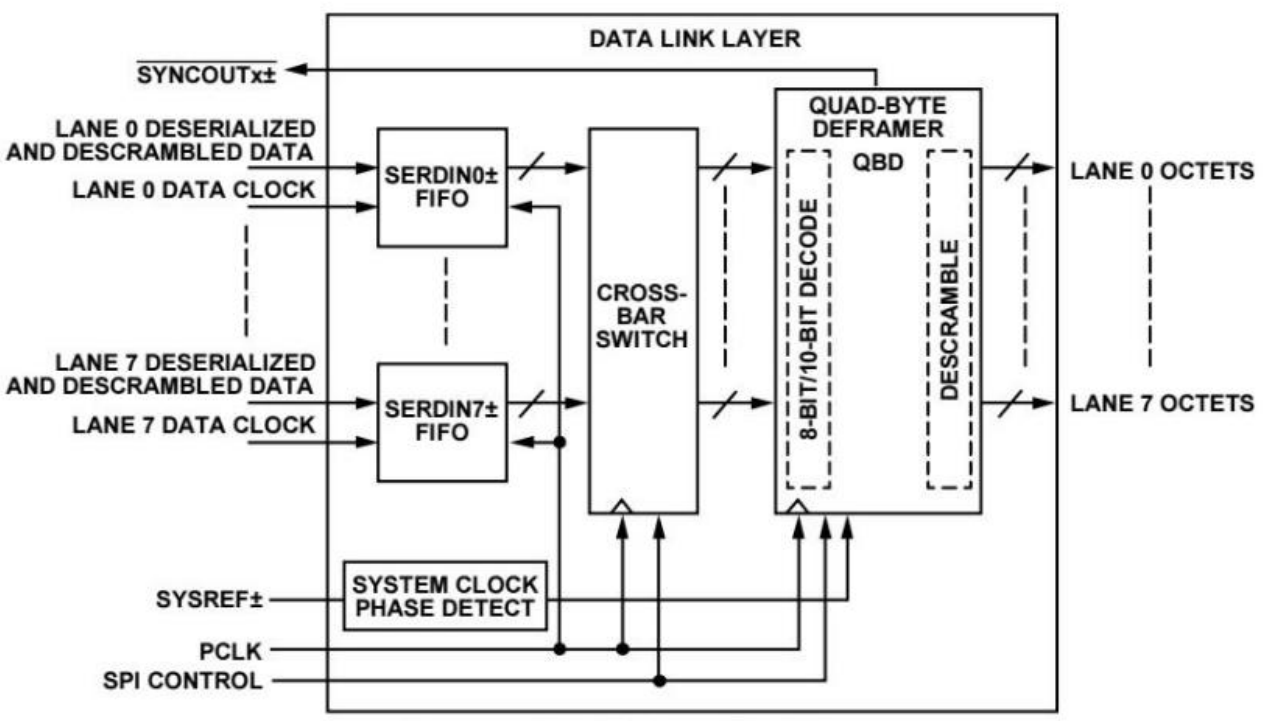


Figure 26: Data link layer block diagram

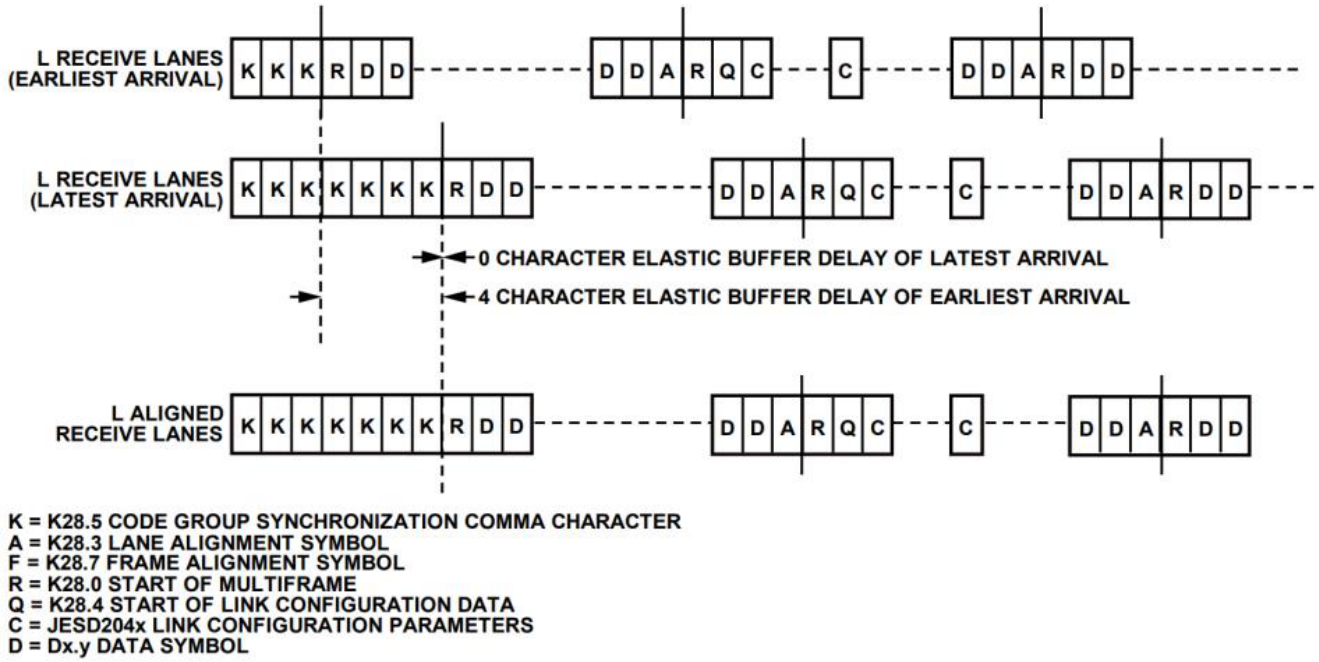


Figure 27: Lane alignment during ILAS

2.4.1 JESD204B 串行链路建立 / 2.4.1 JESD204B Serial Link Establishment

English: The high-speed serial link establishment process for Subclass 1 is briefly summarized. Full details are in Section 5.3.3 of the JESD204B specification document.

Step 1 — Code group synchronization. Each receiver must locate the /K/ (K28.5) character in its input data stream. After four consecutive /K/ characters are detected on all links, the receiver block issues the SYNCOUTx$\bar{\pm}$ signal to the transmitter block on the receiver LMFC edge. The transmitter captures the change of the SYNCOUTx$\bar{\pm}$ signal and, on the subsequent transmitter LMFC rising edge, starts ILAS.

Step 2 — Initial lane alignment sequence. The main purpose of this phase is to align all lanes of the link and verify the link parameters.

Before link establishment, each link parameter is written into the receiving device to specify how data is sent to the receiver block.

ILAS consists of four or more multiframes. The last character of each multiframe is a multiframe alignment character /A/. The first, third and fourth multiframes are filled with predetermined data values. Section 8.2 of the JESD204B specification document describes the expected data ramp during ILAS. The deframer uses the last character /A/ of each lane to align the two ends of the multiframe within the receiver. The second multiframe contains a character /R/ (K.28.0) and a character /Q/ (K.28.4), with the data corresponding to the link parameters. If the receiver requires it, additional multiframes can be added in ILAS. By default, the SXD052 uses four multiframes in ILAS (changeable in Register 0x478). If Subclass 1 is used, four multiframes must be used.

After the last /A/ character of ILAS, multiframe data begins to flow. The receiver adjusts the position of the /A/ character so that the receiver's internal LMFC aligns with it at that point.

Step 3 — Data flow. In this phase, data flows from the transmitter block to the receiver block.

The data can optionally be scrambled. Scrambling usually starts at the first octet after ILAS.

The receiver block processes and checks the data it receives for errors, mainly including the following: - Running disparity (8-bit/10-bit error) - Not in table (8-bit/10-bit error) - Unexpected control character - Bad ILAS - Inter-lane skew error (via character replacement)

If these errors exist, they are fed back to the transmitter in one of the following ways (see the JESD204B error monitoring section for details): - SYNCOUTx± assertion: when the last two errors occur, resynchronization is required (SYNCOUTx± pulled low). For the first three errors, resynchronization occurs when the error counter reaches a set error threshold. - For the first three errors, each multiframe with an error generates a small pulse on the respective SYNCOUTx± pin. - After an error occurs, an interrupt request (IRQ) event can optionally be triggered and sent to the transmitter.

For more information on the various test modes for verifying link integrity, see the JESD204B test modes section.

中文： 对子类 1 的高速串行链路建立过程进行了简要总结。完整的细节见 JESD204B 规范文件的第 5.3.3 节。

步骤 1-码组同步：每个接收器必须在其输入数据流中定位/K/（K28.5）字符。在所有链路上检测到四个连续的/K/字符后，接收器模块在接收器 LMFC 边沿向发射器模块发出 SYNCOUTx± 信号。发射器捕捉到 SYNCOUTx± 信号的变化，并在后续的发送器 LMFC 上升沿，启动 ILAS。

步骤 2-初始通道对齐序列：这一阶段的主要目的是对齐链路的所有通道，并验证链路的参数。在链路建立前，将每个链路参数写入接收设备，以指定数据是如何发送到接收模块的。ILAS 由四个或多个多帧组成。每个多帧的最后一个字符是一个多帧对齐字符/A/。第一、第三和第四个多帧由预先确定的数据值填充。JESD204B 规范文件的第 8.2 节描述了 ILAS 期间预期的数据斜率。解帧器使用每个通道的最后一个字符/A/来对齐接收器内多帧的两端。第二个多帧包含一个字符/R/（K.28.0）和字符/Q/（K.28.4），数据和链路参数相对应。如果接收器需要，可以在 ILAS 中添加额外的多帧。默认情况下，SXD052 在 ILAS 中使用四个多帧（可在寄存器 0x478 中更改）。如果使用子类 1，必须使用四个多帧。在 ILAS 的最后一个/A/字符之后，多帧数据开始流动。接收器调整/A/字符的位置，使接收器的内部 LMFC 在该点与其保持一致。

步骤 3-数据流：在这个阶段，数据从发射器模块流向接收器模块。也可以选择对数据进行加扰。通常在 ILAS 之后的第一个八位字，开始加扰。接收器模块处理并检查其收到的数据是否有错误，主要包括以下内容：出现运行差异（8 位/10 位错误）；不在表中（8 位/10 位错误）；意外的控制字符；糟糕的 ILAS；线路间的倾斜误差（通过字符替换）。如果这些错误存在，它们会以下列方式之一反馈给发射器（详见 JESD204B 错误监测部分）：SYNCOUTx± 信号置位：当出现最后两个错误时，必须重新同步（SYNCOUTx± 信号拉低）。而对于前三个错误，当错误计数器达到一个设定的错误阈值时，再重新同步。对于前三个错误，每个有错误的多帧都会在各自的 SYNCOUTx± 引脚上产生一个小脉冲。出现错误后，可以选择性地触发一个中断请求（IRQ）事件，该事件可以被发送到发送器。关于验证链路完整性的各种测试模式的更多信息，请参阅 JESD204B 测试模式部分。

2.4.2 通道先入先出（FIFO）/ 2.4.2 Lane FIFO

English: The FIFO in front of the crossbar switch and the descrambler synchronizes the samples sent on the high-speed serial data interface with the descrambler clock by adjusting the phase of the incoming data. The FIFO absorbs timing variation between the data source and the deframer, allowing transmitter drift within two PCLK cycles. Whether the FIFO is full or empty can be determined by monitoring the FIFO_STATUS_REG_0 register and the FIFO_STATUS_REG_1 register (Register 0x30C and Register 0x30D, respectively).

Lane FIFO IRQ. The collected lane FIFO error bits can also serve as an IRQ event. Use Bit 2 of Register 0x020 to enable the lane FIFO error bits, then use Bit 2 of Register 0x024 to read back their status and reset the IRQ signal. For more information, see the Interrupt Request Operation section.

中文： 纵横式开关和解扰器前面的 FIFO 通过调整传入数据的相位，完成高速串行数据接口上发送的样本与解扰器时钟的同步。FIFO 吸收了数据源和解帧器之间的时序变化，允许发射器的漂移在两个 PCLK 周期内。可以通过监测 FIFO_STATUS_REG_0 寄存器和 FIFO_STATUS_REG_1 寄存器（分别为寄存器 0x30C 和寄存器 0x30D），来确定 FIFO 是满还是空。

通道 FIFO IRQ：集合的通道 FIFO 错误位也可以作为一个 IRQ 事件。使用寄存器 0x020 的 Bit2 来启用通道 FIFO 错误位，然后使用寄存器 0x024 的 Bit2 来读回其状态并重置 IRQ 信号。更多信息请参阅中断请求操作部分。

2.4.3 横式开关 / 2.4.3 Crossbar Switch

English: Registers 0x308 to 0x30B can map any physical lane (SERDINx±) to the logical lane used by the SERDES deframer.

中文： 寄存器 0x308 到寄存器 0x30B 可以将物理通道(SERDINx±)任意映射到 SERDES 解帧器使用的逻辑通道。

表 11 纵横式寄存器 / Table 11. Crossbar Registers

地址 / Address	位 / Bits	逻辑通道 / Logical Lane
0x308	[2:0]	SRC_LANE0
0x308	[5:3]	SRC_LANE1
0x309	[2:0]	SRC_LANE2
0x309	[5:3]	SRC_LANE3
0x30A	[2:0]	SRC_LANE4
0x30A	[5:3]	SRC_LANE5
0x30B	[2:0]	SRC_LANE6
0x30B	[5:3]	SRC_LANE7

English: In each SRC_LANEy, write the number (x) of the desired physical lane (SERDINx±) from which data is obtained. By default, all logical lanes use the corresponding physical lane as their data source. For example, by default SRC_LANE0 = 0, so logical lane 0 obtains data from physical lane 0 (SERDIN0±). To use SERDIN4± as the source for logical lane 0, the user must write SRC_LANE0 = 4.

中文： 在每个 SRC_LANEy 中写入所需物理通道(SERDINx±)的编号(x)，从中获取数据。默认情况下，所有逻辑通道使用相应的物理通道作为其数据源。例如，默认情况下，SRC_LANE0=0。因此，逻辑通道 0 从物理通道 0(SERDIN0±)获得数据。要使用 SERDIN4±作为逻辑通道 0 的来源，用户必须写入 SRC_LANE0=4。

2.4.4 通道反转 / 2.4.4 Lane Inversion

English: Register 0x334 can invert the desired logical lanes, to simplify the routing of the SERDINx± signals. For each logical lane x, set Bit x of Register 0x334 to 1 to invert it.

中文： 寄存器 0x334 可以反转所需的逻辑通道，用于简化 SERDINx±信号的路径。对于每个逻辑通道 x，将寄存器 0x334 的 Bit x 设置为 1，用来反转它。

2.4.5 解帧器 / 2.4.5 Deframer

English: The SXD052 contains two four-byte deframers (QBDs), distinguished by the LINK_PAGE at Bit 2 of Register 0x300. The deframer accepts 8-bit/10-bit encoded data from the deserializer (through the crossbar switch), decodes it, deframes it into JESD204B frames, and passes it to the transport layer, which converts it into DAC samples. The deframer processes four symbols (or octets) in each processing clock (PCLK) cycle.

The deframer uses the JESD204B parameters programmed into the register map to identify how the data is packed and unpacks it. The JESD204B parameters are described in detail in the transport layer section. Many parameters are also needed in the transport layer to convert JESD204B frames into samples.

Descrambler. The SXD052 provides an optional descrambler block using a self-synchronizing descrambler with the polynomial: $1 + X^{14} + X^{15}$. Enabling data scrambling reduces the spectral peaks produced when the same data octet repeats from frame to frame. Data scrambling makes the spectral data independent, avoiding frequency-selective effects that may appear on the electrical interface and cause data-dependent errors. Data descrambling is enabled by setting the SCR bit (Bit 7 of Register 0x453) to 1.

中文： SXD052 包含两个四字节解帧器（QBD），由寄存器 0x300 的 Bit2 的 LINK_PAGE 来区分这两个字节。解帧器接受来自解串器的 8 位/10 位编码数据（通过纵横式开关），对其进行解码，并将其解帧为 JESD204B 帧，然后传递给传输层，将其转换为 DAC 样本。解帧器在每个处理时钟（PCLK）周期处理四个符号（或八位字）。

解帧器使用用户编入到寄存器图的 JESD204B 参数来识别数据的包装方式，并将其解压出来。JESD204B 参数在传输层部分有详细描述。在传输层中也需要许多参数来将 JESD204B 帧转换为样本。

解扰器：SXD052 提供了一个可选的解扰器模块，使用自同步解扰器，其多项式如下：1+X14+X15。启用数据加扰可以减少同一数据八位字在帧与帧之间重复时产生的频谱峰值。数据加扰可使频谱数据独立，从而避免在电气接口上可能出现的频率选择效应，导致数据依赖性错误。通过将 SCR 位（寄存器 0x453 的 Bit7）设置为 1 来启用数据解扰。

2.5 传输层 / 2.5 Transport Layer

English: The transport layer receives and descrambles the JESD204B frames and converts them into DAC samples according to the programmed JESD204B parameters shown in Table 12. The device parameters are defined as shown in Table 13.

中文： 传输层接收并解扰 JESD204B 帧，根据表 12 所示的编程的 JESD204B 参数将其转换为 DAC 样本。器件参数定义如表 13 所示。

表 12 JESD204B 传输层参数 / Table 12. JESD204B Transport Layer Parameters

参数 / Parameter	描述 / Description
F	每通道每帧的八位字数。1、2、3、4 或 8。/ Number of octets per frame per lane. 1, 2, 3, 4 or 8.
K	每个多帧的帧数：K = 32。/ Number of frames per multiframe: K = 32.

参数 / Parameter	描述 / Description
L	每个转换器器件（每条链路）的通道数，如下所示：1、2、3、4 或 8。/ Number of lanes per converter device (per link), as follows: 1, 2, 3, 4 or 8.
M	每个器件（每链路）的转换器数量，如下所示：对于实数模式，M 是实数转换器的数量（如果总插值为 1×）。对于复数数据模式，M 是复数数据子通道的数量，I 或 Q。/ Number of converters per device (per link): for real mode, M is the number of real converters (if total interpolation is 1×); for complex data mode, M is the number of complex data subchannels, I or Q.
S	每个转换器，每帧的采样数量：1、2、4 或 8。/ Number of samples per converter per frame: 1, 2, 4 or 8.

表 13 JESD204B 器件参数 / Table 13. JESD204B Device Parameters

参数 / Parameter	描述 / Description
CF	每条链路每个器件时钟的控制字数量。不支持，必须为 0。/ Number of control words per link per device clock. Not supported; must be 0.
CS	每个转换样本的控制位数量。不支持，必须为 0。/ Number of control bits per conversion sample. Not supported; must be 0.
HD	高密度用户数据格式。这个参数总是被设置为 1。/ High-density user data format. This parameter is always set to 1.
N	转换器分辨率。/ Converter resolution.
N'（或 NP）/ N' (or NP)	每个样本的总比特数。/ Total number of bits per sample.

English: The SXD052 supports specific combinations of these parameters. The parameter lists of the supported single-link and dual-link modes are in Table 15 and Table 16, respectively. Table 15 and Table 16 list the JESD204B parameters of each mode. Table 14 lists the JESD204B parameters with fixed values.

中文： SXD052 支持这些参数的特定组合。支持的单链路和双链路模式的参数列表，分别见表 15 和表 16。表 15 和表 16 列出了每种模式的 JESD204B 参数。表 14 列出了具有固定值的 JESD204B 参数。

表 14 具有固定值的 JESD204B 参数 / Table 14. JESD204B Parameters with Fixed Values

参数 / Parameter	值 / Value
K	32
CF	0
HD	1
CS	0

表 15 单链路 JESD204B 工作模式 / Table 15. Single-Link JESD204B Operating Modes

（参数行与表 3 相同 / parameter rows identical to Table 3）

参数 / Parameter	0	1	2	3	4	5	6	7	8	9	10	11	12	18	19	20	21	22
L（通道数 / lanes）	1	2	3	2	4	1	2	1	4	4	8	8	8	4	4	8	8	4
M（转换器计数 / converters）	2	4	6	2	4	2	4	4	2	2	2	2	2	1	1	1	1	2

参数 / Parameter	0	1	2	3	4	5	6	7	8	9	10	11	12	18	19	20	21	22
F（每通道每帧八位字 / octets per frame per lane）	4	4	4	2	2	3	3	8	1	2	1	2	3	1	2	1	2	3
S（每帧转换器的采样数 / samples per frame per converter）	1	1	1	1	1	1	1	1	1	2	2	4	8	2	4	4	8	4
NP（每个样本的总比特数 / total bits per sample）	16	16	16	16	16	12	12	16	16	16	16	16	12	16	16	16	16	12
N（转换器分辨率 / converter resolution）	16	16	16	16	16	12	12	16	16	16	16	16	12	16	16	16	16	12

表 16 双链路 JESD204B 工作模式 / Table 16. Dual-Link JESD204B Operating Modes

（参数行与表 4 相同 / parameter rows identical to Table 4）

参数 / Parameter	0	1	2	3	4	5	6	7	8	9	18	19	22
L（通道数 / lanes）	1	2	3	2	4	1	2	1	4	4	4	4	4
M（转换器计数 / converters）	2	4	6	2	4	2	4	4	2	2	1	1	2
F（每通道每帧八位字 / octets per frame per lane）	4	4	4	2	2	3	3	8	1	2	1	2	3
S（每帧转换器的采样数 / samples per frame per converter）	1	1	1	1	1	1	1	1	1	2	2	4	4
NP（每个样本的总比特数 / total bits per sample）	16	16	16	16	16	12	12	16	16	16	16	16	12
N（转换器分辨率 / converter resolution）	16	16	16	16	16	12	12	16	16	16	16	16	12

2.5.1 配置参数 / 2.5.1 Configuration Parameters

English: The SXD052 mode refers to the link configuration parameters L, K, M, N, NP, S and F; Table 17 provides the descriptions and addresses of these settings.

中文： SXD052 模式是指 L、K、M、N、NP、S 和 F 的链路配置参数，表 17 提供了这些设置的说明和地址。

表 17 配置参数 / Table 17. Configuration Parameters

JESD204B 设置 / Setting	描述 / Description	地址 / Address
L–1	通道数量减去 1。/ Number of lanes minus 1.	寄存器 0x453，Bit[4:0] / Register 0x453, Bits[4:0]
F-1	（每通道的（每帧八位字））减去 1 的数量。/ Number of octets per frame per lane, minus 1.	寄存器 0x454，Bit [7:0] / Register 0x454, Bits[7:0]
K–1	每个多帧的帧数减去 1。/ Number of frames per multiframe minus 1.	寄存器 0x455，Bit [4:0] / Register 0x455, Bits[4:0]
M-1	转换器的数量减去 1。/ Number of converters minus 1.	寄存器 0x456，Bit [7:0] / Register 0x456, Bits[7:0]
N-1	转换器的比特分辨率减去 1。/ Converter bit resolution minus 1.	寄存器 0x457，Bit [4:0] / Register 0x457, Bits[4:0]
NP–1	每个样本的比特包减去 1。/ Bits per sample minus 1.	寄存器 0x458，Bit [4:0] / Register 0x458, Bits[4:0]

JESD204B 设置 / Setting	描述 / Description	地址 / Address
S-1	（每帧（每个转换器的样本））数量减去 1。/ Number of samples per converter per frame, minus 1.	寄存器 0x459，Bit [4:0] / Register 0x459, Bits[4:0]
HD	高密度格式。设置为 1。/ High-density format. Set to 1.	寄存器 0x45A，Bit 7 / Register 0x45A, Bit 7
DID	器件 ID。匹配由发射器发送的器件 ID。/ Device ID. Matches the device ID sent by the transmitter.	寄存器 0x450，Bit [7:0] / Register 0x450, Bits[7:0]
BID	库 ID。匹配由发射器发送的库 ID。/ Bank ID. Matches the bank ID sent by the transmitter.	寄存器 0x451，Bit [7:0] / Register 0x451, Bits[7:0]
LID0	通道 0 的通道 ID。匹配由发射器发送的通道 ID 到逻辑通道 0。/ Lane ID of Lane 0. Matches the lane ID sent by the transmitter to logical Lane 0.	寄存器 0x452，Bit [4:0] / Register 0x452, Bits[4:0]
JESDV	JESD204x 版本。匹配由发射器发送的版本 (0x0=JESD204A，0x1=JESD204B)。/ JESD204x version. Matches the version sent by the transmitter (0x0 = JESD204A, 0x1 = JESD204B).	寄存器 0x459，Bit [7:5] / Register 0x459, Bits[7:5]

English: The SXD052 truncates the output of the main digital datapath to the N-bit value of the selected mode and then sends it to the DAC core. Data values of NP bits can be sent, with the lower NP−N LSBs padded with 0, or all NP bits of data can be sent through the SERDES lanes. In both cases, the lower NP−N LSBs are truncated before the DAC core.

中文： SXD052 将主数字数据通路的输出截断为所选模式的 N 位值，然后将其发送到 DAC 内核。可以发送 NP 位数的数据值，将较低的 NP-N LSB 填充为 0，或者通过 SERDES 通道发送全部 NP 位数的数据。在这两种情况下，较低的 NP-N LSB 在 DAC 内核之前被截断。

2.5.2 通过 JESD204B 接收器的数据流 / 2.5.2 Data Flow Through the JESD204B Receiver

English: The link configuration parameters determine how the serial bits on the JESD204B receiver interface are deframed as data samples and passed to the DAC.

中文： 链路配置参数决定了 JESD204B 接收器接口上的串行位如何作为数据样本被解帧并传递给 DAC。

2.5.3 纠偏和启用逻辑通道 / 2.5.3 Deskewing and Enabling Logical Lanes

English: Once correctly configured, the logical lanes are deskewed automatically. The corresponding logical lanes are enabled or disabled according to the number of lanes of the mode setting selected in Bits[4:0] of Register 0x110. By default, all physical lanes are powered up. To power down an unused physical lane, setting bit x in Register 0x201 to 1 disables physical lane x; conversely, setting it to 0 enables it. When logical lanes are enabled and deskewed, they must be controlled on a per-link basis using the LINK_PAGE signal (Register 0x300, Bit 2). Setting bit x in Register 0x46C to 1 deskews link logical lane x for the selected link page.

中文： 正确配置后，逻辑通道会自动纠偏。根据寄存器 0x110 的 Bit[4:0]中选择的模式设置的通道数量来启用或禁用相应的逻辑通道。默认情况下，物理通道都是通电的。要关闭不使用的物理通道电源，将寄存器 0x201 中的位 x 设置为 1 可以禁用物理通道 x，反之，设置为 0 则可以启用。逻辑通道在启用和纠偏时，必须在每个链路的基础上使用 LINK_PAGE 信号来控制（寄存器 0x300，Bit2）。将寄存器 0x46C 中的位 x 设置为 1，为选定的链路页面纠偏链路逻辑通道 x。

2.6 JESD204B 测试模式 / 2.6 JESD204B Test Modes

2.6.1 PRBS 测试 / 2.6.1 PRBS Test

English: The JESD204B receiver of the SXD052 includes a PRBS pattern checker at the back end of the physical layer. The pattern checker supports the PRBS7, PRBS15 and PRBS31 data patterns, as defined in the JESD204B specification. The PRBS pattern can come from an external JESD204B transmitter such as a field-programmable gate array (FPGA), or be selectively generated by the internal PRBS7 generator, as described in the internal PRBS7 generator section. This function allows testing of the bit error rate (BER) of each physical lane of the SXD052 and of the overall JESD204B PHY. A low BER during PRBS testing confirms correct clocking and clock synchronization, and confirms the quality of the interconnection (wires, connectors and routing) between the JESD204B transmitter and receiver is good enough. Although the PHY PRBS pattern checker does not require full JESD204B link establishment, the JESD204B mode on the SXD052 must be configured so that the physical lanes are correctly clocked and ready to receive PRBS data. PRBS data must not be 8-bit/10-bit encoded. PRBS pattern verification can be performed on multiple lanes simultaneously or on one lane at a time. The error count of each failing JESD204B lane is reported independently.

The procedure to enable the PRBS checker on the SXD052 is as follows: 1. Start transmitting a looping PRBS7, PRBS15 or PRBS31 pattern, either from the JESD204B transmitter or from the internal PRBS7 generator of the SXD052. 2. By writing Bits[3:2] of Register 0x316, select the appropriate PRBS mode to receive, as shown in Table 18. 3. By writing PHY_TEST_EN (Register 0x315), enable the physical test on all lanes under test. Each bit of Register 0x315 enables the PRBS test of the corresponding lane. For example, writing 1 to Bit 0 enables the PRBS test of physical lane 0. Any running JESD204B link is interrupted at this point. 4. Toggle PHY_TEST_RESET (Bit 0 of Register 0x316) from 0 to 1 and back to 0 to reset the status registers to their default values. 5. Set PHY_PRBS_TEST_THRESHOLD_xBITS (Registers 0x319 to 0x317, Bits[23:0]) as required. 6. Write a 0 and then a 1 to PHY_TEST_START (Register 0x316, Bit 1). The rising edge of PHY_TEST_START starts the test. In some cases, Step 4 may need to be repeated at this point: toggle PHY_TEST_RESET (Register 0x316, Bit 0) from 0 to 1 and back to 0. 7. Wait until the required number of bits has accumulated, or at least 500 ms. 8. Stop the test by writing PHY_TEST_START (Register 0x316, Bit 1) = 0. 9. Read the PRBS test results from the PRBS status registers.

Each bit of PHY_PRBS_PASS (Register 0x31D) corresponds to one SERDES lane (0 = fail, 1 = pass). The default value after reset is pass. To confirm that the reported results are not false, before running a long BER test, force a failure condition on one or all lanes. Alternatively, temporarily disable some previously test-enabled lanes and confirm the test fails, or select a wrong PRBS pattern type in Step 2 and observe failures on all lanes. Then reconfigure the test appropriately and run the test to accumulate BER results.

By writing the number of the lane to check (0 to 7) in PHY_SRC_ERR_CNT (Register 0x316, Bits[6:4]) and reading PHY_PRBS_ERR_CNT_xBITS (Registers 0x31A to 0x31C), the number of PRBS errors seen on each failing lane can be read. The maximum error count is $2^{24}-1$. If all bits of Registers 0x31A to 0x31C are high, the maximum error count of the selected lane has been exceeded.

中文： SXD052 的 JESD204B 接收器在物理层的后端包括一个 PRBS 模式检查器。该模式检查器支持 PRBS7、PRBS15 和 PRBS31 数据模式，正如 JESD204B 规范中所定义的。PRBS 模式可以来自外部 JESD204B 发射器，如现场可编程门阵列（FPGA），或者由内部 PRBS7 发生器选择性生成，如内部 PRBS7 发生器部分所述。该功能允许对 SXD052 的每个物理通道以及 JESD204B 的整体 PHY 的误码率（BER）进行测试。PRBS 测试期间的低误码率证实了正确的时钟和时钟同步，并证实了 JESD204B 发射器和接收器之间的互连（导线、连接器和布线）

的质量足够好。尽管 PHY PRBS 模式检查器不要求完全建立 JESD204B 链路，但必须配置 SXD052 上的 JESD204B 模式，以便物理通道正确地进行时钟控制并准备好接收 PRBS 数据。PRBS 数据不得采用 8 位/10 位编码。PRBS 模式验证可同时在多个通道或一次在一个通道上执行。每个失败的 JESD204B 通道的错误计数都会独立报告。

在 SXD052 上启用 PRBS 检查器的过程如下： 1. 开始发送 PRBS7、PRBS15 或 PRBS31 循环模式，可从 JESD204B 发射器或 SXD052 的内部 PRBS7 发生器发送。 2. 通过写入寄存器 0x316 的 Bit[3:2]，选择合适的 PRBS 模式进行接收，如表 18 所示。 3. 通过写入 PHY_TEST_EN（寄存器 0x315），启用所有被测通道的物理测试。寄存器 0x315 的每个位都启用相应通道的 PRBS 测试。例如，向 Bit0 写入 1，启用物理通道 0 的 PRBS 测试。任何正在运行的 JESD204B 链路在这一点上被中断。 4. 将 PHY_TEST_RESET（寄存器 0x316 的 Bit0）从 0 切换到 1，然后回到 0，将状态寄存器复位为默认值。 5. 根据需要设置 PHY_PRBS_TEST_THRESHOLD_xBITS（寄存器 0x319 至寄存器 0x317，Bit[23:0]）。 6. 向 PHY_TEST_START（寄存器 0x316，Bit1）写入一个 0，然后写入一个 1。PHY_TEST_START 的上升沿会开始测试。在某些情况下，这时可能需要重复步骤 4：将 PHY_TEST_RESET（寄存器 0x316，位 0）从 0 切换到 1，然后再回到 0。 7. 等待积累到所需的位数，或至少 500 毫秒。 8. 通过写入 PHY_TEST_START（寄存器 0x316 的 Bit1）=0 停止测试。 9. 从 PRBS 状态寄存器中读取 PRBS 测试结果。

PHY_PRBS_PASS(寄存器 0x31D)的每一位对应一个 SERDES 通道(0=不通过，1=通过)。复位后的默认值是通过。为了确认报告的结果不是假的，在运行长时间的误码率测试之前，在一个或所有的通道上强制执行失败条件。或者暂时禁用一些先前启用测试的通道，确认测试失败，或者在步骤 2 中选择一个错误类型的 PRBS 模式，观察所有通道的失败情况。然后，适当地重新配置测试，并运行测试以积累误码率结果。

通过在 PHY_SRC_ERR_CNT（寄存器 0x316 的 Bit[6:4]）中写入要检查的通道数（0 至 7）并读取 PHY_PRBS_ERR_CNT_xBITS（寄存器 0x31A 至寄存器 0x31C），可以读取每个失败通道上看到的 PRBS 错误数。最大的错误计数是 2^{24}-1。如果寄存器 0x31A 至寄存器 0x31C 的所有位都是高位，则超过了所选通道的最大错误计数。

表 18 PHY PRBS 模式选择 / Table 18. PHY PRBS Pattern Selection

PHY_PRBS_PAT_SEL 设置（寄存器 0x316 的 Bit[3:2]）/ Setting (Register 0x316, Bits[3:2])	PRBS 模式 / PRBS Pattern
0b00（默认 / default）	PRBS7
0b01	PRBS15
0b10	PRBS31

2.6.2 内部 PRBS7 发生器 / 2.6.2 Internal PRBS7 Generator

English: The SXD052 integrates an internal PRBS7 generator that can be used to test the JESD204B PHY without inputting external PRBS data from a JESD204B transmitter. Although this method only confirms the internal PHY portion of the SXD052, it confirms that the PRBS checker and the internal clock domains are running and correctly configured. The internal PRBS test is best followed by a more thorough external PHY PRBS test, in which case the JESD204B transmitter device provides the pattern.

The procedure to configure the internal PRBS7 generator on the SXD052 is as follows: 1. Set the EQ_BOOST_PHYx bits (Bits[7:0] of Register 0x240 and Bits[7:0] of Register 0x241) to 0. 2. Set the SEL_IF_PARDATAINV_DES_RC_CH bits (Bits[7:0] of Register 0x234) to 0, to ensure the lanes are not inverted. 3. By writing EN_LBT_DES_RC_CH (Register 0x250), enable the loopback test on all lanes under test. Each bit of Register 0x250 enables the loopback test of the corresponding lane. For example, writing 1

to Bit 0 enables the test of physical lane 0. 4. For half-rate, set EN_LBT_HALFRATE_DES_RC (Bit 1 of Register 0x251) to 1. Otherwise, set this bit to 0. 5. Toggle INIT_LBT_SYNC_DES_RC (Bit 0 of Register 0x251) from 0 to 1 and back to 0. 6. Refer to the PRBS test section for how to configure the PRBS checker for a PRBS7 test.

中文： SXD052 集成了一个内部 PRBS7 发生器，可用于测试 JESD204B PHY，无需从 JESD204B 发射器输入外部 PRBS 数据。虽然这种方法只确认了 SXD052 内部 PHY 部分，但它确认了 PRBS 检查器和内部时钟域都在运行并正确配置。内部 PRBS 测试之后最好进行更彻底的外部 PHY PRBS 测试，在此情况下，JESD204B 发射器器件提供此模式。

在 SXD052 上配置内部 PRBS7 发生器的过程如下： 1. 将 EQ_BOOST_PHYx 位（寄存器 0x240 的 Bit[7:0]和寄存器 0x241 的 Bit[7:0]）设置为 0。 2. 将 SEL_IF_PARDATAINV_DES_RC_CH 位（寄存器 0x234 的 Bit[7:0]）设为 0，以确保通道不倒置。 3. 通过写入 EN_LBT_DES_RC_CH（寄存器 0x250），启用所有被测通道的回环测试。寄存器 0x250 的每个位都启用相应通道的回环测试。例如，向位 0 写入 1 可以启用物理通道 0 的测试。 4. 对于半帧，将 EN_LBT_HALFRATE_DES_RC（寄存器 0x251 的 Bit1）设为 1。否则，将此位设为 0。 5. 将 INIT_LBT_SYNC_DES_RC（寄存器 0x251 的 Bit0）从 0 切换到 1，然后回到 0。 6. 请参考 PRBS 测试部分，了解如何配置 PRBS 检查器进行 PRBS7 测试。

2.6.3 传输层测试 / 2.6.3 Transport Layer Test

English: The JESD204B receiver in the SXD052 supports the short transport layer (STPL) test described in the JESD204B standard. Use this test to verify the data mapping between the JESD204B transmitter and receiver. To perform this test, the function must be implemented and enabled in the logic device. Before running the test at the receive end, the link must be established and running without errors.

The STPL test ensures that the samples of each converter are properly mapped according to the number of converters (M) and the number of samples per converter (S). Per the details of the JESD204B standard, the converter manufacturer specifies the test samples to be transmitted. Each sample must have a unique value. For example, if M=2 and S=2, four unique samples are transmitted repeatedly until the test stops. The expected samples must be programmed into the device; the expected samples are compared with the received samples, one sample at a time, until all are tested. The procedure for performing this test on the SXD052 is described as follows: 1. Synchronize and establish the JESD204B link between the transmitter and the SXD052. 2. Enable the STPL test on the JESD204B transmitter. Depending on the JESD204B mode, each link may have up to six data streams, providing up to three complex subchannels (M=6), and each frame can contain up to eight samples (S=8). 3. Configure SHORT_TPL_REF_SP_MSB (Register 0x32E) and SHORT_TPL_REF_SP_LSB (Register 0x32D) to match one sample within a single frame. For N=12 modes, the integer value of the expected sample is multiplied by 16 (binary, a 4-bit shift operation). 4. If testing a dual-link JESD204B, set SHORT_TPL_LINK_SEL (Bit 7 of Register 0x32F) to select whether to test Link 0 (DAC0 datapath) or Link 1 (DAC1 datapath). 5. Set SHORT_TPL_CHAN_SEL (Bits[3:2] of Register 0x32C) to select the channel. 6. Set SHORT_TPL_IQ_PATH_SEL (Bit 6 of Register 0x32F) to select the I path or the Q path of the channel under test. 7. Set SHORT_TPL_SP_SEL (Bits[7:4] of Register 0x32C) to select which sample in each frame is expected to have the value shown in Step 3. 8. Set SHORT_TPL_TEST_EN (Bit 0 of Register 0x32C) to 1. 9. Set SHORT_TPL_TEST_RESET (Bit 1 of Register 0x32C) to 1, then back to 0. 10. Wait for the required time. The required time is calculated as 1/(sample rate × BER). For example, given BER = 1×10^{-10} and a sample rate of 1 GSPS, the required time = 10 seconds. 11. Read the test result in SHORT_TPL_FAIL (Bit 0 of Register 0x32F). 12. Select other samples of the same or another M and continue testing, until all samples of both converters in a frame are verified.

中文： SXD052 中的 JESD204B 接收器支持 JESD204B 标准中所述的短传输层（STPL）测试。使用该测试来验证 JESD204B 发射器和接收器之间的数据映射。要执行这项测试，必须在逻辑器件中实现并启用这项功能。在接收端运行测试之前，链路必须建立并运行无误。

STPL 测试确保每个转换器的样本都根据转换器的数量(M)和每个转换器的样本数(S)进行适当地映射。按照 JESD204B 标准的细节，转换器制造商指定传输的测试样本。每个样本必须有一个唯一的值。例如，如果 M=2，S=2，则四个唯一的样本被反复传输，直到测试停止。预期的样本必须被编程到器件中，预期的样本与收到的样本进行比较，一次一个样本，直到全部测试完毕。在 SXD052 上进行这项测试的过程描述如下： 1 在发射器和 SXD052 之间同步并建立 JESD204B 链路。 2. 在 JESD204B 发射器上启用 STPL 测试。根据 JESD204B 模式，每条链路可能有多达六个数据流，以提供多达三个复数子通道（M=6），每个帧可以包含多达八个样本（S=8）。 3. 配置 SHORT_TPL_REF_SP_MSB(寄存器 0x32E)和 SHORT_TPL_REF_SP_LSB (寄存器 0x32D)来匹配单帧内的一个样本。对于 N=12 模式，预期样本的整数值要乘以 16（二进制，4 位移位操作）。 4. 如果测试双链路 JESD204B，设置 SHORT_TPL_LINK_SEL（寄存器 0x32F 的 Bit7）以选择测试链路 0（DAC0 数据路径）还是链路 1（DAC1 数据路径）。 5. 设置 SHORT_TPL_CHAN_SEL（寄存器 0x32C 的 Bit[3:2]）来选择通道。 6. 设置 SHORT_TPL_IQ_PATH_SEL（寄存器 0x32F 的 Bit6）来选择被测通道的 I 路或 Q 路。 7. 设置 SHORT_TPL_SP_SEL(寄存器 0x32C 的 Bit[7:4])，以选择每一帧中的哪一个样本预期具有步骤 3 中所示的值。 8. 将 SHORT_TPL_TEST_EN（寄存器 0x32C 的 Bit0）设为 1。 9. 将 SHORT_TPL_TEST_RESET（寄存器 0x32C 的 Bit1）设置为 1，然后回到 0。 10. 等待所需的时间。所需时间的计算方法是 1/（采样率×误码率）。例如，给定 BER=1×10-10，采样率=1GSPS，所需时间=10 秒。 11. 在 SHORT_TPL_FAIL（寄存器 0x32F 的 Bit0）读取测试结果。 12. 选择同一个或另一个 M 的其他样本继续测试，直到一帧中两个转换器的所有样本都得到验证。

2.6.4 重复的 CGS 和 ILAS 测试 / 2.6.4 Repeated CGS and ILAS Tests

English: Per Section 5.3.3.8.2 of the JESD204B specification, the SXD052 can check whether it is receiving a constant stream of /K28.5/ characters, or whether it is receiving a constant ILAS stream following CGS.

To run the repeated CGS test, send a constant stream of /K28.5/ characters to the SXD052 SERDES inputs. Next, set up the device and enable the link. By reading Register 0x470, verify that SYNCOUTx$\bar{\pm}$ is deasserted and that CGS has passed on all enabled link lanes, ensuring that /K28.5/ characters are received.

To run the CGS-then-repeated-ILAS-sequence test, follow the procedure to set up the link, but before performing the final write (enabling the link), enable the ILAS test mode by writing 1 to Bit 7 of Register 0x477. Then enable the link. When the device recognizes four CGS characters on each lane, it deasserts SYNCOUTx±. At this time, the transmitter starts sending a repeated ILAS sequence.

Read Register 0x473 to verify that initial lane synchronization has passed on all enabled link lanes.

中文： 根据 JESD204B 规范的第 5.3.3.8.2 节，SXD052 可以检查是否正在接收/K28.5/字符的恒定流，或者是否正在接收 CGS 之后的 ILAS 恒定流。

要运行重复的 CGS 测试，向 SXD052 SERDES 输入端发送/K28.5/字符的恒定流。接下来，设置器件并启用链路。通过读取寄存器 0x470 验证 SYNCOUTx± 是否解除置位，以及所有启用链路通道的 CGS 是否通过，确保收到/K28.5/字符。

要运行 CGS，然后重复 ILAS 序列测试，可遵循程序来设置链路，但是，在执行最后一次写入（启用链路）之前，请通过向寄存器 0x477 的 Bit7 写入 1 来启用 ILAS 测试模式。然后，启用链路。当器件在每个通道上识别到四个 CGS 字符时，它就会解除 SYNCOUTx± 置位。在这时，发射器开始发送一个重复的 ILAS 序列。

读取寄存器 0x473 以验证所有启用链路通道的初始通道同步已经通过。

2.7 JESD204B 错误监测 / 2.7 JESD204B Error Monitoring

2.7.1 差异、不在表和意外控制（K）字符错误 / 2.7.1 Disparity, Not-in-Table and Unexpected Control (K) Character Errors

English: Per Section 7.6 of the JESD204B specification, the SXD052 can detect disparity errors, not-in-table (NIT) errors and unexpected control character errors, and can optionally issue a synchronization request to reinitialize the link when an error occurs.

This section notes several other interpretations of the JESD204B specification. When three NIT errors are injected into a lane and QUAL_RDERR (Register 0x476, Bit 4) = 1, the readback value of the disparity error (BDE) count register is 1. A disparity error at the same character position as an NIT error cannot be reported. There is no such restriction for a disparity error in a character following an NIT error. Therefore, an NIT error may cause a BDE error; this is expected behavior.

Checking the error count. The error count can be checked for disparity errors, NIT errors and unexpected control character errors. Error counting is on a per-lane and per-error-type basis. Each error type and lane has a dedicated register. To check the error count, the following steps must be performed: 1. By selecting in Bits[5:3] of Register 0x480 to Bits[5:3] of Register 0x487, enable the errors to be monitored. Writing 1 to the appropriate bits, as described in Table 50, selects unexpected K (UEK) character, BDE and NIT error monitoring for each lane. These bits are enabled by default. 2. The bits that reset the corresponding error counters are in Bits[2:0] of Register 0x480 to Bits[2:0] of Register 0x487. Write 1 to the corresponding bit to reset that error counter. 3. Bits[2:0] of Register 0x488 to Bits[2:0] of Register 0x48F hold the terminal-count hold indicators of each error counter. If this flag is enabled, when the terminal error count 0xFF is reached, the counter stops counting and holds the value until reset. Otherwise, it rolls over to 0x00 and continues counting. Select the desired behavior and program the corresponding register bits of each lane accordingly.

Checking whether the error count exceeds the threshold. To check whether the error count exceeds the threshold, follow these steps: 1. Define the error-counter threshold. The error-counter threshold can be set in Register 0x47C to a user-defined value, or the default value 0xFF can be kept. When the error threshold is reached, an IRQ is generated, SYNCOUTx$\bar{±}$ is asserted, or both, depending on the mask register settings. This error threshold is used for all three error types (UEK, NIT and BDE). 2. Set the SYNC_ASSERT_MASK bits. The SYNCOUTx$\bar{±}$ assertion behavior is set in Bits[2:0] of Register 0x47D. By default, when the error counter of any lane equals the threshold, it asserts the SYNCOUTx$\bar{±}$ signal (Bits[2:0] of Register 0x47D = 0b111). When setting the SYNC_ASSERT_MASK bits, LINK_PAGE (Register 0x300, Bit 2) must be set to 1. 3. Read the error count that reached the indicator. Each error counter has a terminal-count-reached indicator on each lane. When the terminal count of the error counter of a specific lane is reached, the indicator is set to 1. These status bits are in Bits[2:0] of Register 0x490 to Bits[2:0] of Register 0x497. Bit 3 can be read back to indicate whether a specific lane is active.

Error counter and IRQ control. For error counter and IRQ control, follow these steps: 1. Enable the interrupts. Enable the JESD204B interrupts. The interrupts of the UEK, NIT and BDE error counters are in Bits[7:5] of Register 0x4B8. When establishing the link, other interrupts also need monitoring, such as lane deskew, initial lane synchronization, good checksum, frame synchronization, code group synchronization (Bits[4:0] of Register 0x4B8), and configuration mismatch (Bit 0 of Register 0x4B9). These bits are off by default, but can be enabled by writing 0b1 to the corresponding bits. 2. Read the JESD204B interrupt

status. The interrupt status bits are in Bits[7:0] of Register 0x4BA and Bit 0 of Register 0x4BB; the positions of the status bits correspond to the positions of the enable bits. 3. It is recommended to enable all interrupts intended for use before starting the JESD204B link. After the link starts, the interrupts can be reset and then used to monitor the link status.

Monitoring errors through SYNCOUTx±. When one or more disparity errors, NIT errors or unexpected control character errors occur, the error is reported on the SYNCOUTx± pin per Section 7.6 of the JESD204B specification. The JESD204B specification states that when an error occurs, the signal is asserted for exactly two frame periods. For the SXD052, the width of the SYNCOUTx± pulse can be programmed to 1/2, 1 or 2 PCLK cycles. Table 19 gives the settings that produce a SYNCOUTx± pulse of two frame clock periods.

中文： 根据 JESD204B 规范的第 7.6 节，SXD052 可以检测差异错误、不在表（NIT）错误和意外控制字符错误，并可选择发出同步请求，在错误发生时对链路进行重新初始化操作。

本节指出了 JESD204B 规范的其他几个解释。当三个 NIT 错误被注入到一个通道，并且 QUAL_RDERR (寄存器 0x476，位 4)=1 时，差异错误(BDE)计数寄存器的回读值为 1。不能报告 NIT 错误的同一字符位置上的差异错误。对于 NIT 错误之后的字符中的差异错误，没有这种限制。因此，NIT 错误可能导致 BDE 错误，是预期之内行为。

检查错误计数：错误计数可以检查差异错误、NIT 错误和意外控制字符错误。错误计数是以每个通道和每个错误类型为基础的。每个错误类型和通道都有一个专门的寄存器。要检查错误计数，必须执行以下步骤。 1. 通过在寄存器 0x480，位[5:3]到寄存器 0x487，位[5:3]中选择并启用要监测的错误。将 1 写入适当的位，如表 50 所述，可以为每个通道选择意外 K（UEK）字符、BDE 和 NIT 错误监测。这些位在默认情况下是启用的。 2. 对应的错误计数器复位的位在寄存器 0x480 的 Bit[2:0]到寄存器 0x487，Bit[2:0]。在对应的位上写入 1 来重置该错误计数器。 3. 寄存器 0x488 的 Bit[2:0]到寄存器 0x48F 的 Bit[2:0]有每个错误计数器的终端计数保持指标。如果启用此标志，当达到终端错误计数 0xFF 时，计数器停止计数并保持该值直到复位。否则，它将回到 0x00 并继续计数。选择所需的行为，并对每个通道相应寄存器位进行编程。

检查错误计数是否超过阈值：要检查错误计数是否超过阈值，请遵循以下步骤。 1. 定义错误计数器的阈值。错误计数器的阈值可以在寄存器 0x47C 中设置为用户定义的值，或保存默认值 0xFF。当达到错误阈值时，产生一个 IRQ，SYNCOUTx± 有效，或两者都有，取决于掩码寄存器的设置。这一错误阈值用于所有三种类型的错误（UEK、NIT 和 BDE）。 2. 设置 SYNC_ASSERT_MASK 位。SYNCOUTx± 信号发出行为在寄存器 0x47D 的 Bit[2:0] 中设置。默认情况下，当任何通道的错误计数器等于阈值时，它将发出 SYNCOUTx± 信号（寄存器 0x47D 的 Bit[2:0] = 0b111)。当设置 SYNC_ASSERT_MASK 位时，LINK_PAGE（寄存器 0x300，位 2）必须被设置为 1。 3. 读取达到指标的错误计数。每个错误计数器在每个通道上都有一个终端计数达到指标。当一个特定通道的错误计数器的终端计数达到时，该指标被设置为 1。这些状态位在寄存器 0x490 的 Bit[2:0]至寄存器 0x497 的 Bit[2:0]。第 3 位可以被回读，以表明某个特定的通道是否处于活动状态。

错误计数器和 IRQ 控制：对于错误计数器和 IRQ 控制，请遵循以下步骤： 1. 启用中断。启用 JESD204B 中断。UEK、NIT 和 BDE 错误计数器的中断在寄存器 0x4B8 的 Bit[7:5]。在建立链路时，还有其他中断需要监测，如通道纠偏、初始通道同步、优良校验和、帧同步、码组同步（寄存器 0x4B8 的 Bit[4:0]），以及配置不匹配（寄存器 0x4B9 的 Bit0）。这些位默认是关闭的，但可以通过向相应的位写入 0b1 来启用。 2. 读取 JESD204B 的中断状态。中断状态位在寄存器 0x4BA 的 Bit[7:0]和寄存器 0x4BB 的 Bit0，状态位的位置与启用位的位置相对应。 3. 建议在启动 JESD204B 链接之前，启用所有计划使用的中断。当链路启动后，中断可以被重置，然后用于监测链路状态。

通过 SYNCOUTx± 监控错误：当发生一个或多个差异错误、NIT 错误或意外控制字符错误时，按照 JESD204B 规范第 7.6 节的规定，在 SYNCOUTx± 引脚上报告该错误。JESD204B 规范规定，当发生错误时，信号正好在两

个帧周期内发出。对于 SXD052，SYNCOUTx± 脉冲的宽度可以编程为 1/2、1 或 2 个 PCLK 周期。表 19 中给出了实现两帧时钟周期的 SYNCOUTx± 脉冲的设置。

表 19 设置 SYNCOUT‾± 错误脉冲持续时间 / Table 19. Setting the SYNCOUT‾± Error Pulse Duration

F	PCLK 因子（帧数/PCLK）/ PCLK Factor (Frames/PCLK)	SYNC_ERR_DUR（寄存器 0x312 的 Bit[7:4]）设置[1] / Setting[1]
1	4	0（default）
2	2	1
3	1.5	2
4	1	2
8	0.5	4

[1] 这些寄存器的设置对两个帧时钟周期的脉冲宽度发出 SYNCOUTx±信号。/ These register settings assert the SYNCOUTx± signal with a pulse width of two frame clock periods.

English — Unexpected control character, NIT and disparity IRQs: For UEK character, NIT and disparity errors, the event of the error count exceeding the threshold can serve as an IRQ event. Enable the IRQ events by writing Bits[7:5] of Register 0x4B8. After the IRQ is enabled, the IRQ event status can be read at Bits[7:5] of Register 0x4BA.

For information on resetting the IRQ, see the error counter and IRQ control section. For more information on IRQs, see the Interrupt Request Operation section.

Errors requiring reinitialization. Per Section 7.1 of the JESD204B specification, link reinitialization occurs automatically when four invalid disparity characters or four NIT characters are received. When link reinitialization occurs, the resynchronization request is at least 5 frames and 9 octets long.

When the error count of a disparity error, NIT error or UEK character error reaches a programmable error threshold, the user can choose to reinitialize the link. The procedure to enable reinitialization for certain error types is as follows: 1. Select and enable the errors to be monitored in Bits[5:3] of Register 0x480 to Bits[5:3] of Register 0x487. See Table 20: by writing 1 to the corresponding bit, UEK, BDE and NIT error monitoring can be selected for each lane. These are enabled by default. 2. Write 0 to the corresponding bits from Bits[2:0] of Register 0x480 to Bits[2:0] of Register 0x487 to bring the counters out of reset. 3. Per Table 20, by writing SYNC_ASSERT_MASK (Bits[2:0] of Register 0x47D), enable the sync-trigger mask for each error type. 4. Program the required error-counter threshold into ERRORTHRES (Register 0x47C). 5. For each error type enabled in the SYNC_ASSERT_MASK register, if the error counter on any lane reaches the programmed threshold, SYNCOUTx‾± falls and issues a synchronization request. When link reinitialization occurs, all error counts are reset. The IRQ is not reset and must be reset manually.

中文 — 意外控制字符，NIT，差异 IRQs： 对于 UEK 字符、NIT 和差异错误，错误计数超过阈值的事件可作为 IRQ 事件。通过写入寄存器 0x4B8 的 Bit[7:5]启用 IRQ 事件。启用 IRQ 后，可在寄存器 0x4BA 的 Bit[7:5]处读取 IRQ 事件状态。

关于重置 IRQ 的信息，请参阅错误计数器和 IRQ 控制部分。关于 IRQ 的更多信息，请参阅中断请求操作部分。

需要重新初始化的错误：根据 JESD204B 规范第 7.1 节，当收到四个无效的差异字符或四个 NIT 字符时，自动发生链路重新初始化。当发生链路重新初始化时，重新同步请求至少有 5 个帧和 9 个八位字节的长度。

当差异错误、NIT 错误或 UEK 字符错误的错误计数达到一个可编程的错误阈值时，用户可以选择重新初始化链路。对某些错误类型启用重新初始化功能的过程如下。 1. 通过在寄存器 0x480 的 Bit[5:3]到寄存器 0x487 的 Bit[5:3]中选择并启用要监测的错误。参阅表 20，通过向对应位写入 1，每个通道都可以选择 UEK、BDE 和 NIT 错误监测。这些以默认值启用。 2. 在从寄存器 0x480 的 Bit[2:0]到寄存器 0x487 的 Bit[2:0]的相应位写入 0，使计数器脱离复位。 3. 根据表 20，通过写入 SYNC_ASSERT_MASK(寄存器 0x47D 的 Bit[2:0])，为每种类型的错误启用同步触发屏蔽掩码。 4. 将所需的错误计数器阈值编入 ERRORTHRES（寄存器 0x47C）。 5. 对于 SYNC_ASSERT_MASK 寄存器中启用的每种错误类型，如果任何通道上的错误计数器达到编程的阈值，SYNCOUTx± 下降，发出一个同步请求。当链路重新初始化发生时，所有的错误计数被重置。IRQ 不会复位，必须对其手动复位。

表 20 Sync Assertion Mask (SYNC_ASSERT_MASK) / Table 20. Sync Assertion Mask

地址 / Address	位号 / Bit	位名称 / Bit Name	描述 / Description
0x47D	2	BDE	设置为 1，则发送 SYNCOUTx±，如果差异错误计数达到阈值 / Set to 1 to assert SYNCOUTx± if the disparity error count reaches the threshold
0x47D	1	NIT	设置为 1，则发送 SYNCOUTx±，如果 NIT 错误计数达到阈值 / Set to 1 to assert SYNCOUTx± if the NIT error count reaches the threshold
0x47D	0	UEK	设置为 1，则发送 SYNCOUTx±，如果 UEK 字符错误计数达到阈值 / Set to 1 to assert SYNCOUTx± if the UEK character error count reaches the threshold

2.8 CGS、帧同步、校验和和 ILAS 监控 / 2.8 CGS, Frame Synchronization, Checksum and ILAS Monitoring

English: Registers 0x470 to 0x473 can be monitored to verify whether each stage of JESD204B link establishment has occurred.

If link lane x has received at least 4 K28.5 characters and passed code group synchronization, bit x of CODE_GRP_SYNC (Register 0x470) is high.

If link lane x has completed initial frame synchronization, bit x of FRAME_SYNC (Register 0x471) is high.

For lane x, if the checksum sent over the lane matches the sum of the JESD204B parameters sent over the lane during ILAS, bit x of GOOD_CHECKSUM (Register 0x472) is high. These parameters can be added by summing the individual fields in the registers or by summing the packed registers. The computed checksum is the low 8 bits of the sum of the following fields: DID, BID, LID, SCR, L−1, F−1, K−1, M−1, N−1, SUBCLASSV, NP−1, JESDV, S−1 and HD.

If link lane x has passed the initial lane alignment sequence, bit x of INIT_LANE_SYNC (Register 0x473) is high.

CGS, frame synchronization, checksum and ILAS IRQs. The fault signals of CGS, frame synchronization, checksum and ILAS can serve as IRQ events. Enable them by writing Bits[3:0] of Register 0x4B8. After the IRQ is enabled, the IRQ event status can be read at Bits[3:0] of Register 0x4BA. Write 1 to Bit 0 of Register 0x4BA to reset the CGS IRQ. Write 1 to Bit 1 of Register 0x4BA to reset the frame synchronization IRQ. Write 1 to Bit 2 of Register 0x4BA to reset the checksum IRQ. Write 1 to Bit 3 of Register 0x4BA to reset the ILAS IRQ. For more information, see the Interrupt Request Operation section.

Configuration mismatch IRQ. The SXD052 has a configuration mismatch flag that can serve as an IRQ event. Use Bit 0 of Register 0x4B9 to enable the mismatch flag (enabled with the default value), then use Bit 0 of Register 0x4BB to read back the status and reset the IRQ signal. For more information, see the Interrupt Request Operation section.

When the link configuration settings (Registers 0x450 to 0x45D) do not match the JESD204B settings received by the device (Registers 0x400 to 0x40D), the configuration mismatch event flag is high.

This function differs from the good checksum flag in Register 0x472. The good checksum flag ensures that the transmit checksum based on the transmit settings matches a computed checksum. The configuration mismatch event ensures that the transmit settings match the configuration settings.

中文： 可以通过监测寄存器 0x470 至寄存器 0x473，以验证 JESD204B 链路建立的每个阶段是否已经发生。

如果链路 x 收到至少 4 个 K28.5 字符并通过码组同步，则 CODE_GRP_SYNC（寄存器 0x470）的第 x 位为高电平。

如果链路通道 x 完成初始帧同步，则 FRAME_SYNC（寄存器 0x471）的位 x 为高电平。

对于通道 x，如果通过通道发送的校验和，与在 ILAS 期间通过通道发送的 JESD204B 参数之和相匹配，则 GOOD_CHECKSUM（寄存器 0x472）的第 x 位为高电平。这些参数可以通过对寄存器中的单个字段求和，或对打包的寄存器求和来添加。计算的校验和是以下字段之和的低 8 位：DID、BID、LID、SCR、L - 1、F - 1、K - 1、M - 1、N - 1、SUBCLASSV、NP - 1、JESDV、S - 1 和 HD。

如果链路通道 x 通过了初始通道对齐序列，INIT_LANE_SYNC（寄存器 0x473）的位 x 为高电平。

CGS、帧同步、校验和以及 ILAS IRQs：可以将 CGS、帧同步、校验和以及 ILAS 的故障信号作为 IRQ 事件。通过写入寄存器 0x4B8 的 Bit[3:0]启用它们。启用 IRQ 后，可在寄存器 0x4BA 的 Bit[3:0]处读取 IRQ 事件状态。向寄存器 0x4BA 的 Bit0 写 1，重置 CGS IRQ。向寄存器 0x4BA 的 Bit1 写 1，重置帧同步 IRQ。向寄存器 0x4BA 的 Bit2 写 1，重置校验和 IRQ。向寄存器 0x4BA 的 Bit3 写 1，复位 ILAS IRQ。更多信息请参见中断请求操作部分。

配置失配 IRQ：SXD052 有配置失配标志，可作为 IRQ 事件。使用寄存器 0x4B9 的 Bit0 启用失配标志（使用默认值启用），然后使用寄存器 0x4BB 的 Bit0 回读状态并重置 IRQ 信号。更多信息请参见中断请求操作部分。

当链路配置设置（寄存器 0x450 到寄存器 0x45D）不匹配器件接收到的 JESD204B 设置（寄存器 0x400 到寄存器 0x40D）时，配置失配事件标志为高电平。

这个功能不同于寄存器 0x472 中的优良校验和标志。优良校验和标志确保了基于发射设置的发射校验和与一个计算校验和相匹配。配置失配事件确保了发射设置匹配配置设置。

3、数字数据通路 / 3. Digital Data Path

English: The SXD052 has two independent digital datapaths, which normally provide data samples to their respective DACx cores respectively. However, through the modulator switch configuration, other methods can also be used to send samples to DAC0, DAC1, or both DACs. For more details, see the Modulator Switch section.

Each digital datapath consists of multiple channel datapaths (channelizers) that are summed into one datapath (the main datapath), which by default connects to its respective DAC core (see Figure 1).

Depending on the JESD204B mode selected by the user, the channelizers and the main datapath can be completely bypassed. Within the channelizers and the main datapath there are multiple digital processing blocks, including interpolation filters, bypassable NCOs that allow digital I/Q modulation of samples or independent (DDS) operation, a power-amplifier protection block (the power detection and protection (PDP) block), and digital gain blocks for ramping or setting sample gain.

中文： SXD052 有两个独立的数字数据通路，通常分别向各自的 DACx 内核提供数据样本。不过，通过调制器开关配置，还可以采用其他方法将样本送至 DAC0、DAC1 或两个 DAC。更多详情，请参阅调制器开关部分。

每个数字数据通路都由多个通道数据通路（信道器）组成，这些通道数据通路汇总成一个数据通路（主数据通路），默认情况下，主数据通路又连接到各自的 DAC 内核（见图 1）。根据用户选择的 JESD204B 模式，通道器和主数据通路完全可以被旁路掉。信道器和主数据通路内有多种数字处理模块，包括插值滤波器、允许样本数字 I/Q 调制或独立（DDS）操作的可旁路 NCO、功率放大器保护模块（功率检测和保护(PDP) 模块）以及用于斜坡或设置采样增益的数字增益模块。

3.1 总数据通路插值 / 3.1 Total Datapath Interpolation

English: The SXD052 contains two stages of decimation filters: one stage is located within each channel datapath and is set to a single value across all channels; the other stage is located within each main datapath. Multiplying the channel interpolation factor by the main datapath interpolation factor determines the total interpolation of the entire digital datapath. The relationship between the DAC sample rate and the input data rate is as shown in the following equations: - Total interpolation = channel interpolation × main interpolation - fDATA = fDAC / (channel interpolation × main interpolation)

Each filter in the various cascaded half-band interpolation filters covers 80% of the total bandwidth (BW) occupied by the input data. Therefore, if interpolation is used (total interpolation > 1), the usable signal bandwidth is 80% of the data rate. If the interpolation stage is bypassed (total interpolation = 1), because complex data is not used, the usable signal bandwidth is 50% of the data rate.

The signal bandwidth is calculated as follows: - Signal BW = 0.8 × fDATA, if total interpolation > 1 - Signal BW = 0.5 × fDATA, if total interpolation = 1

Interpolation programming is as shown in Table 21.

中文： SXD052 包含两级细分滤波器：一级位于每个通道数据通路内，并在所有通道中设置为单一值；另一级位于每个主数据通路内。将通道内插系数乘以主数据通路内插系数，即可确定整个数字数据通路的总插值。DAC 采样率与输入数据率之间的关系如下式所示： 总插值=通道插值×主插值 fDATA=fDAC（通道插值×主插值）

各种级联半带插值滤波器中的每个滤波器都能覆盖输入数据所占总带宽(BW)的 80%。因此，如果使用插值（总插值> 1），可用信号带宽为数据速率的 80%。如果绕过插值级（总插值=1），由于不使用复合数据，可用信号带宽为数据速率的 50%。

信号带宽的计算方法如下： 信号 BW=0.8×fDATA，如果总插值>1 信号 BW=0.5×fDATA，如果总插值=1

插值编程如表 21 所示。

表 21 插值因子寄存器设置 / Table 21. Interpolation Factor Register Settings

插值系数 / Interpolation Factor	主数据路径，寄存器 0x111，位[7:4] / Main Datapath, Register 0x111, Bits[7:4]	通道数据路径，寄存器 0x111，位[3:0] / Channel Datapath, Register 0x111, Bits[3:0]
1×	0x1	0x1
2×	0x2	0x2
3×	不适用 / Not applicable	0x3
4×	0x4	0x4
6×	0x6	0x6
8×	0x8	0x8
12×	0xC	不适用 / Not applicable

表 22 插值模式和可用带宽 / Table 22. Interpolation Modes and Usable Bandwidth

总插值 / Total Interpolation	可用信号带宽 / Usable Signal Bandwidth	fDATA
1×（旁路 / bypass）	0.5×fDATA	fDAC
2×, 4×, 6×, 8×, 12×, 16×, 18×, 24×, 32×, 36×, 48×, 64×	0.8×fDATA	fDAC/总插值 / fDAC/total interpolation

3.1.1 滤波器性能 / 3.1.1 Filter Performance

English: The interpolation filters interpolate the input data samples so that the variation of the input data is minimized, while suppressing any interpolation images. As shown in Table 22, the usable bandwidth refers to the frequency band in which the filter passband ripple is less than ±0.001 dB and the image rejection is greater than 85 dB. Figure 28 and Figure 29 are conceptual diagrams of the relative bandwidth of each filter. All filters have the same maximum passband amplitude. In Figure 28 and Figure 29, different amplitudes are deliberately shown for ease of understanding; in fact, regardless of the interpolation rate the user selects, the amplitude of all filters is constant and consistent.

中文： 插值滤波器对输入的数据样本进行插值，使输入数据的变化最小，同时抑制任何插值图像。如表 22 所示，可用带宽是指滤波器通带纹波小于±0.001dB 且图像抑制大于 85 dB 的频带。图 28 和图 29 是每个滤波器相对带宽的概念图。所有滤波器的最大通带振幅相同。在图 28 和图 29 中，为了加深理解，特意显示了不同的振幅，实际上，无论用户选择何种插值率，所有滤波器的振幅都是恒定一致的。

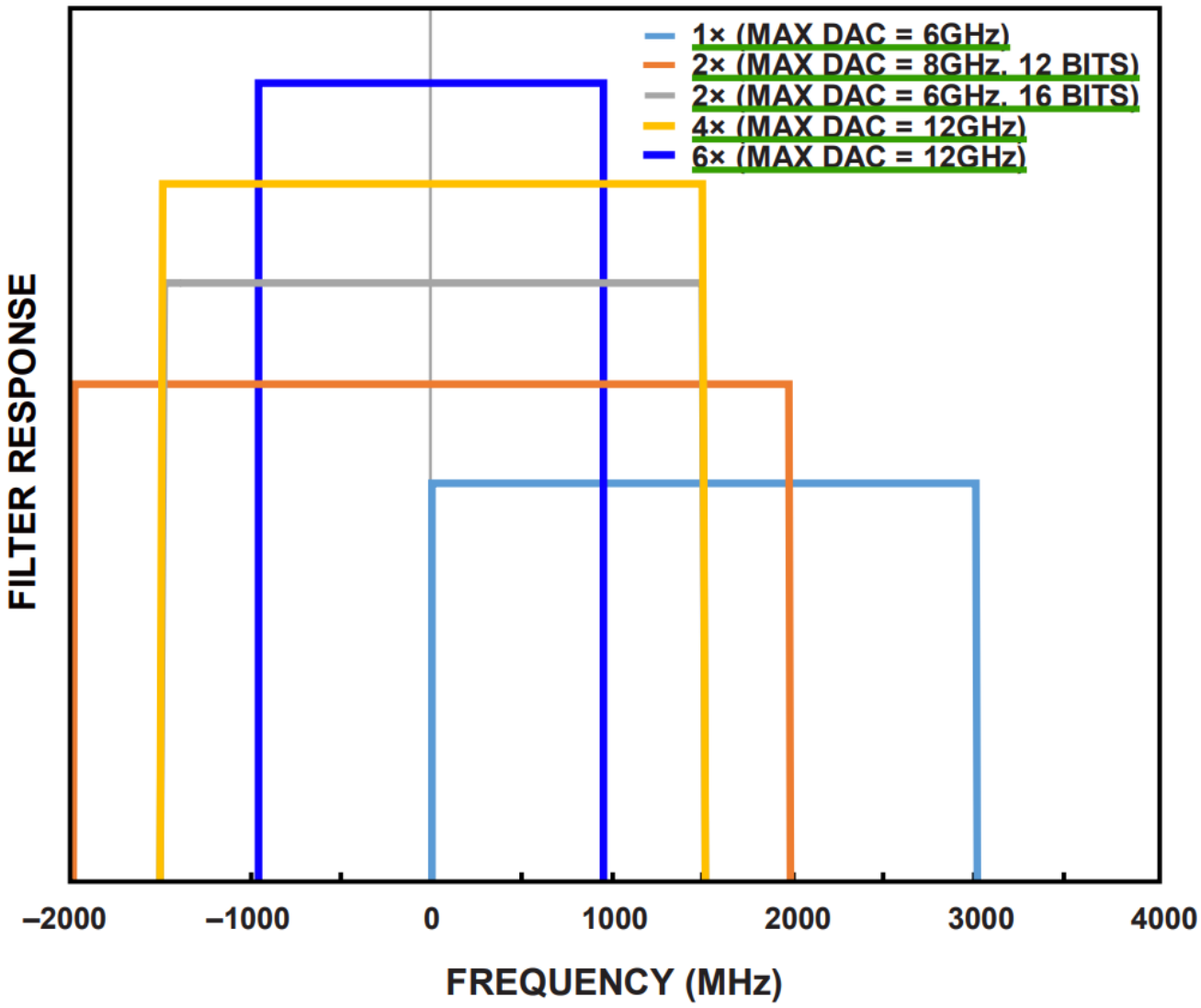


Figure 28: Band response for total interpolation rates of 1×, 2×, 4× and 6× at the maximum achievable DAC rates and resolutions

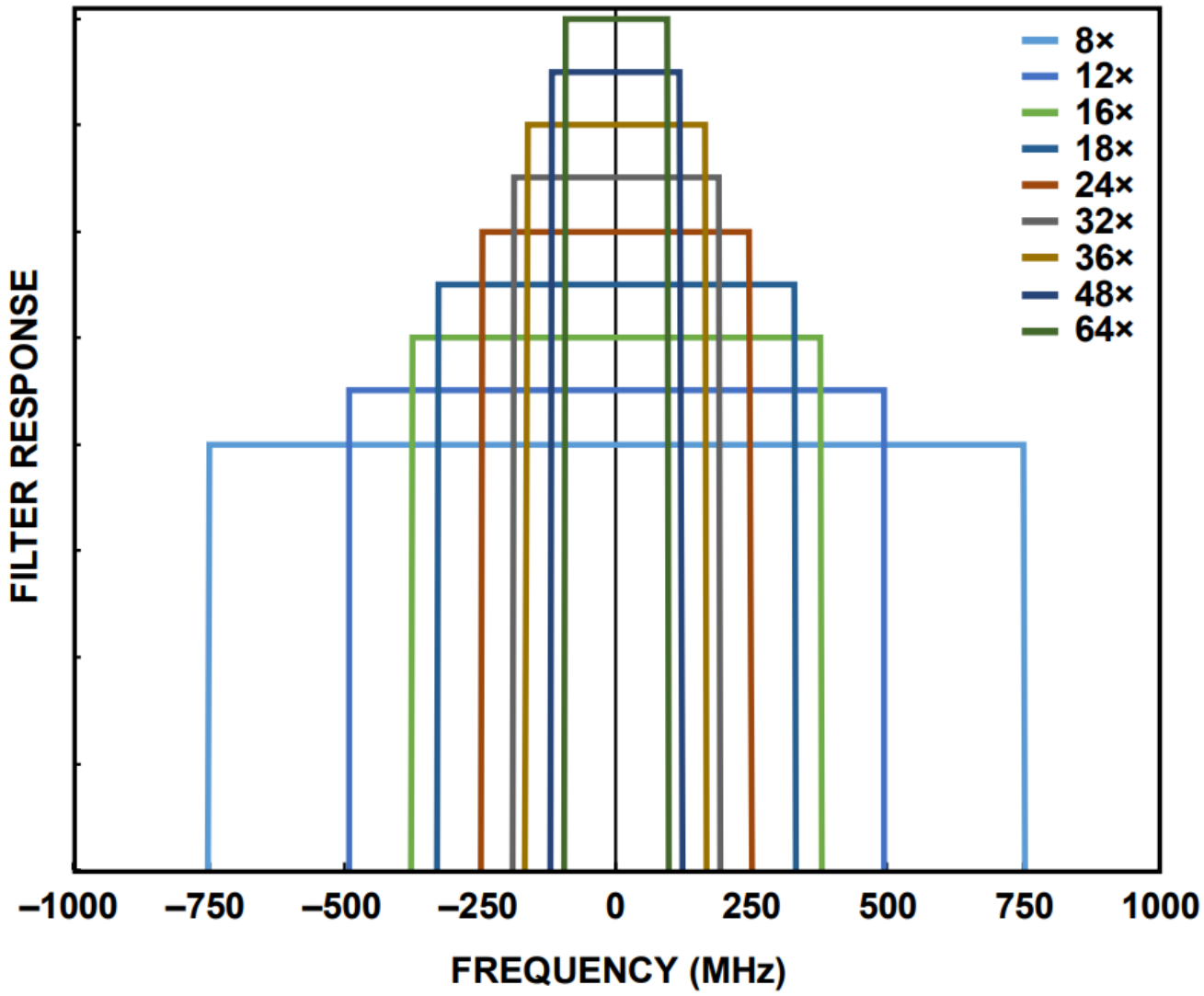


Figure 29: Band response at 12GHz for total interpolation rates of 8×, 12×, 16×, 18×, 24×, 32×, 36× and 64×

3.2 通道数字数据通路 / 3.2 Channel Digital Datapath

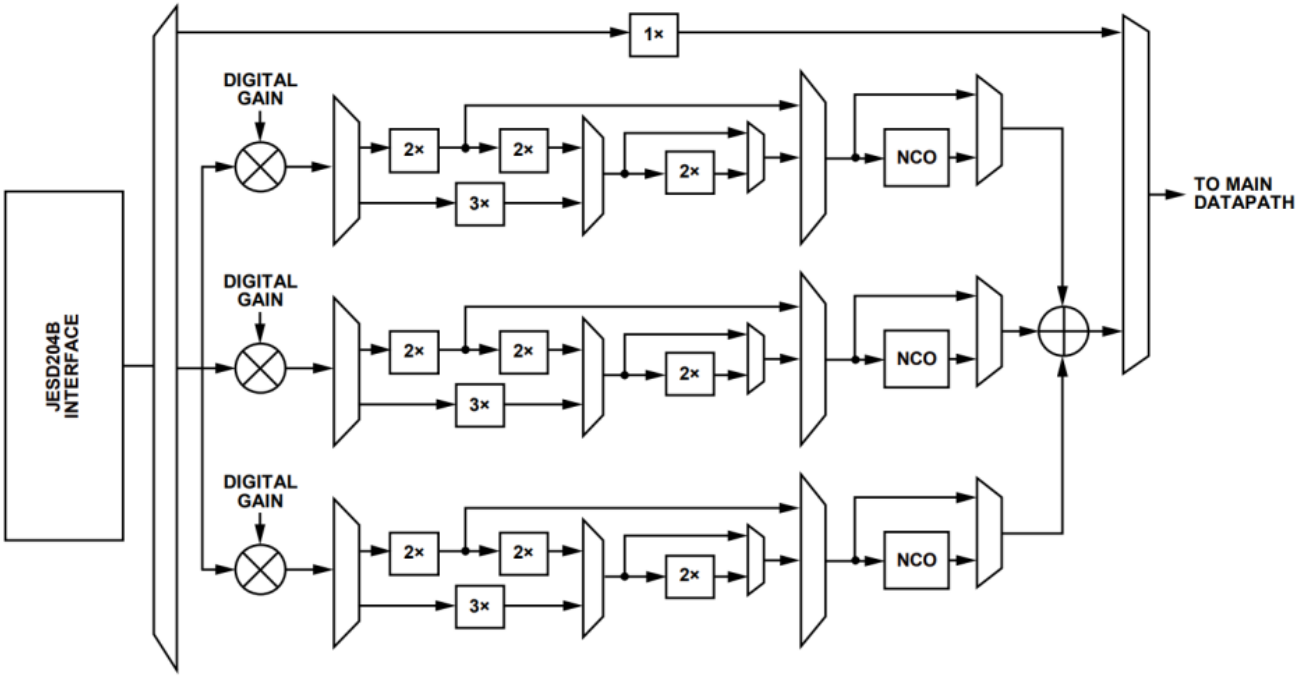


Figure 30: Channel digital datapath block diagram per main DAC output

English: The JESD204B mode selected by the user determines whether one or all channelizers in each datapath are enabled. Each channelizer consists of a digital gain stage, a complex interpolation block and a complex 48-bit modulus NCO. The channelizers and the summing node can be completely bypassed (the 1× interpolation option). The interpolation rate selection applies to all channelizers and cannot be controlled individually. However, the gain stage and complex NCO settings can each be controlled independently. The control of these blocks is paged by the channel paging mask in the CHANNEL_PAGE bits (Bits[5:0] of Register 0x008), as described in Table 23. Each bit of the paging mask corresponds to one channel datapath. The channelizers can be paged individually to apply settings specific to a particular channel, or paged as a group to address multiple channelizers with a single set of SPI writes.

中文： 用户选择的 JESD204B 模式决定了是否启用每个数据通路中的一个或全部信道器。每个信道器由数字增益级、复数插值块和复数 48 位模量 NCO 组成。信道器和求和节点可以完全旁路（1×插值选项）。插值率选择适用于所有信道器，不能单独控制。不过，增益级和复数 NCO 设置均可独立控制。这些模块的控制由 CHANNEL_PAGE 位（寄存器 0x008 的 Bit[5:0]）中的通道分页掩码进行分页，如表 23 所述。分页掩码的每一位都对应一个通道数据通路。信道器可以单独分页，以应用特定通道特有的设置，也可以分组分页，使用单组 SPI 写入寻址多个信道器。

表 23 通道页面屏蔽 / Table 23. Channel Page Mask

频道页面（寄存器 0x008，位 [5:0]）/ Channel Page (Register 0x008, Bits[5:0])	通道分页 / Channel Page	通道数据通路已更新 / Channel Datapath Updated
0x01（位 0 / Bit 0）	通道 0 / Channel 0	DAC0 的通道 0 / DAC0 Channel 0
0x02（位 1 / Bit 1）	频道 1 / Channel 1	DAC0 的通道 1 / DAC0 Channel 1
0x04（位 2 / Bit 2）	频道 2 / Channel 2	DAC0 的通道 2 / DAC0 Channel 2
0x08（位 3 / Bit 3）	频道 3 / Channel 3	DAC1 的通道 0 / DAC1 Channel 0

频道页面（寄存器 0x008，位 [5:0]）/ Channel Page (Register 0x008, Bits[5:0])	通道分页 / Channel Page	通道数据通路已更新 / Channel Datapath Updated
0x10（位 4 / Bit 4）	频道 4 / Channel 4	DAC1 的通道 1 / DAC1 Channel 1
0x20（位 5 / Bit 5）	频道 5 / Channel 5	DAC1 的通道 2 / DAC1 Channel 2

3.2.1 数字增益 / 3.2.1 Digital Gain

English: Each channelizer has an independent gain control that can apply unique gain scaling to each complex data stream. The gain code of each channel has 12-bit resolution, located in Registers 0x146 and 0x147, and can be calculated by the following formulas: - 0 ⩽ Gain ⩽ $(2^{12}-1)/2^{11}$ - −∞ dB < dB Gain ⩽ +6.018 dB - Gain = Gain code × (1/2048) - dB Gain = 20 × $\log_{10}$(Gain) - Gain Code = 2048 × Gain = 2^{11} × 10^(dB Gain/20)

The gain code control (CHNL_GAIN) is paged by the channel page mask (CHANNEL_PAGE) in Bits[5:0] of Register 0x008.

Because the outputs of the three channels are all summed before the main datapath, great care must be taken when setting the gain to avoid clipping of samples when the combined amplitude after summing exceeds full scale. For example, if three channels are used and all three data streams contain samples greater than 1/3 of full scale, clipping may occur. In other words, at any given point in time, the sum of the samples at the outputs of all enabled channels must be between -2^{15} and $+(2^{15}-1)$.

The digital gain function can be used in all JESD204B modes, except when using 1× channel interpolation, because in that mode the channel digital processing functions are bypassed, as shown in Figure 31.

中文： 每个 channelizer 都有一个独立的增益控制，可对每个复数数据流进行独特的增益缩放。每个通道的增益代码为 12 位分辨率，位于寄存器 0x146 和寄存器 0x147，可通过以下公式计算： 0⩽增益⩽$(2^{12}-1)/2^{11}$ -∞dB< dB Gain ⩽+6.018dB Gain=Gain code×(1/2048) dB Gain=20×log10(Gain) Gain Code=2048×Gain=2^{11}×10(dB Gain/20)

增益代码控制（CHNL_GAIN）被寄存器 0x008 的 Bit[5:0] 中的通道页面屏蔽（CHANNEL_PAGE）所分页。

由于三个通道的输出都是在主数据通路之前求和的，因此在设置增益时要格外小心，以避免在求和后组合幅度超过满刻度，从而出现采样削波。例如，如果使用了三个通道，且三个数据流都包含大于 1/3 满刻度的采样，则可能出现削波。换言之，在任何特定时间点，所有启用通道输出端的采样之和必须介于-2^{15} 和$+(2^{15}-1)$之间。

数字增益功能可用于所有 JESD204B 模式，但使用 1×通道插值时除外，因为在该模式下通道数字处理功能被旁路，如图 31 所示。

3.2.2 通道插值 / 3.2.2 Channel Interpolation

English: The channel interpolation options include bypass (1×), 2×, 3×, 4×, 6× and 8×. Each half-band filter used for interpolation has up to 80% bandwidth and 85 dB of stopband rejection. The channel half-band cascade configuration is shown in Figure 31, and Table 24 lists the usable bandwidth of each channel decimation [原文"细分" / source wording] filter.

中文： 通道插值选项包括旁路(1×)、2×、3×、4×、6×和 8×。每个用于插值的半带滤波器都具有高达 80%的带宽和 85dB 的阻带抑制。通道半带级联配置如图 31 所示，表 24 列出了每个通道细分滤波器的可用带宽。

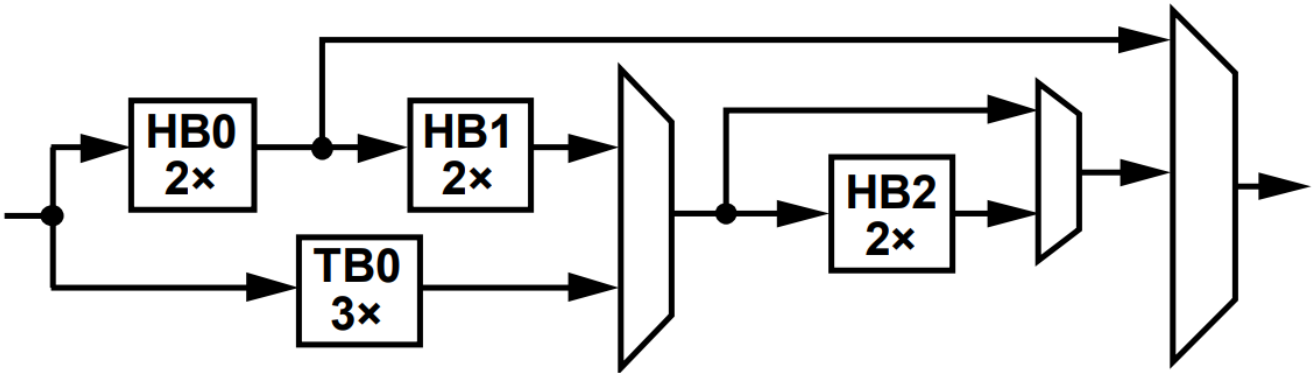


Figure 31: Channel interpolation half-band filter block diagram

表 24 通道插值的可用带宽和抑制 / Table 24. Usable Bandwidth and Rejection of Channel Interpolation

半带滤波器 / Half-Band Filter	带宽 (×fIN_FILTER1)(%) / Bandwidth (% × fIN_FILTER1)	停止带抑制 (dB) / Stopband Rejection (dB)
HB0	80	85
TB0	54	85
HB1	40	85
HB2	27	85

3.2.3 通道数字调制 / 3.2.3 Channel Digital Modulation

English: Each channelizer includes a 48-bit dual-modulus NCO that can I/Q-modulate each channel's data to an independent carrier frequency, with each channelizer having its own phase offset control. The 48-bit NCO can be configured in integer or modulus (DDS) mode. In modulus mode, the A/B ratio is added to the integer FTW of the NCO, enabling frequency synthesis with almost unlimited precision. See the 48-bit integer/modulus NCO section for more information. The NCO mode selection is as shown in Table 25. These controls are paged by the channel page mask in the CHANNEL_PAGE bits (Bits[5:0] of Register 0x008).

The channel NCO block also contains a sideband selection control and options for how the FTW and phase offset controls are updated. The phase offset word control is calculated as follows: - −180° ⩽ degree offset ⩽ +180° - Degree offset = 180° × (DDSC_NCO_PHASE_OFFSET/2)[15]

where DDSC_PHASE_OFFSET is the 16-bit two's-complement value programmed in the registers listed in Table 26.

中文： 每个信道处理器都包括一个 48 位双模量 NCO，可对每个通道数据进行 I/Q 调制，使其达到独立的载波频率，每个信道都有自己的相位偏移控制。48 位 NCO 可配置为整数或模量(DDS)模式。在模量模式下，A/B 比率加到 NCO 的整数 FTW 上，可实现近乎无限精度的频率合成。请参阅 48 位整数/模数 NCO 部分获取更多信息。NCO 模式的选择如表 25 所示。这些控制按 CHANNEL_PAGE 位（寄存器 0x008 的 Bit[5:0]）中的通道页面屏蔽进行分页。

通道 NCO 模块还包含边带选择控制以及如何更新 FTW 和相位偏移控制的选项。相位偏移字控制的计算方法如下： -180°⩽度数偏移⩽+180° 度数偏移=180°×(DDSC_NCO_PHASE_OFFSET/2)15

其中，DDSC_PHASE_OFFSET 是表 26 所列寄存器中编程的 16 位二位二进制值。

表 25 通道调制模式选择 / Table 25. Channel Modulation Mode Selection

调制模式 / Modulation Mode	调制类型 — 寄存器 0x130，第 6 位 / Register 0x130, Bit 6	调制类型 — 寄存器 0x130，第 2 位 / Register 0x130, Bit 2
无 / None	0b0	0b0
48 位整数 NCO / 48-bit integer NCO	0b1	0b0
48 位双模数 NCO / 48-bit dual-modulus NCO	0b1	0b1

表 26 通道 NCO 相位偏移寄存器 / Table 26. Channel NCO Phase Offset Registers

地址 / Address	价值 / Value	说明 / Description
0x138	DDSC_NCO 相位偏移[7:0]	8 LSB 相位偏移 / 8 LSBs of phase offset
0x139	DDSC_NCO_PHASE_OFFSET[15:8]	8 个 MSB 相位偏移 / 8 MSBs of phase offset

3.2.4 48 位整数/模量 NCO / 3.2.4 48-Bit Integer/Modulus NCO

English: The 48-bit integer/modulus NCO combines an NCO block, a phase shifter and a complex modulator to modulate the signal onto a user-defined carrier frequency, as shown in Table 27. With this configuration, the output signal can be phase-shifted to any position in the output spectrum, with a frequency resolution up to ±fNCO/2.

The NCO generates a quadrature carrier that converts the input signal to a new center frequency. The quadrature carrier is a pair of sine waveforms of the same frequency, offset from each other by 90°. The frequency of the quadrature carrier is set by the FTW. As shown in Figure 32, the quadrature carrier is mixed with the I and Q data and then summed into the I and Q datapaths.

Each channel 48-bit NCO can be configured to operate in integer mode (i.e. only the FTW value defines the NCO output frequency). The FTW value partly depends on the clock speed at which the NCO block operates (fNCO,CLK). For any channel NCO, the clock rate equals the rate of the summing node (maximum 1.575 GSPS), and can be calculated by the following formula: fNCO,CLK = fDATA × channel interpolation, or fNCO,CLK = fDAC/main interpolation = fSUMMING_NODE

The FTW of each NCO can be programmed individually and calculated by the following formula: −fNCO,CLK/2 ⩽ fCARRIER < fNCO,CLK/2; DDSC_FTW = (fCARRIER/fNCO,CLK) × 2^{48}

where DDSC_FTW is a 48-bit binary number, fCARRIER is the output frequency of the NCO, and fNCO,CLK is the sampling clock frequency of the NCO. The frequency tuning word settings are as shown in Table 27.

Unlike other NCO control registers, the FTW registers are not applied to the NCO block immediately after the control registers are written. Instead, the FTW registers are applied on the rising edge of DDSC_FTW_LOAD_REQ (Bit 0 of Register 0x131) after the control registers are written. After the update request is issued, DDSC_FTW_LOAD_ACK (Bit 1 of Register 0x131) must show a high state to confirm that the FTW has been updated.

The DDSC_SEL_SIDEBAND bit (Bit 1 of Register 0x130 = 0b1) is a convenience bit used to control whether the lower sideband or the upper sideband is used (for modulating data), equivalent to flipping the sign of the FTW.

中文： 48 位整数/模数 NCO 将一个 NCO 模块、一个移相器和一个复合调制器结合在一起，将信号调制到用户定义的载波频率上，如表 27 所示。通过这种配置，输出信号可以在输出频谱的任意位置进行移相，频率分辨率可达±fNCO/2。

NCO 产生正交载波，将输入信号转换为新的中心频率。正交载波是一对频率相同、相互偏移 90°的正弦波形。正交载波的频率通过 FTW 设置。如图 32 所示，正交载波与 I 和 Q 数据混合，然后汇总到 I 和 Q 数据通路中。

每个通道 48 位 NCO 都可以配置为整数模式运行（即只有 FTW 值定义 NCO 输出频率）。FTW 值部分取决于 NCO 块运行的时钟速度（fNCO,CLK）。对于任何通道 NCO，时钟速率都等于求和节点的速率（最大为 1.575GSPS），并可通过以下公式计算： fNCO,CLK=fDATA×通道插值 或 fNCO,CLK=fDAC/主插值 =fSUMMING_NODE

每个 NCO 的 FTW 可以单独编程，并通过以下公式计算： -fNCO,CLK/2≤fCARRIER<fNCO,CLK/2; DDSC_FTW=(fCARRIER/fNCO,CLK)×2^{48}

其中，DDSC_FTW 是一个 48 位的二进制数。fCARRIER 是 NCO 的输出频率。fNCO,CLK 是 NCO 的采样时钟频率。频率调整字的设置如表 27 所示。

与其他 NCO 控制寄存器不同，FTW 寄存器不会在写入控制寄存器后立即应用于 NCO 块。相反，FTW 寄存器是在写入控制寄存器后 DDSC_FTW_LOAD_REQ（寄存器 0x131 的 Bit0）的上升沿应用。更新请求发出后，DDSC_FTW_LOAD_ACK（寄存器 0x131 的 Bit1）必须显示高电平状态，以确认 FTW 已更新。

DDSC_SEL_SIDEBAND 位（寄存器 0x130 的 Bit1=0b1）是一个便利位，用于控制使用下边带还是上边带（用于调制数据），相当于翻转 FTW 的符号。

表 27 通道 NCO FTW 寄存器 / Table 27. Channel NCO FTW Registers

地址 / Address	价值 / Value	说明 / Description
0x132	DDSC_FTW[7:0]	8 LSB 的 FTW / 8 LSBs of FTW
0x133	DDSC_FTW[15:8]	FTW 的下八个比特 / Next 8 bits of FTW
0x134	ddsc_ftw[23:16]	FTW 的下八个比特 / Next 8 bits of FTW
0x135	ddsc_ftw[31:24]	FTW 的下八个比特 / Next 8 bits of FTW
0x136	ddsc_ftw[39:32]	FTW 的下八个比特 / Next 8 bits of FTW
0x137	ddsc_ftw[47:40]	FTW 的 8 个 MSB / 8 MSBs of FTW

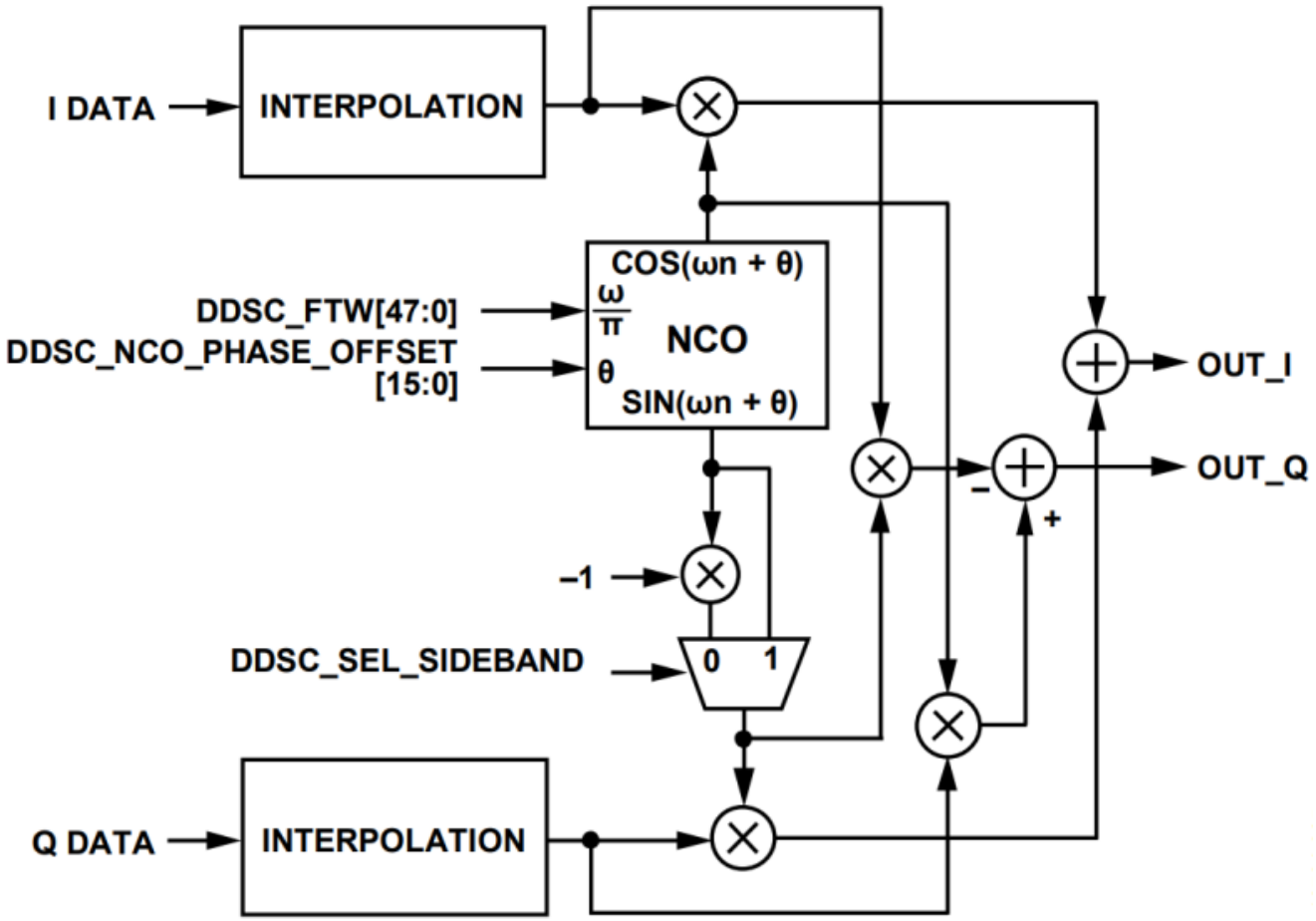


Figure 32: NCO modulator block diagram

English — Channel modulus NCO mode (direct digital synthesis (DDS) mode): Each 48-bit channel NCO can also be used in dual-modulus mode to create fractional frequencies beyond the 48-bit precision provided by integer mode, which can be meaningful in applications where the NCO runs for a long time without reset, because even a small initial frequency error of a 48-bit integer NCO can cause significant phase drift relative to other clocks in the system. Modulus mode is enabled by programming the DDSC_MODULUS_EN bit in the DDSC_DATAPATH_CFG register to 1 (Bit 2 of Register 0x130 = 0b1).

The frequency ratio of the programmable-modulus DDS is very similar to that of a typical accumulator-based DDS. The only difference is that the programmable modulus does not require N to be an integer power of 2 (as in an integer NCO), but can be any integer. In practice, hardware constraints limit the range of N. Modulus therefore extends the application of the NCO to frequency synthesis applications requiring exact rational numbers. The basic function of the programmable-modulus technique is to change the modulus of the accumulator.

With the programmable-modulus function implemented in the SXD052, the fraction M/N can be expressed by the following equation. The equation represents a composite frequency tuning word, where X represents the integer part and A/B represents the fractional part: fCARRIER/fNCO,CLK = M/N = (X + A/B)/ 2^{48}.

where X is the FTW, the programmed value in Registers 0x132 to 0x137. A is the programmed value in Registers 0x140 to 0x145. B is the programmed value in Registers 0x13A to 0x13F.

Since X, A and B are all 48-bit words, modulus mode allows the user to set the NCO output frequency (fCARRIER) with a precision of (fNCO,CLK)/2^(2×48).

Programmable-modulus example. Assume fNCO,CLK = 1500 MHz and the desired value of fCARRIER is 150 MHz. In this case, the synthesized output frequency is not a power-of-2 fraction of the sample rate, i.e. fCARRIER = (1/10)fNCO,CLK, which is impossible for a typical accumulator-based DDS. For the frequency ratio fCARRIER/fNCO,CLK, by reducing the fraction (150M/1500M) to its lowest terms, M and N can be derived directly: M/N = 150M/1500M = 1/10, therefore M=1, N=10.

After calculation, X = 28,147,497,671,065, A = 3, B = 5. Programming these values into the registers of X, A and B (for DDSC_ACC_DELTAx, A is programmed in Registers 0x140 to 0x145; for DDSC_ACC_MODULUSx, B is programmed in Registers 0x13A to 0x13F; for DDSC_FTWx, X is programmed in Registers 0x132 to 0x137) makes the NCO produce an exact 150 MHz output frequency at a 1500 MHz sample clock.

NCO reset. Resetting the NCO is very useful when determining the start time and phase of a specific NCO. Each channel NCO can be configured to reset in response to one of the following events: a direct request via SPI (Bit 0 of Register 0x131), a change of the FTW register value, or the next SYSREF± rising edge. The reset method is controlled by Register 0x131. For more information, see the detailed description of Register 0x131.

中文 — 通道模数 NCO 模式（直接数字合成 (DDS) 模式）： 每个 48 位通道 NCO 还可用于双模量模式，以创建超出整数模式所提供的 48 位精度的分数频率，这在 NCO 长时间运行而不复位的应用中可能很有意义，因为即使 48 位整数 NCO 的初始频率误差很小，也可能导致相对于系统中其他时钟的明显相位漂移。通过将 DDSC_DATAPATH_CFG 寄存器中的 DDSC_MODULUS_EN 位编程为 1（寄存器 0x130 的 Bit2=0b1），可启用模量模式。

可编程模量 DDS 的频率比与典型的基于累加器的 DDS 非常相似。唯一不同的是，可编程模量不要求 N 是 2 的整数次幂（与整数 NCO 一样），而是可以是任意整数。实际上，硬件约束限制了 N 的取值范围。因此，模量将 NCO 的应用扩展到了需要精确有理数的频率合成的应用。可编程模量技术的基本功能是改变累加器的模量。

在 SXD052 中实现可编程模量功能后，分数 M/N 可用下式表示。等式表示一个复合频率调谐字，X 代表整数部分，A/B 代表分数部分。[原文公式排版残缺]

其中，X 是 FTW，在寄存器 0x132 至寄存器 0x137 中的编程值。A 是在寄存器 0x140 至寄存器 0x145 中的编程值。B 是在寄存器 0x13A 至寄存器 0x13F 中编程值。

由于 X、A 和 B 均为 48 位字，因此模量模式允许用户以(fNCO,CLK)/2(2 48)的精度设置 NCO 输出频率 (fCARRIER)。

可编程模量示例：假设 fNCO,CLK=1500MHz，而 fCARRIER 的期望值为 150MHz。这种情况下，合成的输出频率不是采样率的 2 次幂，即 fCARRIER=(1/10)fNCO,CLK，而这是不可能，对于一个典型的基于累加器的 DDS。对于频率比 fCARRIER/ fNCO,CLK，通过将分数（150M/1500M）化为最小项，可以直接得出 M 和 N，即 M/N=150M/1500M=1/10，因此，M=1，N=10。

经过计算，X=28,147,497,671,065，A=3，B=5。将这些值编程到 X、A 和 B 的寄存器中（对于 DDSC_ACC_DELTAx，A 在寄存器 0x140 至寄存器 0x145 中编程；对于 DDSC_ACC_MODULUSx，B 在寄存器 0x13A 至寄存器 0x13F 中编程；对于 DDSC_FTWx，X 在寄存器 0x132 至寄存器 0x137 中编程），使 NCO 在 1500 MHz 采样时钟下产生精确的 150 MHz 输出频率。

NCO 重置：在确定特定 NCO 的启动时间和相位时，复位 NCO 是非常有用的。每个通道 NCO 都可配置为响应以下事件之一而复位：通过 SPI（寄存器 0x131 的 Bit0）直接请求、FTW 寄存器值变化或处于下一个 SYSREF±上升沿。复位方法由寄存器 0x131 控制。更多信息，请参阅寄存器 0x131 的详细说明。

3.2.5 通道求和节点 / 3.2.5 Channel Summing Node

English: The outputs of the channelizers are combined at the summing node and then sent to their respective main datapaths. The summed value of any number of channels used must not exceed $\pm 2^{15}$, to avoid clipping (binary overflow) of the 16-bit data samples summed into the main datapath. When the channel interpolation is greater than 1×, the maximum data rate of each channel is limited by the maximum speed of the summing node, i.e. 1.575 GSPS. As shown in Figure 30, if the channel datapath is bypassed (channel interpolation of 1×), the summing node block is also bypassed. Bypassing the channelizers allows data to be transferred to the main digital datapath at a higher data rate. For the JESD204B modes and the corresponding maximum data rates, see Table 1.

中文： 信道器的输出在求和节点处合并，然后再送入各自的主数据通路。所使用的任何通道数的求和值范围不得超过$\pm 2^{15}$，以避免被求和到主数据通路的 16 位数据样本出现削波（二进制溢出）。当通道插值大于 1 倍时，每个通道的最大数据速率受限于求和节点的最大速度，即 1.575GSPS。如图 30 所示，如果将通道数据通路旁路掉（通道插值为 1×），求和节点模块也将被旁路掉。旁路掉信道器，可以按更高的数据速率向主数字数据通路传输数据。有关 JESD204B 模式和相应的最大数据速率，请参阅表 1。

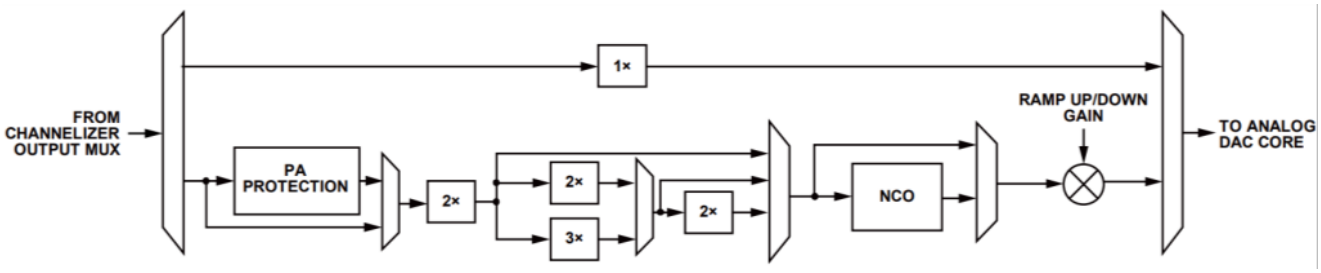


Figure 33: Main digital datapath block diagram per main DAC output

English: Each main digital datapath consists of a power-amplifier (PA) protection block, a set of complex interpolation filters, a 48-bit complex main datapath NCO, and a ramp-on/ramp-down gain stage. The main datapath can be bypassed (selecting 1× interpolation), thereby bypassing all digital processing blocks in the main datapath. All main datapath interpolation selections are set to the same value and cannot be controlled independently. However, the power-amplifier protection block, the complex NCO settings and the gain ramp can each be configured independently.

The control of these blocks is paged by the main DAC datapath paging mask MAINDAC_PAGE (Bits[7:6] of Register 0x008), as shown in Table 28. Each bit of the paging mask corresponds to one main DAC datapath. The datapaths can be paged individually to apply settings unique to a specific main datapath, or paged as a group to address both datapaths with a single set of SPI writes.

Each digital block in the main datapath is described in detail below.

中文： 每个主数字数据通路由一个功率放大器（PA）保护模块、一组复杂的插值滤波器、一个 48 位复数的主数据通路 NCO 和一个 ramp-on/ramp-down 增益级组成。主数据通路可以被旁路掉（选择 1×插值），从而将主数据通路中的所有数字处理模块都旁路掉。所有主数据通路的插值选择都被设置为相同的值，不能独立控制。不过，功率放大器保护模块、复数 NCO 设置和增益 ramp 均可独立配置。

这些模块的控制由主 DAC 数据通路分页掩码 MAINDAC_PAGE（寄存器 0x008 的 Bit[7:6]）分页，如表 28 所示。分页掩码的每一位都对应一个主 DAC 数据通路。数据通路可以单独分页，以应用特定主数据通路的唯一设置，也可以分页为一组，使用单组 SPI 写入来处理两个数据通路。

下文将详细介绍主数据通路中的每个数字模块。

表 28 主 DAC 数据通路页面屏蔽 / Table 28. Main DAC Datapath Page Mask

MAINDAC_PAGE（寄存器 0x008，位[7:6]）/ (Register 0x008, Bits[7:6])	DAC 分页 / DAC Page	DAC 数据通道已更新 / DAC Datapath Updated
0x40（Bit6）	DAC0	DAC0
0x80（Bit7）	DAC1	DAC1

3.2.6 下游保护（PA 保护）/ 3.2.6 Downstream Protection (PA Protection)

English: The SXD052 has multiple circuits that can quickly reduce (or suppress) the amplitude of samples about to reach either DAC core, thereby protecting power amplifiers or other external system components located downstream of the SXD052 output. As shown in Figure 34, the DACx output can ramp up or down gradually, turning on or off, according to the following trigger signals: - PDP_PROTECT. This signal indicates when the computed digital sample amplitude exceeds a programmable threshold. - INTERFACE_PROTECT. This signal indicates when a specific JESD204B error occurs. - SPI_PROTECT. This signal indicates when the user writes an SPI control register directly. - BSM_PROTECT. This signal triggers the blanking state machine (BSM) block, which flushes the datapath on the rising edge of the TXEN0 or TXEN1 signal (which may come from an SPI write or from the external TXEN0, TXEN1 pins).

When a trigger event occurs, the system triggers a series of flags, which can also be routed to the IRQx I/O pins ($\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$) to shut down other external downstream components or serve as indicators.

The DAC output on/off function is realized through the trigger-signal feedback of the ramp-up/ramp-down digital gain block in front of the analog DAC core at the end of the main datapath.

Power detection and protection (PDP) block. The PDP block computes the expected average power at the output of the DACx core, preventing the SXD052 from outputting out-of-range signals to avoid potentially destructive breakdown of power-sensitive devices (such as power amplifiers). The protection block provides a signal PDP_PROTECT, which can be used to reduce the DAC output or routed to an I/O pin to shut down flagged external components.

The PDP block uses an independent path with shorter delay than the datapath, to ensure that PDP_PROTECT is triggered before an out-of-range signal reaches the analog DAC core (except when the total interpolation is 1×). The sum of I^2 and Q^2 is computed as a representation of the input signal power (to shorten the response time, only the first six MSBs of the data samples are used). The computed sample power values are accumulated through a sliding-average filter, whose output is the average of the input signal power over a certain number of samples. There are two types of averaging filters, each with a different length: a short filter, used to detect high-power pulses that may cause voltage breakdown, and a long filter, used to detect sustained high-power signals whose duration may exceed the thermal time constant of a power amplifier or other device.

When the output of the averaging filter is greater than the threshold, the internal signal PDP_PROTECT goes high and can optionally be configured to trigger an IRQ flag and to shut down the DAC output through ramp-on/ramp-down. The PDP block function is shown in Figure 35.

The long averaging time and the short averaging time are controlled by LONG_PA_AVG_TIME (Bits[3:0] of Register 0x585) and SHORT_PA_AVG_TIME (Bits[1:0] of Register 0x58A). The averaging window size is determined using the following calculation: long averaging window = 2^(LONG_PA_AVG_TIME+9), short averaging window = 2^SHORT_PA_AVG_TIME.

When the computed average power exceeds the specified threshold, a trigger signal is issued. Table 29 lists the threshold programming registers of the long and short averaging filters, and the respective readback registers of the computed detected power.

中文： SXD052 具有多个电路，这些电路可快速降低（或抑制）即将到达任一 DAC 内核的样本幅度，从而保护位于 SXD052 输出下游的功率放大器或其他外部系统元件。如图 34 所示，DACx 输出可根据以下触发信号逐渐升高或降低，打开或关闭： PDP_PROTECT。该信号表征当计算出的数字采样振幅超过可编程阈值时。 INTERFACE_PROTECT。该信号表征当发生特定的 JESD204B 错误时。 SPI_PROTECT。该信号表征当用户直接写入 SPI 控制寄存器时。 BSM_PROTECT。该信号触发 blanking 状态机（BSM）模块，在 TXEN0 或 TXEN1 信号（可能来自 SPI 写入或外部 TXEN0、TXEN1 引脚）的上升沿到来时刷新数据通路。

在触发事件发生时，系统会触发一系列标志，这些标志也可被传输到 IRQx I/O 引脚（IRQ0¯和 IRQ1¯），以关闭其他外部下游元件或作为指示器。

通过主数据通路末端的模拟 DAC 内核前面的 ramp-up/ramp-down 数字增益块的反馈触发信号，可以实现 DAC 输出开/关功能。

电源检测和保护（PDP）模块：PDP 模块计算 DACx 内核输出的预期平均功率，防止 SXD052 输出超范围信号，以避免功率敏感器件（如功率放大器）发生潜在的破坏性击穿。保护模块提供一个信号 PDP_PROTECT，可用于降低 DAC 输出或寻径至 I/O 引脚，以关闭标记的外部元件。

PDP 模块使用比数据路径延迟更短的独立路径，以确保在超范围信号到达模拟 DAC 内核之前触发 PDP_PROTECT（总插值为 1 倍时除外）。计算出 I2 和 Q2 的总和，作为输入信号功率的代表（为缩短响应时间，仅使用数据样本的前六个 MSB）。计算出的样本功率值通过滑动均值滤波器累加，其输出是输入信号功率在一定样本数内的平均值。均值滤波器有两种类型，每种滤波器具有不同长度：短滤波器用于检测可能导致电压击穿的高功率脉冲，长滤波器用于检测持续时间可能高于功率放大器或其他设备热常数的持续高功率信号。

当均值滤波器的输出大于阈值时，内部信号 PDP_PROTECT 将变为高电平，可选择将其配置为触发 IRQ 的标志，并通过 ramp-on/ramp-down 关闭 DAC 输出。PDP 模块功能如图 35 所示。

长平均时间和短平均时间由 LONG_ PA_AVG_TIME（寄存器 0x585 的 Bit[3:0]）和 SHORT_ PA_AVG_TIME（寄存器 0x58A 的 Bit[1:0]）控制。使用以下计算方法确定平均窗口大小时间：长平均窗口 =2^(LONG_PP_AVG_TIME+9)，短平均窗口=2^SHORT_PA_AVG_TIME。

当计算出的平均功率超过指定阈值时，就会发出触发信号。表 29 列出了长均值滤波器和短均值滤波器的阈值编程寄存器，以及各自的计算检测功率的回读寄存器。

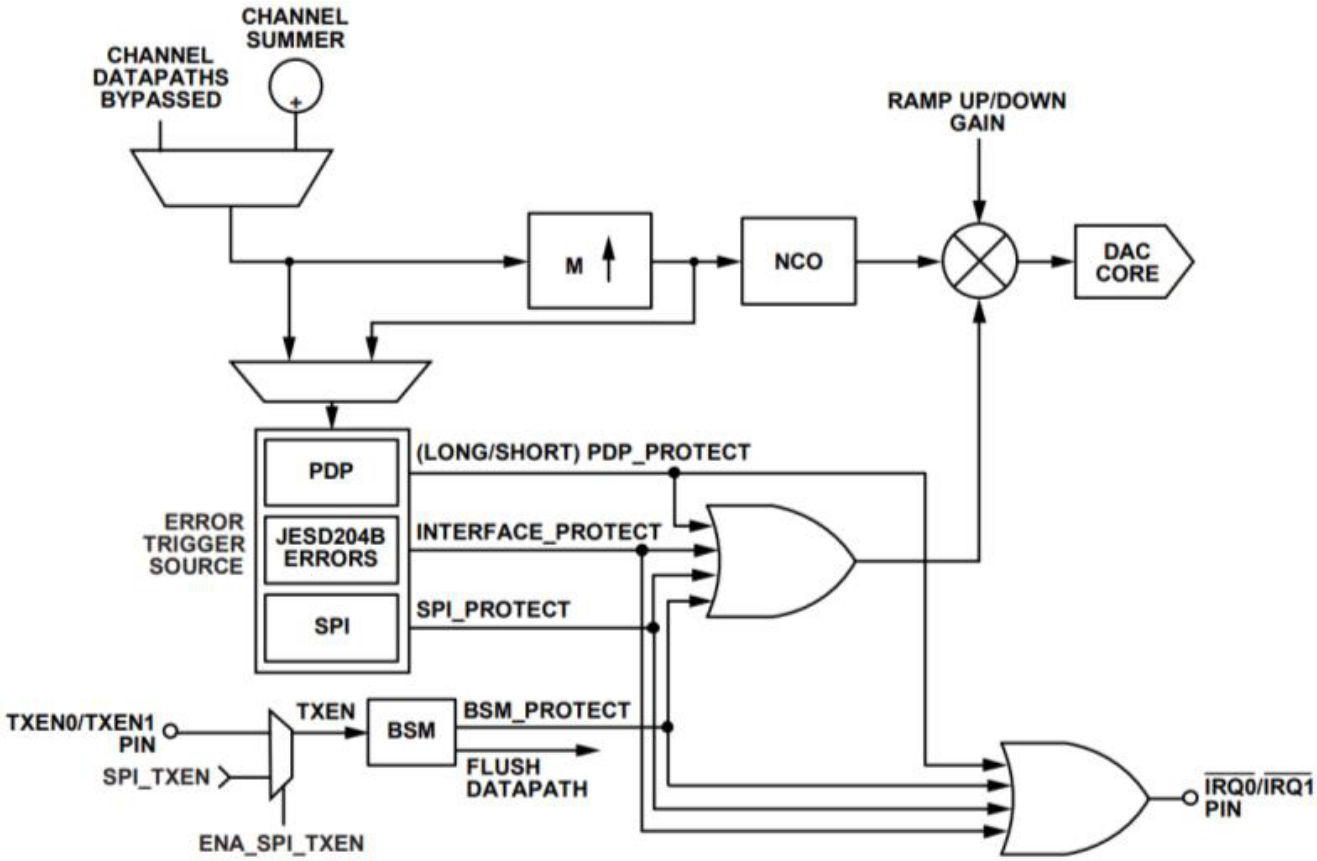


Figure 34: Downstream protection trigger block diagram

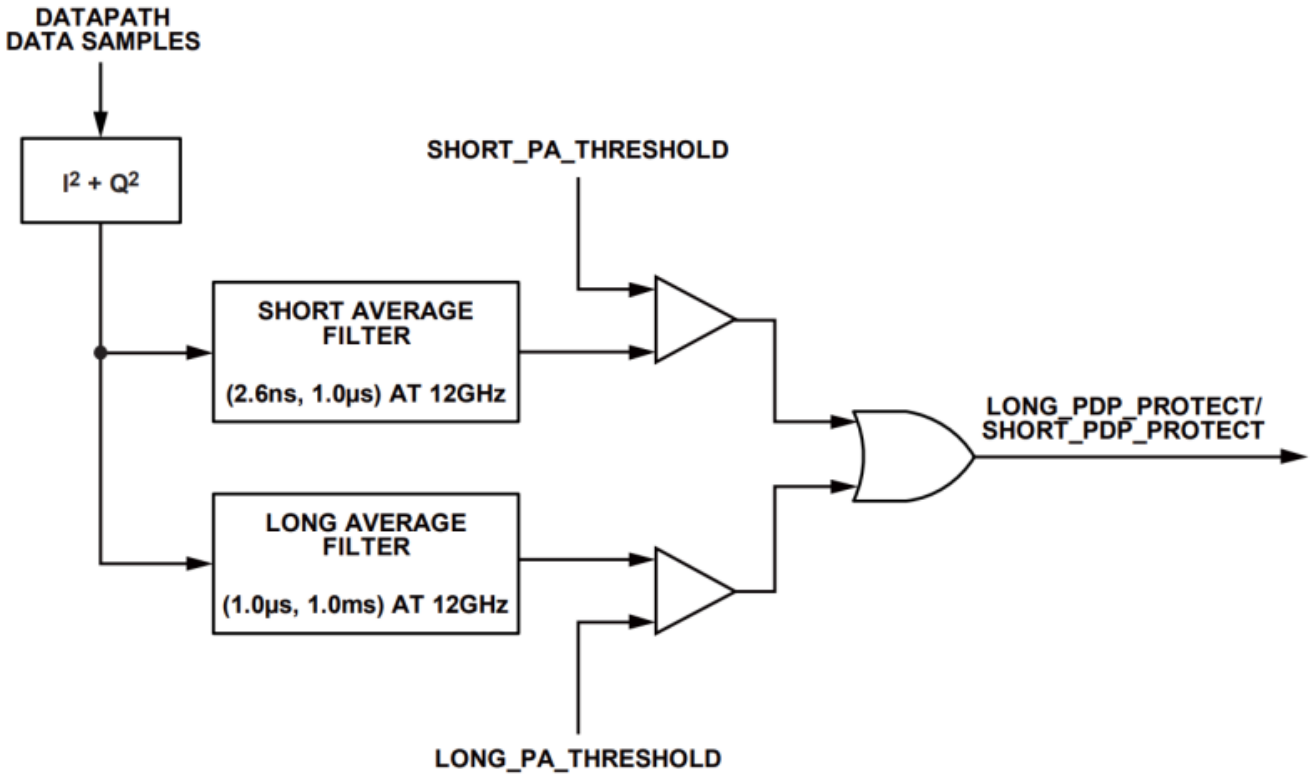


Figure 35: PDP block diagram

表 29 PDP 阈值和功率计算控制 / Table 29. PDP Threshold and Power Calculation Controls

注册 / Register	位 / Bits	控制 / Control
0x583	[7:0]	LONG_PA_THRESHOLD[7:0]
0x584	[4:0]	LONG_PA_THRESHOLD[12:8]
0x586	[7:0]	LONG_PA_POWER[7:0]
0x587	[4:0]	LONG_PA_POWER[12:8]
0x588	[7:0]	SHORT_PA_THRESHOLD[7:0]
0x589	[4:0]	SHORT_PA_THRESHOLD[12:8]
0x58B	[7:0]	SHORT_PA_POWER[7:0]
0x58C	[4:0]	SHORT_PA_POWER[12:8]

3.2.7 主数据通路插值 / 3.2.7 Main Datapath Interpolation

English: The interpolation options in the main datapath include bypass (1×), 2×, 4×, 6×, 8× and 12×. Each half-band filter used for interpolation has up to 80% bandwidth and 85 dB of stopband rejection. The channel half-band cascade configuration is shown in Figure 36, and Table 30 lists the usable bandwidth of each interpolation filter.

中文： 主数据通路中的插值选项包括旁路（1×）、2×、4×、6×、8×和 12×。每个用于插值的半带滤波器都具有高达 80%的带宽和 85dB 的阻带抑制。通道半带级联配置如图 36 所示，表 30 列出了每个插值滤波器的可用带宽。

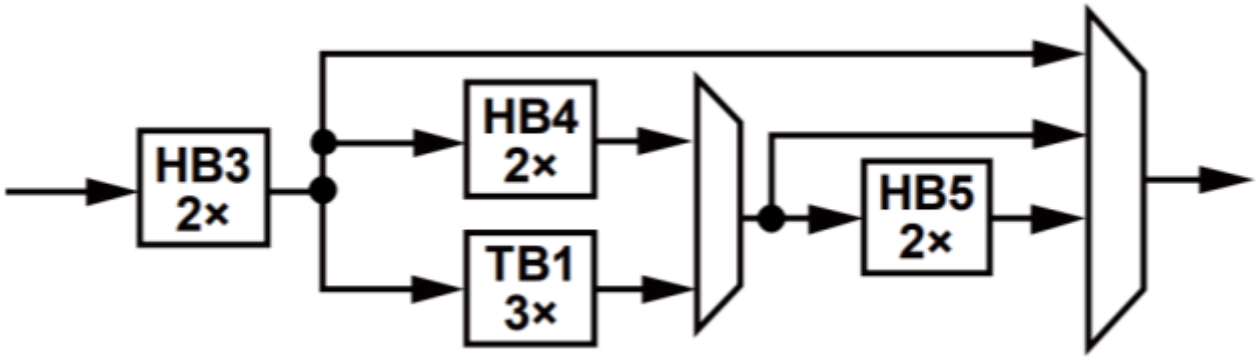


Figure 36: Main datapath interpolation half-band filter block diagram

表 30 主数据通路插值可用带宽和抑制 / Table 30. Main Datapath Interpolation Usable Bandwidth and Rejection

半波段滤波器 / Half-Band Filter	带宽 (×fIN_FILTER) / Bandwidth (×fIN_FILTER)	停止带抑制 (dB) / Stopband Rejection (dB)
HB3	80%	85
HB4	40%	85
TB1	27%	85
HB5	20%	85

3.2.8 主数据通路数字调制 / 3.2.8 Main Datapath Digital Modulation

English: The structure of the main datapath 48-bit NCO is basically the same as the channelizer NCO introduced in the preceding sections. Their operation is also similar. However, unlike the channelizer NCO, the main datapath NCO operates at a higher clock rate, the same rate as the analog DAC core (fDAC), which allows the NCO to generate frequencies over a wider range. See the 48-bit Integer/Modulus NCO section for details.

The NCO mode selection is as shown in Table 31. These controls are paged according to the main DAC paging mask MAINDAC_PAGE (Bits[7:6] of Register 0x008).

The main NCO block also contains a sideband selection control and options regarding how the FTW and phase offset controls are updated.

The phase offset word control is calculated as follows: −180° ⩽ degree offset ⩽ +180° Degree offset = 180° × (DDSM_NCO_PHASE_OFFSET/2)^{15}

where DDSM_NCO_PHASE_OFFSET/2 is the 16-bit two's-complement value programmed in the registers listed in Table 32.

中文： 主数据通路 48 位 NCO 的结构与前几节介绍的 channelizer NCO 基本相同。它们的运行也类似。不过，与 channelizer NCO 不同的是，主数据通路 NCO 以更高的时钟速率工作，与模拟 DAC 内核(fDAC)的速率相同，这使得 NCO 可以在更宽的范围内产生频率。参见 48 位 Inter/Modulus NCO 部分的详细信息。

NCO 模式的选择如表 31 所示。这些控制根据主 DAC 分页掩码 MAINDAC_PAGE（寄存器 0x008 的 Bit[7:6]）进行分页。

主 NCO 模块还包含边带选择控制以及关于如何更新 FTW 和相位偏移控制的选项。

相位偏移字控制的计算方法如下： -180°⩽度数偏移⩽+180° 度数偏移=180°×(DDSM_NCO_PHASE_OFFSET/2)15

其中，DDSM_NCO_PHASE_OFFSET/2 是表 32 所列寄存器中编程的 16 位 2 进制值。

表 31 主调制模式选择 / Table 31. Main Modulation Mode Selection

调制模式 / Modulation Mode	调制类型 — 寄存器 0x112，第 3 位 / Register 0x112, Bit 3	调制类型 — 寄存器 0x112，第 2 位 / Register 0x112, Bit 2
无 / None	0b0	0b0
48 位 Integer NCO / 48-bit Integer NCO	0b1	0b0
48 位 Dual Modulus NCO / 48-bit Dual Modulus NCO	0b1	0b1

表 32 主数据通路 NCO 相位偏移寄存器 / Table 32. Main Datapath NCO Phase Offset Registers

地址 / Address	价值 / Value	说明 / Description
0x11C	ddsm_nco_phase_offset[7:0]（相位偏移 / phase offset）	8LSB 相位偏移 / 8 LSBs of phase offset
0x11D	ddsm_nco_phase_offset[15:8]（相位偏移 / phase offset）	8MSB 相位偏移 / 8 MSBs of phase offset

3.2.9 48 位 Integer/Modulus NCO / 3.2.9 48-Bit Integer/Modulus NCO

English: As shown in Figure 32, the main datapath NCO uses a structure similar to the Channelizer NCO. Because the clock frequency of the main datapath NCO is the same as fDAC, this configuration allows the output signal to be placed anywhere within ±fDAC/2 of the output spectrum, with high frequency resolution.

The NCO generates a quadrature carrier that converts the input signal to a new carrier frequency, similar to the Channelizer NCO. For more details, see the corresponding Channelizer NCO section.

The FTW calculation method of the main datapath NCO is the same as that of the Channelizer NCO. One important difference is that the clock rate (fNCO,CLK) of the main datapath NCO equals the DAC sample rate (fDAC, maximum 12 GSPS). fNCO,CLK is calculated using the following formula: fNCO,CLK = fDAC = fDATA × channel interpolation × main interpolation

The FTW of each NCO can be programmed individually and calculated by the following formula: $-fNCO,CLK/2 \leqslant fCARRIER < fNCO,CLK/2$; $DDSM_FTW = (fCARRIER/fNCO,CLK) \times 2^{48}$

where fCARRIER is the output frequency of the NCO, fNCO,CLK is the sampling clock frequency of the NCO, and DDSM_FTW is a 48-bit two's-complement number. The frequency tuning word settings are as shown in Table 33.

Unlike other NCO control registers, the FTW registers are not applied to the NCO block immediately after the control registers are written. Instead, the FTW registers are applied (reset) on the rising edge of DDSM_FTW_LOAD_REQ (Bit 0 of Register 0x113). After the update request is issued, DDSM_FTW_LOAD_ACK (Bit 1 of Register 0x113) must show a high level to confirm that the FTW has been updated.

The DDSC_SEL_SIDEBAND bit (Bit 1 of Register 0x112 = 0b1) is a convenience bit used to control whether the lower sideband or the upper sideband of the modulated data is used, equivalent to flipping the sign of the FTW.

Each main datapath 48-bit NCO can also be used in Dual modulus mode to create fractional frequencies beyond 48-bit precision. Modulus mode is enabled by programming the DDSM_MODULUS_EN bit in the DDSM_DATAPATH_CFG register to 1 (Bit 2 of Register 0x112 = 0b1).

The structure of the main datapath Modulus NCO is similar to that of the channel modulus NCO, and the X (FTW), A and B values are calculated in a similar way: $fCARRIER/fNCO,CLK = M/N = (X + A/B)/2^{48}$ X is the FTW, programmed in Registers 0x114 to 0x119. A is programmed in Registers 0x12A to 0x12F. B is programmed in Registers 0x124 to 0x129.

For more details and examples, see the Channel Modulus Mode (Direct Digital Synthesis (DDS) Mode) section. The main datapath NCO operates at a higher clock rate (fNCO,CLK) than the channel NCO and is addressed through different SPI registers.

NCO reset. Resetting the main datapath NCO is very useful when determining the start time and phase of the NCO. Each NCO can be configured to reset in response to one of the following events: a direct request via SPI (Bit 0 of Register 0x113), a change of the FTW register value, or the arrival of the next SYSREF± rising edge. The reset method is controlled by Register 0x113. For more information, see the detailed description of Register 0x113 in Table 50.

中文： 如图 32 所示，主数据通路 NCO 采用与 Channelizer NCO 相似的结构。由于主数据通路 NCO 的时钟频率与 fDAC 相同，因此这种配置允许将输出信号放置在输出频谱±fDAC/2 内的任何位置，且具有较高的频率分辨率。

NCO 产生正交载波，将输入信号转换为新的载波频率，与 Channelizer NCO 类似。更多详情，请参阅相应的 Channelizer NCO 部分。

主数据通路 NCO 的 FTW 计算方法与 Channelizer NCO 的 FTW 计算方法相同。一个重要的区别是，主数据通路 NCO 的时钟速率(fNCO,CLK)等于 DAC 采样速率（fDAC，最大 12GSPS）。使用以下公式计算 fNCO,CLK：fNCO,CLK=fDAC=fDATA×通道插值×主插值

每个 NCO 的 FTW 均可单独编程，并按以下公式计算： -fNCO,CLK/2≤fCARRIER＜fNCO,CLK/2；DDSM_FTW=(fCARRIER/fNCO,CLK)×2^{48}

其中，fCARRIER 是 NCO 的输出频率。fNCO,CLK 是 NCO 的采样时钟频率。DDSM_FTW 是一个 48 位的二进制补码数。频率调整字的设置如表 33 所示。

与其他 NCO 控制寄存器不同，FTW 寄存器不会在写入控制寄存器后立即应用于 NCO 块。相反，FTW 寄存器在 DDSM_FTW_LOAD_REQ（寄存器 0x113 的 Bit0）的上升沿应用（复位）。更新请求发出后，DDSM_FTW_LOAD_ACK（寄存器 0x113 的 Bit1）必须显示高电平，以确认 FTW 已更新。

DDSC_SEL_SIDEBAND 位（寄存器 0x112 的 Bit1=0b1）是一个便利位，用于控制使用调制数据的下边带还是上边带，相当于翻转 FTW 的符号。

每个主数据通路 48 位 NCO 还可用于 Dual modulus 模式，以创建超出 48 位精度的分数频率。通过将 DDSM_DATAPATH_ CFG 寄存器中的 DDSM_MODULUS_EN 位编程为 1（寄存器 0x112 的 Bit2=0b1），可启用 modulus 模式。

主数据通路 Modulus NCO 的结构与通道 modulus NCO 相似，X(FTW)、A 和 B 值的计算方式也类似：fCARRIER/fNCO,CLK=M/N=(X+A/B)/2^{48} X 是 FTW，在寄存器 0x114 至寄存器 0x119 中编程。 A 在寄存器 0x12A 至寄存器 0x12F 中编程。 B 在寄存器 0x124 至寄存器 0x129 中编程。

更多详情和示例，请参阅 Channel Modulus 模式（直接数字合成(DDS)模式）部分。主数据通路 NCO 以比通道 NCO 更高的时钟速率 (fNCO, CLK) 工作，并通过不同的 SPI 寄存器寻址。

NCO 重置：复位主数据通路 NCO 在确定 NCO 的启动时间和相位时非常有用。每个 NCO 都可配置为响应以下事件之一而复位：通过 SPI（寄存器 0x113 的 Bit0）直接请求、FTW 寄存器值变化或下一个 SYSREF±上升沿到来。复位方式由寄存器 0x113 控制。更多信息请参见表 50 中寄存器 0x113 的详细说明。

表 33 主数据通路 NCO FTW 寄存器 / Table 33. Main Datapath NCO FTW Registers

地址 / Address	价值 / Value	说明 / Description
0x114	DDSM_FTW[7:0]	8LSB 的 FTW / 8 LSBs of FTW
0x115	DDSM_FTW[15:8]	下一个 8 位 FTW / Next 8 bits of FTW
0x116	ddsm_ftw[23:16]	下一个 8 位 FTW / Next 8 bits of FTW
0x117	ddsm_ftw[31:24]	下一个 8 位 FTW / Next 8 bits of FTW
0x118	DDSM_FTW[39:32]	下一个 8 位 FTW / Next 8 bits of FTW
0x119	DDSM_FTW[47:40]	8MSB 的 FTW / 8 MSBs of FTW

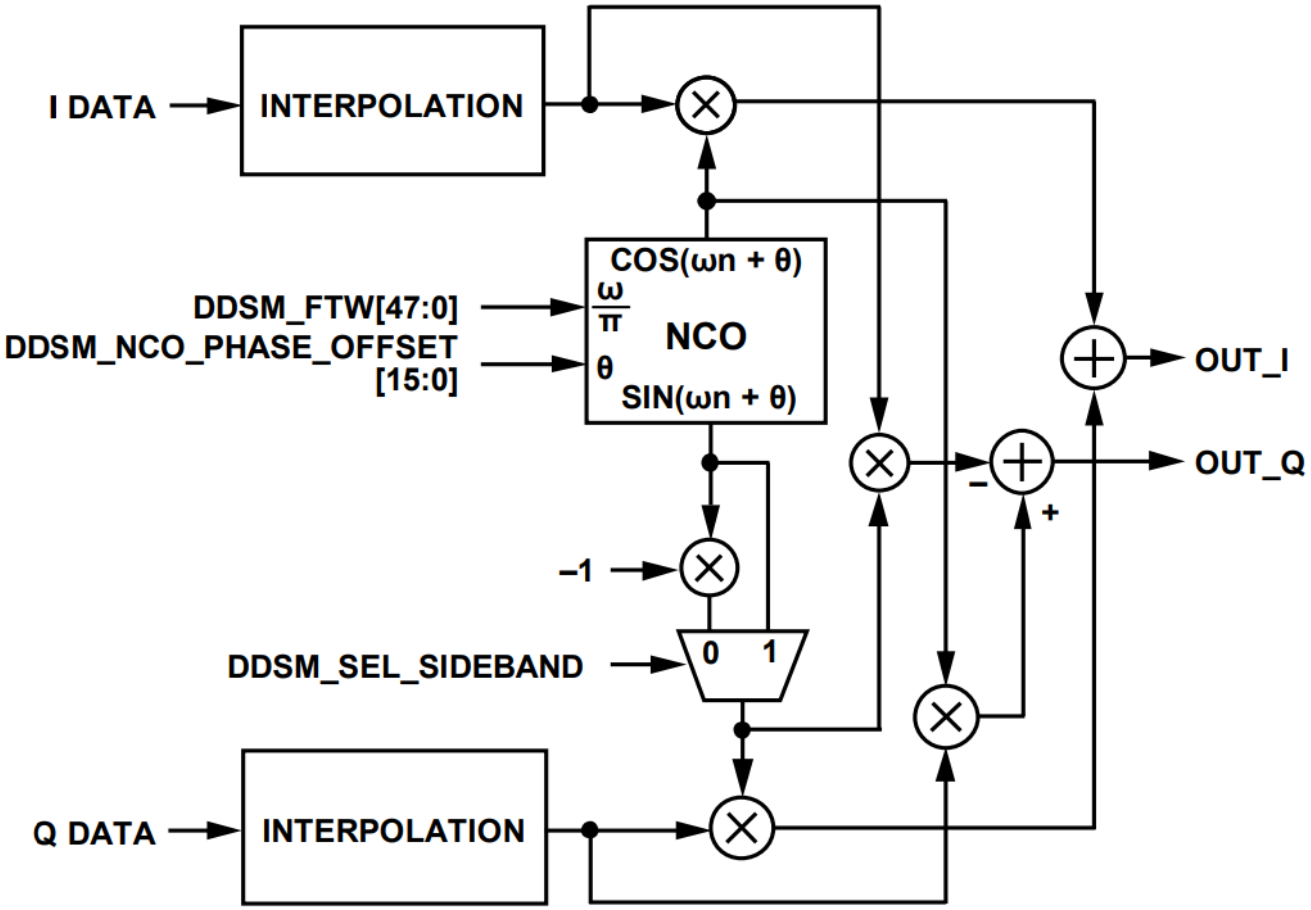


Figure 37: NCO modulator block diagram, main datapath modulus NCO mode (DDS)

3.2.10 快速跳频 (FFH) / 3.2.10 Fast Frequency Hopping (FFH)

English: Each main datapath NCO in the SXD052 has multiple functions enabling FFH between preconfigured carrier frequencies. The 48-bit main NCO is a general-purpose NCO combined with a set of 31 FFH NCOs (each NCO with 32 bits).

FFH NCO. Each FFH NCO is implemented in the main 48-bit NCO, and the associated group of 31 FTW registers is located in Registers 0x806 to 0x881. When a specific NCO is reset, the FTW registers can be preloaded with the tuning words loaded into the frequency-hopping register group. Any one of the 32 FTWs can be selected with a single register write to the HOPF_SEL bits in the DDSM_HOPF_CTRL register (Bits[4:0] of Register 0x800). The way the phase transitions when a specific NCO hops between carrier frequencies is determined by the NCO frequency change mode. These modes include phase-continuous hopping, phase-discontinuous hopping and phase-coherent hopping. The hopping mode is controlled by Bits[7:6] of Register 0x800, as described in Table 34.

In phase-discontinuous mode, the FTW of the NCO is updated and the phase accumulator is reset, causing the phase of the NCO to change abruptly each time it hops to a new frequency. Discontinuous phase may cause undesirable glitches at the transition point. In addition, during phase-continuous switching, the FTW of the NCO is updated while the main phase accumulator keeps counting throughout the update, making the phase transition between carrier frequencies smooth.

In phase-coherent mode, a set of 31 additional phase accumulators is enabled, and whichever accumulator's value is applied to the main accumulator keeps counting. Therefore, for each carrier

frequency, at any time, the phases of all 32 FTWs are known, so phase coherence relative to time 0 (the time of the last NCO reset) can be maintained between frequency hops. It is therefore recommended to preload all FTWs first and then select the phase-coherent switching mode, so that the NCO phase accumulators start simultaneously.

To save power, each of the 31 additional NCOs is enabled only when its corresponding FTW is programmed to a value other than 0x0. The default value of all NCO FTWs is 0x0. Note that the main phase accumulator (corresponding to the 48-bit FTW, i.e. FTW0) is simultaneously enabled by the DDSM_NCO_EN bit in the DDSM_DATAPATH_CFG register (Bit 3 of Register 0x112 = 0b1).

Each 32-bit NCO can be powered down at the user's convenience. If a 32-bit NCO is initially powered up, it is recommended to first program the FTW to 0x0001 to clear residual values in the accumulator, and then program the FTW to 0x0000, thereby turning off the NCO output but not the accumulator. This method avoids any residual spurious tones at the outputs of adjacent NCOs during power-down, although this possibility is small.

中文： SXD052 中的每一个主数据通路 NCO 都具有多种功能，可在预配置的载波频率之间进行 FFH。48 位主 NCO 是一个通用 NCO，与一组 31 个 FFH NCO（每个 NCO 有 32 位）相结合。

FFH NCO：每个 FFH NCO 都在主 48 位 NCO 中实现，相关的 31 个 FTW 寄存器组位于寄存器 0x806 至寄存器 0x881 中。当重置特定 NCO 时，FTW 寄存器可预载已载入跳频寄存器组的调谐字。32 个 FTW 中的任何一个都可以选择，只需向 DDSM_HOPF_CTRL 寄存器（寄存器 0x800 的 Bit[4:0]）中的 HOPF_SEL 位做一次寄存器写入即可。特定 NCO 在载波频率之间跳变时的相位转换方式由 NCO 频率变化模式决定。这些模式包括相位连续跳变、相位不连续跳变和相位相干跳变。跳频模式由寄存器 0x800 的 Bit[7:6]控制，如表 34 所述。

在相位不连续模式下，NCO 的 FTW 会被更新，相位累加器会被重置，导致 NCO 每次跳频到一个新频率时相位发生突然变化。不连续的相位可能会导致在转换点出现不理想的毛刺。另外，在相位连续切换过程中，NCO 的频率调谐字会被更新，而主相位累加器会在整个更新过程中保持计数，从而使载波频率之间的相变平稳。

在相位一致性模式下，一组 31 个额外的相位累加器被启用，无论哪个累加器的值被应用到主累加器上，都能保持计数。因此，对于每个载波频率，在任何时候，所有 32 个 FTW 的相位都是已知的，因此可以在跳频之间保持相对于时间 0（NCO 最后一次复位的时间）的相位一致性。因此，建议先预载所有 FTW，然后再选择相位一致性切换模式，以便 NCO 相位累加器同时启动。

为节省功耗，31 个附加 NCO 中的每一个只有在其相应的 FTW 编程为 0x0 以外的值时才会启用。所有 NCO FTW 的默认值均为 0x0。请注意，主相位累加器（对应 48 位 FTW，即 FTW0）同时由 DDSM_DATAPATH_CFG 寄存器（寄存器 0x112 的 Bit3=0b1）中的 DDSM_NCO_EN 位启用。

每个 32 位 NCO 都可以在用户方便时关闭电源。如果对一个 32 位 NCO 初始上电，建议先将 FTW 编程为 0x0001，以清除累加器中的残余值，然后再将 FTW 编程为 0x0000，从而将 NCO 输出关闭，但不会关闭累加器。这种方法可以避免在断电期间相邻 NCO 的输出端出现任何残留的杂散 tone，尽管这种可能性很小。

表 34 NCO 频率变化模式 / Table 34. NCO Frequency Change Modes

寄存器 0x800 的 Bit[7:6] / Register 0x800, Bits[7:6]	说明 / Description
0b00	相位连续开关 / Phase-continuous switching
0b01	相位不连续开关（复位 NCO 累加器）/ Phase-discontinuous switching (resets the NCO accumulator)

寄存器 0x800 的 Bit[7:6] / Register 0x800, Bits[7:6]	说明 / Description
0b10	相位相干开关 / Phase-coherent switching

3.2.11 校准 NCO / 3.2.11 Calibration NCO

English: In addition to the 48-bit NCO and the 31 32-bit NCOs, there is a 32-bit calibration NCO, which is also part of the main datapath NCO block, as shown in Figure 32. This NCO is independent of the 48-bit NCO and can conveniently generate calibration tones without modifying the configuration of the main datapath. Like all other NCOs, this NCO can be used in NCO-only mode, or to convert input data to a new carrier frequency. Bit 0 of Register 0x1E6 is used to control whether the 32-bit calibration NCO is connected to the main datapath or to the normal 48-bit main NCO. To use the 32-bit calibration NCO, first enable the accumulator of the calibration NCO by setting Bit 2 of Register 0x1E6 to 1. Then program the calibration NCO FTW in Registers 0x1E2 to 0x1E5, and update the FTW to take effect by toggling Bit 0 of Register 0x113 from 0 to 1. By setting Bit 0 of Register 0x1E6 to 1, the calibration NCO is selected in place of the main NCO. Like other NCOs, by setting Bit 1 of Register 0x1E6 to 1, the calibration NCO can be configured for NCO-only mode operation.

The tone amplitude can be set in Registers 0x148 and 0x149. For details, see the NCO-only mode section.

中文： 除了 48 位 NCO 和 31、32 位 NCO 外，还有一个 32 位校准 NCO，它也是主数据通路 NCO 模块的一部分，如图 32 所示。该 NCO 独立于 48 位 NCO，可以方便地生成校准 tone，而无需修改主数据通路的配置。与所有其他 NCO 类似，该 NCO 可用于仅 NCO 模式，也可用于将输入数据转换为新的载波频率。寄存器 0x1E6 的 Bit0 用于控制 32 位校准 NCO 是连接到主数据通路，还是连接到正常的 48 位主 NCO。要使用 32 位校准 NCO，首先要通过设置寄存器 0x1E6 的 Bit2=1 来启用校准 NCO 的累加器。然后，对寄存器 0x1E2 至寄存器 0x1E5 中的校准 NCO FTW 进行编程，并通过将寄存器 0x113 的 Bit0 从 0 切换为 1 来更新 FTW，使其生效。通过设置寄存器 0x1E6 的 Bit0=1，选择校准 NCO 以代替主 NCO。与其他 NCO 类似，通过设置寄存器 0x1E6 的 Bit1=1，校准 NCO 可配置为仅 NCO 模式运行。

Tone 幅值可在寄存器 0x148 和寄存器 0x149 中设置。详情请参阅仅 NCO 模式。

3.2.12 仅 NCO 模式 / 3.2.12 NCO-Only Mode

English: The NCOs of the SXD052 can operate in standalone mode, i.e. with the JESD204B link disconnected (or disabled), outputting one or more NCO tones from DAC0 and/or DAC1. The correct JESD204B mode must be selected to configure the corresponding channelizer and/or main datapath clock domains. In NCO-only mode, each NCO uses internally generated DC samples to modulate the NCO output, generating a single-tone sine wave. The amplitude of the DC sample corresponds directly to the NCO tone amplitude at the DAC core output. The amplitude of each channel NCO can be controlled independently by correctly paging the channel registers (Registers 0x148 and 0x149). Note that the main NCO amplitude is controlled by paging Channel 0 of channel NCO0 and Channel 1 of channel NCO1 (the NCOx channel and the main NCOx channel share the DC word).

In NCO-only mode, the data source of the digital datapath is the DC data word, which means that regardless of whether the JESD204B link was initially started, link data is not passed to the datapath. However, the input of the datapath can be easily switched between the DC data input and the SERDES block input through Register 0x130 or Register 0x1E6, depending on the datapath. As long as the JESD204B link is configured in advance and suitable data samples are provided, an instant connection can

be achieved. As mentioned earlier, during the transition, the PA protection block can be used to protect sensitive external components.

To use any NCO in NCO-only mode, the user can configure the SXD052 to operate in JESD204B Mode 0, Mode 1 or Mode 2, depending on the number of channel NCOs required. As long as the NCO is not bypassed (interpolation = 1), any JESD204B mode can be selected. To enable the NCOs connected to DAC1, a dual-link JESD204B mode can be configured. There is no need to establish a JESD204B link through an external source such as an FPGA; only a few SPI register writes are needed to enable the necessary JESD204B mode, thereby establishing the clock domain corresponding to each NCO.

In general, NCO-only mode is suitable for starting transmitter radio signal chains that initially do not require a digital data source, and also suitable for applications that only require a sine-wave output (also called DDS mode), such as local oscillator (LO) generation.

There is also an optional calibration NCO block that can be used as part of initial system calibration, without changing the configuration of the digital datapath.

中文： SXD052 的 NCO 可在独立模式下工作，即断开（或禁用）JESD204B 链接，并从 DAC0 和/或 DAC1 输出一个或多个 NCO tone。必须选择正确的 JESD204B 模式，以配置相应的 channelizer 和/或主数据通路时钟域。在仅 NCO 模式下，每个 NCO 利用内部生成的直流样本调制 NCO 输出，来生成单音正弦波。直流样本的幅值直接对应于 DAC 内核输出的 NCO tone 幅值。每个通道 NCO 的幅值可通过将通道寄存器（寄存器 0x148 和寄存器 0x149）正确分页来进行独立控制。请注意，主 NCO 幅值是通过对通道 NCO0 的通道 0 和通道 NCO1 的通道 1 分页来进行控制的（NCOx 通道和主 NCOx 通道共享直流字）。

在仅 NCO 模式下，数字数据通路的数据源是直流数据字，这意味着无论 JESD204B 链路最初是否启动，链路数据都不会传递到数据通路。不过，数据通路的输入可以通过寄存器 0x130 或寄存器 0x1E6 在直流数据输入和 SERDES 模块输入之间轻松切换，具体取决于数据通路。只要提前配置好 JESD204B 链路，并提供合适的数据样本，就能实现即时连接。如前所述，在转换过程中，可使用 PA 保护模块保护敏感的外部元件。

要在仅 NCO 模式下使用任何的 NCO，用户可根据所需的通道 NCO 数量，选择将 SXD052 配置为在 JESD204B 模式 0、模式 1 或模式 2 下运行。只要不旁路 NCO（插值=1），可选择任意 JESD204B 模式。为了启用连接到 DAC1 的 NCO，可以配置双链路 JESD204B 模式。无需通过 FPGA 等外部源建立 JESD204B 链路，只需写入几个 SPI 寄存器即可启用必要的 JESD204B 模式，从而建立与每个 NCO 相对应的时钟域。

一般来说，仅 NCO 模式适用于启动最初不需要数字数据源的发射机无线电信号链，也适用于只需要正弦波输出的应用（也称为 DDS 模式），如本地振荡器(LO)产生。

另外还有一个可选的校准 NCO 块，可用作初始系统校准的一部分，从而无需改变数字数据通路的配置。

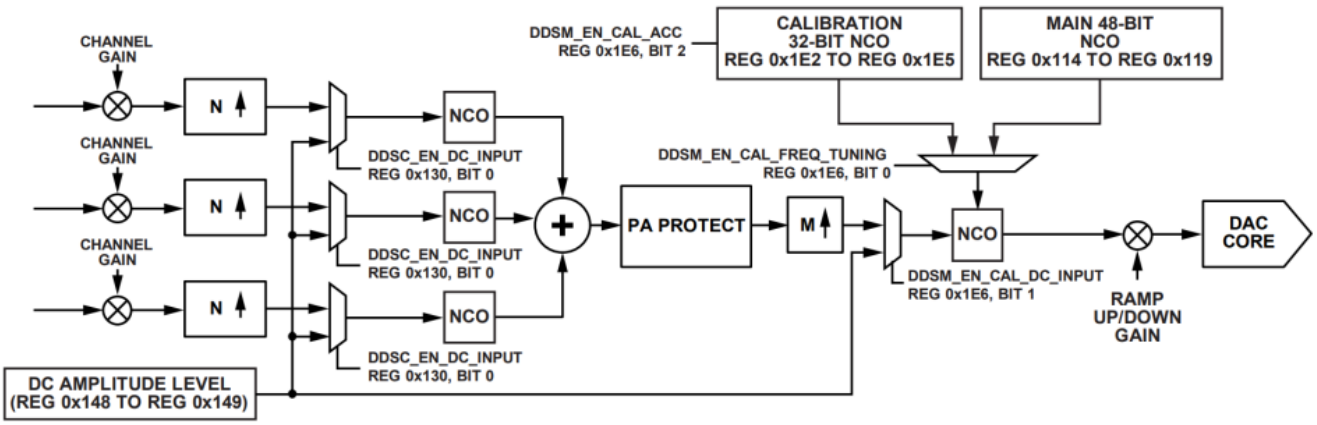


Figure 38: DC amplitude injection block diagram for NCO mode

3.3 调制器开关 / 3.3 Modulator Switch

English: For added flexibility, the last NCO block (NCO0 and NCO1, corresponding by default to the DAC cores in Configuration 0) contains a modulator switch that allows the user to send the desired I and/or Q samples to one or all DAC cores. NCOx is located near the output of its respective main digital datapath. The switch has four configurations, as shown in Figure 39 to Figure 42. Some configurations completely bypass the NCO and send the complex I and Q samples of each datapath to the DAC.

Other modes send the output of the NCO to DAC0 and DAC1. Of particular note is Configuration 2, shown in Figure 41, in which the I samples are sent to DAC0 and the Q samples to DAC1, making the SXD052 operate as a traditional IF DAC. The transmission of Configuration 3 also depends on whether NCO1 and/or DAC1 are enabled. The configuration is set through Bits[5:4] of Register 0x112 and is paged by the MAINDAC_PAGE register control.

中文： 为了增加灵活性，最后一个 NCO 模块（NCO0 和 NCO1，默认情况下与配置 0 中的 DAC 内核相对应）包含一个调制器开关，允许用户将所需的 I 和/或 Q 采样发送到一个或所有 DAC 内核。NCOx 位于各自的主数字数据通路的输出附近。开关有四种配置，如图 39 至图 42 所示。某些配置完全旁路 NCO，并将每个数据通路的复数 I 和 Q 样本发送至 DAC。

而其他模式则将 NCO 的输出发送到 DAC0 和 DAC1。特别值得注意的是图 41 所示的配置 2，其中 I 样本发送到 DAC0，Q 样本发送到 DAC1，使 SXD052 作为传统的中频 DAC 运行。配置 3 发送也取决于是否启用 NCO1 和/或 DAC1。配置通过寄存器 0x112 的 Bit[5:4]设置，并由 MAINDAC_PAGE 寄存器控制分页。

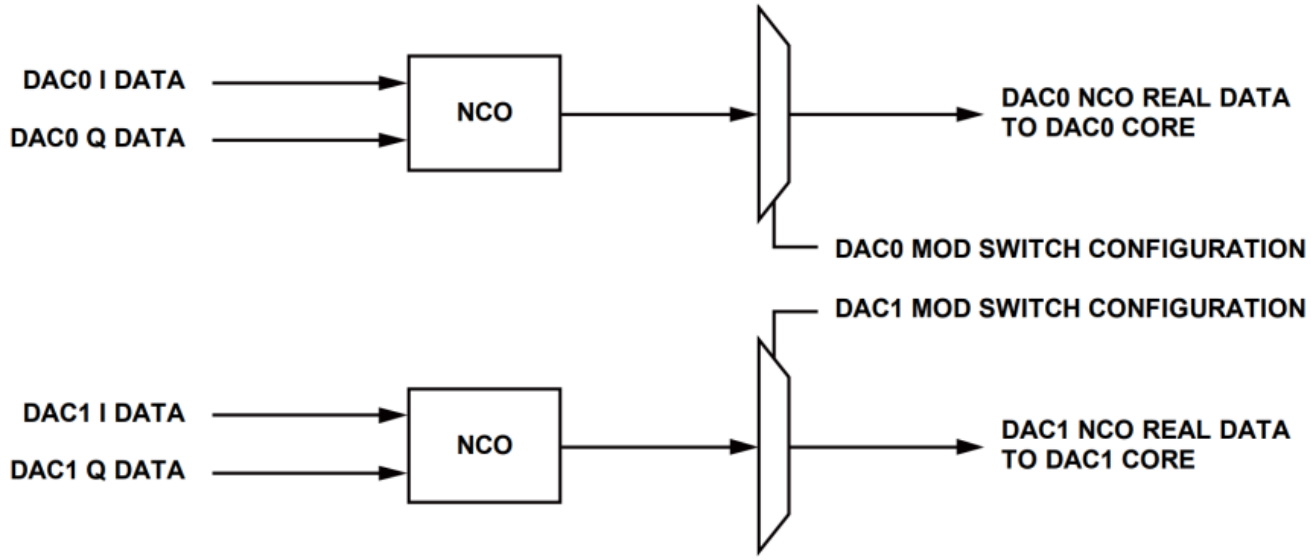


Figure 39: Configuration 0 — DAC0 = I0, DAC1 = I1

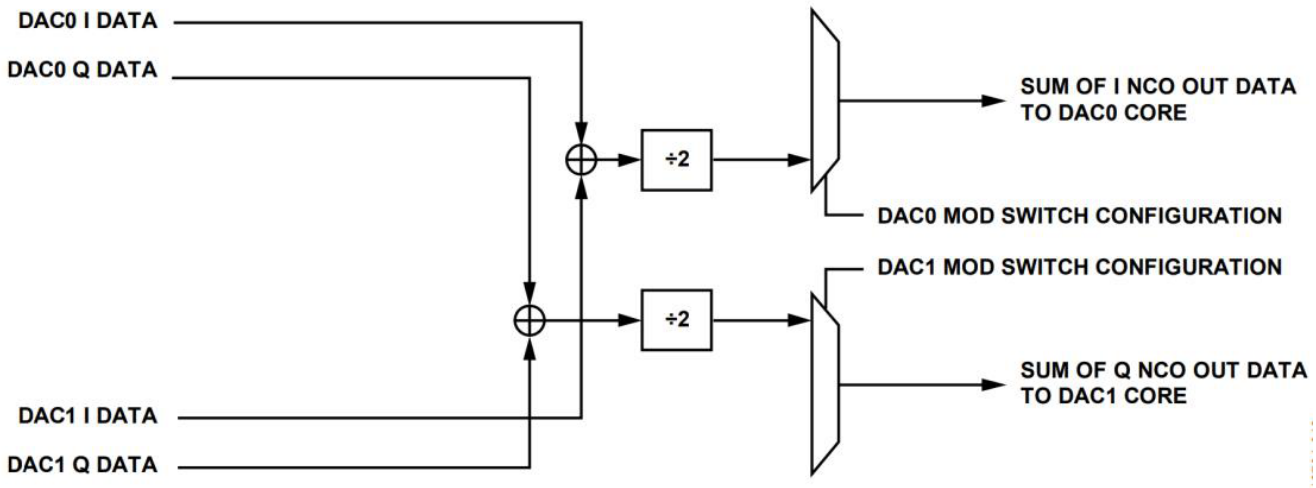


Figure 40: Configuration 1, CMPLX_MOD_DIV2_DISABLE=0 — DAC0=I0+I1, DAC1=Q0+Q1

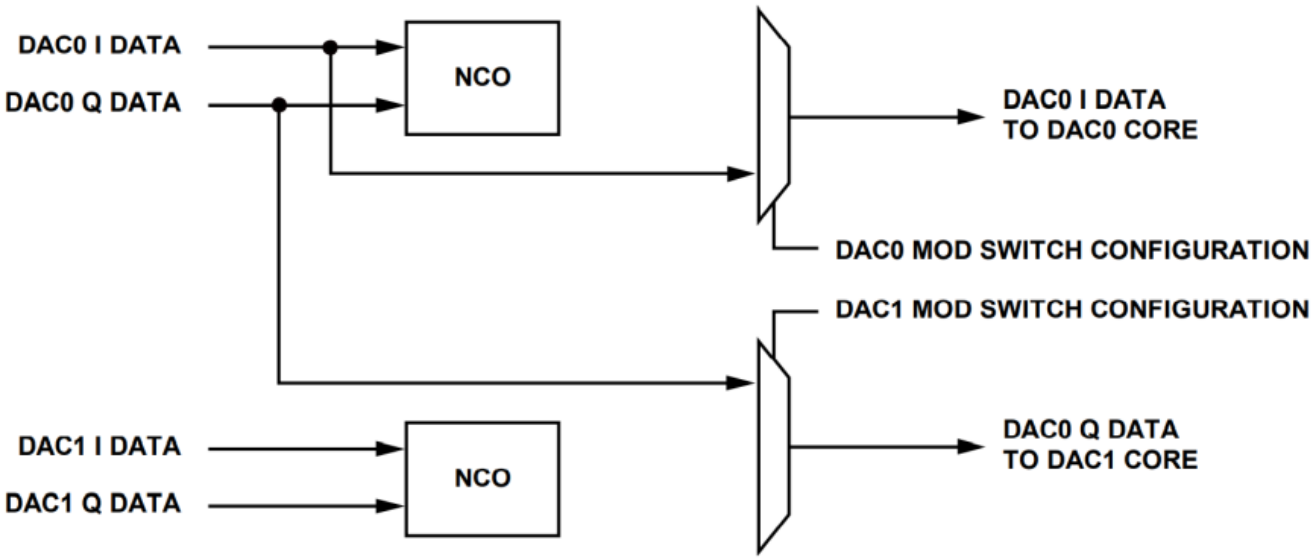


Figure 41: Configuration 2 — DAC0=I0, DAC1=Q0

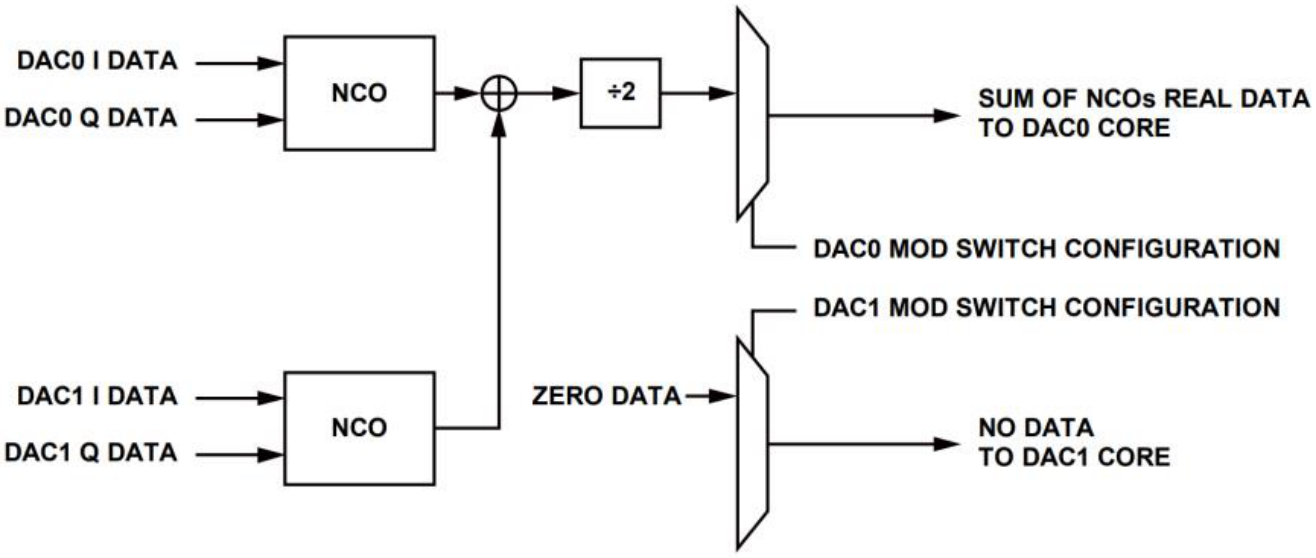


Figure 42: Configuration 3, CMPLX_MOD_DIV2_DISABLE=0 — DAC0=I0+I1, DAC1=0

3.3.1 复数调制器开关配置 / 3.3.1 Complex Modulator Switch Configuration

English: The switch configurations introduced earlier only support complex samples when the NCO is bypassed. To support complex samples when the NCO is used, Configuration 3 can be additionally reconfigured so that complex samples run at the output of the NCO, controlled by the EN_CMPLX_MOD bit (Bit 6 of Register 0x112). The specific configuration also depends on whether NCO1 is enabled, as shown in Figure 43 and Figure 44.

To set Configuration 3A, set the EN_CMPLX_MOD bit to 1, set the switch to Configuration 3, and enable both NCO0 and NCO1. The quadrature output of each main datapath NCO is also sent to DAC1 (no longer sending zero data from DAC1 as in the default Configuration 3, as shown in Figure 42). If NCO1 is disabled and EN_CMPLX_MOD = 1, the real output of NCO0 is sent to DAC0 and the quadrature output of NCO0 is set to DAC1. This setting is similar to Configuration 2, but the samples are at the output of NCO0 (see Figure 43 and Figure 44).

The divide-by-2 block at the multiplexer switch input can be disabled using the CMPLX_MOD_DIV2_DISABLE bit in Register 0x0FF. Otherwise, the outputs of DAC0 and DAC1 will be 6 dB lower than expected, because the divide-by-2 block is enabled by default.

Table 35 lists the complete list of SPI writes required to enable each configuration.

中文： 前面介绍的开关配置仅支持 NCO 被旁路时的复数采样。为了支持使用 NCO 时的复数采样，可以对配置 3 进行额外的重新配置，以便在 NCO 的输出端运行复数采样，操作由 EN_CMPLX_MOD 位（寄存器 0x112 的 Bit6）控制。具体配置也取决于是否启用 NCO1，如图 43 和图 44 所示。

要设置配置 3A，需将 EN_CMPLX_MOD 位设为 1，并将开关设为配置 3，同时启用 NCO0 和 NCO1。每个主数据通路的 NCO 正交输出也会发送到 DAC1（不再像默认配置 3 中那样从 DAC1 发送零数据，如图 42 所示）如果禁用 NCO1 且 EN_CMPLX_MOD=1，NCO0 的真实输出会被发送到 DAC0，NCO0 的正交输出被设置到 DAC1。此设置与配置 2 类似，但采样在 NCO0 的输出端（见图 43 和图 44）。

可以使用寄存器 0x0FF 中的 CMPLX_MOD_DIV2_DISABLE 位禁用多路复用开关输入端的除 2 模块。否则，DAC0 和 DAC1 的输出将比预期低 6dB，因为在默认情况下，除 2 模块是启用的。

表 35 列出了启用每种配置所需的 SPI 写入的完整列表。

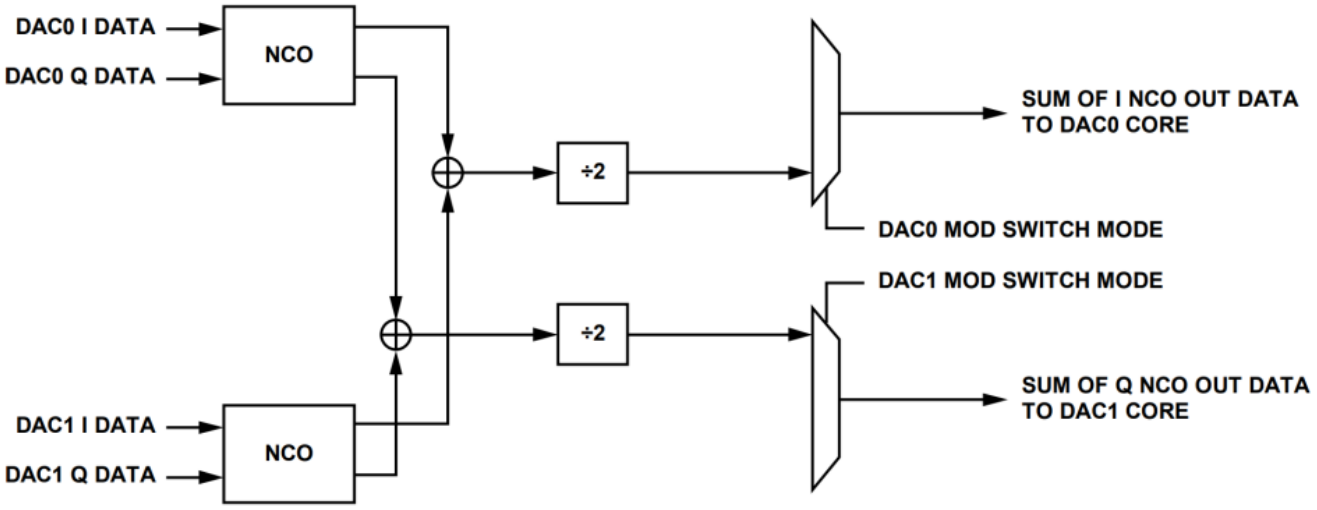


Figure 43: Configuration 3A, EN_CMPLX_MOD=1, CMPLX_MOD_DIV2_DISABLE=0, both main NCOs enabled — DAC0=I0_NCO+I1_NCO, DAC1=Q0_NCO+Q1_NCO

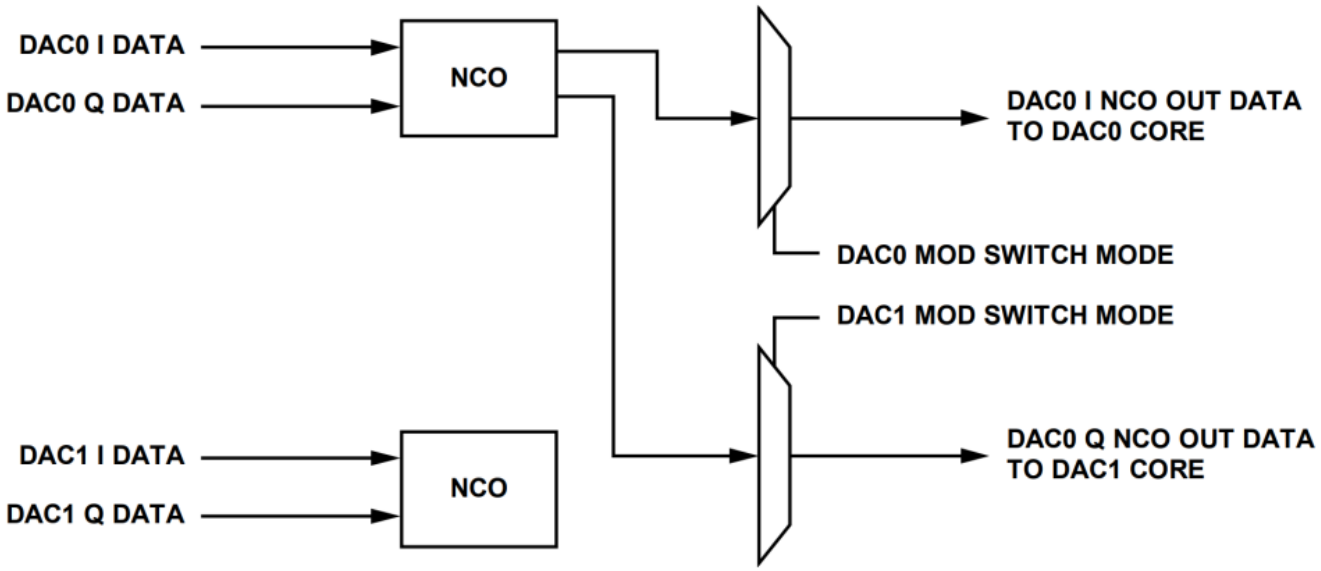


Figure 44: Configuration 3A, EN_CMPLX_MOD=1, CMPLX_MOD_DIV2_DISABLE=1, DAC1 main NCO disabled — DAC0=I0_NCO, DAC1=Q0_NCO

表 35 每种调制器开关配置所需的 SPI 写入量 / Table 35. SPI Writes Required for Each Modulator Switch Configuration

配置 / Configuration	寄存器 0x112 的 Bit6 (EN_COMPLEX_MOD) / Register 0x112 Bit 6	寄存器 0x112 的 Bit[5:4] (DDSM_MODE) / Register 0x112 Bits[5:4]	寄存器 0x112 的 Bit3（分页）— 启用 NCO0 / Register 0x112 Bit 3 (paged) — Enable NCO0	寄存器 0x112 的 Bit3（分页）— 启用 NCO1 / Register 0x112 Bit 3 (paged) — Enable NCO1	寄存器 0x0FF 的 Bit1 (CMPLX_MOD_DIV2_DISABLE) / Register 0x0FF Bit 1
配置 0 / Configuration 0	0	0	1	1	0
配置 1 / Configuration 1	0	1	0	0	0
配置 2 / Configuration 2	0	2	0	0	0
配置 3 / Configuration 3	0	3	1	1	0
复数配置 3A / Complex Configuration 3A	1	3	1	1	0
复数配置 3B / Complex	1	3	1	0	1

配置 / Configuration	寄存器 0x112 的 Bit6 (EN_COMPLEX_MOD) / Register 0x112 Bit 6	寄存器 0x112 的 Bit[5:4] (DDSM_MODE) / Register 0x112 Bits[5:4]	寄存器 0x112 的 Bit3（分页）— 启用 NCO0 / Register 0x112 Bit 3 (paged) — Enable NCO0	寄存器 0x112 的 Bit3（分页）— 启用 NCO1 / Register 0x112 Bit 3 (paged) — Enable NCO1	寄存器 0x0FF 的 Bit1 (CMPLX_MOD_DIV2_DISABLE) / Register 0x0FF Bit 1
Configuration 3B					

3.3.2 Ramp-Up/Ramp-Down 增益模块 / 3.3.2 Ramp-Up/Ramp-Down Gain Block

English: The ramp-up/ramp-down gain block is located at the output end of each main datapath, before the samples are sent to the analog DAC core for decoding. This block is an extension of the PDP block; together these blocks protect downstream components from large signal peaks or sustained average power exceeding a user-defined threshold.

As shown in Figure 34, various trigger methods can be configured in the PA protection block to trigger a gain decrease and mute the data transmitted from the SXD052. The ramp-up and ramp-down steps can be configured via SPI in Bits[2:0] of Register 0x580. The ramp-up and ramp-down equations are performed in 32 steps within 2^(CODE+8) DAC clock cycles. This control can be configured individually for each DAC ramp block through the MAINDAC_PAGE control in Register 0x008.

After a trigger event causes the data to ramp down gradually, assuming the trigger event (error) has been cleared, the data can ramp up gradually in two different ways. If the SPI protection control bit triggered the ramp-down interrupt, the data ramps up by setting Bit 7 of Register 0x582 from 0 to 1 and back to 0. In addition, if the ROTATE_SOFT_OFF_EN control in Bit 2 of Register 0x581 is set to 1, the digital data can also be muted during digital clock rotation. With this bit set, a synchronous logic rotation triggers the ramp-up/ramp-down block, making the output ramp down gradually, rotating the digital clock, and then making the output ramp up gradually. During synchronous logic rotation, these behaviors occur only when Bit 1 of the ROTATION_MODE control in Register 0x03B is set to 1, thereby enabling datapath clock rotation.

中文： Ramp-up/ramp-down 增益模块位于每个主数据通路的输出端，在样本被发送到模拟 DAC 内核进行解码之前。该模块是 PDP 模块的延伸，这些模块共同保护下游元件免受大信号峰值或超过用户定义阈值的持续平均功率的影响。

如图 34 所示，可以在 PA 保护模块中配置各种触发方法，来触发增益下降，使 SXD052 传输出来的数据静音。ramp-up 和 ramp-down 步骤可通过寄存器 0x580 的 Bit[2:0]中的 SPI 进行配置。Ramp-up 和 ramp-down 的方程在 2^(CODE+8) DAC 时钟周期内按 32 步进行。可通过寄存器 0x008 中的 MAINDAC_PAGE 控制，为每个 DAC ramp 模块单独配置该控制。

在触发事件导致数据逐渐下降后，假定触发事件（错误）已被清除，数据可以通过两种不同的方式逐渐上升。如果 SPI 保护控制位触发了下降中断，通过将寄存器 0x582 的 Bit7 从 0 设置为 1，再回到 0，数据会逐渐上升。此外，如果寄存器 0x581 的 Bit2 中的 ROTATE_SOFT_OFF_EN 控制被设置为 1，也可以在数字时钟翻转期间将数字数据静音。设置该位后，同步逻辑翻转会触发 ramp-up/ramp-down 模块，使输出逐渐下降，翻转数字时钟，再然后使输出逐渐上升。在同步逻辑翻转时，只有当寄存器 0x03B 中的 ROTATION_MODE 控制的 Bit1 设置为 1 时，从而启用数据通路时钟翻转，这些行为才会发生。

4、中断请求操作 / 4. Interrupt Request Operation

English: The SXD052 provides interrupt request output signals (IRQ0̄ and IRQ1̄) on pin D9 (IRQ0̄) and pin E9 (IRQ1̄), which can be used to notify an external host processor of important device events. By setting the corresponding bits of the IRQx̄ signals in Registers 0x028, 0x029, 0x02A and 0x02B, the IRQ output can be switched between the IRQ0̄ pin and the IRQ1̄ pin. After an interrupt occurs, query the device to determine the exact event that occurred. The IRQx̄ pins are open-drain, active-low outputs. Pull the IRQx̄ pins high externally to the device. These pins can be connected together with the interrupt pins of other devices that have open-drain outputs.

Figure 45 shows a simplified block diagram of the working principle of the IRQ block. If IRQ_EN is low, the INTERRUPT_SOURCE signal is set to 0. If IRQ_EN is high, the rising edge of EVENT causes the INTERRUPT_SOURCE signal to be set to 1. If the INTERRUPT_SOURCE signal is high, the IRQx̄ pin is pulled low. The INTERRUPT_SOURCE can be reset to 0 by the IRQ_RESET signal or the DEVICE_RESET signal.

According to the STATUS_MODE signal, EVENT_STATUS reads back the INTERRUPT_SOURCE signal or the event signal. The SXD052 has multiple IRQ register blocks that can monitor up to 86 events, depending on the device configuration. Some details of the IRQ register blocks differ, as described in Table 36.

Table 37 shows the source registers of the IRQ_EN, IRQ_RESET and STATUS_MODE signals in Figure 45, and the addresses for reading back EVENT_STATUS.

中文： SXD052 在引脚 D9(IRQ0̄)和引脚 E9(IRQ1̄)上提供中断请求输出信号(IRQx̄)，可用于向外部主机处理器通知重要的设备事件。通过设置寄存器 0x028、寄存器 0x029、寄存器 0x02A 和寄存器 0x02B 中 IRQx̄ 信号的相应位，可在 IRQ0̄ 引脚或 IRQ1̄ 引脚之间切换 IRQ 输出。中断发生后，查询设备以确定发生的确切事件。IRQx̄ 引脚为 open-drain，低输出有效。在设备外部将 IRQx̄ 引脚拉高。可将这些引脚与其他设备的带 open-drain 输出的中断引脚连接起来。

图 45 表示 IRQ 模块的工作原理的简化框图。如果 IRQ_EN 为低电平，则 INTERRUPT_SOURCE 信号被置 0。如果 IRQ_EN 为高电平，EVENT 的上升沿会导致 INTERRUPT_SOURCE 信号被置 1。如果 INTERRUPT_SOURCE 信号为高电平，IRQx̄ 引脚将被拉低。通过 IRQ_RESET 信号或 DEVICE_RESET 信号，可将 INTERRUPT_SOURCE 复位为 0。

根据 STATUS_MODE 信号，EVENT_STATUS 回读 INTERRUPT_SOURCE 信号或事件信号。SXD052 有多个 IRQ 寄存器模块，可监控多达 86 个事件，具体取决于设备配置。IRQ 寄存器模块的某些细节有所不同，如表 36 所述。

表 37 展示了图 41 中 IRQ_EN、IRQ_RESET 和 STATUS_MODE 信号的源寄存器，以及回读 EVENT_STATUS 的地址。

表 36 寄存器块详情 / Table 36. Register Block Details

寄存器模块 / Register Block	报告事件 / Reported Events	EVENT_STATUS
0x020 至 0x27	每个芯片 / Per chip	INTERRUPT_SOURCE 如果启用 IRQ；否则，为事件 / INTERRUPT_SOURCE if IRQ is enabled; otherwise, the event
0x4B8 至 0x4BB；0x470 至 0x473	每条链路和通道 / Per link and lane	INTERRUPT_SOURCE 如果启用 IRQ；否则，为 0 / INTERRUPT_SOURCE if IRQ is enabled; otherwise, 0

4.1 中断服务例程 / 4.1 Interrupt Service Routine

English: Interrupt request management first requires selecting a set of event flags that require host intervention or monitoring. Enable the events that require host action so that the host is notified when an event occurs. For events that require host intervention after IRQx̄ activation, run the following routine to clear the interrupt request: 1. Read the status of the event flag bits being monitored. 2. Write 0 to IRQ_EN to disable the interrupt. 3. Read the event source. 4. Perform any action required to clear the cause of the event. In many cases, no specific action may be required. 5. Verify that the event source acts as expected. 6. Write 1 to IRQ_RESET to clear the interrupt. 7. Write 1 to IRQ_EN to enable the interrupt.

中文： 中断请求管理首先要选择一组需要主机干预或监控的事件标志。启用需要主机操作的事情，以便在事件发生时通知主机。对于 IRQx̄ 激活后需要主机干预的事件，运行以下例程清除中断请求： 1. 读取正在监控的事件标志位的状态。 2. 向 IRQ_EN 写入 0，禁用中断。 3. 读取事件源。 4. 执行清除事件原因所需的任何操作。在许多情况下，可能不需要采取具体措施。 5. 验证事件源是否按预期起作用。 6. 向 IRQ_RESET 写入 1，清除中断。 7. 向 IRQ_EN 写入 1，启用中断。

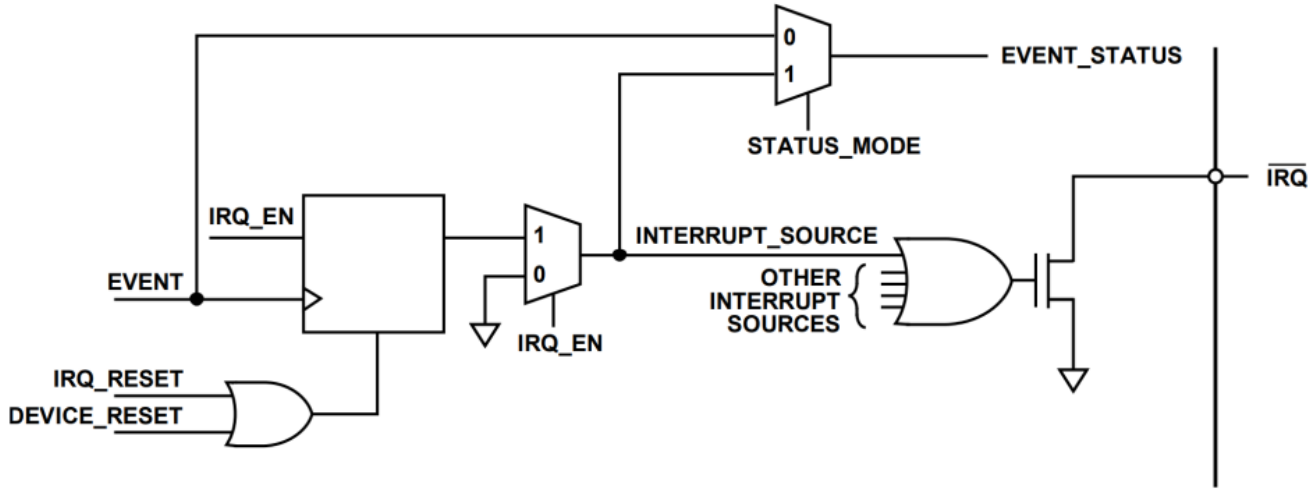


Figure 45: Circuit simplified schematic diagram (IRQ block)

表 37 寄存器的 IRQ 信号块地址详情 / Table 37. IRQ Signal Block Address Details per Register

寄存器模块 / Register Block	IRQ_EN — IRQ 信号地址[1] / IRQ Signal Address[1]	IRQ_RESET	STATUS_MODE	EVENT_STATUS
0x020 至 0x023	0x020 至 0x023；R/W per chip	0x024 至 0x027；per chip	STATUS_MODE=IRQ_EN	0x024 至 0x027；R per chip
0x4B8 至 0x4BB	0x4B8 至 0x4B9；W per error type	0x4BA，0x4BB；W per error type	不适用，STATUS_MODE=1 / Not applicable, STATUS_MODE=1	0x4BA，0x4BB；W per chip
0x470 至 0x473	0x470 至 0x473；W per error type	0x470 至 0x473；W per link	不适用，STATUS_MODE=1 / Not applicable, STATUS_MODE=1	0x470 至 0x473；W per link

[1] R 表示读，W 表示写，R/W 表示读/写。/ R denotes read, W denotes write, R/W denotes read/write.

5、模拟接口 / 5. Analog Interface

5.1 DAC 输入时钟配置 / 5.1 DAC Input Clock Configuration

English: The SXD052 DAC sample clock or device clock (DACCLK) can be received directly through CLKIN± (pin H12 and pin J12), or generated using the on-chip integrated integer PLL/VCO, with the reference clock provided by the same CLKIN± differential input pins. DACCLK can serve as the reference for all clock domains within the SXD052.

The SXD052 uses a low-jitter differential clock receiver that can connect directly to a differential or single-ended clock source. Because the input is self-biased with a calibrated impedance of 100 Ω, AC coupling of the clock source to the CLKIN± input pins is recommended. Phase noise performance can be improved by a higher clock input level (a larger swing, resulting in a higher effective slew rate), up to the maximum limit. Because DACCLK is the data sampling clock of the analog core (DACx), the quality of the clock signal at the SXD052 clock input pins is crucial and directly affects the analog AC performance of the DAC. Select a clock source whose phase noise and spurious characteristics meet the requirements of the target application. In general, using a PLL/VCO or other clock multiplier (inside or outside the DAC) also multiplies the resulting phase noise (jitter). Typically, the best phase noise performance is achieved with an external clock running at the required DAC clock rate, with the PLL/VCO bypassed.

Where low phase noise is not required, the PLL/VCO provides a convenient method allowing the SXD052 to operate at DAC clock rates up to 12.4 GHz without a complex gigahertz clock solution. The PLL reference frequency at CLKIN± is usually several orders of magnitude lower than the operating frequency of DACCLK. The PLL then generates a control voltage for the downstream VCO, and the VCO effectively multiplies the reference clock frequency to the required DACCLK frequency.

Figure 46 shows the typical phase noise performance of the SXD052 when driven directly by a clock with the input clock duty-cycle correction on (enabled by default), compared with the phase noise generated by the on-chip PLL/VCO.

中文： SXD052 DAC 采样时钟或器件时钟（DACCLK）可直接通过 CLKIN±（引脚 H12 和引脚 J12）接收，或使用片上集成的整数 PLL/VCO 生成，参考时钟由相同的 CLKIN±差分输入引脚提供。DACCLK 可作为 SXD052 内所有时钟域的基准。

SXD052 采用低抖动差分时钟接收器，能够直接连接差分或单端时钟源。由于输入是自偏置的，标定阻抗为 100Ω，故建议将时钟源与 CLKIN±输入引脚进行交流耦合。相位噪声性能可通过更高的时钟输入电平（更大的摆幅，导致更高的有效压摆率）得到改善，最高可达最大限制。由于 DACCLK 是模拟核(DACx)的数据采样时钟，因此 SXD052 时钟输入引脚的时钟信号质量至关重要，并直接影响 DAC 的模拟交流性能。选择相位噪声和杂散特性符合目标应用要求的时钟源。一般来说，使用 PLL/VCO 或其他时钟乘法器（DAC 内部或外部）也会使产生的相位噪声（抖动）成倍增加。通常，在旁路 PLL/VCO 的情况下，使用一个运行在所需 DAC 时钟速率下的外部时钟，可以实现最佳的相位噪声性能。

在不要求低相位噪声的情况下，PLL/VCO 提供了一种简便的方法，使 SXD052 能够在高达 12.4GHz 的 DAC 时钟速率下工作，而无需复杂的千兆赫兹时钟解决方案。在 CLKIN±处的 PLL 参考频率通常比 DACCLK 的工作频率低几个数量级。然后，PLL 为下游 VCO 产生控制电压，VCO 实际上将参考时钟的频率倍增到了所需的 DACCLK 频率。

图 46 显示了 SXD052 直接受时钟驱动，并且输入时钟占空比校正开启（默认启用）时的典型相位噪声性能，并与片内 PLL/VCO 产生的相位噪声进行了比较。

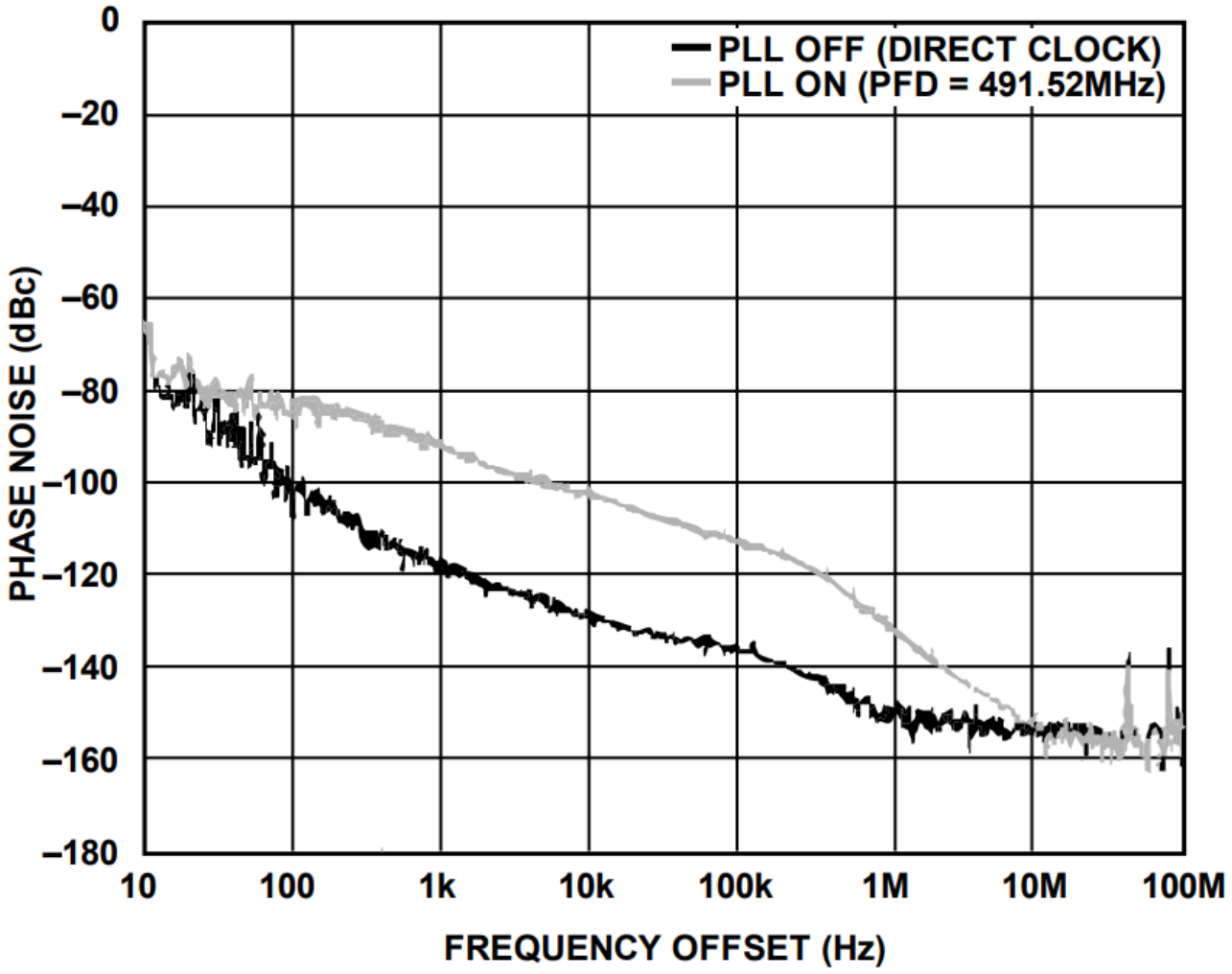


Figure 46: Phase noise vs. frequency offset; direct clock and PLL phase noise, 12GHz DAC sample rate, 1.65 GHz output frequency

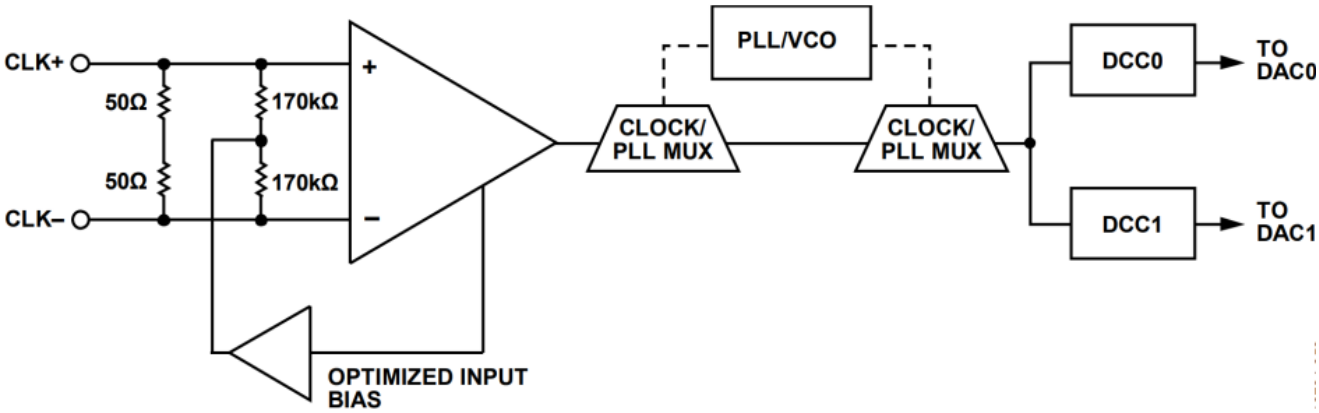


Figure 47: Clock receiver input simplified equivalent circuit

5.1.1 DAC 片上 PLL / 5.1.1 DAC On-Chip PLL

English: The SXD052 includes an internal PLL/VCO block that can generate the DAC clock (fDAC) from an external reference frequency (fREF) of 25 MHz to 3080 MHz applied to the CLKIN± pins (see Figure 48). When using the on-chip PLL, the prescaler (M) is selected through Bits[1:0] of Register 0x793, dividing the

reference frequency internally into the 25 MHz to 770 MHz range at the input of the phase frequency detector (PFD) circuit block. The DAC PLL synthesizer is enabled by setting Bit 0 of Register 0x095 to 0.

The operating frequency range of the internal VCO is 8.74 GHz to 12.4 GHz; if the application requires a lower DACCLK, additional divider settings are available. By setting Bits[1:0] of Register 0x094, the user can configure the DAC clock rate as the VCO frequency (8.74 GHz to 12.4 GHz), the VCO frequency divided by 2 (4.37 GHz to 6.2 GHz), or the VCO frequency divided by 3 (2.92 GHz to 4.1 GHz). For instructions on how to program the PLL, see the start-up sequence section.

To generate the required VCO control voltage from the output of the charge pump (CP), the SXD052 DAC PLL requires an external loop filter. A passive low-pass filter with a topology similar to that shown in Figure 48 is recommended. In general, the passband width (bandwidth) of the filter is a trade-off between the loop response time when the frequency changes and loop stability, after initial frequency lock. Correct layout and component selection of the filter can bring the best performance for most applications. However, the user may tailor a filter adapted to a specific application according to the requirements of the PFD frequency, the reference clock phase noise and the DAC output phase noise.

For example, to reduce DACCLK jitter when using the PLL, a higher PFD frequency minimizes the in-band noise of the PLL. When setting the PLL filter bandwidth, the in-band noise of the PLL should intersect the open-loop noise of the VCO, to minimize the impact of the two blocks on the overall noise.

The best jitter performance is usually obtained when using an external high-performance clock source.

The DAC PLL uses an integer synthesizer to generate DACCLK for DAC0 and DAC1, which means the generated DACCLK must be an integer multiple of the input reference clock. The relationship between the DAC clock and the reference clock is as follows: fDAC = (8 × N × fREF)/M/(Register 0x094, Bits[1:0] + 1)

where fDAC is the required DAC clock frequency, N is the feedback divider ratio of the VCO, ranging from 2 to 50, fREF is the reference clock, and M is the reference clock divider ratio. By setting Bits[1:0] of Register 0x793, the valid values of the reference clock division (prescaling) are 1, 2, 3 or 4.

The falling edge of Bit 1 of Register 0x792, transitioning from a logic high level to a logic low level, triggers the VCO automatic calibration. The lock detect bit (Bit 0 of Register 0x7B5) is used to indicate whether the DAC PLL has achieved lock. If Bit 0 of Register 0x7B5 = 1, the PLL is locked.

中文： SXD052 包括一个内部 PLL/VCO 模块，可从 25MHz 至 3080MHz 的外部参考频率(fREF)生成 DAC 时钟(fDAC)，并将其应用到 CLKIN±引脚（见图 48）使用片内 PLL 时，通过寄存器 0x793 的 Bit[1:0]选择预分频器(M)，将参考频率内部分频至相位频率检测器(PFD)电路模块输入的 25MHz 至 770MHz 范围内。通过将寄存器 0x095 的 Bit0 设置为 0，启用 DAC PLL 合成器。

内部 VCO 的工作频率范围为 8.74GHz 至 12.4GHz，如果应用需要更低的 DACCLK，还可进行额外的分频器设置。通过设置寄存器 0x094 的 Bit[1:0]，用户可将 DAC 时钟速率配置为 VCO 频率（8.74GHz 至 12.4GHz）、VCO 频率除以 2（4.37GHz 至 6.2GHz）或 VCO 频率除以 3（2.92GHz 至 4.1GHz）。有关如何编程 PLL 的说明，请参阅启动序列部分。

为了从电荷泵(CP)的输出，产生所需的 VCO 控制电压，SXD052 DAC PLL 需要一个外部环路滤波器。建议使用拓扑结构类似图 48 所示的无源低通滤波器。一般来说，滤波器的通带宽度（带宽）是在初始频率锁定后，根据频率变化时的环路响应时间和环路稳定性来综合考虑的。滤波器的正确布局和元件选择可以为大多数应用带来最佳性能。不过，用户可能会根据 PFD 频率、参考时钟相位噪声和 DAC 输出相位噪声的要求，定制适应特定应用的滤波器。

例如，为了在使用 PLL 时降低 DACCLK 抖动，较高的 PFD 频率可将 PLL 的带内噪声降至最低。设置 PLL 滤波器带宽时，应使 PLL 的带内噪声与 VCO 的开环噪声相交，以最大限度地减少两个模块对整体噪声的影响。

在使用外部高性能时钟源时，通常可获得最佳抖动性能。

DAC PLL 使用整数型合成器为 DAC0 和 DAC1 生成 DACCLK，这意味着生成的 DACCLK 必须是输入参考时钟的整数倍。DAC 时钟与参考时钟之间的关系如下： fDAC=(8×N×fREF)/M/(Register 0x094，Bits[1:0]+1) 其中，fDAC 是所需的 DAC 时钟频率，N 是 VCO 的反馈分频比，范围为 2 至 50，fREF 是参考时钟。M 是参考时钟分频比。通过设置寄存器 0x793 的 Bit[1:0]，参考时钟分频（预分频）的有效值为 1、2、3 或 4。

寄存器 0x792 的 Bit1 的下降沿从逻辑高电平转换为逻辑低电平时，将触发 VCO 自动校准。锁定检测位（寄存器 0x7B5 的 Bit0）用于指示 DAC PLL 是否实现锁定。如果寄存器 0x7B5 的 Bit0=1，则 PLL 已锁定。

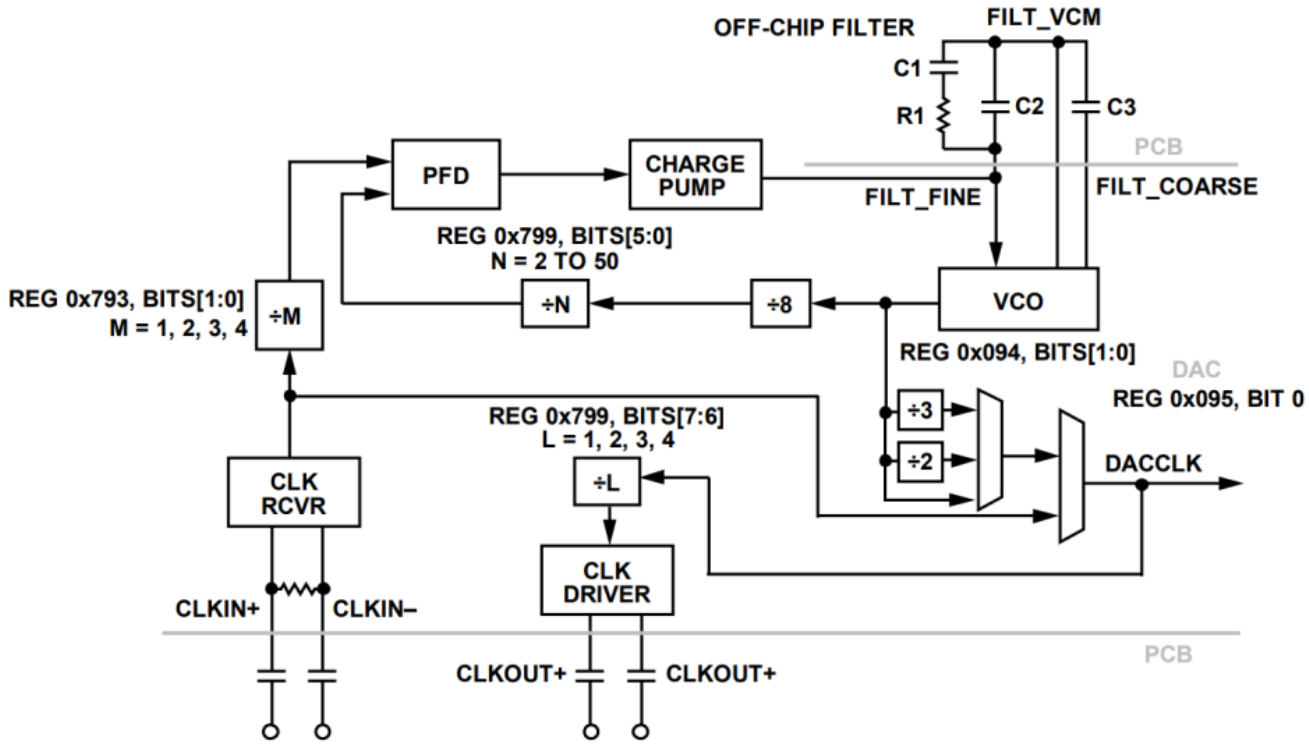


Figure 48: DAC PLL and clock path block diagram

5.2 时钟输出驱动器 / 5.2 Clock Output Driver

English: The SXD052 can generate a high-quality, divided-down DACCLK that can be used to clock critical system components (such as a companion ADC). The integer clock divider supports divide ratios of 1, 2, 3 and 4, programmable through Bits[7:6] of Register 0x799 to set the required output frequency. The 3 dB bandwidth of the clock driver is between 727.5 MHz and 3 GHz; when the generated frequency exceeds this range, the power and spurious performance of the clock output are affected to some extent.

The clock driver does not affect the performance of the DACx analog outputs.

中文： SXD052 能够产生高质量的、分频后的 DACCLK，可用于为关键系统元件（如配套的 ADC）提供时钟。整数时钟分频器支持 1、2、3 和 4 的分频比，可通过寄存器 0x799 的 Bit[7:6]进行编程，以设置所需的输出频率。时钟驱动器的 3dB 带宽介于 727.5MHz 和 3GHz 之间，当产生的频率超出此范围后，时钟输出的功率和杂散性能都会受到一定影响。

时钟驱动器不会影响 DACx 模拟输出的性能。

5.3 模拟输出 / 5.3 Analog Output

English: The SXD052 provides two completely independent DAC cores (DAC0 and DAC1), each of which can output differentially. Figure 49 shows the equivalent output circuit of a single DAC core. Each output is connected to a 100 Ω resistor (RINT), so no resistive termination of the DAC output is needed externally on the PCB. To correctly DC-bias the output stage, two RF chokes are required (one for each output branch) to provide a DC current path for the static current of each DACx output. The inductance value of the chokes depends on the required output frequency range. In general, the larger the choke, the lower the cutoff output frequency.

Due to parasitic capacitance and inductance at the output, a constant 100 Ω termination impedance cannot easily be maintained over the entire operating frequency range of the SXD052. The output impedance of each DAC can be determined by measurement. In general, when the DAC output is matched to a typical single-ended 50 Ω load, a ~2:1 balun is recommended for operating frequencies below 2 GHz. When the operating frequency is above ~2 GHz, a 1:1 balun is recommended; with suitable PCB layout techniques, the output 3 dB bandwidth can also be extended above 4 GHz.

中文： SXD052 提供两个完全独立的 DAC 内核（DAC0 和 DAC1），每个内核都可差分输出。图 49 显示了单个 DAC 内核的等效输出电路。每个输出均接一个 100Ω 的电阻(RINT)，因此无需在 PCB 外部对 DAC 输出进行电阻端接。为了正确地对输出级进行直流偏置，需要两个射频扼流圈（每个输出分支一个），以便为每个 DACx 输出的静态电流提供直流电流路径。扼流圈的电感值取决于所需的输出频率范围。一般来说，扼流圈越大，截止输出频率越低。

由于输出端存在寄生电容和电感，在 SXD052 的整个工作频率范围内无法轻松保持恒定的 100Ω 终端阻抗。每个 DAC 的输出阻抗可通过测量来确定。一般来说，当 DAC 输出与典型的单端 50Ω 负载相匹配时，工作频率低于 2GHz 时，建议使用~2:1 的平衡器。当工作频率高于~2GHz 时，建议使用 1:1 平衡器，通过合适的 PCB 布局技巧，还可将输出的 3dB 带宽扩展到 4GHz 以上。

5.3.1 DAC 满刻度功率 / 5.3.1 DAC Full-Scale Power

English: IOUTFS is the full-scale current output of the positive and negative branches of the DACx output, denoted IP and IN respectively in Figure 49 to Figure 51. The default full-scale current setting is 19.531 mA, but it can be adjusted from 15.625 mA to 25.977 mA by setting an appropriate value in Register 0x05A.

$$IOUTFS = -15.625\ mA + FSC_CTRL \times (25/256)\ (mA)$$

As shown in Figure 49 to Figure 51, the power delivered to the external load depends on multiple factors, such as the IOUTFS setting, the internal impedance of the DAC, the external load, and the parasitic inductance and capacitance of the PCB and other components at the output. The true power that can be delivered to the load is determined by measurement.

Alternatively, the DAC output power can be estimated through a DAC equivalent model, by making assumptions about the parasitic load produced by a specific PCB design. Assume the DAC output can be modeled as a pair of DC current sources continuously providing DC current (set to IOUTFS/2), summed with a parallel AC current source set by the input data samples (i.e. DACCODE), sampling the analog output at the DACCLK rate. Together these three current sources model the output switch network inside

each analog output and determine the instantaneous current of each positive and negative branch of the differential output (IP and IN, respectively).

Assuming the parasitic capacitance and inductance are negligible (which is not always the case in practice, especially at output frequencies above ~2 GHz), the output current into the load can be calculated as follows: IP = (DACCODE + 2^(N−1)) × ILSB, IN = ((2^(N−1−1)) − DACCODE) × ILSB and ILOAD = (IP − IN) × RINT/(RINT + RLOAD)

where ILSB = IOUTFS/2^N, and DACCODE is a sample value between −2^(N−1) and 2^(N−1)−1 (as the signed decimal representation of the binary data).

For a single-tone output (a pure sine wave), the RMS power delivered to the load can be calculated as follows: ILOAD(RMS) = ILOAD_MAX/$\sqrt{2}$ where ILOAD_MAX is the maximum load current output at the maximum DACCODE. PLOAD(W) = $(\text{ILOAD(RMS)})^2$ × RLOAD PLOAD(dBm) = 10 × log(PLOAD(W × 1000))

中文： IOUTFS 是 DACx 输出正负分支的满量程电流输出，在图 49 至图 51 中分别表示为 IP 和 IN。默认满量程电流设置为 19.531mA，但可通过在寄存器 0x05A 中设置合适的值，将其调整为 15.625mA 至 25.977mA。

IOUTFS=-15.625mA+FSC_CTRL×(25/256)(mA)

如图 49 至图 51 所示，输出到外部负载的功率取决于多种因素，如 IOUTFS 设置、DAC 的内部阻抗、外部负载以及 PCB 和其他元件在输出端的寄生电感和电容。可输送到负载的真正功率是通过测量确定的。

另外，也可以通过 DAC 等效模型估算 DAC 输出功率，方法是对特定 PCB 设计所产生的寄生负载做出假设。假设 DAC 输出可模拟为一对持续提供直流电的直流电流源（设置为 IOUTFS/2），与输入数据样本（即 DACCODE）设置的并联交流电流源相加，以 DACCLK 的速率对模拟输出进行采样。这三个电流源共同模拟了每个模拟输出内部的输出开关网络，确定了每个差分输出正负分支（分别为 IP 和 IN）的瞬时电流。

假定寄生电容和电感可以忽略不计（实际情况并非总是如此，尤其是在输出频率高于~2GHz 时），负载的输出电流可按下式计算： IP=(DACCODE+2N-1)×ILSB，IN=((2N-1-1)-DACCODE)×ILSB 和 ILOAD=(IP-IN)×RINT/(RINT+RLOAD) 其中，ILSB=IOUTFS/2N，DACCODE 是介于-2N-1 和 2N-1-1 之间的采样值（作为二进制数据的带符号十进制表示）。

对于单音输出（纯正弦波），输送到负载的均方根功率可计算如下： ILOAD(RMS)=ILOAD_MAX/ 其中，ILOAD_MAX 是在最大 DACCODE 下输出的最大负载电流 PLOAD(W)=(ILOAD(RMS))2×RLOAD PLOAD(dBm)=10×log(PLOAD(W×1000))

5.3.2 MSB Shuffle / 5.3.2 MSB Shuffle

English: Depending on the analog signal level, part or all of the MSB current sources of the DAC may be static (unused). Especially at lower signal levels, when most MSBs are static, the mismatch errors of the few dynamic MSBs may cause the spurious performance of the analog output to degrade. If, before the DACx analog output samples, the active MSBs are continuously remapped (or shuffled) and randomly selected from the total number of available MSBs, the spurious performance improves. MSB shuffle is a form of error averaging. Because the accumulated error is pseudorandom, the improvement in SFDR comes at the cost of a higher NSD.

Shuffle is only feasible when there are spare MSBs. Therefore, as the number of dynamic MSBs increases, the effect of shuffle decreases, for example for signals that frequently peak near the DAC full-scale current.

Taking a full-scale sine-wave output as an example, MSB shuffle has almost no advantage compared with the performance of traditional (thermometer) coding.

As mentioned earlier, MSB shuffle is a form of error averaging. A specific SXD052 device has its own automatic calibration factors and unique production process variations; at certain signal levels, the spurious performance may improve with MSB shuffle disabled. However, if applied to a group of devices with static functionality, the overall spurious performance improves.

MSB shuffle can be enabled through the MSB_SHUFFLE_EN bit (Bit 4 of Register 0x151).

中文： 根据模拟信号电平的不同，DAC 的部分或全部 MSB 电流源可能是静态的（未使用）。特别是在较低的信号电平下，当大多数 MSB 都是静态时，少数动态 MSB 的失配误差可能会导致模拟输出的杂散性能下降。如果在 DACx 模拟输出采样前，从可用 MSB 总数中连续重新映射（or shuffled）和随机选择有效 MSB，则杂散性能会得到改善。MSB shuffle 是误差平均化的一种形式。由于累积误差是伪随机的，因此 SFDR 的改善是以更高的 NSD 为代价的。

只有在有空余的 MSB 的情况下，shuffle 才是可行的。因此，随着动态 MSB 数量的增加，shullfe 的作用会下降，例如对于在 DAC 满量程电流附近频繁出现峰值的信号。以满量程正弦波输出为例，与传统（温度计）编码的性能相比，MSB shuffle 的几乎毫无优势。

如前所述，MSB shuffle 是一种误差平均化的形式。特定的 SXD052 器件有自己的自动校准因子和独特的生产工艺变化，在禁用 MSB shuffle 后，某些信号电平的杂散性能可能会有所改善。但是，如果应用到一组具有静态功能的器件，则总体杂散性能会有所改善。

可通过 MSB_SHUFFLE_EN 位（寄存器 0x151 的 Bit4）启用 MSB shuffle。

5.3.3 直流耦合操作 / 5.3.3 DC-Coupled Operation

English: In some applications, the analog output needs to be DC-coupled to an external device, such as a modulator or a differential amplifier.

As long as the common-mode voltage (the DC voltage shared by the positive and negative branches of a specific analog output) is kept below 100 mV, the performance of the SXD052 analog output is not degraded when DC-coupled. For AC-coupled operation, the output is usually DC-shorted to ground or 0 V through an RF choke or a specific balun configuration.

Raising the common-mode voltage to between 100 mV and 300 mV causes performance degradation. Raising the common-mode voltage above 300 mV may cause long-term, irreversible damage to the analog output.

Ideally, the common-mode voltage at the analog output is kept at or near 0 V or ground, while the load impedance at the analog output matches its internal impedance. Using a 50 Ω resistor connected to ground in place of the RF choke used in AC-coupled operation is not recommended, because this causes an excessively high common-mode voltage, close to 250 mV. Instead, the 50 Ω resistor should be connected to a −0.6 V reference supply, thereby maintaining proper DC bias on the analog output devices inside each DAC output.

The 0 V common-mode output voltage of the SXD052 can be resistively matched to the nonzero common-mode input voltage of a downstream device (such as the 0.5 V input common-mode typical of some

modulators). This matching inevitably causes a loss of the maximum power delivered to the downstream device, because part of the power is dissipated in the resistive matching network.

中文： 在某些应用中，需要将模拟输出直流耦合到外部设备，如调制器或差分放大器。

只要共模电压（特定模拟输出的正负分支共用的直流电压）保持在 100mV 以下，SXD052 模拟输出被直流耦合时，就不会降低性能。对于交流耦合操作，输出通常通过射频扼流圈或特定的平衡器配置将直流短路至接地端或 0V。

将共模电压提高到 100mV 至 300mV 之间会导致性能下降。将共模电压提高到 300mV 以上可能会对模拟输出造成长期、不可逆的损坏。

理想情况下，模拟输出端的共模电压保持在 0V 或接地附近，同时模拟输出端的负载阻抗与其内部阻抗相匹配。不建议用 50Ω 电阻接通接地端来代替交流耦合操作中使用的射频扼流圈，因为这会导致过高的共模电压，接近 250mV。相反，应将 50Ω 电阻与-0.6V 基准电源相连，从而在每个 DAC 输出内部的模拟输出设备上保持适当的直流偏置。

可以将 SXD052 的 0V 共模输出电压与下游设备的非零共模输入电压（如某些调制器典型的 0.5V 输入共模）进行电阻匹配。这种匹配不可避免地会导致向下游设备输出的最大功率的损失，因为部分功率会耗散在电阻匹配网络中。

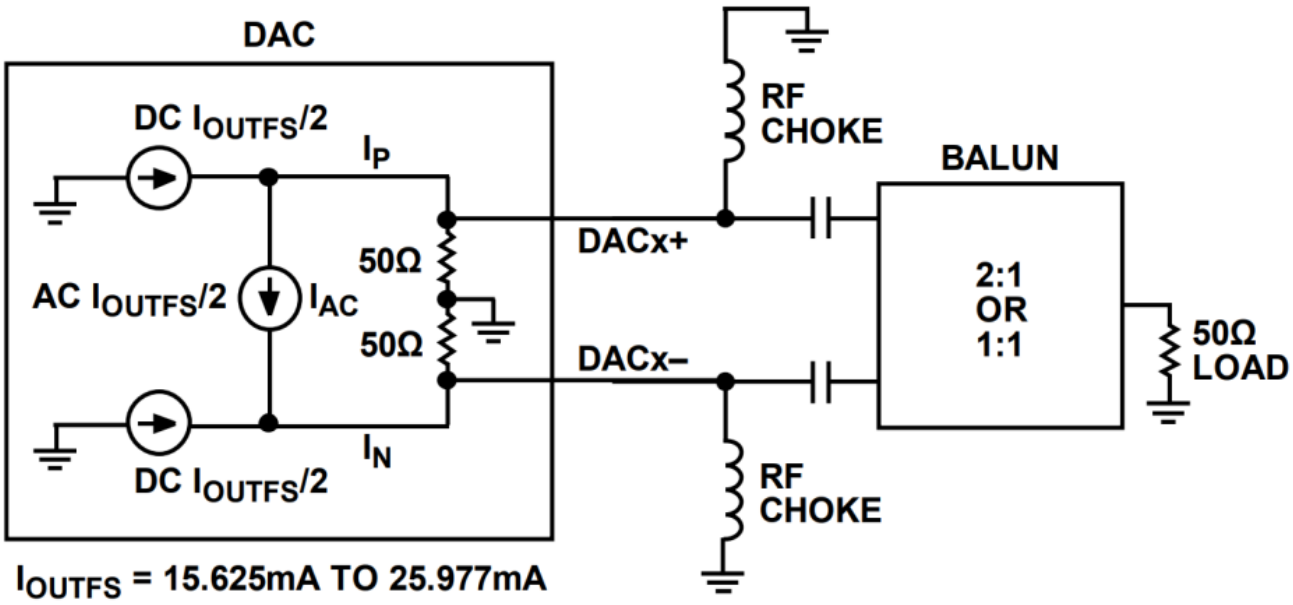


Figure 49: Equivalent DAC output circuit and recommended DAC output network

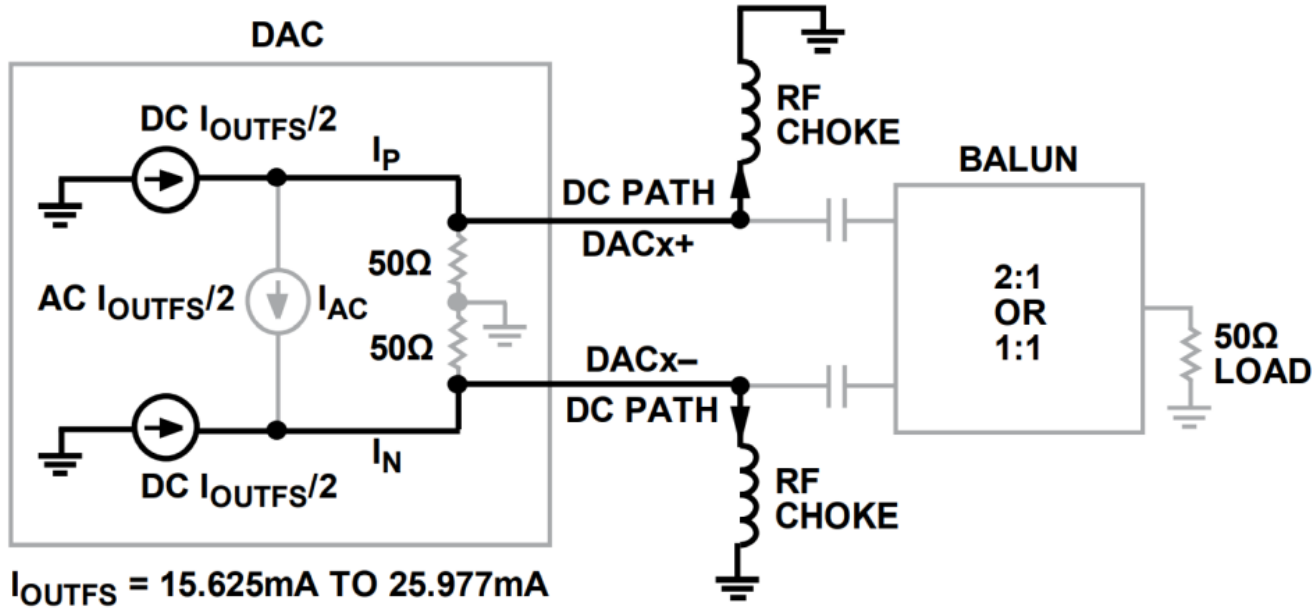


Figure 50: DACx output, DC path (AC-coupled operation)

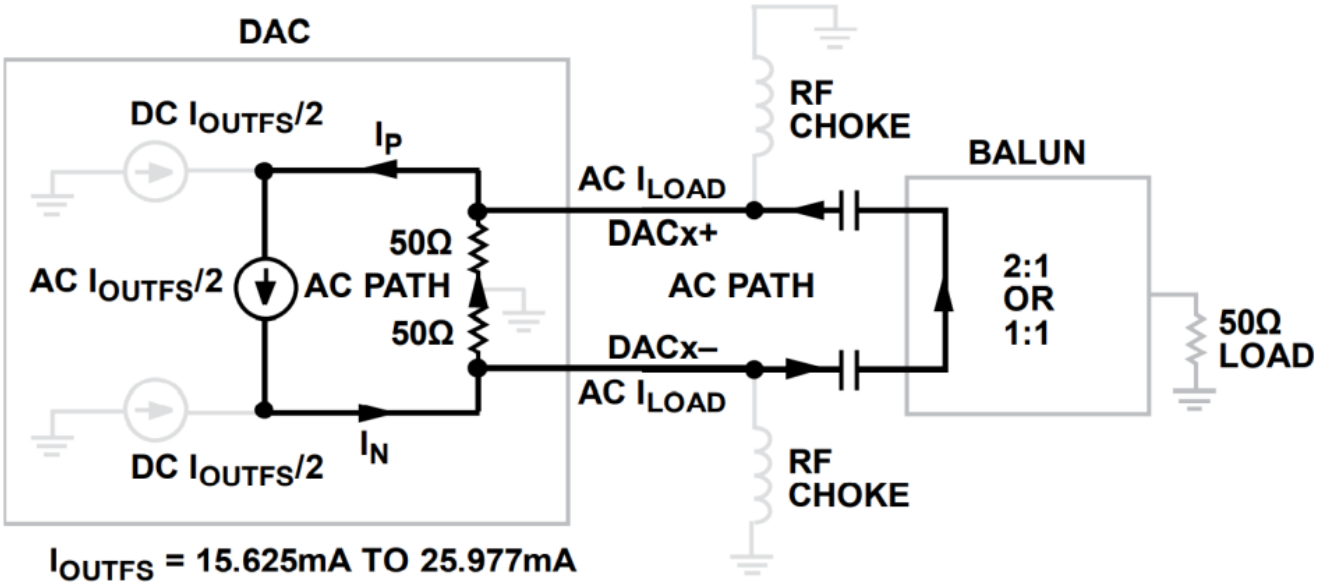


Figure 51: DACx output, DC path (AC-coupled operation)

6、应用信息 / 6. Application Information

6.1 硬件注意事项 / 6.1 Hardware Considerations

6.1.1 电源建议 / 6.1.1 Power Supply Recommendations

English: All SXD052 power domains must be kept as noise-free as possible for best operating condition. The frequency components of power supply noise affect performance, expressed in Vrms.

An LC filter is recommended at the power supply output to attenuate noise, and it must be as close to the SXD052 as possible. The AVDD1.0 supply, which powers the clock receiver and the DAC analog core circuitry, and the AVDD1.8 supply, which powers the DAC output and DAC PLL blocks, are the most noise-

sensitive supplies on the device. Ultra-low-noise regulators such as the ADP1763 and ADM7154 are strongly recommended to power AVDD1.0 and AVDD1.8 separately, to achieve the best possible phase noise performance. Noisier regulators bring phase noise to the DAC output.

The DVDD1.0 supply powers the digital datapath blocks, and the SVDD1.0 supply powers the SERDES circuitry on the chip. The DVDD1.8 supply powers the circuit blocks associated with the SPI, the SYNCOUTx± transmitter, the SYSREF receiver, IRQ0̄/IRQ1̄, SDO and TXENx circuits.

Note the maximum power consumption shown in Table 38, to ensure the power supply design can withstand extreme temperatures and IC process variations. The current consumed depends on the selected use case; Table 38 provides the specifications of several use cases to illustrate the contribution of the individual blocks and to help calculate the maximum current required by each supply.

Another consideration in power supply design is peak current handling capability. Compared with idle mode or synthesizing a DC signal, when the SXD052 synthesizes signals with large amplitude variation (such as modulated signals), the current of the main digital supply is larger. Therefore, the power supply must be able to deliver current quickly to accommodate burst signals, such as GSM, TDMA or other signals with on/off time-domain responses.

Because the amount of current variation depends on the signal used, laboratory testing is best performed first to determine the range. Typically the difference can reach several hundred milliamps.

中文： 所有 SXD052 电源域都必须尽可能保持无噪声，以实现最佳运行状态。电源噪声的频率成分会影响性能，其单位为 Vrms。

建议在电源输出端安装一个 LC 滤波器来衰减噪声，而且必须尽可能靠近 SXD052。为时钟接收器和 DAC 模拟核心电路供电的 AVDD1.0 电源和为 DAC 输出和 DAC PLL 模块供电的 AVDD1.8 电源是器件上对噪声最敏感的电源。强烈建议使用 ADP1763 和 ADM7154 等超低噪声稳压器单独为 AVDD1.0 和 AVDD1.8 供电，以尽可能实现最佳的相位噪声性能。噪声较大的稳压器会给 DAC 输出带来相位噪声。

DVDD1.0 电源为数字数据通路模块供电，SVDD1.0 电源为芯片上的 SERDES 电路供电。DVDD1.8 电源为与 SPI、SYNCOUTx± 发送器、SYSREF 接收器、IRQ0̄、IRQ1̄、SDO 和 TXENx 电路相关的电路模块供电。

请注意表 38 中显示的最大功耗，以确保电源设计能够承受极端温度和集成电路工艺变化。所消耗的电流取决于所选择的用例，表 38 提供了几个用例的规格，以举例说明各个模块的贡献，并帮助计算每个电源所需的最大电流。

电源设计的另一个考虑因素是峰值电流处理能力。与空闲模式或合成直流信号相比，SXD052 在合成幅度变化较大的信号（如调制信号）时，主数字电源的电流更大。因此，电源必须能够快速提供电流，以适应突发信号，如 GSM、TDMA 或其他具有开或关时域响应的信号。

由于电流变化量取决于所使用的信号，因此最好先进行实验室测试以确定范围。通常差异可达几百毫安。

表 38 电源直流规格表 / Table 38. Power Supply DC Specifications

参数 / Parameter	测试条件/说明 / Test Conditions / Notes	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
双链路模式，模式 1 (L = 2, M = 4, NP = 16, N = 16) / Dual-link mode, Mode 1 — DAC 速率 11.7965 GSPS，PLL 参考时钟 184.32					

参数 / Parameter	测试条件/说明 / Test Conditions / Notes	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
MHz，总插值 32 倍 (4x, 8x)，-3 dBFS 下 40 MHz 音调，通道增益 = -6 dB，通道 NCO = ±150 MHz，主 NCO = 2 GHz，SYNCOUTx± 处于 LVDS 模式 / DAC rate 11.7965 GSPS, PLL reference clock 184.32 MHz, total interpolation 32× (4x, 8x), 40 MHz tone at -3 dBFS, channel gain = -6 dB, channel NCO = ±150 MHz, main NCO = 2 GHz, SYNCOUTx± in LVDS mode					
AVDD1.0	所有电源电平设置为标称值 / All supply levels set to nominal		725	1020	mA
AVDD1.0	所有电源电平设置为 5% 容差 / All supply levels at 5% tolerance		775	1120	mA
AVDD1.8			110	130	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；所有电源电平设置为标称值 / Current consumption combined with the DAVDD1.0 supply; nominal		1100	1670	mA
DVDD1.0	所有电源处于 5% 容差 / All supplies at 5% tolerance		1170	1850	mA
DVDD1.8			35	50	mA
SVDD1.0	所有电源电平设置为标称值 / Nominal		290	510	mA
SVDD1.0	所有电源处于 5% 容差 / 5% tolerance		305	560	mA
总功耗 / Total power			2.37	3.38	W
模式 4 (L = 4, M = 4, NP = 16, N = 16) / Mode 4 — DAC 速率 11.7965 GSPS，PLL 参考时钟 491.52 MHz，总插值 24 倍 (3x, 8x)，-3 dBFS 下 40 MHz 音调，通道增益 = -6 dB，通道 NCO = ±150 MHz，主 NCO = 2 GHz，SYNCOUTx± 处于 LVDS 模式 / DAC rate 11.7965 GSPS, PLL ref 491.52 MHz, total interpolation 24× (3x, 8x), 40 MHz tone at -3 dBFS, channel gain -6 dB, channel NCO ±150 MHz, main NCO 2 GHz, SYNCOUTx± LVDS					
AVDD1.0			725		mA
AVDD1.8			110		mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗 / Combined with DAVDD1.0		1150		mA
DVDD1.8			35		mA
SVDD1.0			425		mA
总功耗 / Total power			2.56		W
模式 0 (L = 1, M = 2, NP = 16, N = 16) / Mode 0 — DAC 速率 5.89824 GSPS，PLL 参考时钟 184.32 MHz，总插值 16 倍 (2x, 8x)，-3 dBFS 下 40 MHz 音调，通道 NCO 禁用，主 NCO = 1.8425 GHz，SYNCOUTx±					

参数 / Parameter	测试条件/说明 / Test Conditions / Notes	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
处于 LVDS 模式 / DAC rate 5.89824 GSPS, PLL ref 184.32 MHz, total interpolation 16× (2x, 8x), 40 MHz tone at -3 dBFS, channel NCO disabled, main NCO 1.8425 GHz, SYNCOUTx± LVDS					
AVDD1.0	所有电源电平设置为标称值 / Nominal		400	670	mA
AVDD1.0	所有电源处于 5% 容差 / 5% tolerance		425	745	mA
AVDD1.8			110	130	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值 / Combined with DAVDD1.0; nominal		570	960	mA
DVDD1.0	所有电源处于 5% 容差 / 5% tolerance		610	1070	mA
DVDD1.8			35	50	mA
SVDD1.0	所有电源电平设置为标称值 / Nominal		175	340	mA
总功耗 / Total power			1.40	2.15	W
模式 3 (L = 2, M = 2, NP = 16, N = 16) / Mode 3 — DAC 速率 11.7965 GSPS，PLL 参考时钟 184.32 MHz，总插值 24 倍 (3x, 8x)，-3 dBFS 下 40 MHz 音调，通道 NCO 禁用，主 NCO = 2.655 GHz，SYNCOUTx± 处于 LVDS 模式 / DAC rate 11.7965 GSPS, PLL ref 184.32 MHz, total interpolation 24× (3x, 8x), 40 MHz tone at -3 dBFS, channel NCO disabled, main NCO 2.655 GHz, SYNCOUTx± LVDS					
AVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		725 / 775		mA
AVDD1.8			110		mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值；5% 容差 / Combined with DAVDD1.0; nominal; 5% tolerance		1020 / 1070		mA
DVDD1.8			35		mA
SVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		245 / 250		mA
总功耗 / Total power			2.25		W
模式 9 (L = 4, M = 2, NP = 16, N = 16) / Mode 9 — DAC 速率 12 GSPS，PLL 参考时钟 187.5 MHz，总插值 8 倍 (1x, 8x)，-3 dBFS 下 10 MHz 音调，通道 NCO 禁用，主 NCO = 3.072 GHz，SYNCOUTx± 处于 LVDS 模式 / DAC rate 12 GSPS, PLL ref 187.5 MHz, total interpolation 8× (1x, 8x), 10 MHz tone at -3 dBFS, channel NCO disabled, main NCO 3.072 GHz, SYNCOUTx± LVDS					
AVDD1.0			740 / 785	1030 / 1135	mA

参数 / Parameter	测试条件/说明 / Test Conditions / Notes	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance				
AVDD1.8			110	130	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值；5% 容差 / Combined with DAVDD1.0; nominal; 5% tolerance		1010 / 1070	1580 / 1740	mA
DVDD1.8			35	50	mA
SVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		530 / 550	840 / 910	mA
总功耗 / Total power			2.54	3.63	W
模式 2 (L = 3, M = 6, NP = 16, N = 16) / Mode 2 — DAC 速率 12 GSPS，PLL 参考时钟 375 MHz，总插值 48 倍 (6x, 8x)，-3 dBFS 下 30 MHz 音调，通道增益 = -11 dB，通道 NCO = 20 MHz，主 NCO = 2.1 GHz / DAC rate 12 GSPS, PLL ref 375 MHz, total interpolation 48× (6x, 8x), 30 MHz tone at -3 dBFS, channel gain -11 dB, channel NCO 20 MHz, main NCO 2.1 GHz					
AVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		735 / 785	1030 / 1135	mA
AVDD1.8			110	130	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值；5% 容差 / Combined with DAVDD1.0; nominal; 5% tolerance		1370 / 1460	1800 / 1980	mA
DVDD1.8			35	50	mA
SVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		410 / 430	680 / 755	mA
总功耗 / Total power			2.77	3.69	W
单链路模式，模式 20 (L = 8, M = 1, NP = 16, N = 16) / Single-link mode, Mode 20 — DAC 速率 6 GSPS，PLL 参考时钟 187.5 MHz，总插值 1 倍 (1x, 1x)，-3 dBFS 下 1.8 GHz 音调，通道和主 NCO 禁用 / DAC rate 6 GSPS, PLL ref 187.5 MHz, total interpolation 1× (1x, 1x), 1.8 GHz tone at -3 dBFS, channel and main NCOs disabled					
AVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		400 / 430	670 / 745	mA
AVDD1.8			75	100	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值；5% 容差 / Combined with DAVDD1.0; nominal; 5% tolerance		390 / 410	700 / 810	mA

参数 / Parameter	测试条件/说明 / Test Conditions / Notes	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
DVDD1.8			35	50	mA
SVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		525 / 550	820 / 880	mA
总功耗 / Total power			1.51	2.34	W
模式 12 (L = 8, M = 2, NP = 12, N = 12) / Mode 12 — DAC 速率 4 GSPS，PLL 参考时钟 187.5 MHz，总插值 1 倍 (1x, 1x)，-3 dBFS 下 1 GHz 音调，通道和主 NCO 禁用 / DAC rate 4 GSPS, PLL ref 187.5 MHz, total interpolation 1× (1x, 1x), 1 GHz tone at -3 dBFS, channel and main NCOs disabled					
AVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		300 / 315	550 / 620	mA
AVDD1.8			75	100	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值；5% 容差 / Combined with DAVDD1.0; nominal; 5% tolerance		320 / 350	630 / 725	mA
DVDD1.8	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		35	50	mA
SVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		525 / 550	820 / 880	mA
总功耗 / Total power			1.34	2.15	W
双链路，模式 3（仅 NCO，单通道模式，无 SERDES）/ Dual-link, Mode 3 (NCO only, single-channel mode, no SERDES) — DAC 速率 6 GSPS，PLL 参考时钟 300 MHz，总插值 8 倍 (1x, 8x)，无输入音调（内部直流电平 = 0x50FF），通道 NCO = 40 MHz，主 NCO = 1.8425 GHz / DAC rate 6 GSPS, PLL ref 300 MHz, total interpolation 8× (1x, 8x), no input tone (internal DC level = 0x50FF), channel NCO 40 MHz, main NCO 1.8425 GHz					
AVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		410 / 435	660 / 750	mA
AVDD1.8			110	130	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值；5% 容差 / Combined with DAVDD1.0; nominal; 5% tolerance		500 / 515	780 / 950	mA
DVDD1.8	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		0.3	1	mA
SVDD1.0			5/3	100 / 120	mA

参数 / Parameter	测试条件/说明 / Test Conditions / Notes	最小值 / Min	典型值 / Typ	最大值 / Max	单位 / Unit
总功耗 / Total power			1.11	1.671	W
双链路，模式 4（仅 NCO，双通道模式，无 SERDES）/ Dual-link, Mode 4 (NCO only, dual-channel mode, no SERDES) — DAC 速率 12 GSPS，PLL 参考时钟 500 MHz，总插值 32 倍 (4x, 8x)，无输入音调（内部直流电平 = 0x2AFF），通道 NCO = ±150 MHz，主 NCO = 2 GHz / DAC rate 12 GSPS, PLL ref 500 MHz, total interpolation 32× (4x, 8x), no input tone (internal DC level = 0x2AFF), channel NCO ±150 MHz, main NCO 2 GHz					
AVDD1.0	所有电源电平设置为标称值；所有电源处于 5% 容差 / Nominal; 5% tolerance		750 / 790	1030 / 1130	mA
AVDD1.8			110	130	mA
DVDD1.0	与 DAVDD1.0 电源合并的电流消耗；标称值；5% 容差 / Combined with DAVDD1.0; nominal; 5% tolerance		1200 / 1300	1590 / 1750	mA
DVDD1.8			0.3	1	mA
SVDD1.0			5	100	mA
总功耗 / Total power			2.15	2.851	W

6.1.2 电源和接地平面 / 6.1.2 Power and Ground Planes

English: A solid ground plane is recommended to avoid forming ground loops and to provide a solid, uninterrupted ground reference for high-speed transmission lines that require controlled impedance. Stacking power planes between ground layers is recommended for high-frequency filtering. In addition to decoupling capacitors, this also adds extra filtering and isolation between power domains.

Do not use a split power plane as the reference for controlled-impedance routing, unless the controlled-impedance trace length crosses only one split plane. The guidelines for these high-speed transmission line topologies and other guidelines are introduced in the JESD204B serial interface inputs (SERDIN0± to SERDIN7±) section.

For some applications requiring the highest performance and higher output frequencies, the choice of PCB material can significantly affect the results. For example, materials such as polyimide or Rogers materials can be used to improve high-temperature tolerance and performance. In some evaluation board designs, Rogers 4350 material was used for the top three layers (between the top signal layer and the ground layer below).

中文： 建议使用实心接地平面，以避免形成接地环路，并为需要控制阻抗的高速传输线提供坚实、不间断的接地参考。建议在接地层之间堆叠电源平面，以实现高频滤波。除了去耦电容外，这样做还能在电源域之间增加额外的滤波和隔离。

除非受控阻抗的走线长度仅穿过一个分段平面，否则不要使用分段电源平面作为受控阻抗的参考。这些高速传输线拓扑结构的指导原则和其他指导原则，在 JESD204B 串行接口输入（SERDIN0±至 SERDIN7±）部分有所介绍。

对于某些需要最高性能和更高输出频率的应用，PCB 材料的选择会对结果产生重大影响。例如，可以使用聚酰亚胺等材料或罗杰斯公司的材料来提高对高温的耐受性和性能。在某些评估板的设计中，顶部三层（在顶部信号层和下面的接地层之间）使用了罗杰斯 4350 材料。

6.1.3 JESD204B 串行接口输入（SERDIN0±至 SERDIN7±）/ 6.1.3 JESD204B Serial Interface Inputs (SERDIN0± to SERDIN7±)

English: When designing the layout of the JESD204B serial interface transmission lines, many factors need to be considered to maintain the best link performance. These factors include insertion loss, return loss, signal skew and the topology of the differential lines.

Insertion loss. The JESD204B specification limits the amount of insertion loss allowed in the transmission channel (see Figure 23). The channel loss allowed by the SXD052 equalization circuitry is far greater than the requirements of the JESD204B specification. PCB designers must still follow the guidelines below to minimize insertion loss: - Place the SXD052 as close as possible to the transmit logic device, and route as directly as possible between the devices, keeping the differential traces short. - With a solid ground plane as the reference, route the differential pairs on a single plane. Routing the SERDES lanes on the same layer as the SXD052 is recommended, to avoid using vias in the SERDES lanes. - Use PCB materials with a low dielectric constant (<4) as much as possible, to minimize loss. - When choosing between stripline technology and microstrip technology, note the following: stripline has lower loss (see Figure 24 and Figure 25) and lower electromagnetic interference, but requires vias, which increases the complexity of impedance control. Microstrip technology is easier to implement (if component placement and density allow routing on the top layer) and simplifies impedance control. - If using the top layer of the printed circuit board is problematic, or the advantages of stripline are desired, follow these recommendations: minimize the number of vias. If possible, use blind vias to eliminate the via stub effect, and use microvias to minimize via inductance. If standard vias are used, use the maximum via length to minimize the stub size. For example, on an 8-layer board, use a stripline pair on Layer 7 (see Figure 52). For each pair of vias, place a pair of ground vias next to them to minimize impedance discontinuity (see Figure 52).

Return loss. The JESD204B specification limits the amount of return loss allowed to exist in the converter device and the logic device, but does not specify the return loss of the channel. Nevertheless, every effort should be made to maintain impedance continuity of the transmission lines between the transmit logic device and the SXD052.

Using few or no vias reduces transmission line impedance mismatch (see the insertion loss section). For microstrip, keep a solid reference below the differential traces (for stripline, above and below the differential traces) to ensure transmission line impedance continuity. If stripline technology is used, follow the guidelines listed in the insertion loss section to minimize impedance mismatch and stub effects.

Another major source of impedance mismatch is the two ends of the transmission line, where the impedance of the termination matches the impedance of the transmission line. The SXD052 handles this matching internally through a termination scheme at the line receiver end that is calibrated. See the interface power-up and input termination section for more information about this circuit and the calibration routine.

Signal skew. There are many sources of signal skew, but the two sources to consider when laying out the PCB are interconnect skew within a single JESD204B link and skew between multiple JESD204B links. In each case, keeping lane length matching within 10 mm (calculated as 12.5 mm × (12.5 Gbps/15.4 Gbps)) is

sufficient for the JESD204B link to operate at up to 15.4 Gbps. This amount of lane length matching is equivalent to about 85% of a UI on the SXD052-FMC-EBZ evaluation board. Managing interconnect skew within a single link is very simple. Managing multiple links across multiple link devices is more complex. However, length matching should follow the 10 mm guideline. Because of the 6-PCLK buffer in the JESD204B receiver, the SXD052 can handle skew larger than 85% UI, but matching lane lengths as closely as possible is still recommended.

Topology. Construct the differential SERDINx± pairs so that each half of the pair has an impedance of 50 Ω to ground. The insertion loss section introduces the trade-offs between stripline and microstrip. In either case, these transmission lines must be isolated from potential noise sources (such as high-speed digital signals and noisy power supplies).

If stripline differential routing is used, a coplanar routing method should be used, routing the two traces on the same layer. Although this method's noise immunity is not as good as the broadside routing method (routing on adjacent layers), it is easier to route and manufacture, thereby maintaining impedance continuity. Figure 53 shows a comparison of broadside and coplanar differential transmitter (Tx) lines.

When considering the relationship between trace width and copper weight and thickness, the speed of the interface must be considered. At gigabit speeds, the surface effect of the conductive material confines the current to the surface. Widening the trace width maximizes the surface area of the conductor, reducing loss. In addition, loosely coupled differential traces can accommodate wider trace widths. When traces must be separated to accommodate components, vias, connectors or other routing obstacles, this coupling helps reduce crosstalk and reduce impedance mismatch. Figure 54 shows a comparison of tightly coupled and loosely coupled differential traces.

AC coupling capacitors. The SXD052 requires the JESD204B input signals to be AC-coupled relative to the signal source. These capacitors must be 100 nF and as close as possible to the transmit logic device. To minimize impedance mismatch at the pads, the package size of the capacitors should be selected so that the pad size on the PCB is as close as possible to the trace width.

中文： 在设计 JESD204B 串行接口传输线的布局时，有许多因素需要考虑，以保持最佳的链路性能。这些因素包括插入损耗、回波损耗、信号偏移和差分线的拓扑结构。

插入损耗：JESD204B 规范限制了传输通道中允许的插入损耗量（见图 23）。SXD052 均衡电路允许的通道损耗远远大于 JESD204B 规范的要求。PCB 设计人员仍然必须遵守以下准则，最大限度地减少插入损耗：将 SXD052 尽可能靠近传输逻辑器件，并尽可能地直接在器件之间布线，从而保持较短的差分走线。以坚实的接地平面为基准，在单个平面上布线差分对。建议在与 SXD052 相同的层上布线 SERDES 通道，以避免在 SERDES 通道中使用通孔。尽可能使用介电常数低（<4）的 PCB 材料，以尽量减少损耗。在选择 stripline 技术和 microstrip 技术时，应注意以下几点：stripline 的损耗较小（见图 24 和图 25），电磁干扰也较小，但需要使用通孔，这会增加阻抗控制的复杂度。microstrip 技术更容易实现（如果元件位置和密度允许在顶层布线），并简化了阻抗控制。如果使用印刷电路板的顶层有问题，或者希望使用 stripline 的优点，请遵循以下建议：尽量减少通孔数量。如果可能的话，使用 blind vias 消除 via stub 效应，使用 microvias 最大限度地降低通孔电感。如果使用标准通孔，请使用最大通孔长度以尽量减小 stub 尺寸。例如，在 8 层电路板上，在第 7 层使用 stripline pair（见图 52）。对于每对通孔，在其旁边放置一对接地通孔，以尽量减少阻抗不连续性（见图 52）。

回波损耗：JESD204B 规范限制了在转换器设备和逻辑设备中允许存在的回波损耗量，但没有规定通道的回波损耗。不过，应尽力保持传输逻辑器件和 SXD052 之间的传输线的阻抗连续。尽量少用或完全不用通孔，可减少传输线阻抗失配（参见插入损耗部分）。对于 microstrip，在差分走线的下方(对于 stripline，在差分走线的上方和下方)，保持稳固的基准，以确保传输线阻抗的连续性。如果使用 stripline 技术，则应遵循插入损耗部分中列

出的指导原则，以尽量减少阻抗失配和 stub 效应。阻抗失配的另一个主要来源是传输线的两端，终端的阻抗与传输线的阻抗相匹配。SXD052 通过校准线路接收端的终端方案在内部处理这种匹配。请参阅接口上电和输入终端部分，了解更多有关该电路和校准例程的详细信息。

信号偏差：信号偏差的来源有很多，但在布局 PCB 时需要考虑的两个来源是单个 JESD204B 链路内的互连偏差和多个 JESD204B 链路之间的偏差。在每种情况下，保持通道长度匹配在 10mm（按 12.5mm×(12.5Gbps/15.4Gbps)计算）以内，就足以让 JESD204B 链路以高达 15.4Gbps 的速度运行。这一通道长度匹配量相当于 SXD052-FMC-EBZ 评估板上约 85%的 UI。管理单个链路内的互连偏移非常简单。在多个链路器件上管理多个链路则更为复杂。不过，长度匹配应遵循 10mm 准则。由于 JESD204B 接收器中的 6PCLK 缓冲器，SXD052 可以处理比 85%UI 更大的偏移，但仍建议尽可能接近匹配的通道长度。

拓扑结构：构建差分 SERDINx±对以实现每对的一半具有对地 50Ω 的阻抗。插入损耗部分介绍了 stripline 与 microstrip 的权衡。无论是哪种情况，都必须将这些传输线与潜在的噪声源（如高速数字信号和噪声电源）隔离。如果使用 stripline 差分走线，则应使用共面的布线方法，将两条走线布在同一层上。虽然这种方法的抗噪能力不如宽侧布线法（在相邻层布线），但它更容易布线和制造，从而保持阻抗的连续性。图 53 显示了宽边和共面差分发射器(Tx)的线路对比。

在考虑走线宽度与铜的重量和厚度的关系时，必须考虑接口的速度。在千兆位速度下，导电材料的表面效应会将电流限制在表面。通过加宽走线宽度来最大化导体的表面积，从而减少损耗。此外，松散耦合差分走线可以适应更宽的走线宽度。当必须分离走线以适应元件、通孔、连接器或其他布线障碍时，这种耦合有助于减少串扰和减少阻抗失配。图 54 显示了紧密耦合与松散耦合的差分走线对比。

交流耦合电容：SXD052 要求 JESD204B 输入信号相对于信号源为交流耦合。这些电容必须为 100nF，并尽可能靠近传输逻辑器件。为尽量减少焊盘处的阻抗失配，应选择电容的封装尺寸，使 PCB 上的焊盘尺寸尽可能地与走线宽度相近。

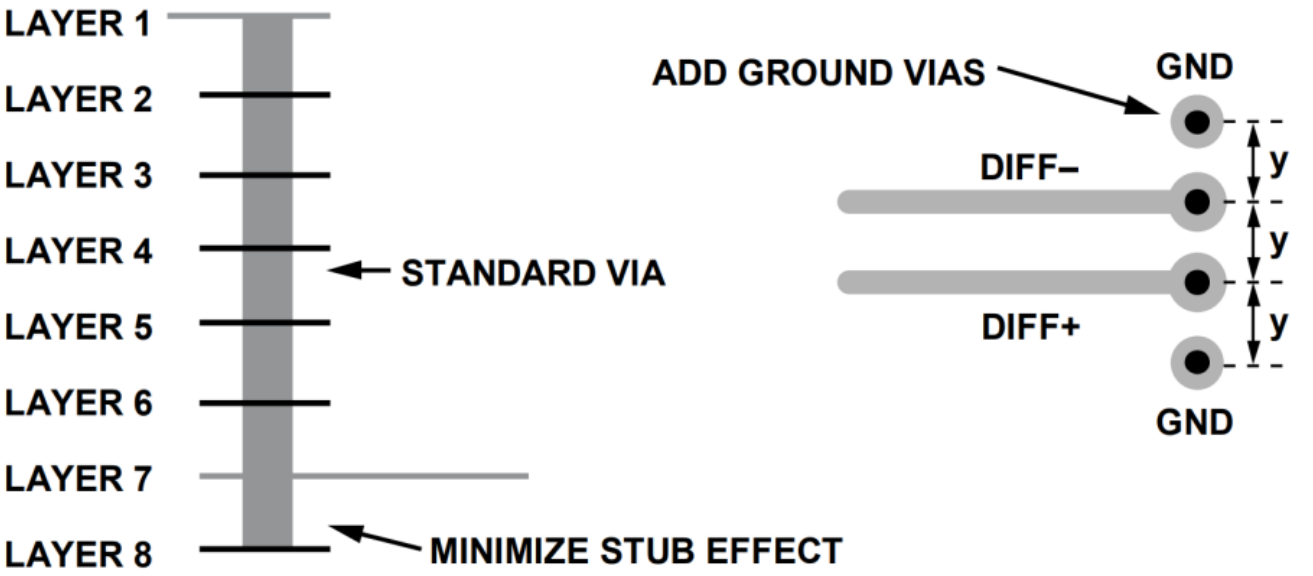


Figure 52: Minimizing stub effects and adding ground vias for differential stripline routing

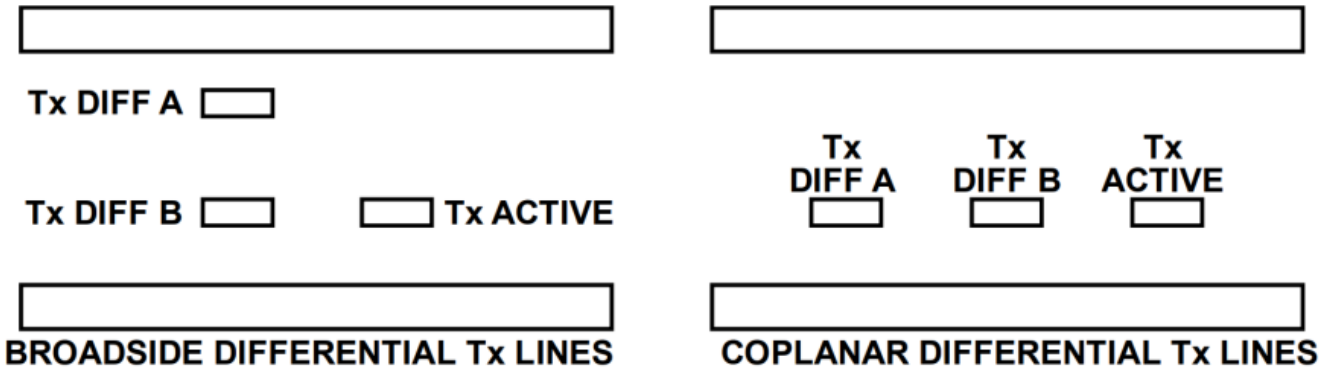


Figure 53: Broadside vs. coplanar differential stripline routing techniques

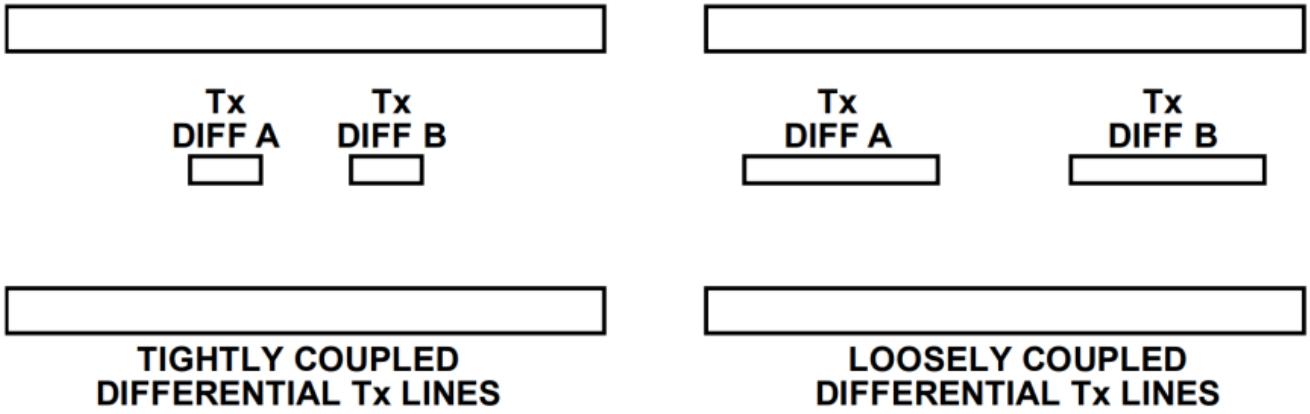


Figure 54: Tightly coupled vs. loosely coupled differential traces

6.1.4 SYSREF±、SYNCOUT$\bar{x}$± 和 CLK±信号 / 6.1.4 SYSREF±, SYNCOUT$\bar{x}$± and CLK± Signals

English: The SYSREF± signal on the SXD052 is a low-speed LVDS differential signal. The SYNCOUTx̄± signals can be in LVDS or CMOS mode. When LVDS mode is selected, these signals should be routed using controlled-impedance traces, routed as 100 Ω differential impedance and 50 Ω to ground. As with SERDIN0± to SERDIN7±, these signals must be separated from potential noise sources such as high-speed digital signals and noisy power supplies. The SYNCOUTx̄± signals are separated from other noisy signals because noise on the SYNCOUTx̄± signals may be understood as a request for /K/ characters. From the clock source to each device at the end of each JESD204B link, the CLK± and SYSREF± signals must keep similar trace lengths (see Figure 55). If a clock chip that can strictly control the CLK± and SYSREF± phases is used, the requirements on trace length matching can be greatly reduced.

中文： SXD052 上的 SYSREF±信号是低速 LVDS 差分信号。SYNCOUTx± 信号可以为 LVDS 或 CMOS 模式。选择 LVDS 模式时，在布线这些信号时，应使用受控阻抗走线，将其布线为 100Ω 差分阻抗和 50Ω 接地。与 SERDIN0±至 SERDIN7±一样，必须将这些信号与高速数字信号和噪声电源等潜在噪声源分离。将 SYNCOUTx± 信号和其他噪声信号分离，是因为 SYNCOUTx± 信号上的噪声可能会被理解为对/K/字符的请求。从时钟源到每一个 JESD204B 链路末端的每个器件，CLK± 和 SYSREF± 信号必须保持相似的走线长度（见图 55）。如果使用可严格控制 CLK± 和 SYSREF±相位的时钟芯片，则可大大降低对走线长度匹配的要求。

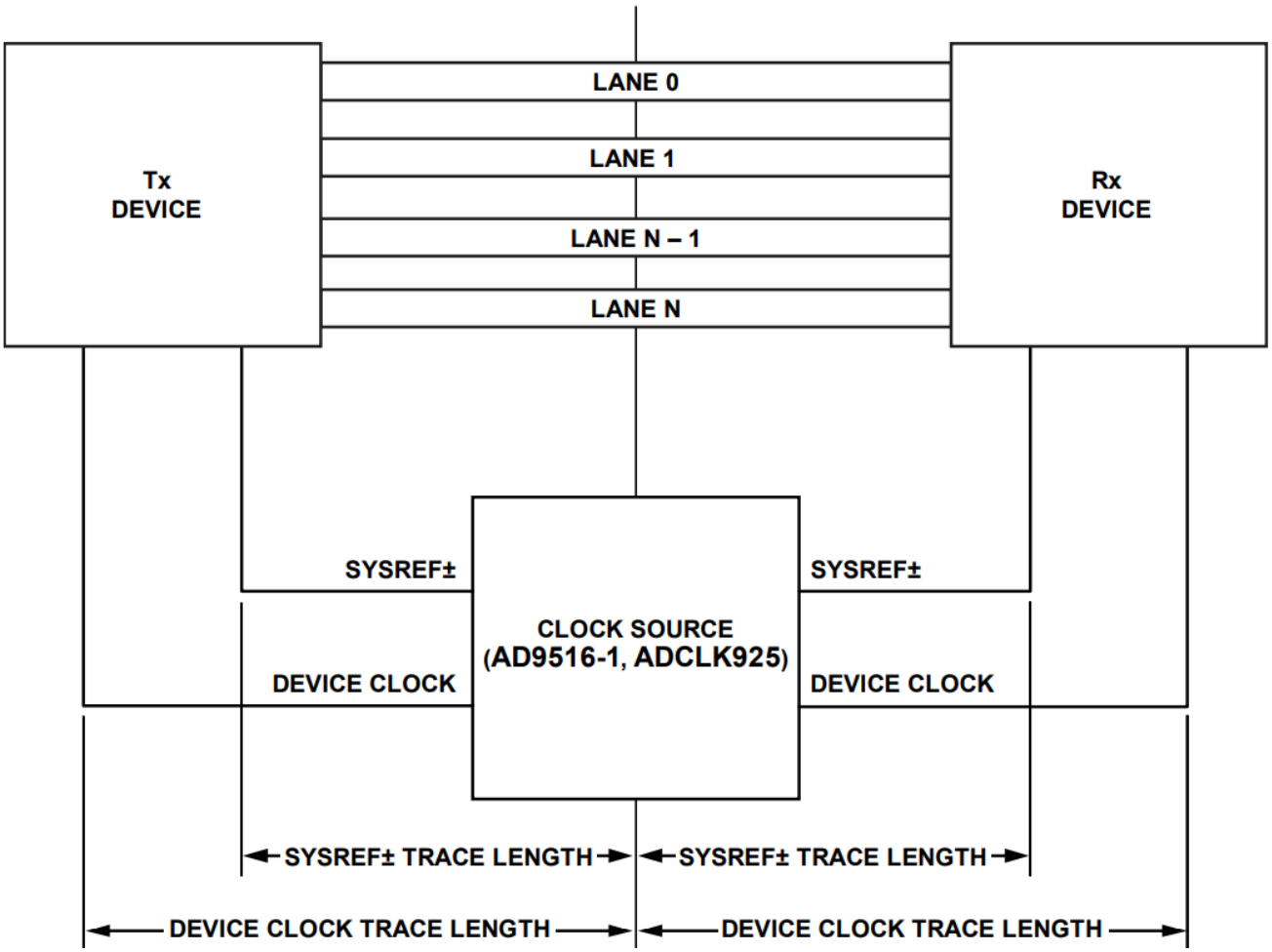


Figure 55: SYSREF± signal and device clock trace lengths

7、启动顺序 / 7. Start-Up Sequence

English: After the SXD052 is powered up, several steps are required to program it to the correct operating state. These steps, listed in Table 39 to Table 48, explain the purpose of each step. The registers noted as "must be written" must be written for proper operation. Blank cells in Table 39 to Table 48, or cells with a variable or bit-field name (capital letters), indicate that the value depends on the result described in the description column.

中文： SXD052 上电后，需要几个步骤才能将其编程到正确的工作状态。这几个步骤，列于表 39 至表 48 中，对每个步骤的目的做出了解释。自用寄存器必须写入才能正常运行。表 39 至表 48 中的空白单元格或带有变量或位字段名称（大写字母）的单元格表示该值取决于说明栏中描述的结果。

表 39 上电和所需寄存器写入 / Table 39. Power-Up and Required Register Writes

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x000	[7:0]	0x81	软重置。/ Soft reset.
W	0x000	[7:0]	0x3C	释放复位并设置为 4 线 SPI（可选；默认为 3 线 SPI）。/ Release reset and set to 4-wire SPI (optional; default is 3-wire SPI).
W	0x091	[7:0]	0x00	上电时钟接收器。/ Power up the clock receiver.

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x206	[7:0]	0x01	使 PHY 脱离复位。/ Bring the PHY out of reset.
W	0x705	[7:0]	0x01	启用 boot loader。/ Enable the boot loader.
W	0x090	[7:0]	0x00	为 DAC 和偏置电路供电。/ Power the DAC and bias circuits.

表 40 DAC PLL 配置 / Table 40. DAC PLL Configuration

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x095	[7:0]	0x00 或 0x01 / 0x00 or 0x01	旁路 PLL。设置为 0x00 时使用内部 DAC PLL。如果用户计划直接提供 DAC 时钟，则将该寄存器设置为 0x01，并执行以下两个寄存器的写入操作；然后跳过本表中的其余写入操作 / Bypass the PLL. Setting 0x00 uses the internal DAC PLL. If the user plans to provide the DAC clock directly, set this register to 0x01, perform the following two register writes, and skip the remaining writes in this table.
W	0x790	[7:0]	0xFF 或 0x00 / 0xFF or 0x00	如果旁路 PLL（寄存器 0x095=0x01），则对该寄存器写入 0xFF。如果使用 PLL，则对该寄存器写入 0x00 / If the PLL is bypassed (Register 0x095 = 0x01), write 0xFF to this register. If the PLL is used, write 0x00.
W	0x791	[7:0]	0x1F 或 0x00	如果旁路 PLL（寄存器 0x095=0x01），则对该寄存器写入 0xFF，然后跳过本表中其余寄存器的写入，继续执行表 41。如果使用 PLL，则对该寄存器写入 0x00，并写入本表中的其余寄存器。/ If the PLL is bypassed, write 0xFF [see flag] to this register, skip the remaining register writes in this table, and continue with Table 41. If the PLL is used, write 0x00 and write the remaining registers in this table.
W	0x796	[7:0]	0xE5	需要写入 DAC PLL / Required DAC PLL write.
W	0x7A0	[7:0]	0xBC	需要写入 DAC PLL / Required DAC PLL write.
W	0x794	[5:0]	DACPLL_CP	设置 DAC PLL 电荷泵电流。建议设置为 0x08，但也可在 0x04 至 0x10 之间进行设置，以实现不同的相位噪声性能目标。/ Set the DAC PLL charge-pump current. A setting of 0x08 is recommended, but 0x04 to 0x10 can also be set for different phase-noise performance targets.
W	0x797	[7:0]	0x10	需要写入 DAC PLL / Required DAC PLL write.
W	0x797	[7:0]	0x20	需要写入 DAC PLL / Required DAC PLL write.
W	0x798	[7:0]	0x10	需要写入 DAC PLL / Required DAC PLL write.
W	0x7A2	[7:0]	0x7F	需要写入 DAC PLL / Required DAC PLL write.
暂停 / Pause				等待 100 毫秒。/ Wait 100 ms.
W	0x799	[7:6]	ADC_CLK_DIVIDER	DAC PLL 分频器设置 — ADC 驱动器/时钟输出分频比。0b00=÷1；0b01=÷2；0b10=÷3；0b11=÷4 / DAC PLL divider setting — ADC driver/clock output divide ratio.
W	0x799	[5:0]	N_DIVIDER	可编程 N 分频器。N_DIVIDER=(fDAC×M_DIVIDER)/(8×参考时钟)。/ Programmable N divider. N_DIVIDER = (fDAC × M_DIVIDER)/(8 × reference clock). [原文"参时钟"为"参考时钟"之略]
W	0x793	[7:2]	0x06	DAC PLL 分频器设置 — 留存这些位的默认值 / DAC PLL divider setting — retain the default values of these bits.
W	0x793	[1:0]	M_DIVIDER_1	可编程预分频器 M_DIVIDER_1（in n-1 notation）。相关计算如下：PFD 频率=参考时钟/M_DIVIDER。0b00=÷1；0b01=÷2；0b10=÷3；0b11=÷4 /

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
				Programmable prescaler M_DIVIDER_1 (in n−1 notation). PFD frequency = reference clock/M_DIVIDER.
W	0x094	[7:2]	0x00	留存这些位的默认值。/ Retain the default values of these bits.
W	0x094	1	PLL_VCO_DIV3_EN	启用 PLL 输出时钟除以 3。如果该位设置为 1，则 DAC 时钟=PLL VCO 频率/3。/ Enable PLL output clock divide-by-3. If set to 1, DAC clock = PLL VCO frequency/3.
W	0x094	0	PLL_VCO_DIV2_EN	启用 PLL 输出时钟除以 2。该寄存器中的该位或位 1 均可设置为 1，但不能同时设置（没有除以 6 选项）。0b0：DAC 时钟=PLL VCO 频率；0b1：DAC 时钟=PLL VCO 频率/2 / Enable PLL output clock divide-by-2. This bit or Bit 1 can be set to 1, but not both (no divide-by-6 option).
W	0x792	[7:0]	0x02	复位 VCO。/ Reset the VCO.
W	0x792	[7:0]	0x00	
暂停 / Pause				等待 PLL 锁定 100 毫秒。/ Wait 100 ms for PLL lock.
R	0x7B5	0	0b1	通过读回该寄存器第 0 位的 1 值，确保 PLL 锁定。/ Ensure PLL lock by reading back a value of 1 at Bit 0 of this register.

表 41 延迟锁定环路 (DLL) 配置 / Table 41. Delay-Locked Loop (DLL) Configuration

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x0C0	[7:0]	0x00	上电延迟线。/ Power up the delay line.
W	0x0DB	[7:0]	0x00	
W	0x0DB	[7:0]	0x01	更新电路的 DLL 设置。/ Update the DLL settings of the circuit.
W	0x0DB	[7:0]	0x00	
W	0x0C1	[7:0]	0x68 或 0x48 / 0x68 or 0x48	设置 DLL 搜索模式。如果 fDAC 频率小于 4.5GHz，则将该寄存器设置为 0x48。否则，将该寄存器设置为 0x68。/ Set the DLL search mode. If the fDAC frequency is less than 4.5 GHz, set this register to 0x48; otherwise set it to 0x68.
W	0x0C1	[7:0]	0x69 或 0x49 / 0x69 or 0x49	设置 DLL 搜索模式。如果 fDAC 频率小于 4.5GHz，则将该寄存器设置为 0x49。否则，将该寄存器设置为 0x69。/ Set the DLL search mode. If fDAC < 4.5 GHz, set 0x49; otherwise set 0x69.
W	0x0C7	[7:0]	0x01	启用 DLL 读取状态。/ Enable DLL read status.
R	0x0C3	0	0b1	通过读回该寄存器第 0 位的 1 值，确保 DLL 锁定。/ Ensure DLL lock by reading back a value of 1 at Bit 0.

表 42 校准 / Table 42. Calibration

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x050	[7:0]	0x2A	优化校准设置寄存器写入。/ Optimized calibration setting register write.
W	0x061	[7:0]	0x68	需要校准控制寄存器写入。/ Required calibration control register write.
W	0x051	[7:0]	0x82	优化校准设置寄存器写入。/ Optimized calibration setting register write.
W	0x051	[7:0]	0x83	需要校准控制寄存器写入。/ Required calibration control register write.

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x081	[7:0]	0x03	需要校准控制寄存器写入。/ Required calibration control register write.

表 43 JESD204B 模式设置 / Table 43. JESD204B Mode Settings

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x100	[7:0]	0x00	当内部时钟稳定时，启动数字数据通路时钟。/ Start the digital datapath clock when the internal clock is stable.
W	0x110	[5:0]	JESD_MODE	JESD_MODE bit field 的第 5 位决定设备是在单链路还是双链路模式下运行。0=单链路模式；1=双链路模式。位[4:0]决定 SERDES JESD204B 工作模式，可从表 3 或表 4 中相应的单链路或双链路模式中选择。/ Bit 5 of the JESD_MODE bit field determines whether the device operates in single-link or dual-link mode: 0 = single-link, 1 = dual-link. Bits[4:0] determine the SERDES JESD204B operating mode, selectable from the corresponding single-link or dual-link modes in Table 3 or Table 4.
W	0x111	[7:4]	DP_INTERP_MODE	主数据通路插值模式。此控制的有效插补选项取决于寄存器 0x110 中选择的 JESD_MODE。如果 JESD_MODE、DP_INTERP_MODE 和 CH_INTERP_MODE 设置不是有效组合，寄存器 0x110 的第 7 位等于 1。/ Main datapath interpolation mode. The valid interpolation options of this control depend on the JESD_MODE selected in Register 0x110. If the JESD_MODE, DP_INTERP_MODE and CH_INTERP_MODE settings are not a valid combination, Bit 7 of Register 0x110 equals 1.
W	0x111	[3:0]	CH_INTERP_MODE	通道数据通路插值模式。此控制的有效插补选项取决于寄存器 0x110 中选择的 JESD_MODE。如果设置不是有效组合，寄存器 0x110 的第 7 位等于 1。/ Channel datapath interpolation mode. Same combination-validity note as above.
W	0x084	6	SYSREF_INPUTMODE	SYSREF±信号输入模式选择。0b0=交流耦合。0b1=直流耦合。/ SYSREF± signal input mode selection. 0b0 = AC-coupled; 0b1 = DC-coupled.
W	0x084	0	SYSREF_PD	如果使用 Subclass0，可将该位设置为 1 以关闭 SYSREF±接收器。如果使用 Subclass1，则保持默认值 0。/ If Subclass 0 is used, this bit can be set to 1 to shut down the SYSREF± receiver. If Subclass 1 is used, keep the default value 0.
W	0x312	[7:4]		根据所选模式设置 SYNCOUT˜± 错误持续时间。/ Set the SYNCOUT˜± error duration according to the selected mode.
W	0x300	3	LINK_MODE	与寄存器 0x110 中的模式选择相对应。0b0=单链路模式。0b1=双链路模式。/ Corresponds to the mode selection in Register 0x110. 0b0 = single-link mode; 0b1 = dual-link mode.
W	0x300	2	0b0	选择链路 0 进行设置。该位选择正被分页的链路 QBD。0b0=链路 0(QBD0)。0b1=链路 1(QBD1)。/ Select Link 0 for setup. This bit selects the link QBD being paged.
W	0x300	[1:0]	LINK_EN	启用链路。0b01=单链路模式。0b11=双链路模式。/ Enable the link. 0b01 = single-link mode; 0b11 = dual-link mode.
W	0x475	[7:0]	0x09	软复位 JESD204B 四字节解帧器。/ Soft-reset the JESD204B quad-byte deframer.
W	0x453	7	SCR	设置 SERDES 数据的加扰选项。0=禁用加扰。1=启用加扰。/ Set the scrambling option of the SERDES data. 0 = scrambling disabled; 1 = scrambling enabled.
W	0x453	[4:0]	L-1	写入所选 JESD_MODE 的 L 值（in n-1 notation）。/ Write the L value of the selected JESD_MODE (in n−1 notation).
W	0x458	[7:5]	SUBCLASSV	对于 Subclass0，将该位设置为 0。对于 Subclass1，将该位设置为 1。/ For Subclass 0, set to 0. For Subclass 1, set to 1.

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x458	[4:0]	NP_1	写入所选 JESD_MODE 的 NP 值（in n-1 notation）。/ Write the NP value of the selected JESD_MODE (in n−1 notation).
W	0x475	[7:0]	0x01	JESD204B 四字节解帧器脱离复位。/ Bring the JESD204B quad-byte deframer out of reset.
W	0x300			如果在双链路模式下运行，按以下步骤重复写入链路 1。如果以单链路模式运行，则跳过本表中的其余步骤。/ If operating in dual-link mode, repeat the following steps for Link 1. If operating in single-link mode, skip the remaining steps in this table.
W	0x300	3	LINK_MODE	与寄存器 0x110 中的模式选择相对应。0b0=单链路模式。0b1=双链路模式。/ Corresponds to the mode selection in Register 0x110.
W	0x300	2	0b1	选择链路 1 进行设置。该位选择正在被分页的链路 QBD。0b0=链路 0(QBD0)。0b1=链路 1(QBD1)。/ Select Link 1 for setup. This bit selects the link QBD being paged.
W	0x300	[1:0]	0b00	在例程结束前，禁用链路。/ Disable the link before the end of the routine.
W	0x475	[7:0]	0x09	软复位 JESD204B 四字节解帧器。/ Soft-reset the JESD204B quad-byte deframer.
W	0x453	7	SCR	设置 SERDES 数据的加扰选项。0=禁用加扰。1=启用加扰。/ Set the SERDES data scrambling option.
W	0x453	[4:0]	L_1	写入所选 JESD_MODE 的 L 值（in n-1 notation）。/ Write the L value of the selected JESD_MODE (in n−1 notation).
W	0x458	[7:5]	SUBCLASSV	对于 Subclass0，将该位设置为 0。对于 Subclass1，将该位设置为 1。/ For Subclass 0, set 0; for Subclass 1, set 1.
W	0x458	[4:0]	NP_1	写入所选 JESD_MODE 的 NP 值（in n-1 notation）。/ Write the NP value (in n−1 notation).
W	0x475	[7:0]	0x01	使 JESD204B 四字节解扰器脱离复位。/ Bring the JESD204B quad-byte deframer out of reset.

English: Table 44 lists the optional registers used to configure the channel datapath when configuring it for a specific application. If the channel datapath is bypassed (for 1× channel interpolation, CH_INTERP_MODE = 1), Table 44 can be skipped in the start-up sequence.

中文： 表 44 列出了可选寄存器，用于在为特定应用配置通道数据通路时配置这些寄存器。如果旁路了通道数据通路（用于 1×通道插值，CH_INTERP_MODE=1），则可在启动序列中跳过表 44。

表 44 通道数据通路设置：数字增益和通道 NCO / Table 44. Channel Datapath Settings: Digital Gain and Channel NCO

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x008	[5:0]		CHANNEL_PAGE。选择要同时编程的通道（或对每个通道重复此模块以独立编程数值）。该控制的 x 位对应于通道 x 数据路径。/ CHANNEL_PAGE. Select the channels to program simultaneously (or repeat this block for each channel to program values independently). Bit x of this control corresponds to channel x datapath.
W	0x146	[7:0]		CHNL_GAIN[7:0]。写入通道数字增益的 LSB。在分页寄存器 0x008 中配置选定通道的数字增益。计算：CHNL_GAIN=2^{11}×10^(dB Gain/20)，其中 dB Gain 是所需通道增益的增益值，单位为 dB。/ CHNL_GAIN[7:0]. Write the LSBs of the channel digital gain.
W	0x147	[7:0]		

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
				CHNL_GAIN[11:8]。写入通道数字增益的 MSB。计算结果显示在寄存器 0x146 中。/ CHNL_GAIN[11:8]. Write the MSBs of the channel digital gain. The calculation is shown in Register 0x146.
W	0x130	6		为分页寄存器 0x008 中的选定通道启用 NCO。0b0=禁用 NCO。0b1=启用 NCO。/ Enable the NCO for the selected channels in the paging Register 0x008. 0b0 = disable; 0b1 = enable.
W	0x130	2		为分页寄存器 0x008 中的选定通道启用 NCO modulus。0b0=禁用。0b1=启用。/ Enable NCO modulus for the selected channels.
W	0x130	1		从调制结果中选择边带。0b0=上边带。0b1=下边带（频谱翻转）。/ Select the sideband from the modulation result. 0b0 = upper sideband; 0b1 = lower sideband (spectral inversion).
W	0x130	0		如果需要直流测试模式或 NCO 测试模式，则将该位设置为 1 以启用测试 tone 生成。否则，将该位设置为默认值 0。整数 NCO 模式计算：DDSC_FTW=(fCARRIER/fNCO)×2^{48}，其中，fNCO=fDATA/CH_INTERP_MODE。/ If DC test mode or NCO test mode is required, set this bit to 1 to enable test tone generation; otherwise set it to the default 0. Integer NCO mode calculation as in source [see flag].
W	0x132	[7:0]		写入 DDSC_FTW[7:0]。/ Write DDSC_FTW[7:0].
W	0x133	[7:0]		写入 DDSC_FTW[15:8]。/ Write DDSC_FTW[15:8].
W	0x134	[7:0]		写入 DDSC_FTW[23:16]。/ Write DDSC_FTW[23:16].
W	0x135	[7:0]		写入 DDSC_FTW[31:24]。/ Write DDSC_FTW[31:24].
W	0x136	[7:0]		写入 DDSC_FTW[39:32]。/ Write DDSC_FTW[39:32].
W	0x137	[7:0]		写入 DDSC_FTW[47:40]。/ Write DDSC_FTW[47:40].
W	0x138	[7:0]		写入 DDSC_NCO_PHASE_OFFSET[7:0]。计算：DDSC_NCO_PHASE_OFFSET=(Degrees Offset/180)×2^{15}。/ Write DDSC_NCO_PHASE_OFFSET[7:0]. Calculation: DDSC_NCO_PHASE_OFFSET = (Degrees Offset/180) × 2^{15}.
W	0x139	[7:0]		写入 DDSC_NCO_PHASE_OFFSET[15:8]。如果使用 NCO modulus 模式，还需对 modulus 参数进行编程。否则，跳过本节。对于 modulus NCO 模式：(fCARRIER/fNCO)=(X+(A/B))/2^{48}，其中，DDSC_FTW=X，DDSC_ACC_DELTA=A，DDSC_ACC_MODULUS=B。/ Write DDSC_NCO_PHASE_OFFSET[15:8]. If NCO modulus mode is used, the modulus parameters must also be programmed; otherwise skip this section. For modulus NCO mode: (fCARRIER/fNCO) = (X + (A/B))/2^{48}, where DDSC_FTW = X, DDSC_ACC_DELTA = A, DDSC_ACC_MODULUS = B.
W	0x13A	[7:0]		写入 DDSC_ACC_MODULUS[7:0]。/ Write DDSC_ACC_MODULUS[7:0].
W	0x13B	[7:0]		写入 DDSC_ACC_MODULUS[15:8]。/ Write DDSC_ACC_MODULUS[15:8].
W	0x13C	[7:0]		写入 DDSC_ACC_MODULUS[23:16]。/ Write DDSC_ACC_MODULUS[23:16].
W	0x13D	[7:0]		写入 DDSC_ACC_MODULUS[31:24]。/ Write DDSC_ACC_MODULUS[31:24].
W	0x13E	[7:0]		写入 DDSC_ACC_MODULUS[39:32]。/ Write DDSC_ACC_MODULUS[39:32].
W	0x13F	[7:0]		写入 DDSC_ACC_MODULUS[47:40]。/ Write DDSC_ACC_MODULUS[47:40].
W	0x140	[7:0]		写入 DDSC_ACC_DELTA[7:0]。/ Write DDSC_ACC_DELTA[7:0].
W	0x141	[7:0]		写入 DDSC_ACC_DELTA[15:8]。/ Write DDSC_ACC_DELTA[15:8].
W	0x142	[7:0]		写入 DDSC_ACC_DELTA[23:16]。/ Write DDSC_ACC_DELTA[23:16].
W	0x143	[7:0]		写入 DDSC_ACC_DELTA[31:24]。/ Write DDSC_ACC_DELTA[31:24].
W	0x144	[7:0]		写入 DDSC_ACC_DELTA[39:32]。/ Write DDSC_ACC_DELTA[39:32].
W	0x145	[7:0]		写入 DDSC_ACC_DELTA[47:40]。/ Write DDSC_ACC_DELTA[47:40].

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x131	0	0b1	更新所有 NCO 相位和 FTW 字。/ Update all NCO phase and FTW words.

English: If configured for a specific application, Table 45 lists the optional registers used to configure the main DAC datapath. If the main DAC datapath is bypassed (for 1× channel interpolation, DP_INTERP_MODE = 1), Table 45 can be skipped in the start-up sequence.

中文： 如果是为特定应用而配置的话，表 45 列出了用于配置主 DAC 数据通路的可选寄存器。如果旁路了主 DAC 数据通路（用于 1×通道插值，DP_INTERP_MODE=1），则可在启动序列中跳过表 45。

表 45 主 DAC 数据通路设置：PA 保护和主 NCO / Table 45. Main DAC Datapath Settings: PA Protection and Main NCO

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x008	[7:6]		MAINDAC_PAGE。选择要同时编程的主 DAC 数据通路（或对每个 DAC 数据通路重复此模块，以独立编程数值）。该控制的位 x 与 DACx 数据通路相对应。/ MAINDAC_PAGE. Select the main DAC datapaths to program simultaneously (or repeat this block for each DAC datapath to program values independently). Bit x of this control corresponds to the DACx datapath.
W	0x112	3		为分页寄存器 0x008 中的选定通道启用 NCO。0b0=禁用 NCO。0b1=启用 NCO。/ Enable the NCO for the selected datapaths in the paging Register 0x008.
W	0x112	2		为分页寄存器 0x008 中的选定通道启用 NCO modulus。0b0=禁用。0b1=启用。/ Enable NCO modulus.
W	0x112	1		从调制结果中选择边带。0b0=上边带。0b1=下边带（频谱翻转）。/ Select the sideband. 0b0 = upper; 0b1 = lower (spectral inversion).
W	0x112	0		将该位设置为 0。整数 NCO 模式计算：DDSM_FTW = (fCARRIER/fDAC) × 2^{48}。/ Set this bit to 0. Integer NCO mode calculation: DDSM_FTW = (fCARRIER/fDAC) × 2^{48}.
W	0x114	[7:0]		写入 DDSM_FTW[7:0]。/ Write DDSM_FTW[7:0].
W	0x115	[7:0]		写入 DDSM_FTW[15:8]。/ Write DDSM_FTW[15:8].
W	0x116	[7:0]		写入 DDSM_FTW[23:16]。/ Write DDSM_FTW[23:16].
W	0x117	[7:0]		写入 DDSM_FTW[31:24]。/ Write DDSM_FTW[31:24].
W	0x118	[7:0]		写入 DDSM_FTW[39:32]。/ Write DDSM_FTW[39:32].
W	0x119	[7:0]		写入 DDSM_FTW[47:40]。/ Write DDSM_FTW[47:40].
W	0x11C	[7:0]		写入 DDSM_NCO_PHASE_OFFSET[7:0]。计算：DDSM_NCO_PHASE_OFFSET = (degrees offset/180) ×2^{15}。/ Write DDSM_NCO_PHASE_OFFSET[7:0]. Calculation: (degrees offset/180) × 2^{15}.
W	0x11D	[7:0]		写入 DDSM_NCO_PHASE_OFFSET[15:8]。如果使用 NCO modulus 模式，还需对 modulus 参数进行编程。否则，跳过本节。对于 modulus NCO 模式：(fCARRIER/fNCO)=(X+(A/B))/2^{48}，其中，DDSC_FTW=X，DDSC_ACC_DELTA=A，DDSC_ACC_MODULUS=B。/ Write DDSM_NCO_PHASE_OFFSET[15:8]. If modulus mode is used, program the modulus parameters as well (formula as in source; see flag).
W	0x124	[7:0]		写入 DDSM_ACC_MODULUS[7:0]。/ Write DDSM_ACC_MODULUS[7:0].
W	0x125	[7:0]		写入 DDSM_ACC_MODULUS[15:8]。/ Write DDSM_ACC_MODULUS[15:8].
W	0x126	[7:0]		写入 DDSM_ACC_MODULUS[23:16]。/ Write DDSM_ACC_MODULUS[23:16].
W	0x127	[7:0]		写入 DDSM_ACC_MODULUS[31:24]。/ Write DDSM_ACC_MODULUS[31:24].

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x128	[7:0]		写入 DDSM_ACC_MODULUS[39:32]。/ Write DDSM_ACC_MODULUS[39:32].
W	0x129	[7:0]		写入 DDSM_ACC_MODULUS[47:40]。/ Write DDSM_ACC_MODULUS[47:40].
W	0x12A	[7:0]		写入 DDSM_ACC_DELTA[7:0]。/ Write DDSM_ACC_DELTA[7:0].
W	0x12B	[7:0]		写入 DDSM_ACC_DELTA[15:8]。/ Write DDSM_ACC_DELTA[15:8].
W	0x12C	[7:0]		写入 DDSM_ACC_DELTA[23:16]。/ Write DDSM_ACC_DELTA[23:16].
W	0x12D	[7:0]		写入 DDSM_ACC_DELTA[31:24]。/ Write DDSM_ACC_DELTA[31:24].
W	0x12E	[7:0]		写入 DDSM_ACC_DELTA[39:32]。/ Write DDSM_ACC_DELTA[39:32].
W	0x12F	[7:0]		写入 DDSM_ACC_DELTA[47:40]。/ Write DDSM_ACC_DELTA[47:40].
W	0x113	0	0b1	更新所有 NCO 相位和 FTW 字样。/ Update all NCO phase and FTW words.

表 46 JESD204B SERDES 所需接口设置 / Table 46. JESD204B SERDES Required Interface Settings

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x240	[7:0]	0xAA 或 0xFF / 0xAA or 0xFF	EQ 设置由插入损耗的大小决定，如表 10 所示。插入损耗≤11dB 时，设置为 0xAA；否则，设置为 0xFF。/ The EQ setting is determined by the magnitude of the insertion loss, as shown in Table 10. For insertion loss ≤11 dB, set 0xAA; otherwise set 0xFF.
W	0x241	[7:0]	0xAA 或 0xFF	EQ 设置由插入损耗的大小决定，如表 10 所示。插入损耗≤11dB 时，设置为 0xAA；否则，设置为 0xFF。/ Same as above.
W	0x242	[7:0]	0x55 或 0xFF / 0x55 or 0xFF	EQ 设置由插入损耗的大小决定，如表 10 所示。插入损耗≤11dB 时，设置为 0x55；否则，设置为 0xFF。/ EQ setting per insertion loss, per Table 10: ≤11 dB → 0x55; otherwise 0xFF.
W	0x243	[7:0]	0x55 或 0xFF	EQ 设置由插入损耗的大小决定，如表 10 所示。插入损耗≤11dB 时，设置为 0x55；否则，设置为 0xFF。/ Same as above.
W	0x244	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x245	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x246	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x247	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x248	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x249	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x24A	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x24B	[7:0]	0x1F	EQ 设置。/ EQ setting.
W	0x201	[7:0]		对未使用的 PHY 断电。位 x 对应 SERDINx±引脚断电。/ Power down the unused PHYs. Bit x corresponds to powering down the SERDINx± pins.
W	0x203	1	0b0	如果处于单链路模式，则设置为 0x01。如果在双链路模式下，并同时使用 SYNCOUTx̄± 信号，则设置为 0x00。通过将该位设置为 0 来为 SYNCOUTx̄± 驱动器上电。 / If in single-link mode, set to 0x01 [see flag]. If in dual-link mode and using the SYNCOUTx̄± signal simultaneously, set to 0x00. Power up the SYNCOUTx̄± driver by setting this bit to 0.
W	0x203	0		

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
				如果使用双链路和两个 SYNCOUTx± 信号，则将该位设置为 0，以为 SYNCOUTx± 驱动器上电。 / If dual-link and two SYNCOUTx± signals are used, set this bit to 0 to power up the SYNCOUTx± driver.
W	0x253	[7:0]	0x01	将 SYNCOUT0± 设置为 LVDS 输出。对于 SYNCOUT0± 的 CMOS 输出，将第 0 位设置为 0。 / Set SYNCOUT0± to LVDS output. For CMOS output of SYNCOUT0±, set Bit 0 to 0.
W	0x254	[7:0]	0x01	将 SYNCOUT1± 设置为 LVDS 输出。对于 SYNCOUT1± 的 CMOS 输出，将位 0 设置为 0。 / Set SYNCOUT1± to LVDS output. For CMOS output, set Bit 0 to 0.
W	0x210	[7:0]	0x16	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x216	[7:0]	0x05	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x212	[7:0]	0xFF	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x212	[7:0]	0x00	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x210	[7:0]	0x87	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x216	[7:0]	0x11	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x01	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x00	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x200	[7:0]	0x00	启动 SERDES 电路模块。/ Start the SERDES circuit block.
暂停 / Pause				等待 100 毫秒。/ Wait 100 ms.
W	0x210	[7:0]	0x86	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x216	[7:0]	0x40	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x01	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x00	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x210	[7:0]	0x86	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x216	[7:0]	0x00	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x01	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x00	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x210	[7:0]	0x87	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x216	[7:0]	0x01	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x01	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x213	[7:0]	0x00	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x280	[7:0]	0x05	SERDES 要求写入寄存器。/ Required SERDES register write.
W	0x280	[7:0]	0x01	启动 SERDES PLL 电路模块，并启动 SERDES PLL 校准。/ Start the SERDES PLL circuit block and start the SERDES PLL calibration.
R	0x281	0	0b1	确保寄存器位 0 读回 1，表示 SERDSES PLL 锁定。/ Ensure Bit 0 of the register reads back 1, indicating the SERDES PLL is locked.

English: Crossbar mapping: the SERDINx input pins that serve as the source of each given logical lane are written into these registers. The x value corresponds to the logical lane that maps data from the SERDINx± pins to the control bit field. The values in Table 47 vary with different PCB layout routing.

中文： Crossbar 映射将作为每个给定逻辑通道的源的 SERDINx 输入引脚写入这些寄存器。x 值对应于将数据从 SERDINx±引脚映射到控制位字段的逻辑通道。表 47 中的值随不同的 PCB 布局布线而变化。

表 47 传输层设置、同步和启用链路 / Table 47. Transport Layer Settings, Synchronization and Link Enable

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x308	[7:0]		Crossbar 设置。编程物理通道值，从而为每个逻辑通道提供数据（the source）。[5:3]=逻辑通道 1 source，[2:0]=逻辑通道 0 source。/ Crossbar setting. Program the physical lane values to provide data (the source) for each logical lane.
W	0x309	[7:0]		[5:3]=逻辑通道 3 source，[2:0]=逻辑通道 2 source。/ [5:3] = logical Lane 3 source, [2:0] = logical Lane 2 source.
W	0x30A	[7:0]		[5:3]=逻辑通道 5 source，[2:0]=逻辑通道 4 source。/ [5:3] = logical Lane 5 source, [2:0] = logical Lane 4 source.
W	0x30B	[7:0]		[5:3]=逻辑通道 7 source，[2:0]=逻辑通道 6 source。/ [5:3] = logical Lane 7 source, [2:0] = logical Lane 6 source.
W	0x306	[7:0]	0x0C	如果在 Subclass0 中运行，则不需要写入该寄存器。/ If operating in Subclass 0, this register does not need to be written.
W	0x307	[7:0]	0x0C	如果在 Subclass0 中运行，则不需要写入该寄存器。/ Same as above.
W	0x304	[7:0]		如果在 Subclass0 中运行，则无需写入该寄存器。对于 Subclass1，这些值必须按照链路延迟部分中提到的一种确定性延迟方法（有或没有已知延迟）来确定。/ If operating in Subclass 0, this register does not need to be written. For Subclass 1, these values must be determined per one of the deterministic latency methods (with or without known latency) mentioned in the link latency section.
W	0x305	[7:0]		如果在 Subclass0 中运行，则无需写入该寄存器。对于 Subclass1，这些值必须按照链路延迟部分中提到的一种确定性延迟方法（有或没有已知延迟）来确定。/ Same as above.
W	0x03B	[7:0]	0xF1	启用同步逻辑，并设置翻转模式，以便在同步复位触发时复位同步逻辑。/ Enable the synchronization logic and set the rotation mode so that the synchronization logic is reset when a synchronization reset is triggered.
W	0x03A	[7:0]	0x02	设置为单次同步模式。/ Set to one-shot synchronization mode.
	SYSREF±			如果在 Subclass1 中运行，则向设备发送 SYSREF±脉冲边沿以进行同步对齐。/ If operating in Subclass 1, send SYSREF± pulse edges to the device for synchronization alignment.
W	0x300	3	LINK_MODE	与寄存器 0x110 中的模式选择相对应。0b0=单链路模式。0b1=双链路模式。/ Corresponds to the mode selection in Register 0x110.
W	0x300	2	0b0	选择链路 0 进行设置。该位选择正在被分页的链路 QBD。0b0=链接 0(QBD0)。0b1=链路 1(QBD1)。/ Select Link 0 for setup. This bit selects the link QBD being paged.
W	0x300	[1:0]	LINK_EN	启用链路。0b01=单链路模式。0b11=双链路模式。/ Enable the link. 0b01 = single-link; 0b11 = dual-link.

表 48 清理寄存器 / Table 48. Cleanup Registers

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
W	0x085	[7:0]	0x13	设置寄存器默认值。/ Set the register default values.
W	0x1DE	[7:0]	0x00	

R/W	寄存器 / Register	位 / Bits	值 / Value	说明 / Description
				禁用模拟 SPI。要调试和继续回读功能，请写入 0x03。/ Disable the analog SPI. To debug and continue the readback function, write 0x03.
W	0x008	[7:0]	0xC0	翻页所有主 DAC，进行 TXEN 控制更新。/ Page all main DACs to perform the TXEN control update.
W	0x596	[7:0]	0x0C	SPI 打开 TXENx 功能。/ SPI enables the TXENx function.

寄存器 / Registers

表 49 寄存器总结 / Table 49. Register Summary

English: In Table 49, a multi-bit field is shown in a single bit column (the column in which its name is centered in the source); the exact bit range of every field is given in Table 50. In Table 50, the formula fragment "/248" in the source denotes /2^48 (the exponent is superscripted in print). Where the source text layer drops the IRQ pin glyphs in a description, the pin names in the English translation are restored as IRQ0/IRQ1 per the context of Section 4.

中文： 表 49 中，多位字段在其名称于原件中居中的单个位列内显示；每个字段的确切位范围见表 50。表 50 中，原件公式片段"/248"表示 /2^48（指数在印刷版中为上标）。原件文本层在个别说明中丢失 IRQ 引脚字形处，英文译文按第 4 章上下文补为 IRQ0/IRQ1.

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x000	SPI_INTFCONFA	SOFTRESET_M	LSBFIRST_M	ADDRINC_M	SDOACTIVE_M	SDOACTIVE	ADDRINC	LSBFIRST	SOFTRESET	0x00	R/W
0x001	SPI_INTFCONFB	SINGLEINS	CSSTALL			RESERVED				0x00	R/W
0x003	SPI_CHIPTYPE				CHIP_TYPE					0x04	R
0x004	SPI_PRODIDL				PROD_ID[7:0]					0x72	R
0x005	SPI_PRODIDH				PROD_ID[15:8]					0x91	R
0x006	SPI_CHIPGRADE			PROD_GRADE			DEV_REVISION			0x04	R
0x008	SPI_PAGEINDX		MAINDAC_PAGE			CHANNEL_PAGE				0xFF	R/W
0x00A	SPI_SCRATCHPAD				SCRATCHPAD					0x00	R/W
0x010	CHIP_ID_L				CHIP_ID[7:0]					0x00	R
0x011	CHIP_ID_M1				CHIP_ID[15:8]					0x00	R
0x012	CHIP_ID_M2				CHIP_ID[23:16]					0x00	R
0x013	CHIP_ID_H				CHIP_ID[31:24]					0x00	R
0x020	IRQ_ENABLE		RESERVED		EN_SYSREF_JITTER	EN_DATA_READY	EN_LANE_FIFO	EN_PRBSQ	EN_PRBSI	0x00	R/W
0x021	IRQ_ENABLE0			RESERVED		EN_DAC0_CAL_DONE		RESERVED	EN_PAERR0	0x00	R/W

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x022	IRQ_ENABLE1			RESERVED		EN_DAC1_CAL_DONE		RESERVED	EN_PAERR1	0x00	R/W
0x023	IRQ_ENABLE2		RESERVED	EN_DLL_LOST	EN_DLL_LOCK	RESERVED		EN_PLL_LOST	EN_PLL_LOCK	0x00	R/W
0x024	IRQ_STATUS		RESERVED		IRQ_SYSREF_JITTER	IRQ_DATA_READY	IRQ_LANE_FIFO	IRQ_PRBSQ	IRQ_PRBSI	0x00	R/W
0x025	IRQ_STATUS0			RESERVED		IRQ_DAC0_CAL_DONE		RESERVED	IRQ_PAERR0	0x00	R/W
0x026	IRQ_STATUS1			RESERVED		IRQ_DAC1_CAL_DONE		RESERVED	IRQ_PAERR1	0x00	R/W
0x027	IRQ_STATUS2		RESERVED	IRQ_DLL_LOST	IRQ_DLL_LOCK	RESERVED		IRQ_PLL_LOST	IRQ_PLL_LOCK	0x00	R/W
0x028	IRQ_OUTPUT_MUX		RESERVED		MUX_SYSREF_JITTER	MUX_DATA_READY	MUX_LANE_FIFO	MUX_PRBSQ	MUX_PRBSI	0x00	R/W
0x029	IRQ_OUTPUT_MUX0			RESERVED		MUX_DAC0_CAL_DONE		RESERVED	MUX_PAERR0	0x00	R/W
0x02A	IRQ_OUTPUT_MUX1			RESERVED		MUX_DAC1_CAL_DONE		RESERVED	MUX_PAERR1	0x00	R/W
0x02B	IRQ_OUTPUT_MUX2		RESERVED	MUX_DLL_LOST	MUX_DLL_LOCK	RESERVED		MUX_PLL_LOST	MUX_PLL_LOCK	0x00	R/W
0x02C	IRQ_STATUS_ALL				RESERVED				IRQ_STATUS_ALL	0x00	R/W
0x036	SYSREF_COUNT				SYSREF_COUNT					0x00	R/W
0x039	SYSREF_ERR_WINDOW	RESERVED				SYSREF_ERR_WINDOW				0x00	R/W
0x03A	SYSREF_MODE		RESERVED		SYNC_ROTATION_DONE	RESERVED		SYSREF_MOOD_ONESHOT	RESERVED	0x10	R/W
0x03B	ROTATION_MODE	SYNCLOGIC_EN	RESERVED	PERIODIC_RST_EN	NCORST_AFTER_ROT_EN	RESERVED		ROTATION_MODE		0xB0	R/W
0x03F	TX_ENABLE		RESERVED	TXEN_DATAPATH_DAC1	TXEN_DATAPATH_DAC0		RESERVED			0x00	R/W
0x050	CAL_CLK_DIV			RESERVED			CAL_CLK_DIV			0x28	R/W
0x051	CAL_CTRL	CAL_CTRL0		RESERVED				CAL_CTRL1	CAL_START	0x82	R/W
0x052	CAL_STAT			RESERVED			CAL_ACTIVE	CAL_FAIL_SEARCH	CAL_FINISH	0x00	R/W
0x05A	FSC1				FSC_CTRL[7:0]					0x28	R/W
0x061	CAL_DEBUG0	RESERVED	CAL_CTRL2	CAL_CTRL3	RESERVED	CAL_CTRL4		RESERVED		0x60	R/W
0x081	CLK_CTRL			RESERVED				CAL_CLK_PD1	CAL_CLK_PD0	0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x083	NVM_CTRL0	NVM_CTRL0A			RESERVED				NVM_CTRL0B	0x02	R/W
0x084	SYSREF_CTRL名称	RESERVED	SYSREF_INPUT_MODE	位5	位4	RESERVED	位2	位1	SYSREF_PD	0x00	R/W
0x085	NVM_CTRL1	RESERVED		NVM_CTRL1A		RESERVED		NVM_CTRL1B	NVM_CTRL1C	0x13	R/W
0x08D	ADC_CLK_CTRL0		RESERVED				CLKOUT_SWING			0x00	R/W
0x08F	ADC_CLK_CTRL2				RESERVED				PD_CLKOUT_DRIVER	0x00	R/W
0x090	DAC_POWERDOWN			RESERVED				DAC_PD1	DAC_PD0	0x03	R/W
0x091	ACLK_CTRL				RESERVED				ACLK_POWER_DOWN	0x01	R/W
0x094	PLL_CLK_DIV			RESERVED				PLL_VCO_DIV3_EN	PLL_VCO_DIV2_EN	0x00	R/W
0x095	PLL_BYPASS				RESERVED				PLL_BYPASS	0x00	R/W
0x09A	NVM_CTRL	PD_BGR				RESERVED				0x00	R/W
0x0C0	DELAY_LINE_PD		RESERVED	DLL_CTRL0B	DLL_CTRL0A		RESERVED		DLL_PD	0x31	R/W
0x0C1	DLL_CTRL0	DLL_CTRL1C		DLL_CTRL1B	DLL_CTRL1A		RESERVED		DLL_ENABLE	0x70	R/W
0x0C3	DLL_STATUS				RESERVED				DLL_LOCK	0x00	R/W
0x0C7	DLL_READ				RESERVED				DLL_READ_EN	0x00	R/W
0x0CC	DLL_FINE_DELAY0		RESERVED			DLL_FINE_DELAY0				0x00	R/W
0x0CD	DLL_FINE_DELAY1		RESERVED			DLL_FINE_DELAY1				0x00	R/W
0x0DB	DLL_UPDATE				RESERVED				DLL_DELAY_UPDATE	0x00	R/W
0x0FF	MOD_SWITCH_DEBUG			RESERVED				CMPLX_MOD_DIV2_DISABLE	RESERVED	0x00	R/W
0x100	DIG_RESET				RESERVED				DIG_DATAPATH_PD	0x01	R/W
0x110	JESD_MODE	MODE_NOT_IN_TABLE	COM_SYNC			JESD_MODE				0x20	R/W
0x111	INTRP_MODE			DP_INTERP_MODE			CH_INTERP_MODE			0x84	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x112	DDSM_DATAPATH_CFG	RESERVED	EN_CMPLX_MOD	DDSM_MODE		DDSM_NCO_EN	DDSM_MODULUS_EN	DDSM_SEL_SIDEBAND	EN_SYNC_ALL_CHNL_NCO_RESETS	0x01	R/W
0x113	DDSM_FTW_UPDATE	RESERVED	DDSM_FTW_REQ_MODE			RESERVED	DDSM_FTW_LOAD_SYSREF	DDSM_FTW_LOAD_ACK	DDSM_FTW_LOAD_REQ	0x00	R/W
0x114	DDSM_FTW0				DDSM_FTW[7:0]					0x00	R/W
0x115	DDSM_FTW1				DDSM_FTW[15:8]					0x00	R/W
0x116	DDSM_FTW2				DDSM_FTW[23:16]					0x00	R/W
0x117	DDSM_FTW3				DDSM_FTW[31:24]					0x00	R/W
0x118	DDSM_FTW4				DDSM_FTW[39:32]					0x00	R/W
0x119	DDSM_FTW5				DDSM_FTW[47:40]					0x00	R/W
0x11C	DDSM_PHASE_OFFSET0				DDSM_NCO_PHASE_OFFSET[7:0]					0x00	R/W
0x11D	DDSM_PHASE_OFFSET1				DDSM_NCO_PHASE_OFFSET[15:8]					0x00	R/W
0x124	DDSM_ACC_MODULUS0				DDSM_ACC_MODULUS[7:0]					0x00	R/W
0x125	DDSM_ACC_MODULUS1				DDSM_ACC_MODULUS[15:8]					0x00	R/W
0x126	DDSM_ACC_MODULUS2				DDSM_ACC_MODULUS[23:16]					0x00	R/W
0x127	DDSM_ACC_MODULUS3				DDSM_ACC_MODULUS[31:24]					0x00	R/W
0x128	DDSM_ACC_MODULUS4				DDSM_ACC_MODULUS[39:32]					0x00	R/W
0x129	DDSM_ACC_MODULUS5				DDSM_ACC_MODULUS[47:40]					0x00	R/W
0x12A	DDSM_ACC_DELTA0名称	位7	位6	位5	DDSM_ACC_DELTA[7:0]	位3	位2	位1	位0	0x00	R/W
0x12B	DDSM_ACC_DELTA1				DDSM_ACC_DELTA[15:8]					0x00	R/W
0x12C	DDSM_ACC_DELTA2				DDSM_ACC_DELTA[23:16]					0x00	R/W
0x12D	DDSM_ACC_DELTA3				DDSM_ACC_DELTA[31:24]					0x00	R/W
0x12E	DDSM_ACC_DELTA4				DDSM_ACC_DELTA[39:32]					0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x12F	DDSM_ACC_DELTA5				DDSM_ACC_DELTA[47:40]					0x00	R/W
0x130	DDSC_DATAPATH_CFG	RESERVED	DDSC_NCO_EN		RESERVED		DDSC_MODULUS_EN	DDSC_SEL_SIDEBAND	DDSC_EN_DC_INPUT	0x00	R/W
0x131	DDSC_FTW_UPDATE			RESERVED			DDSC_FTW_LOAD_SYSREF	DDSC_FTW_LOAD_ACK	DDSC_FTW_LOAD_REQ	0x00	R/W
0x132	DDSC_FTW0				DDSC_FTW[7:0]					0x00	R/W
0x133	DDSC_FTW1				DDSC_FTW[15:8]					0x00	R/W
0x134	DDSC_FTW2				DDSC_FTW[23:16]					0x00	R/W
0x135	DDSC_FTW3				DDSC_FTW[31:24]					0x00	R/W
0x136	DDSC_FTW4				DDSC_FTW[39:32]					0x00	R/W
0x137	DDSC_FTW5				DDSC_FTW[47:40]					0x00	R/W
0x138	DDSC_PHASE_OFFSET0				DDSC_NCOO	PHASE_OFFSET[7:0]				0x00	R/W
0x139	DDSC_PHASE_OFFSET1				DDSC_NCO_PHASE_OFFSET[15:8]					0x00	R/W
0x13A	DDSC_ACC_MODULUS0				DDSC_ACC_MODULUS[7:0]					0x00	R/W
0x13B	DDSC_ACC_MODULUS1				DDSC_ACC_MODULUS[15:8]					0x00	R/W
0x13C	DDSC_ACC_MODULUS2				DDSC_ACC_MODULUS[23:16]					0x00	R/W
0x13D	DDSC_ACC_MODULUS3				DDSC_ACC_MODULUS[31:24]					0x00	R/W
0x13E	DDSC_ACC_MODULUS4				DDSC_ACC_MODULUS[39:32]					0x00	R/W
0x13F	DDSC_ACC_MODULUS5				DDSC_ACC_MODULUS[47:40]					0x00	R/W
0x140	DDSC_ACC_DELTA0				DDSC_ACC_DELTA[7:0]					0x00	R/W
0x141	DDSC_ACC_DELTA1				DDSC_ACC_DELTA[15:8]					0x00	R/W
0x142	DDSC_ACC_DELTA2				DDSC_ACC_DELTA[23:16]					0x00	R/W
0x143	DDSC_ACC_DELTA3				DDSC_ACC_DELTA[31:24]					0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x144	DDSC_ACC_DELTA4				DDSC_ACC_DELTA[39:32]					0x00	R/W
0x145	DDSC_ACC_DELTA5				DDSC_ACC_DELTA[47:40]					0x00	R/W
0x146	CHNL_GAIN0				CHNL_GAIN[7:0]					0x00	R/W
0x147	CHNL_GAIN1			RESERVED			CHNL_GAGEN[11:8]			0x08	R/W
0x148	DC_CAL_TONE0				DC_TEST_INPUT_AMPLITUDE[7:0]					0x00	R/W
0x149	DC_CAL_TONE1				DC_TEST_INPUT_AMPLITUDE[15:8]					0x00	R/W
0x14B	PRBS	PRBS_GOOD_Q	PRBS_GOOD_I	RESERVED	PRBS_INV_Q	PRBS_INV_I	PRBS_MODE	PRBS_RESET	PRBS_EN	0x10	R/W
0x14C	PRBS_ERROR_I				PRBS_COUNT_I					0x00	R
0x14D	PRBS_ERROR_Q				PRBS_COUNT_Q					0x00	R
0x14E	PRBS_CHANSEL			RESERVED			PRBS_CHANSEL			0x07	R/W
0x151	DECODE_MODE		RESERVED		MSB_SHUFFLE_EN		RESERVED			0x00	R/W
0x1DE	SPI_ENABLE			RESERVED				SPI_EN1	SPI_EN0	0x03	R/W
0x1E2	DDSM_CAL_FTW0				DDSM_CAL_FTW[7:0]					0x00	R/W
0x1E3	DDSM_CAL_FTW1				DSM_CAL_FTW[15:8]					0x00	R/W
0x1E4	DDSM_CAL_FTW2名称	位7	位6	位5	DSM_CAL_FTW[23:16]	位3位2		位1	位0	0x00	R/W
0x1E5	DDSM_CAL_FTW3				DSM_CAL_FTW[31:24]。					0x00	R/W
0x1E6	DDSM_CAL_MODE_DEF			RESERVED		C	DDSM_EN_CAL_AC	DDSM_EN_CAL_DC_INPUT	DDSM_EN_CAL_FREQ_TUNE	0x00	R/W
0x1E7	DATAPATH_NCO_SYNC_CFG			RESERVED				ALL_NCO_SYNC_ACK	START_NCO_SYNC	0x00	R/W
0x200	MASTER_PD				RESERVED				SERDES_	0x01	R/W
0x201	PHY_PD				PHY_PD					0xEE	R/W
0x203	GENERIC_PD			RESERVED				PD_SYNCOUT0	PD_SYNCOUT1	0x01	R/W
0x206	CDR_RESET				RESERVED				CDR_PHY_RESET	0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x210	CBUS_ADDR				SERDES_CBUS_ADDR					0x00	R/W
0x212	CBUS_WRSTROBE_PHY				SERDES_CBUS_WR0					0x00	R/W
0x213	CBUS_WRSTROBE_OTHER				RESERVED				SERDES_CBUS_WR1	0x00	R/W
0x216	CBUS_WDATA				SERDES_CBUS_DATA					0x00	R/W
0x234	CDR_BITINVERSE				SEL_IF_PARDATAINV_DES_RC_CH					0x66	R/W
0x240	EQ_BOOST_PHY_3_0	EQ_BOOST_PHY3		EQ_BOOST_PHY2		EQ_BOOST_PHY1		EQ_BOOST_PHY0		0xFF	R/W
0x241	EQ_BOOST_PHY_7_4	EQ_BOOST_PHY7		EQ_BOOST_PHY6		EQ_BOOST_PHY5		EQ_BOOST_PHY4		0xFF	R/W
0x242	EQ_GAIN_PHY_3_0	EQ_GAIN_PHY3		EQ_GAIN_PHY2		EQ_GAIN_PHY1		EQ_GAIN_PHY0		0xFF	R/W
0x243	EQ_GAIN_PHY_7_4	EQ_GAIN_PHY7		EQ_GAIN_PHY6		EQ_GAIN_PHY5		EQ_GAIN_PHY4		0xFF	R/W
0x244	EQ_FB_PHY_0		RESERVED				EQ_PHY_0			0x19	R/W
0x245	EQ_FB_PHY_1		RESERVED				EQ_PHY 1			0x19	R/W
0x246	EQ_FB_PHY_2		RESERVED				EQ_PHY 2			0x19	R/W
0x247	EQ_FB_PHY_3		RESERVED				EQ_PHY 3			0x19	R/W
0x248	EQ_FB_PHY_4		RESERVED				EQ_PHY 4			0x19	R/W
0x249	EQ_FB_PHY_5		RESERVED				EQ_PHY 5			0x19	R/W
0x24A	EQ_FB_PHY_6		RESERVED				EQ_PHY 6			0x19	R/W
0x24B	EQ_FB_PHY_7		RESERVED				EQ_PHY 7			0x19	R/W
0x250	LBT_REG_CNTRL_0				EN_LBT_DES_RC_CH					0x00	R/W
0x251	LBT_REG_CNTRL_1			RESERVED				EN_LBT_HALDRATE_DES_RC	INIT_LBT_SYNC_DES_RC	0x02	R/W
0x253	_CTRL				RESERVED				SEL__MODE	0x00	R/W
0x254	_CTRL				RESERVED				SEL__MODE	0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x280	PLL_ENABLE_CTRL			RESERVED			LOLSTICKY_CLEAR_LCPLL_RC	LDSYNTH_LCPLL_RC	SERDES_PLL_STARTUP	0x01	R/W
0x281	PLL_STATUS				RESERVED				SERDES_PLL_LOCK	0x00	R
0x300	GENERAL_JRX_CTRL_0			RESERVED		LINK_MODE	LINK_PAGE		LINK_EN	0x00	R/W
0x302	DYN_LINK_LATENCY_0		RESERVED			DYN_LINK_LATENCY_0				0x00	R
0x303	DYN_LINK_LATENCY_1		RESERVED			DYN_LINK_LATENCY_1				0x00	R
0x304	LMFC_DELAY_0		RESERVED			LMFC_DELAY_0				0x00	R/W
0x305	LMFC_DELAY_1		RESERVED			LMFC_DELAY_1				0x00	R/W
0x306	LMFC_VAR_0		RESERVED			LMFC_VAR_0				0x3F	R/W
0x307	LMFC_VAR_1		RESERVED			LMFC_VAR_1				0x3F	R/W
0x308	XBAR_LN_0_1		RESERVED	LOGICAL_LANE1_SRC			LOGICAL_LANE0_SRC			0x08	R/W
0x309	XBAR_LN_2_3		RESERVED	LOGICAL_LANE3_SRC			LOGICAL_LANE2_SRC			0x1A	R/W
0x30A	XBAR_LN_4_5名称	位7	RESERVED	LOGICAL_LANE5_SRC	位4位	3位	LOGICAL_LANE4_SRC	位1	位0	0x2C	R/W
0x30B	XBAR_LN_6_7		RESERVED	LOGICAL_LANE7_SRC			LOGICAL_LANE6_SRC			0x3E	R/W
0x30C	FIFO_STATUS_REG_0				LANE_FIFO_FULL					0x00	R
0x30D	FIFO_STATUS_REG_1				LANE_FIFO_EMPTY					0x00	R
0x311	SYNCOUT_GEN_0			RESERVED		EOMF_MASK_1	EOMF_MASK_0	EOF_MASK_1	EOF_MASK_0	0x00	R/W
0x312	SYNCOUT_GEN_1			SYNC_ERR_DUR			RESERVED			0x00	R/W
0x315	PHY_PRBS_TEST_EN				PHY_TEST_EN					0x00	R/W
0x316	PHY_PRBS_TEST_CTRL	RESERVED	PHY_SRC_ERR_CNT			PHY_PRBS_PAT_SEL		PHY_TEST_START	PHY_TEST_RESET	0x00	R/W
0x317	PHY_PRBS_TEST_THRESHOLD_LOBITS				PHY_PRBS_THRESHOLD_LOBITS					0x00	R/W
0x318	PHY_PRBS_TEST_THRESHOLD_MIDBITS				PHY_PRBS_THRESHOLD_MIDBITS					0x00	R/W
0x319	PHY_PRBS_TEST_THRESHOLD_HIBITS				PHY_PRBS_THRESHOLD_HIBITS					0x00	R/W
0x31A	PHY_PRBS_TEST_ERRCNT_LOBITS				PHY_PRBS_ERR_CNT_LOBITS					0x00	R

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x31B	PHY_PRBS_TEST_ERRCNT_MIDBITS				PHY_PRBS_ERR_CNT_MIDBITS					0x00	R
0x31C	PHY_PRBS_TEST_ERRCNT_HIBITS				PHY_PRBS_ERR_CNT_HIBITS					0x00	R
0x31D	PHY_PRBS_TEST_STATUS				PHY_PRBS_PASS					0xFF	R
0x31E	PHY_DATA_SNAPSHOT_CTRL			RESERVED				PHY_GRAB_MODE	PHY_GRAB_DATA	0x00	R/W
0x31F	PHY_SNAPSHOT_DATA_BYTE0				PHY_SNAPSHOT_DATA_BYTE0					0x00	R
0x320	PHY_SNAPSHOT_DATA_BYTE1				PHY_SNAPSHOT_DATA_BYTE1					0x00	R
0x321	PHY_SNAPSHOT_DATA_BYTE2				PHY_SNAPSHOT_DATA_BYTE2					0x00	R
0x322	PHY_SNAPSHOT_DATA_BYTE3				PHY_SNAPSHOT_DATA_BYTE3					0x00	R
0x323	PHY_SNAPSHOT_DATA_BYTE4				PHY_SNAPSHOT_DATA_BYTE4					0x00	R
0x32C	SHORT_TPL_TEST_0			SHORT_TPL_SP_SEL		SHORT_TPL_CHAN_SEL		SHORT_TPL_TEST_RESET	SHORT_TPL_TEST_EN	0x00	R/W
0x32D	SHORT_TPL_TEST_1				SHORT_TPL_REF_SP_LSB					0x00	R/W
0x32E	SHORT_TPL_TEST_2				SHORT_TPL_REF_SP_MSB					0x00	R/W
0x32F	SHORT_TPL_TEST_3	SHORT_TPL_LINK_SEL	SHORT_TPL_IQ_SAMPLE_SEL			RESERVED			SHORT_TPL_FAIL	0x00	R/W
0x334	JESD_BIT_INVERSE_CTRL				JESD_BIT_INVERSE					0x00	R/W
0x400	DID_REG				DID_RD					0x00	R
0x401	BID_REG				BID_RD					0x00	R
0x402	LID0_REG	RESERVED	ADJDIR_RD	PHADJ_RD			LL_LID0			0x00	R
0x403	SCR_L_REG	SCR_RD		RESERVED			L_RD_1			0x00	R
0x404	F_REG				F_RD_1					0x00	R
0x405	K_REG		RESERVED				K_RD_1			0x00	R
0x406	M_REG名称	位7	位6	位5	M_RD_1	位3	位2	位1	位0	0x00	R
0x407	CS_N_REG		CS_RD	RESERVED			N_RD_1			0x00	R
0x408	NP_REG		SUBCLASSV_RD				NP_RD_1			0x00	R
0x409	S_REG		JESDV_RD_1				S_RD_1			0x00	R
0x40A	HD_CF_REG	HD_RD		RESERVED			CF_RD			0x00	R
0x40B	RES1_REG				RES1_RD					0x00	R
0x40C	RES2_REG				RES2_RD					0x00	R
0x40D	CHECKSUM0_REG				LL_FCHK0					0x00	R
0x40E	COMPSUM0_REG				LL_FCMP0					0x00	R
0x412	LID1_REG		RESERVED				LL_LID1			0x00	R
0x415	CHECKSUM1_REG				LL_FCHK1					0x00	R
0x416	COMPSUM1_REG				LL_FCMP1					0x00	R

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x41A	LID2_REG		RESERVED				LL_LID2			0x00	R
0x41D	CHECKSUM2_REG				LL_FCHK2					0x00	R
0x41E	COMPSUM2_REG				LL_FCMP2					0x00	R
0x422	LID3_REG		RESERVED				LL_LID3			0x00	R
0x425	CHECKSUM3_REG				LL_FCHK3					0x00	R
0x426	COMPSUM3_REG				LL_FCMP3					0x00	R
0x42A	LID4_REG		RESERVED				LL_LID4			0x00	R
0x42D	CHECKSUM4_REG				LL_FCHK4					0x00	R
0x42E	COMPSUM4_REG				LL_FCMP4					0x00	R
0x432	LID5_REG		RESERVED				LL_LID5			0x00	R
0x435	CHECKSUM5_REG				LL_FCHK5					0x00	R
0x436	COMPSUM5_REG				LL_FCMP5					0x00	R
0x43A	LID6_REG		RESERVED				LL_LID6			0x00	R
0x43D	CHECKSUM6_REG				LL_FCHK6					0x00	R
0x43E	COMPSUM6_REG				LL_FCMP6					0x00	R
0x442	LID7_REG		RESERVED				LL_LID7			0x00	R
0x445	CHECKSUM7_REG				LL_FCHK7					0x00	R
0x446	COMPSUM7_REG				LL_FCMP7					0x00	R
0x450	ILS_DID				DID					0x00	R/W
0x451	ILS_BID				BID					0x00	R/W
0x452	ILS_LID0	RESERVED	ADJDIR	PHADJ			LID0			0x00	R/W
0x453	ILS_SCR_L	SCR		RESERVED			L_1			0x87	R/W
0x454	ILS_F				F_1					0x00	R/W
0x455	ILS_K		RESERVED				K_1			0x1F	R/W
0x456	ILS_M				M_1					0x01	R/W
0x457	ILS_CS_N		CS	RESERVED			N_1			0x0F	R/W
0x458	ILS_NP		SUBCLASSV				NP_1			0x0F	R/W
0x459	ILS_S		JESDV				S_1			0x01	R/W
0x45A	ILS_HD_CF	HD		RESERVED			CF			0x80	R

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x45B	ILS_RES1				RES1					0x00	R/W
0x45C	ILS_RES2				RES2					0x00	R/W
0x45D	ILS_CHECKSUM				FCHK0					0x00	R/W
0x46C	LANE_DESKEW	ILD7	ILD6	ILD5	ILD4	ILD3	ILD2	ILD1	ILD0	0x00	R
0x46D	BAD_DISPARITY	BDE7	BDE6	BDE5	BDE4	BDE3	BDE2	BDE1	BDE0	0x00	R
0x46E	NOT_IN_TABLE	NIT7	NIT6	NIT5	NIT4	NIT3	NIT2	NIT1	NIT0	0x00	R
0x46F	UNEXPECTED_KCHAR	UEK7	UEK6	UEK5	UEK4	UEK3	UEK2	UEK1	UEK0	0x00	R
0x470	CODE_GRP_SYNC	CGS7	CGS6	CGS5	CGS4	CGS3	CGS2	CGS1	CGS0	0x00	R
0x471	FRAME_SYNC名称	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0	0x00	R
0x472	GOOD_CHECKSUM	CKS7	CKS6	CKS5	CKS4CKS3	CKS2		CKS1	CKS0	0x00	R
0x473	INIT_LANE_SYNC	ILS7	ILS6	ILS5	ILS4ILS3	ILS2		ILS1	ILS0	0x00	R
0x475	CTRLREG0			RESERVED		SOFTRST	FORCE_SYNCREQ	RESERVED	REPL_FRM_ENA	0x01	R/W
0x476	CTRLREG1		RESERVED		QUAL_RDERR		RESERVED		FCHK_N	0x14	R/W
0x477	CTRLREG2	ILS_MODE	RESERVED	REPDATATEST	QUETESTERR	AR_ECNTR		RESERVED		0x00	R/W
0x478	KVAL				KSYNC					0x01	R/W
0x47C	ERRORTHRES				ETH					0xFF	R/W
0x47D	SYNC_ASSERT_MASK			RESERVED			SYNC_ASSERT_MASK			0x07	R/W
0x480	ECNT_CTRL0		RESERVED		ECNT_ENA0			ECNT_RST0		0x3F	R/W
0x481	ECNT_CTRL1		RESERVED		ECNT_ENA1			ECNT_RST1		0x3F	R/W
0x482	ECNT_CTRL2		RESERVED		ECNT_ENA2			ECNT_RST2		0x3F	R/W
0x483	ECNT_CTRL3		RESERVED		ECNT_ENA3			ECNT_RST3		0x3F	R/W
0x484	ECNT_CTRL4		RESERVED		ECNT_ENA4			ECNT_RST4		0x3F	R/W
0x485	ECNT_CTRL5		RESERVED		ECNT_ENA5			ECNT_RST5		0x3F	R/W
0x486	ECNT_CTRL6		RESERVED		ECNT_ENA6			ECNT_RST6		0x3F	R/W
0x487	ECNT_CTRL7		RESERVED		ECNT_ENA7			ECNT_RST7		0x3F	R/W

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x488	ECNT_TCH0			RESERVED				ECNT_TCH0		0x07	R/W
0x489	ECNT_TCH1			RESERVED				ECNT_TCH1		0x07	R/W
0x48A	ECNT_TCH2			RESERVED				ECNT_TCH2		0x07	R/W
0x48B	ECNT_TCH3			RESERVED				ECNT_TCH3		0x07	R/W
0x48C	ECNT_TCH4			RESERVED				ECNT_TCH4		0x07	R/W
0x48D	ECNT_TCH5			RESERVED				ECNT_TCH5		0x07	R/W
0x48E	ECNT_TCH6			RESERVED				ECNT_TCH6		0x07	R/W
0x48F	ECNT_TCH7			RESERVED				ECNT_TCH7		0x07	R/W
0x490	ECNT_STAT0			RESERVED		LANE_ENA0		ECNT_TCR0		0x00	R
0x491	ECNT_STAT1			RESERVED		LANE_ENA1		ECNT_TCR1		0x00	R
0x492	ECNT_STAT2			RESERVED		LANE_ENA2		ECNT_TCR2		0x00	R
0x493	ECNT_STAT3			RESERVED		LANE_ENA3		ECNT_TCR3		0x00	R
0x494	ECNT_STAT4			RESERVED		LANE_ENA4		ECNT_TCR4		0x00	R
0x495	ECNT_STAT5			RESERVED		LANE_ENA5		ECNT_TCR5		0x00	R
0x496	ECNT_STAT6			RESERVED		LANE_ENA6		ECNT_TCR6		0x00	R
0x497	ECNT_STAT7			RESERVED		LANE_ENA7		ECNT_TCR7		0x00	R
0x4B0	LINK_STATUS0	BDE0	NIT0	UEK0	ILD0ILS0	CKS0		FS0	CGS0	0x00	R
0x4B1	LINK_STATUS1	BDE1	NIT1	UEK1	ILD1ILS1	CKS1		FS1	CGS1	0x00	R
0x4B2	LINK_STATUS2	BDE2	NIT2	UEK2	ILD2ILS2	CKS2		FS2	CGS2	0x00	R
0x4B3	LINK_STATUS3	BDE3	NIT3	UEK3	ILD3ILS3	CKS3		FS3	CGS3	0x00	R
0x4B4	LINK_STATUS4	BDE4	NIT4	UEK4	ILD4ILS4	CKS4		FS4	CGS4	0x00	R
0x4B5	LINK_STATUS5	BDE5	NIT5	UEK5	ILD5ILS5	CKS5		FS5	CGS5	0x00	R
0x4B6	LINK_STATUS6	BDE6	NIT6	UEK6	ILD6ILS6	CKS6		FS6	CGS6	0x00	R
0x4B7	LINK_STATUS7	BDE7	NIT7	UEK7	ILD7ILS7	CKS7		FS7	CGS7	0x00	R
0x4B8	JESD_IRQ_ENABLEA	EN_BDE	EN_NIT	EN_UEK	EN_ILD	EN_ILSEN_CKS		EN_FS	EN_CGS	0x00	R/W
0x4B9	JESD_IRQ_ENABLEB				RESERVED				EN_ILAS	0x00	R/W
0x4BA	JESD_IRQ_STATUSA	IRQ_BDE	IRQ_NIT	IRQ_UEK	IRQ_ILD	IRQ_ILSIRQ_CKS		IRQ_FS	IRQ_CGS	0x00	R/W
0x4BB	JESD_IRQ_STATUSB				RESERVED				IRQ_ILAS	0x00	R/W

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x4BC	IRQ_OUTPUT_MUX_JESD				RESERVED				MUX_JESD_IRQ	0x00	R/W
0x580	BE_SOFT_OFF_GAIN_CTRL	BE_SOFY_OFF_GAIN_EN		RESERVED			BE_GAIN_RAMP_RATE			0x00	R/W
0x581	BE_SOFT_OFF_ENABLE	ENA_SHORT_PAERR_SOFTOFF	ENA_LONG_PAERR_SOFTOFF	RESERVED		ENA_JESD_ERR_SOFTOFF_EN	ROTATE_SOFT_OFF	TXEN_SOFT_OFF_EN	SPI_SOFT_OFF_EN	0xC6	R/W
0x582	BE_SOFT_ON_ENABLE	SPI_SOFT_ON_EN	LONG_LEVEL_SOFTON_EN			RESERVED				0x40	R/W
0x583	LONG_PA_THRES_LSB				LONG_PA_THRESHOLD[7:0]					0x00	R/W
0x584	LONG_PA_THRES_MSB名称	位7	RESERVED	位5	LONG_PA_THRESHOLD[12:8]	位3	位2	位1	位0	0x00	R/W
0x585	LONG_PA_CONTROL	LONG_PA_ENABLE		RESERVED		LONG_PA_AVG_TIME				0x00	R/W
0x586	LONG_PA_POWER_LSB				LONG_POWER[7:0]					0x00	R
0x587	LONG_PA_POWER_MSB		RESERVED				LONG_PA_POWER[12:8]			0x00	R
0x588	SHORT_PA_THRES_LSB				SHORT_PA_THRESHOLD	[7:0]				0x00	R/W
0x589	SHORT_PA_THRES_MSB		RESERVED		SHORT_PA_THRESHOLD[12:8]					0x00	R/W
0x58A	SHORT_PA_CONTROL	SHORT_PA_ENABLE			RESERVED			SHORT_PA_AVG_TIME		0x00	R/W
0x58B	SHORT_PA_POWER_LSB				SHORT_PA_POWER[7:0]					0x00	R
0x58C	SHORT_PA_POWER_MSB		RESERVED				SHORT_PA_POWER[12:8]			0x00	R
0x58D	TXEN_SM_0				RESERVED				ENA_TXENSM	0x50	R/W
0x596	BLANKING_CTRL			RESERVED		SPI_TXEN	ENA_SPI_TXEN	RESERVED		0x00	R/W
0x597	JESD_PA_INT0				JESD_PA_INT_CNTRL[7:0]					0x00	R/W
0x598	JESD_PA_INT1				RESERVED				JESD_PA_INT_CNTRL[8]	0x00	R/W
0x599	TXEN_FLUSH_CTRL0				RESERVED				SPI_FLUSH_EN	0x01	R/W
0x705	NVM_LOADER_EN				RESERVED				NVM_BLR_EN	0x00	R/W
0x790	DACPLL_PDCTRL0	PLL_PD5		PLL_PD4		PLL_PD3		PLL_PD2 PLL_PD1	PLL_PD0	0x02	R/W
0x791	DACPLL_PDCTRL1		RESERVED		PLL_PD10	PLL_PD9		PLL_PD8 PLL_PD7	PLL_PD6	0x00	R/W
0x792	DACPLL_CTRL0			RESERVED				D_CAL_RESET	D_RESET_VCO_DIV	0x02	R/W

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x793	DACPLL_CTRL1			RESERVED				M_DIVIDER-1		0x18	R/W
0x794	DACPLL_CTRL2		RESERVED			DACPLL_CP				0x04	R/W
0x795	DACPLL_CTRL3			RESERVED			D_CP_CALBITS			0x08	R/W
0x796	DACPLL_CTRL4			PLL_CTRL0			RESERVED			0xD2	R/W
0x797	DACPLL_CTRL5		RESERVED			PLL_CTRL1				0x20	R/W
0x798	DACPLL_CTRL6	RESERVED	PLL_CTRL3			PLL_CTRL2				0x1C	R/W
0x799	DACPLL_CTRL7	ADC_CLK_DIVIDER				N_DIVIDER				0x08	R/W
0x7A0	DACPLL_CTRL9		RESERVED	D_EN_VAR_FINE_PRE	RESERVED		D_EN_VAR_COARSE_PRE	RESERVED		0x90	R/W
0x7A2	DACPLL_CTRL10	RESERVED	D_REGULATOR_CAL_WAIT		D_VCO_CAL_WAIT		D_VCO_CAL_CYCLES		RESERVED	0x35	R/W
0x7B5	PLL_STATUS				RESERVED				PLL_LOCK	0x00	R
0x800	DDSM_HOPF_CTRL	HOPF_MODE		RESERVED			HOPF_SEL			0x00	R/W
0x806	DDSM_HOPF_FTW1_0				HOPF_FTW1[7:0]					0x00	R/W
0x807	DDSM_HOPF_FTW1_1				HOPF_FTW1[15:8]					0x00	R/W
0x808	DDSM_HOPF_FTW1_2				HOPF_FTW1[23:16]					0x00	R/W
0x809	DDSM_HOPF_FTW1_3				HOPF_FTW1[31:24]					0x00	R/W
0x80A	DDSM_HOPF_FTW2_0				HOPF_FTW2[7:0]					0x00	R/W
0x80B	DDSM_HOPF_FTW2_1				HOPF_FTW2[15:8]					0x00	R/W
0x80C	DDSM_HOPF_FTW2_2				HOPF_FTW2[23:16]					0x00	R/W
0x80D	DDSM_HOPF_FTW2_3				HOPF_FTW2[31:24]					0x00	R/W
0x80E	DDSM_HOPF_FTW3_0				HOPF_FTW3[7:0]					0x00	R/W
0x80F	DDSM_HOPF_FTW3_1名称	位7	位6	位5	HOPF_FTW3[15:8]	位3	位2	位1	位0	0x00	R/W
0x810	DDSM_HOPF_FTW3_2				HOPF_FTW3[23:16]					0x00	R/W

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
0x811	DDSM_HOPF_FTW3_3				HOPF_FTW3[31:24]					0x00	R/W
0x812	DDSM_HOPF_FTW4_0				HOPF_FTW4[7:0]					0x00	R/W
0x813	DDSM_HOPF_FTW4_1				HOPF_FTW4[15:8]					0x00	R/W
0x814	DDSM_HOPF_FTW4_2				HOPF_FTW4[23:16]					0x00	R/W
0x815	DDSM_HOPF_FTW4_3				HOPF_FTW4[31:24]					0x00	R/W
0x816	DDSM_HOPF_FTW5_0				HOPF_FTW5[7:0]					0x00	R/W
0x817	DDSM_HOPF_FTW5_1				HOPF_FTW5[15:8]					0x00	R/W
0x818	DDSM_HOPF_FTW5_2				HOPF_FTW5[23:16]					0x00	R/W
0x819	DDSM_HOPF_FTW5_3				HOPF_FTW5[31:24]					0x00	R/W
0x81A	DDSM_HOPF_FTW6_0				HOPF_FTW6[7:0]					0x00	R/W
0x81B	DDSM_HOPF_FTW6_1				HOPF_FTW6[15:8]					0x00	R/W
0x81C	DDSM_HOPF_FTW6_2				HOPF_FTW6[23:16]					0x00	R/W
0x81D	DDSM_HOPF_FTW6_3				HOPF_FTW6[31:24]					0x00	R/W
0x81E	DDSM_HOPF_FTW7_0				HOPF_FTW7[7:0]					0x00	R/W
0x81F	DDSM_HOPF_FTW7_1				HOPF_FTW7[15:8]					0x00	R/W
0x820	DDSM_HOPF_FTW7_2				HOPF_FTW7[23:16]					0x00	R/W
0x821	DDSM_HOPF_FTW7_3				HOPF_FTW7[31:24]					0x00	R/W
0x822	DDSM_HOPF_FTW8_0				HOPF_FTW8[7:0]					0x00	R/W
0x823	DDSM_HOPF_FTW8_1				HOPF_FTW8[15:8]					0x00	R/W
0x824	DDSM_HOPF_FTW8_2				HOPF_FTW8[23:16]					0x00	R/W
0x825	DDSM_HOPF_FTW8_3				HOPF_FTW8[31:24]					0x00	R/W
0x826	DDSM_HOPF_FTW9_0				HOPF_FTW9[7:0]					0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x827	DDSM_HOPF_FTW9_1				HOPF_FTW9[15:8]					0x00	R/W
0x828	DDSM_HOPF_FTW9_2				HOPF_FTW9[23:16]					0x00	R/W
0x829	DDSM_HOPF_FTW9_3				HOPF_FTW9[31:24]					0x00	R/W
0x82A	DDSM_HOPF_FTW10_0				HOPF_FTW10[7:0]					0x00	R/W
0x82B	DDSM_HOPF_FTW10_1				HOPF_FTW10[15:8]					0x00	R/W
0x82C	DDSM_HOPF_FTW10_2				HOPF_FTW10[23:16]					0x00	R/W
0x82D	DDSM_HOPF_FTW10_3				HOPF_FTW10[31:24]					0x00	R/W
0x82E	DDSM_HOPF_FTW11_0				HOPF_FTW11[7:0]					0x00	R/W
0x82F	DDSM_HOPF_FTW11_1				HOPF_FTW11[15:8]					0x00	R/W
0x830	DDSM_HOPF_FTW11_2				HOPF_FTW11[23:16]					0x00	R/W
0x831	DDSM_HOPF_FTW11_3				HOPF_FTW11[31:24]					0x00	R/W
0x832	DDSM_HOPF_FTW12_0名称	位7	位6	位5	HOPF_FTW12[7:0]	位3	位2	位1	位0	0x00	R/W
0x833	DDSM_HOPF_FTW12_1				HOPF_FTW12[15:8]					0x00	R/W
0x834	DDSM_HOPF_FTW12_2				HOPF_FTW12[23:16]					0x00	R/W
0x835	DDSM_HOPF_FTW12_3				HOPF_FTW12[31:24]					0x00	R/W
0x836	DDSM_HOPF_FTW13_0				HOPF_FTW13[7:0]					0x00	R/W
0x837	DDSM_HOPF_FTW13_1				HOPF_FTW13[15:8]					0x00	R/W
0x838	DDSM_HOPF_FTW13_2				HOPF_FTW13[23:16]					0x00	R/W
0x839	DDSM_HOPF_FTW13_3				HOPF_FTW13[31:24]					0x00	R/W
0x83A	DDSM_HOPF_FTW14_0				HOPF_FTW14[7:0]					0x00	R/W
0x83B	DDSM_HOPF_FTW14_1				HOPF_FTW14[15:8]					0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x83C	DDSM_HOPF_FTW14_2				HOPF_FTW14[23:16]					0x00	R/W
0x83D	DDSM_HOPF_FTW14_3				HOPF_FTW14[31:24]					0x00	R/W
0x83E	DDSM_HOPF_FTW15_0				HOPF_FTW15[7:0]					0x00	R/W
0x83F	DDSM_HOPF_FTW15_1				HOPF_FTW15[15:8]					0x00	R/W
0x840	DDSM_HOPF_FTW15_2				HOPF_FTW15[23:16]					0x00	R/W
0x841	DDSM_HOPF_FTW15_3				HOPF_FTW15[31:24]					0x00	R/W
0x842	DDSM_HOPF_FTW16_0				HOPF_FTW16[7:0]					0x00	R/W
0x843	DDSM_HOPF_FTW16_1				HOPF_FTW16[15:8]					0x00	R/W
0x844	DDSM_HOPF_FTW16_2				HOPF_FTW16[23:16]					0x00	R/W
0x845	DDSM_HOPF_FTW16_3				HOPF_FTW16[31:24]					0x00	R/W
0x846	DDSM_HOPF_FTW17_0				HOPF_FTW17[7:0]					0x00	R/W
0x847	DDSM_HOPF_FTW17_1				HOPF_FTW17[15:8]					0x00	R/W
0x848	DDSM_HOPF_FTW17_2				HOPF_FTW17[23:16]					0x00	R/W
0x849	DDSM_HOPF_FTW17_3				HOPF_FTW17[31:24]					0x00	R/W
0x84A	DDSM_HOPF_FTW18_0				HOPF_FTW18[7:0]					0x00	R/W
0x84B	DDSM_HOPF_FTW18_1				HOPF_FTW18[15:8]					0x00	R/W
0x84C	DDSM_HOPF_FTW18_2				HOPF_FTW18[23:16]					0x00	R/W
0x84D	DDSM_HOPF_FTW18_3				HOPF_FTW18[31:24]					0x00	R/W
0x84E	DDSM_HOPF_FTW19_0				HOPF_FTW19[7:0]					0x00	R/W
0x84F	DDSM_HOPF_FTW19_1				HOPF_FTW19[15:8]					0x00	R/W
0x850	DDSM_HOPF_FTW19_2				HOPF_FTW19[23:16]					0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x851	DDSM_HOPF_FTW19_3				HOPF_FTW19[31:24]					0x00	R/W
0x852	DDSM_HOPF_FTW20_0				HOPF_FTW20[7:0]					0x00	R/W
0x853	DDSM_HOPF_FTW20_1				HOPF_FTW20[15:8]					0x00	R/W
0x854	DDSM_HOPF_FTW20_2				HOPF_FTW20[23:16]					0x00	R/W
0x855	DDSM_HOPF_FTW20_3名称	位7	位6	位5	HOPF_FTW20[31:24]	位3	位2	位1	位0	0x00	R/W
0x856	DDSM_HOPF_FTW21_0				HOPF_FTW21[7:0]					0x00	R/W
0x857	DDSM_HOPF_FTW21_1				HOPF_FTW21[15:8]					0x00	R/W
0x858	DDSM_HOPF_FTW21_2				HOPF_FTW21[23:16]					0x00	R/W
0x859	DDSM_HOPF_FTW21_3				HOPF_FTW21[31:24]					0x00	R/W
0x85A	DDSM_HOPF_FTW22_0				HOPF_FTW22[7:0]					0x00	R/W
0x85B	DDSM_HOPF_FTW22_1				HOPF_FTW22[15:8]					0x00	R/W
0x85C	DDSM_HOPF_FTW22_2				HOPF_FTW22[23:16]					0x00	R/W
0x85D	DDSM_HOPF_FTW22_3				HOPF_FTW22[31:24]					0x00	R/W
0x85E	DDSM_HOPF_FTW23_0				HOPF_FTW23[7:0]					0x00	R/W
0x85F	DDSM_HOPF_FTW23_1				HOPF_FTW23[15:8]					0x00	R/W
0x860	DDSM_HOPF_FTW23_2				HOPF_FTW23[23:16]					0x00	R/W
0x861	DDSM_HOPF_FTW23_3				HOPF_FTW23[31:24]					0x00	R/W
0x862	DDSM_HOPF_FTW24_0				HOPF_FTW24[7:0]					0x00	R/W
0x863	DDSM_HOPF_FTW24_1				HOPF_FTW24[15:8]					0x00	R/W
0x864	DDSM_HOPF_FTW24_2				HOPF_FTW24[23:16]					0x00	R/W
0x865	DDSM_HOPF_FTW24_3				HOPF_FTW24[31:24]					0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x866	DDSM_HOPF_FTW25_0				HOPF_FTW25[7:0]					0x00	R/W
0x867	DDSM_HOPF_FTW25_1				HOPF_FTW25[15:8]					0x00	R/W
0x868	DDSM_HOPF_FTW25_2				HOPF_FTW25[23:16]					0x00	R/W
0x869	DDSM_HOPF_FTW25_3				HOPF_FTW25[31:24]					0x00	R/W
0x86A	DDSM_HOPF_FTW26_0				HOPF_FTW26[7:0]					0x00	R/W
0x86B	DDSM_HOPF_FTW26_1				HOPF_FTW26[15:8]					0x00	R/W
0x86C	DDSM_HOPF_FTW26_2				HOPF_FTW26[23:16]					0x00	R/W
0x86D	DDSM_HOPF_FTW26_3				HOPF_FTW26[31:24]					0x00	R/W
0x86E	DDSM_HOPF_FTW27_0				HOPF_FTW27[7:0]					0x00	R/W
0x86F	DDSM_HOPF_FTW27_1				HOPF_FTW27[15:8]					0x00	R/W
0x870	DDSM_HOPF_FTW27_2				HOPF_FTW27[23:16]					0x00	R/W
0x871	DDSM_HOPF_FTW27_3				HOPF_FTW27[31:24]					0x00	R/W
0x872	DDSM_HOPF_FTW28_0				HOPF_FTW28[7:0]					0x00	R/W
0x873	DDSM_HOPF_FTW28_1				HOPF_FTW28[15:8]					0x00	R/W
0x874	DDSM_HOPF_FTW28_2				HOPF_FTW28[23:16]					0x00	R/W
0x875	DDSM_HOPF_FTW28_3				HOPF_FTW28[31:24]					0x00	R/W
0x876	DDSM_HOPF_FTW29_0				HOPF_FTW29[7:0]					0x00	R/W
0x877	DDSM_HOPF_FTW29_1				HOPF_FTW29[15:8]					0x00	R/W
0x878	DDSM_HOPF_FTW29_2名称	位7	位6	位5	HOPF_FTW29[23:16]	位3	位2	位1	位0	0x00	R/W
0x879	DDSM_HOPF_FTW29_3				HOPF_FTW29[31:24]					0x00	R/W
0x87A	DDSM_HOPF_FTW30_0				HOPF_FTW30[7:0]					0x00	

地址 / Address	名称 / Name	位 7 / Bit 7	位 6 / Bit 6	位 5 / Bit 5	位 4 / Bit 4	位 3 / Bit 3	位 2 / Bit 2	位 1 / Bit 1	位 0 / Bit 0	重置 / Reset	R/W
											R/W
0x87B	DDSM_HOPF_FTW30_1				HOPF_FTW 30[15:8]					0x00	R/W
0x87C	DDSM_HOPF_FTW30_2				HOPF_FTW 30[23:16]					0x00	R/W
0x87D	DDSM_HOPF_FTW30_3				HOPF_FTW 30[31:24]					0x00	R/W
0x87E	DDSM_HOPF_FTW31_0				HOPF_FTW 31[7:0]					0x00	R/W
0x87F	DDSM_HOPF_FTW31_1				HOPF_FTW 31[15:8]					0x00	R/W
0x880	DDSM_HOPF_FTW31_2				HOPF_FTW 31[23:16]					0x00	R/W
0x881	DDSM_HOPF_FTW31_3				HOPF_FTW 31[31:24]					0x00	R/W

1、寄存器详细信息 / 1. Register Details

表 50 寄存器详细信息 / Table 50. Register Details

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x000	SPI_INTFCONFA	7	SOFTRESET_M	软复位（镜像）。将该位设置为镜像位0。 / Soft reset (mirror). Set this bit as mirror Bit 0.	0x0	R
0x000	SPI_INTFCONFA	6	LSBFIRST_M	LSB优先（镜像）。将该位设置为镜像位1。 / LSB first (mirror). Set this bit as mirror Bit 1.	0x0	R
0x000	SPI_INTFCONFA	5	ADDRINC_M	地址递增（镜像）。将该位设置为镜像位2。 / Address increment(mirror). Set this bit as mirror Bit 2.	0x0	R
0x000	SPI_INTFCONFA	4	SDOACTIVE_M	SDO激活（镜像）。将该位设置为镜像位3。SDO激活。启用4线SPI总线模式。 / SDO active (mirror). Set this bit as mirror Bit 3. SDO active.Enables the 4-wire SPI bus mode.	0x0	R
0x000	SPI_INTFCONFA	3	SDOACTIVE		0x0	R/W
0x000	SPI_INTFCONFA	2	ADDRINC	地址增量。设置时，该位导致streaming addresses递增；否则，生成descending addresses。streaming adress递增。1 streaming adress递减。0 / Address increment. When set, this bit causes the streaming addresses to increment; otherwise, descending addresses are generated.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				Streaming adress increments. 1.Streaming adress decrements. 0.		
0x000	SPI_INTFCONFA	1	LSBFIRST	LSB优先。设置该位后，SPI输入输出数据以LSB为先。如果该位清零，则数据以MSB为先。优先移位LSB。1优先移位MSB。0 / LSB first. After this bit is set, the SPI input/output data is LSB first. If this bit is cleared, the data is MSB first. Shift LSB first. 1.Shift MSB first. 0.	0x0	R/W
0x000	SPI_INTFCONFA	0	SOFTRESET	1软复位。执行复位操作后，该位自动清零。设置复位。0在软复位完成后，该位自动清除。脉冲软复位线路。重置软复位线路。 / 1. Soft reset. After the reset operation is executed, this bit is automatically cleared. Set reset. 0. After the soft reset completes, this bit is automatically cleared. Pulse the soft-reset line. Reset the soft-reset line.	0x0	R/W
0x001	SPI_INTFCONFB	7	SINGLEINS	单一指令。1执行单次转移。0执行多次转移。 / Single instruction. 1:execute a single transfer. 0: execute multiple transfers.	0x0	R/W
0x001	SPI_INTFCONFB	6	CSSTALL	0 stalling。1禁用stalling。启用stalling。 / 0: stalling. 1: disable stalling. Enable stalling.	0x0	R/W
0x001	SPI_INTFCONFB	[5:0]	RESERVED	保留 / Reserved.	0x0	R/W
0x003	SPI_CHIPTYPE	[7:0]	CHIP_TYPE	芯片类型 / Chip type.	0x4	R
0x004	SPI_PRODIDL	[7:0]	PROD_ID[7:0]	产品编号。启动程序完成后更新 / Product ID number. Updated after the boot program completes.	0x72	R
0x005	SPI_PRODIDH	[7:0]	PROD_ID[15:8]	产品编号。启动程序完成后更新 / Product ID number. Updated after the boot program completes.	0x91	R
0x006	SPI_CHIPGRADE	[7:4]	PORD_GRADE	产品等级 / Product grade.	0x0	R
0x006	SPI_CHIPGRADE	[3:0]	DEV_REVISION	Device revision / Device revision.	0x4	R
0x008	SPI_PAGEINDX	[7:6]	MAINDAC_PAGE	设置主DAC分页。该字段中的每个高位从LSB开始分页一个DAC。如果需要，可以同时对两个主DAC进行分页和编程。 / Set the main DAC paging. Each high bit in this field,starting from the LSB, pages one DAC. If required, both main DACs can be paged and programmed simultaneously.	0x3	R/W
0x008	SPI_PAGEINDX	[5:0]	CHANNEL_PAGE	设置通道分页。该字段的每个高位从LSB开始分页一个复合通道。如果需	0x3F	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				要，可以同时对多个通道进行分页和编程。 / Set the channel paging.Each high bit of this field, starting from the LSB, pages one complex channel. If required, multiple channels can be paged and programmed simultaneously.		
0x00A	SPI_SCRATCHPAD	[7:0]	SCRATCHPAD	Scratch pad读写寄存器。 / Scratch pad read/write register.	0x0	R/W
0x010	CHIP_ID_L	[7:0]	CHIP_ID[7:0]	芯片ID序列号。 / Chip ID serial number.	0x0	R
0x011	CHIP_ID_M1	[7:0]	CHIP_ID[15:8]	芯片ID序列号。 / Chip ID serial number.	0x0	R
0x012	CHIP_ID_M2	[7:0]	CHIP_ID[23:16]	芯片ID序列号。 / Chip ID serial number.	0x0	R
0x013	CHIP_ID_H	[7:0]	CHIP_ID[31:24]	芯片ID序列号。 / Chip ID serial number.	0x0	R
0x020	IRQ_ENABLE	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x020	IRQ_ENABLE	4	EN_SYSREF_JITTER	启用SYSREF±抖动中断。 / Enable the SYSREF+/- jitter interrupt.	0x0	R/W
0x020	IRQ_ENABLE	3	EN_DATA_READY	启用JESD204B接收机准备(JRX_DATA_READY)低中断。 / Enable the JESD204B receiver ready (JRX_DATA_READY) low interrupt.	0x0	R/W
0x020	IRQ_ENABLE	2	EN_LANE_FIFO	启用通道FIFO溢出/下溢中断。 / Enable the lane FIFO overflow/ underflow interrupt.	0x0	R/W
0x020	IRQ_ENABLE	1	EN_PRBSQ	启用PRBS虚假错误中断。 / Enable the PRBS false error interrupt.	0x0	R/W
0x020	IRQ_ENABLE	0	EN_PRBSI	启用PRBS真实错误中断。 / Enable the PRBS real error interrupt.	0x0	R/W
0x021	IRQ_ENABLE0	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x021	IRQ_ENABLE0	3	EN_DAC0_CAL_DONE	启用DAC0校准完成中断。 / Enable the DAC0 calibration-done interrupt.	0x0	R/W
0x021	IRQ_ENABLE0	[2:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x021	IRQ_ENABLE0	0	EN_PAERR0	启用DAC0的PA保护错误中断。 / Enable the DAC0 PA protection error interrupt.	0x0	R/W
0x022	IRQ_ENABLE1	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x022	IRQ_ENABLE1	3	EN_DAC1_CAL_DONE	启用DAC1校准完成中断。 / Enable the DAC1 calibration-done interrupt.	0x0	R/W
0x022	IRQ_ENABLE1	[2:1]	RESERVED	保留。 / Reserved.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x022	IRQ_ENABLE1	0	EN_PAERR1	启用DAC1的PA保护错误中断。 / Enable the DAC1 PA protection error interrupt.	0x0	R/W
0x023	IRQ_ENABLE2	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x023	IRQ_ENABLE2	5	EN_DLL_LOST	启用DLL锁定丢失中断。 / Enable the DLL lock-lost interrupt.	0x0	R/W
0x023	IRQ_ENABLE2	4	EN_DLL_LOCK	启用DLL锁定中断。 / Enable the DLL lock interrupt.	0x0	R/W
0x023	IRQ_ENABLE2	[3:2]	RESERVED	保留。 / Reserved.	0x0	R/W
0x023	IRQ_ENABLE2	1	EN_PLL_LOST	启用PLL锁定丢失中断。 / Enable the PLL lock-lost interrupt.	0x0	R/W
0x023	IRQ_ENABLE2	0	EN_PLL_LOCK	启用PLL锁定中断。 / Enable the PLL lock interrupt.	0x0	R/W
0x024	IRQ_STATUS	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x024	IRQ_STATUS	4	IRQ_SYSREF_JITTER	SYSREF±抖动过大。如果EN_SYSREF_JITTER为低电平，IRQ_SYSREF_JITTER将显示当前状态。如果EN_SYSREF_JITTER为高电平，IRQ_SYSREF_JITTER就会锁存并将引脚拉低（x=MUX_SYSREF_JITTER设置）。在锁存时向IRQ_SYSREF_JITTER写1会清除该位。 / SYSREF+/- jitter too large. If EN_SYSREF_JITTER is low,IRQ_SYSREF_JITTER shows the current status. If EN_SYSREF_JITTER is high,IRQ_SYSREF_JITTER latches and pulls the pin low (x=MUX_SYSREF_JITTER setting).Writing 1 to IRQ_SYSREF_JITTER while latched clears the bit.	0x0	R/W
0x024	IRQ_STATUS	3	IRQ_DATA_READY	JESD204x接收机数据准备为低电平。如果EN_DATA_READY为低电平，则IRQ_DATA_READY显示当前状态。如果EN_DATA_READY为高电平，IRQ_DATA_READY会锁存并将引脚拉低（x=MUX_DATA_READY设置）。在锁存时向IRQ_DATA_READY写1会清除该位。 / JESD204x receiver data ready is low. If EN_DATA_READY is low,IRQ_DATA_READY shows the current status. If EN_DATA_READY is high, IRQ_DATA_READY latches and pulls the pin low (x=MUX_DATA_READY setting). Writing 1 to IRQ_DATA_READY while latched clears the bit.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x024	IRQ_STATUS	2	IRQ_LANE_FIFO	通道FIFO溢出/下溢。如果EN_LANE_FIFO为低电平，IRQ_LANE_FIFO将显示当前状态。如果EN_LANE_FIFO为高电平，IRQ_LANE_FIFO会锁存并将引脚拉低（x= MUX_LANE_FIFO设置）。在锁存时向IRQ_LANE_FIFO写1会清除该位。 / Lane FIFO overflow/ underflow. If EN_LANE_FIFO is low,IRQ_LANE_FIFO shows the current status. If EN_LANE_FIFO is high,IRQ_LANE_FIFO latches and pulls the pin low (x = MUX_LANE_FIFO setting). Writing 1 to IRQ_LANE_FIFO while latched clears the bit.	0x0	R/W
0x024	IRQ_STATUS	1	IRQ_PRBSQDAC1	PRBS错误。如果EN_PRBSQ为低电平，IRQ_PRBSQ将显示当前状态。如果EN_PRBSQ为高电平，IRQ_PRBSQ会锁存并将引脚拉低（x=MUX_PRBSQ设置）。在锁存时，向IRQ_PRBSQ写1会清除该位。 / PRBS error. If EN_PRBSQ is low, IRQ_PRBSQ shows the current status. If EN_PRBSQ is high,IRQ_PRBSQ latches and pulls the pin low (x = MUX_PRBSQ setting).Writing 1 to IRQ_PRBSQ while latched clears the bit.	0x0	R/W
0x024	IRQ_STATUS	0	IRQ_PRBSIDAC0PRBS	错误。如果EN_PRBSI为低电平，IRQ_PRBSI将显示当前状态。如果EN_PRBSI为高电平，IRQ_PRBSI会锁存并将引脚拉低(x=MUX_PRBSI设置)。在锁存时向IRQ_PRBSI写1会清除该位。 / Error. If EN_PRBSI is low,IRQ_PRBSI shows the current status. If EN_PRBSI is high,IRQ_PRBSI latches and pulls the pin low (x = MUX_PRBSI setting).Writing 1 to IRQ_PRBSI while latched clears the bit.	0x0	R/W
0x025	IRQ_STATUS0	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x025	IRQ_STATUS0	3	IRQ_DAC0_CAL_DONE	DAC0校准完成。如果EN_DAC0_CAL_ DONE为低电平，则IRQ_DAC0_CAL_ DONE显示当前状态。如果EN_DAC0_ CAL_DONE为高电平，则IRQ_DAC0_ CAL_DONE会锁存并将引脚拉低（x=MUX_DAC0_CAL_DONE设置）。锁定后，向IRQ_DAC0_CAL_DONE写1会清除该位。 / DAC0 calibration complete. If EN_DAC0_CAL_DONE is low, IRQ_DAC0_CAL_DONE	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				shows the current status. If EN_DAC0_CAL_DONE is high,IRQ_DAC0_CAL_DONE latches and pulls the pin low (x =MUX_DAC0_CAL_DONE setting).After latching, writing 1 to IRQ_DAC0_CAL_DONE clears the bit.		
0x025	IRQ_STATUS0	[2:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x025	IRQ_STATUS0	0	IRQ_PAERR0DAC0PA	错误。如果EN_PAERR0为低电平，IRQ_PAERR0将显示当前状态。如果EN_PAERR0为高电平，IRQ_PAERR0会锁存并将引脚拉低(x=MUX_PAERR0设置)。在锁存时，向其写1将清除该位。 / Error. If EN_PAERR0 is low, IRQ_PAERR0 shows the current status. If EN_PAERR0 is high, IRQ_PAERR0 latches and pulls the pin low (x =MUX_PAERR0 setting). Writing 1 to it while latched clears the bit.	0x0	R/W
0x026	IRQ_STATUS1	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x026	IRQ_STATUS1	3	IRQ_DAC1_CAL_DONE	DAC1校准完成。如果EN_DAC0_CAL_ DONE为低电平，则IRQ_DAC1_CAL_ DONE显示当前状态。如果EN_DAC1_CAL_DONE为高电平，则IRQ_DAC1_CAL_DONE会锁存并将引脚拉低（x = MUX_DAC1_CAL_DONE设置）。当被锁存时，向IRQ_DAC1_CAL_DONE写1会清除该位。 / DAC1 calibration complete. If EN_DAC0_CAL_DONE is low,IRQ_DAC1_CAL_DONE shows the current status. If EN_DAC1_CAL_DONE is high,IRQ_DAC1_CAL_DONE latches and pulls the pin low (x =MUX_DAC1_CAL_DONE setting).When latched, writing 1 to IRQ_DAC1_CAL_DONE clears the bit.	0x0	R/W
0x026	IRQ_STATUS1	[2:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x026	IRQ_STATUS1	0	IRQ_PAERR1DAC1PA	错误。如果EN_PAERR1为低电平，IRQ_PAERR1将显示当前状态。如果EN_PAERR1为高电平，IRQ_PAERR1会锁存并将引脚拉低（x=MUX_PAERR1设置）。在锁存时，向IRQ_PAERR1写1会清除该位。 / Error. If EN_PAERR1 is low,IRQ_PAERR1 shows the current status. If EN_PAERR1 is high,IRQ_PAERR1 latches and pulls the	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				pin low (x = MUX_PAERR1 setting).Writing 1 to it while latched clears the bit.		
0x027	IRQ_STATUS2	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x027	IRQ_STATUS2	5	IRQ_DLL_LOSTDLL	丢失。如果EN_DLL_LOST为低电平，IRQ_DLL_LOST将显示当前状态。如果EN_DLL_LOST为高电平，IRQ_DLL_LOST会锁存并将引脚拉低（x=MUX_DLL_LOST设置）。在锁存时向IRQ_DLL_LOST写1会清除该位。 / Lost. If EN_DLL_LOST is low,IRQ_DLL_LOST shows the current status. If EN_DLL_LOST is high,IRQ_DLL_LOST latches and pulls the pin low (x = MUX_DLL_LOST setting). Writing 1 to IRQ_DLL_LOST while latched clears the bit.	0x0	R/W
0x027	IRQ_STATUS2	4	IRQ_DLL_LOCKDLL	锁定。如果EN_DLL_LOCK为低电平，则IRQ_DLL_LOCK显示当前状态。如果EN_DLL_LOCK为高电平，IRQ_DLL_LOCK将锁定并将引脚拉低（x=MUX_DLL_LOCK设置）。在锁存时向IRQ_DLL_LOCK写1会清除该位。 / Locked. If EN_DLL_LOCK is low, IRQ_DLL_LOCK shows the current status. If EN_DLL_LOCK is high, IRQ_DLL_LOCK latches and pulls the pin low (x =MUX_DLL_LOCK setting). Writing 1 to IRQ_DLL_LOCK while latched clears the bit.	0x0	R/W
0x027	IRQ_STATUS2	[3:2]	RESERVED	保留。 / Reserved.	0x0	R/W
0x027	IRQ_STATUS2	1	IRQ_PLL_LOST	DACPLL锁定丢失。如果EN_PLL_LOST为低电平，IRQ_PLL_LOST会显示当前状态。如果EN_PLL_LOST为高电平，IRQ_PLL_LOST会锁存并将引脚拉低（x=MUX_PLL_LOST设置）。当IRQ_PLL_LOST锁定时，向其写1将清除该位。 / DAC PLL lock lost. If EN_PLL_LOST is low,IRQ_PLL_LOST shows the current status. If EN_PLL_LOST is high,IRQ_PLL_LOST latches and pulls the pin low (x = MUX_PLL_LOST setting). When IRQ_PLL_LOST is latched, writing 1 to it clears the bit.	0x0	R/W
0x027	IRQ_STATUS2	0	IRQ_PLL_LOCKDAC	PLL锁定。如果EN_PLL_LOCK为低电平，则IRQ_PLL_LOCK显示当前状态。如果EN_PLL_LOCK为高电平，	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				则IRQ_PLL_LOCK锁定并将引脚拉低（x=MUX_PLL_LOCK设置）。在锁存时向IRQ_PLL_LOCK写1会清除该位。 / PLL locked. If EN_PLL_LOCK is low, IRQ_PLL_LOCK shows the current status. If EN_PLL_LOCK is high, IRQ_PLL_LOCK latches and pulls the pin low (x =MUX_PLL_LOCK setting). Writing 1 to IRQ_PLL_LOCK while latched clears the bit.		
0x028	IRQ_OUTPUT_MUX	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x028	IRQ_OUTPUT_MUX	4	MUX_SYSREF_JITTER	如果设置了EN_SYSREF_JITTER，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_SYSREF_JITTER is set, this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x028	IRQ_OUTPUT_MUX	3	MUX_DATA_READY	如果设置了EN_DATA_READY，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_DATA_READY is set, this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1: send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x028	IRQ_OUTPUT_MUX	2	MUX_LANE_FIFO	如果设置了EN_LANE_FIFO，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_LANE_FIFO is set, this control selects the output pin of the trigger event. 0:send the IRQ trigger signal to the IRQ0 pin. 1: send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x028	IRQ_OUTPUT_MUX	1	MUX_PRBSQ	如果设置了EN_PRBSQ，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				送到引脚。 / If EN_PRBSQ is set,this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]		
0x028	IRQ_OUTPUT_MUX	0	MUX_PRBSI	如果设置了EN_PRBSI，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_PRBSI is set, this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x029	IRQ_OUTPUT_MUX0	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x029	IRQ_OUTPUT_MUX0	3	MUX_DAC0_CAL_	已如果设置了EN_DAC0_CAL_DONE，该控制将完成选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_DAC0_CAL_DONE is set, this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x029	IRQ_OUTPUT_MUX0	[2:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x029	IRQ_OUTPUT_MUX0	0	MUX_PAERR0	如果设置了EN_PAERR0，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_PAERR0 is set,this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x02A	IRQ_OUTPUT_MUX1	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x02A	IRQ_OUTPUT_MUX1	3	MUX_DAC1_CAL_DONE		0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				如果设置了EN_DAC1_CAL_DONE，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_DAC1_CAL_DONE is set, this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]		
0x02A	IRQ_OUTPUT_MUX1	[2:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x02A	IRQ_OUTPUT_MUX1	0	MUX_PAERR1	如果设置了EN_PAERR1，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_PAERR1 is set,this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x02B	IRQ_OUTPUT_MUX2	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x02B	IRQ_OUTPUT_MUX2	5	MUX_DLL_LOST	如果设置了EN_DLL_LOST，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_DLL_LOST is set, this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin.1: send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x02B	IRQ_OUTPUT_MUX2	4	MUX_DLL_LOCK	如果设置了EN_DLL_LOCK，该控制将选择触发事件的输出引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_DLL_LOCK is set, this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin.1: send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x02B	IRQ_OUTPUT_MUX2	[3:2]	RESERVED	保留。 / Reserved.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x02B	IRQ_OUTPUT_MUX2	1	MUX_PLL_LOST	如果设置了EN_PLL_LOST，该控制将选择触发事件的引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_PLL_LOST is set,this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x02B	IRQ_OUTPUT_MUX2	0	MUX_PLL_LOCK	如果设置了EN_PLL_LOCK，该控制将选择触发事件的引脚。0将IRQ触发信号发送到引脚。1将IRQ触发信号发送到引脚。 / If EN_PLL_LOCK is set,this control selects the output pin of the trigger event. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x02C	IRQ_STATUS_ALL	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x02C	IRQ_STATUS_ALL	0	IRQ_STATUS_ALL	该位是寄存器0x24至寄存器0x27中所有位的OR。向该位写入1将清除任何在寄存器0x24至寄存器0x27中锁存的的信号。 / This bit is the OR of all bits in Register 0x24 to Register 0x27. Writing 1 to this bit clears any signal latched in Register 0x24 to Register 0x27.	0x0	R/W
0x036	SYSREF_COUNT	[7:0]	SYSREF_COUNT	同步前要忽略的SYSREF±上升沿数（脉冲计数模式）。 / Number of SYSREF+/- rising edges to ignore before synchronization (pulse count mode).	0x0	R/W
0x039	SYSREF_ERR_	7	RESERVED	保留。WINDOW [6:0] SYSREF_ERR_SYSREF±输入允许的抖动量。SYSREF±抖动变WINDOW化大于此值时会触发中断。单位为DAC时钟。 / Reserved.SYSREF_ERR_WINDOW [6:0]: the amount of jitter allowed on the SYSREF+/- input. When the SYSREF+/- jitter variation becomes greater than this value, an interrupt is triggered. The unit is DAC clocks.	0x0	R
0x03A	SYSREF_MODE	[7:5]	RESERVED	保留。 / Reserved.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x03A	SYSREF_MODE	4		同步旋转完成同步逻辑翻转完成标志。 / Synchronization rotation complete / synchronization logic rotation complete flag.	0x1	R
0x03A	SYSREF_MODE	[3:2]	RESERVED	保留。 / Reserved.	0x0	R
0x03A	SYSREF_MODE	1	SYSREF_MODE_ONESHOT	启用单次同步翻转模式。00监控模式。如果SYSREF±边沿在错误窗口之外，则IRQ_SYSREF_JITTER的状态/错误标志为1（寄存器0x039，位[6:0]）。01在下一次SYSREF±时执行单次同步，然后切换到监控模式。 / Enable the one-shot synchronization rotation mode. 00:monitor mode. If a SYSREF+/- edge is outside the error window, the IRQ_SYSREF_JITTER status/ error flag is 1 (Register 0x039, Bits[6:0]).01: perform a one-shot synchronization at the next SYSREF+/-, then switch to monitor mode.	0x0	R/W
0x03A	SYSREF_MODE	0	RESERVED	保留。 / Reserved.	0x0	R/W
0x03B		6	RESERVED	保留。若要正常运行，请将该位写入1。 / Reserved. For normal operation, write this bit to 1.	0x0	R/W
0x03B		5	PERIODIC_RST_EN	需要同步设置。对于Subclass0和Subclass1操作，始终将该位设置为1。 / Synchronization setting required. For Subclass 0 and Subclass 1 operation, always set this bit to 1.	0x1	R/W
0x03B		4	NCORST_AFTER_ROT_EN	将该位设置为1，可在数字复位或同步旋转后复位所有NCO。该控制或START_NCO_ SYNC位（寄存器0x1E7，位0）均可用于重置所有NCO（主数据通路和通道数据通路）。 /Setting this bit to 1 resets all NCOs after a digital reset or synchronization rotation. This control or the START_NCO_SYNC bit (Register 0x1E7, Bit 0) can be used to reset all NCOs (main datapath and channel datapath).	0x1	R/W
0x03B		[3:2]	RESERVED	保留。 / Reserved.	0x0	R
0x03B		[1:0]	ROTITION_MODE	选择同步翻转时复位的电路。某些设置为1的位将决定同步翻转时采取的操作。位0对应SERDES时钟复位和重新调整。位1对应数据通路软关闭/打开增益，只有在使用PA保护时才可使用。如果不使用PA保护，则将位1设置为0。当同步翻转发生时，SERDES	0x0	R/W

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				时钟或数据通路都0不会发生任何动作。链路中断，SERDES时钟重置。建议将该位设置1为高电平，以便在执行同步翻转时，SERDES时钟能正确对齐。在同步翻转期间，数据通路会自动使用软开启/ 10关闭功能开启和关闭数据通路流，以避免传输损坏的数据。只有在使用PA保护块时才能使用此功能。SERDES时钟复位和数据通路软开启/关闭功能11均已启用。 / Select the circuits that are reset on a synchronization rotation. The bits set to 1 determine the action taken on a synchronization rotation. Bit 0 corresponds to SERDES clock reset and realignment. Bit 1 corresponds to datapath soft off/on, which can be used only when PA protection is used. If PA protection is not used,set Bit 1 to 0. 00: when a synchronization rotation occurs,neither the SERDES clock nor the datapath takes any action; the link is interrupted. 01: SERDES clock reset. It is recommended to set this bit high so that the SERDES clock aligns correctly when a synchronization rotation is performed. During a synchronization rotation, the datapath automatically uses the soft on/off function to turn the datapath stream on and off to avoid transmitting corrupted data.This function can be used only when the PA protection block is used. 11: both the SERDES clock reset and the datapath soft on/off functions are enabled.		
0x03F	TX_ENABLE	[7:6]	RESERVED	保留。 / Reserved.	0x0	R/W
0x03F	TX_ENABLE	5	TXEN_DATAPATH_DAC1	选择TXEN1引脚为低电平时，DAC1的数据通路是否减弱。0数据通路输出正常。1如果TXEN1=0，数据通路输出立即清零。如果TXEN1=1，数据通路输出正常运行。 / Select whether the DAC1 datapath is attenuated when the TXEN1 pin is low. 0: datapath output is normal.1: if TXEN1 = 0, the datapath output is immediately cleared to zero; if TXEN1 = 1, the datapath output operates normally.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x03F	TX_ENABLE	4	TXEN_DATAPATH_DAC0	选择TXEN0引脚为低电平时，DAC0的数据通路是否减弱。0数据通路输出正常。1如果TXEN0=0，数据通路输出立即清零。如果TXEN0=1，数据通路输出正常运行。 / Select whether the DAC0 datapath is attenuated when the TXEN0 pin is low. 0: datapath output is normal.1: if TXEN0 = 0, the datapath output is immediately cleared to zero; if TXEN0 = 1, the datapath output operates normally.	0x0	R/W
0x03F	TX_ENABLE	[3:0]	RESERVED	保留。 / Reserved.	0x0	R/W
0x050	CAL_CLK_DIV	[7:4]	RESERVED	保留 / Reserved.	0x2	R/W
0x050	CAL_CLK_DIV	[3:0]	CAL_CLK_DIV	校准寄存器控制。将这些位设置为0xA，以优化校准设置。 / Calibration register control. Set these bits to 0xA to optimize the calibration settings.	0x8	R/W
0x051	CAL_CTRL	7	CAL_CTRL0	校准设置。将该位设置为1。重置校准引擎。0启用校准例程。1 / Calibration setting. Set this bit to 1.Reset the calibration engine. 0:enable the calibration routine. 1:[text ends here in source].	0x1	R/W
0x051	CAL_CTRL	[6:3]	RESERVED	保留。 / Reserved.	0x0	R/W
0x051	CAL_CTRL	[2:1]	CAL_CTRL1	校准模式选择。将该位字段设为1可优化校准模式。由寄存器0x008中的MAINDAC_ PAGE位分页。1配置校准控制设置。 / Calibration mode selection. Setting this bit field to 1 optimizes the calibration mode.Paged by the MAINDAC_PAGE bit in Register 0x008. 1: configure the calibration control settings.	0x1	R/W
0x051	CAL_CTRL	0	CAL_START	开始校准。开始校准后，请勿写入寄存器0x051至寄存器0x061中的任何寄存器，直至寄存器0x052位2读为低电平（表示校准不再激活）。由寄存器0x00中的MAINDAC_PAGE位分页。 /Start calibration. After starting calibration, do not write to any register from Register 0x051 to Register 0x061 until Bit 2 of Register 0x052 reads low(indicating that calibration is no longer active). Paged by the MAINDAC_PAGE bit in Register 0x00.	0x0	R/W
0x052	CAL_STAT	[7:3]	RESERVED	保留。 / Reserved.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x052	CAL_STAT	2	CAL_ACTIVE	校准激活状态标志。回读1表示校准例程仍在进行中。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Calibration active status flag.Reading back 1 indicates the calibration routine is still in progress. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R
0x052	CAL_STAT	1	CAL_FAIL_SEARCH	校准失败标志。回读1表示校准例程失败，可能无效。此控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Calibration fail flag. Reading back 1 indicates the calibration routine failed and may be invalid.This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R
0x052	CAL_STAT	0	CAL_FINISH	校准完成标志。回读1表示校准完成。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Calibration finished flag. Reading back 1 indicates calibration is complete. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R
0x05A	FSC1	[7:0]	FSC_CTRL[7:0]	设置DACx模拟输出可用的满量程（最大）电流。该控制由寄存器0x008中的MAINDAC_PAGE位分页。满量程电流=15.625mA+FSC_CTRL×(25/256)(mA)。 / Set the full-scale(maximum) current available at the DACx analog output. This control is paged by the MAINDAC_PAGE bit in Register 0x008. Full-scale current =15.625 mA + FSC_CTRL x (25/256)(mA).	0x28	R/W
0x061	CAL_DEBUG0	7	RESERVED	保留。 / Reserved.	0x0	R/W
0x061	CAL_DEBUG0	6	CAL_CTRL2	校准控制。将该位设置为1可优化校准设置。 / Calibration control.Setting this bit to 1 optimizes the calibration settings.	0x1	R/W
0x061	CAL_DEBUG0	5	CAL_CTRL3	校准控制。将该位设置为1可优化校准设置。 / Calibration control.Setting this bit to 1 optimizes the calibration settings.	0x1	R/W
0x061	CAL_DEBUG0	4	RESERVED	保留。 / Reserved.	0x0	R/W
0x061	CAL_DEBUG0	3	CAL_CTRL4	校准控制。将该位设置为1可优化校准设置。 / Calibration control.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				Setting this bit to 1 optimizes the calibration settings.		
0x061	CAL_DEBUG0	[2:0]	RESERVED	保留。 / Reserved.	0x0	R/W
0x081	CLK_CTRL	[7:2]	RESERVED	保留。 / Reserved.	0x0	R/W
0x081	CLK_CTRL	1	CAL_CLK_PD1	DAC1校准完成后（寄存器0x052，位0=1），将该位设置为高电平以关闭校准时钟。 / After DAC1 calibration is complete (Register 0x052, Bit 0 =1), set this bit high to shut down the calibration clock.	0x0	R/W
0x081	CLK_CTRL	0	CAL_CLK_PD0	DAC0校准完成后（寄存器0x052，位0=1），将该位设置为高电平以关闭校准时钟。 / After DAC0 calibration is complete (Register 0x052, Bit 0 =1), set this bit high to shut down the calibration clock.	0x0	R/W
0x083	NVM_CTRL0	7	NVM_CTRL0A	用于控制环形振荡器的NVM寄存器。 / NVM register used to control the ring oscillator.	0x0	R/W
0x083	NVM_CTRL0	[6:2]	RESERVED	保留。 / Reserved.	0x0	R
0x083	NVM_CTRL0	[1:0]	NVM_CTRL0B	用于控制环形振荡器的NVM寄存器。00除以8。01除以16。10除以32。11除以64。 / NVM register used to control the ring oscillator. 00:divide by 8. 01: divide by 16. 10:divide by 32. 11: divide by 64.	0x2	R/W
0x084	SYSREF_CTRL	7	RESERVED	保留。 / Reserved.	0x0	R/W
0x084	SYSREF_CTRL	6	SYSREF_INPUTMODE	设置SYSREF±引脚的输入模式类型。0交流耦合SYSREF±。1直流耦合SYSREF±。 / Set the input mode type of the SYSREF+/- pin. 0: AC-coupled SYSREF+/-. 1: DC-coupled SYSREF+/-.	0x0	R/W
0x084	SYSREF_CTRL	[5:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x084	SYSREF_CTRL	0	SYSREF_PD	关闭SYSREF±接收器和同步电路。如果使用Subclass0，则将该位设置为1，因为不使用SYSREF±引脚。0 SYSREF±接收器上电。1 SYSREF±接收器断电。 / Shut down the SYSREF+/- receiver and synchronization circuitry. If Subclass 0 is used, set this bit to 1 because the SYSREF+/- pin is not used. 0: SYSREF+/- receiver powered up. 1: SYSREF+/- receiver powered down.	0x0	R/W
0x085	NVM_CTRL1	7	RESERVED	保留。 / Reserved.	0x0	R
0x085	NVM_CTRL1	[6:4]	NVM_CTRL1A		0x1	R/W

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				NVM控制。在配置序列开始时将此控制设置为1（如启动序列部分所示），在启动例程结束，不再对设备编程时将其设置为0。93 / NVM control. Set this control to 1 at the start of the configuration sequence(as shown in the start-up sequence section); at the end of the start-up routine, when the device is no longer being programmed, set it to 0.		
0x085	NVM_CTRL1	[3:2]	RESERVED	保留。 / Reserved.	0x0	R
0x085	NVM_CTRL1	1	NVM_CTRL1B	NVM控制。在配置序列开始时将此控制设置为1（如启动序列部分所示），在启动例程结束，不再对设备编程时将其设置为0。 / NVM control.Set this control to 1 at the start of the configuration sequence (as shown in the start-up sequence section); at the end of the start-up routine, when the device is no longer being programmed, set it to 0.	0x1	R/W
0x085	NVM_CTRL1	0	NVM_CTRL1C	NVM控制。在配置序列开始时将此控制设置为0（如启动序列部分所示），在启动例程结束，不再对设备编程时将其设置为1。 / NVM control.Set this control to 0 at the start of the configuration sequence (as shown in the start-up sequence section); at the end of the start-up routine, when the device is no longer being programmed, set it to 1.	0x1	R/W
0x08D	ADC_CLK_CTRL0	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x08D	ADC_CLK_CTRL0	[4:0]	CLKOUT_SWING	控制ADC时钟驱动器的摆动电平。摆幅可以为负（反转时钟）。代码0至代码9的计算方法如下：ADC驱动器摆幅=993mV-CLKOUT_SWING×77mV。代码10至代码19的计算方法如下：ADC驱动器摆幅=(20-CLKOUT_SWING×77 mV)-1V。 /Control the swing level of the ADC clock driver. The swing can be negative (inverted clock). For codes 0 to 9, the calculation is as follows:ADC driver swing = 993 mV -CLKOUT_SWING x 77 mV. For codes 10 to 19, the calculation is as follows: ADC driver swing = (20 -CLKOUT_SWING x 77 mV) - 1 V.	0x0	R/W
0x08F	ADC_CLK_CTRL2	[7:1]	RESERVED	保留。 / Reserved.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x08F	ADC_CLK_CTRL2	0	PD_CLKOUT_DRIVER	关闭CLKOUT±输出驱动器。 / Shut down the CLKOUT+/- output driver.	0x0	R/W
0x090	DAC_POWERDOWN	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x090	DAC_POWERDOWN	1	DAC_PD1	关闭DAC1。0启动DAC1。1关闭DAC1。 / Shut down DAC1. 0: start DAC1. 1: shut down DAC1.	0x1	R/W
0x090	DAC_POWERDOWN	0	DAC_PD0	关闭DAC0。0启动DAC0。1关闭DAC0。 / Shut down DAC0. 0: start DAC0. 1: shut down DAC0.	0x1	R/W
0x091	ACLK_CTRL	[7:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x091	ACLK_CTRL	0	ACLK_POWERDOWN	模拟时钟接收器断电。 / Analog clock receiver power-down.	0x1	R/W
0x094	PLL_CLK_DIV	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x094	PLL_CLK_DIV	1	PLL_VCO_DIV3_EN	启用PLL输出时钟除以3。 / Enable PLL output clock divide-by-3.	0x0	R/W
0x094	PLL_CLK_DIV	0	PLL_VCO_DIV2_EN	启用PLL输出时钟除以2。0 DAC时钟=PLL VCO时钟频率。1 DAC时钟=PLL VCO时钟频率÷2。 / Enable PLL output clock divide-by-2. 0: DAC clock = PLL VCO clock frequency. 1:DAC clock = PLL VCO clock frequency / 2.	0x0	R/W
0x095	PLL_BYPASS	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x095	PLL_BYPASS	0	PLL_BYPASS	启用直接时钟（绕过PLL时钟）。0使用内部PLL产生DAC时钟。1绕过PLL，直接使用DAC时钟频率。 /Enable direct clock (bypass the PLL clock). 0: use the internal PLL to generate the DAC clock. 1: bypass the PLL and use the DAC clock frequency directly.	0x0	R/W
0x09A	NVM_CTRL	7	PD_BGR	偏置断电。将该位设置为1，可关闭内部偏置电源。 / Bias power-down.Setting this bit to 1 shuts down the internal bias supply.	0x0	R/W
0x09A	NVM_CTRL	[6:0]	RESERVED	保留。 / Reserved.	0x0	R/W
0x0C0	DELAY_LINE_PD	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x0C0	DELAY_LINE_PD	5	DLL_CTRL0B	DLL控制。将该位设置为0，可在设备配置序列中为延迟线上电。 / DLL control. Setting this bit to 0 powers up the delay line in the device configuration sequence.	0x1	R/W
0x0C0	DELAY_LINE_PD	4	DLL_CTRL0A	DLL控制。将该位设置为0，可在设备配置序列中为延迟线上电。 / DLL control. Setting this bit to 0 powers	0x1	R/W

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				up the delay line in the device configuration sequence.		
0x0C0	DELAY_LINE_PD	[3:1]	RESERVED	保留。 / Reserved.	0x0	R
0x0C0	DELAY_LINE_PD	0	DLL_PD	延迟线断电。将该位设置为0，可在设备配置序列期间为延迟线上电。0上电并启用延迟线。1断电并旁路延迟线。 / Delay line power-down.Setting this bit to 0 powers up the delay line during the device configuration sequence. 0: power up and enable the delay line. 1:power down and bypass the delay line.	0x1	R/W
0x0C1	DLL_CTRL0	[7:6]	DLL_CTRL1C	DAC控制设置。将此控制设置为1，可获得最佳性能。 / DAC control setting. Set this control to 1 for best performance.	0x1	R/W
0x0C1	DLL_CTRL0	5	DLL_CTRL1B	DLL控制搜索模式。如果DAC频率小于4.5 GHz，将该位设置为0；否则该位设置为1。 / DLL control search mode. If the DAC frequency is less than 4.5 GHz, set this bit to 0;otherwise set this bit to 1.	0x1	R/W
0x0C1	DLL_CTRL0	[4:3]	DLL_CTRL1A	DLL控制搜索方向。将此控制设置为1，可获得最佳性能。 / DLL control search direction. Set this control to 1 for best performance.	0x2	R/W
0x0C1	DLL_CTRL0	[2:1]	RESERVED	保留。 / Reserved.	0x0	R
0x0C1	DLL_CTRL0	0	DLL_ENABLE	启用DLL控制器。0禁用DLL。1启用DLL。 / Enable the DLL controller.0: disable the DLL. 1: enable the DLL.	0x0	R/W
0x0C3	DLL_STATUS	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x0C3	DLL_STATUS	0	DLL_LOCK	DLL锁定指示器。如果DLL锁定，则该控制读回1。 / DLL lock indicator.If the DLL is locked, this control reads back 1.	0x0	R
0x0C7	DLL_READ	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x0C7	DLL_READ	0	DLL_READ_EN	启用DLL状态回读。0到1的转换会更新寄存器0x0C3中的锁定状态位回读。 / Enable DLL status readback.A 0-to-1 transition updates the lock status bit readback in Register 0x0C3.	0x0	R/W
0x0CC		[5:0]	DLL_FINE_DELAY0	DLL延迟控制 / DLL delay control.	0x0	R/W
0x0CD		[5:0]	DLL_FINE_DELAY1	DLL延迟控制 / DLL delay control.	0x0	R/W
0x0DB	DLL_UPDATE	[7:1]	RESERVED	保留。 / Reserved.	0x0	R

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0x0DB	DLL_UPDATE	0	DLL_DELAY_UPDATE	DLL更新控制。根据当前寄存器控制设置，利用从0到1的转换，更新DLL电路。 / DLL update control. Using a 0-to-1 transition, update the DLL circuitry according to the current register control settings.	0x0	R/W
0x0FF		1	CMPLX_MOD_DIV2_DISABLE	禁用调制器开关路径中的除以2模块。设置为1，可旁路除2模块。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Disable the divide-by-2 block in the modulator switch path. Setting to 1 bypasses the divide-by-2 block.This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x0FF		0	RESERVED	保留。 / Reserved.	0x0	R
0x100	DIG_RESET	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x100	DIG_RESET	0	DIG_DATAPATH_PD	将所有数字逻辑（SERDES数字、数字时钟发生和数字数据通路）保持在复位状态，直至时钟树稳定。0正常运行模式。1将数字逻辑保持在复位状态。必须在芯片时钟稳定（PLL和DLL块锁定）后释放（设置为0），才能使用数字数据通路。 / Hold all digital logic (SERDES digital, digital clock generation and digital datapath) in reset until the clock tree is stable. 0: normal operating mode. 1: hold the digital logic in reset. It must be released (set to 0)after the chip clocks are stable (the PLL and DLL blocks are locked)before the digital datapath can be used.	0x1	R/W
0x110	JESD_MODE	7	MODE_NOT_IN_TABLE	已编程的JESD204B模式和内插模式组合无效。请选择其他组合。 / The programmed JESD204B mode and interpolation mode combination is invalid. Select another combination.	0x0	R
0x110	JESD_MODE	6	COM_SYNC	在双信号链路案例里，将信号合并。 / In the dual-signal link case,combine the signals.	0x0	R/W
0x110	JESD_MODE	[5:0]	JESD_MODE	设置JESD204B模式配置。支持的JESD204B工作模式和兼容的插值率，请参见表1。该控制位的第5位决定单链路（设置为0）或双链路（设置为1）。位[4:0]根据表1设置所需的JESD204B模式。 / Set the JESD204B mode configuration. See	0x20	R/W

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				Table 1 for the supported JESD204B operating modes and compatible interpolation rates. Bit 5 of this control determines single-link (set to 0) or dual-link (set to 1)operation. Bits[4:0] set the required JESD204B mode per Table 1.		
0x111	INTRP_MODE	[7:4]	DP_INTERP_MODE	设置主数据通路插值率。支持的JESD204B工作模式以及兼容的JESD204B模式和通道插值率，请参见表1。0x1 1× 0x2 2× 0x4 4× 0x6 6× 0x8 8× 0xC 12× / Set the main datapath interpolation rate. See Table 1 for the supported JESD204B operating modes and the compatible JESD204B modes and channel interpolation rates.0x1: 1x. 0x2: 2x. 0x4: 4x. 0x6: 6x.0x8: 8x. 0xC: 12x.	0x8	R/W
0x111	INTRP_MODE	[3:0]	CH_INTERP_MODE	设置通道插值率。有关支持的JESD204B工作模式以及兼容的JESD204B模式和主数据通路插值率，请参见表1。0x1 1× 0x2 2× 0x3 3× 0x4 4× 0x6 6× 0x8 8× / Set the channel interpolation rate. See Table 1 for the supported JESD204B operating modes and the compatible JESD204B modes and main datapath interpolation rates. 0x1: 1x. 0x2: 2x. 0x3: 3x. 0x4:4x. 0x6: 6x. 0x8: 8x.	0x4	R/W
0x112	DDSM_DATAPATH_	7		保留保留。CFG 6 EN_CMPLX_MOD调制器开关模式选择。通过该控制可以修改调制器开关的配置3，使来自各NCO的复数（I/Q）数据传递到DACx。该功能取决于寄存器0x112中位[5:4]的设置。当该位设置为高电平时，寄存器的位[5:4]将设置为0b11（调制器开关配置3）。该控制由寄存器0x008中的MAINDAC_PAGE位分页。开关配置由位[5:4]定义。0 当位[5:4]=0b11且DAC1主NCO启用时，1 DAC0=I0_NCO+I1_NCO，DAC1=Q0_NCO +Q1_NCO。当位[5:4]=0b11，并禁用DAC1主NCO时，DAC0=I0_NCO，DAC1=Q0_NCO。96 / Modulator switch mode selection. This control can modify Modulator Switch Configuration 3, so that the complex (I/Q) data from each NCO is passed to DACx. This function	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				depends on the setting of Bits[5:4]in Register 0x112. When this bit is set high, Bits[5:4] of the register are set to 0b11 (Modulator Switch Configuration 3). This control is paged by the MAINDAC_PAGE bit in Register 0x008. The switch configuration is defined by Bits[5:4]. 0: when Bits[5:4] = 0b11 and the DAC1 main NCO is enabled,DAC0 = I0_NCO + I1_NCO, DAC1 =Q0_NCO + Q1_NCO. 1: when Bits[5:4] = 0b11 and the DAC1 main NCO is disabled, DAC0 = I0_NCO,DAC1 = Q0_NCO.		
0x112	DDSM_DATAPATH_	[5:4]	DDSM_MODE	调制器开关模式选择。该控制可为正在配置的主数据通路NCO选择工作模式。该控制由寄存器0x008中的MAINDAC_PAGE位分页。DAC0=I0;DAC1=I1。00 DAC0=I0+I1;DAC1=Q0+Q1。01 DAC0=I0;DAC1=Q0。10 DAC0=I0+I1;DAC1=0。11 / Modulator switch mode selection. This control selects the operating mode for the main datapath NCO being configured. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 00: DAC0 = I0; DAC1= I1. 01: DAC0 = I0 + I1; DAC1 = Q0 +Q1. 10: DAC0 = I0; DAC1 = Q0. 11:DAC0 = I0 + I1; DAC1 = 0. [option values re-aligned in printed order]	0x0	R/W
0x112	DDSM_DATAPATH_	3	DDSM_NCO_EN	主数据通路调制启用。如果选择的JESD204B模式是复数模式（主数据通路插值>1×），则必须将使用的每个主数据通路的该位设置为1。如果不需要调制，则将FTW设置为0。该控制由寄存器0x008中的MAINDAC_PAGE位分页。禁用主数据路径NCO。0启用主数据路径NCO。1 / Main datapath modulation enable. If the selected JESD204B mode is a complex mode (main datapath interpolation > 1x), this bit must be set to 1 for each main datapath used. If modulation is not required, set the FTW to 0. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: disable the main datapath NCO. 1: enable the main datapath NCO.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x112	DDSM_DATAPATH_	2	DDSM_MODULUS_EN	启用主数据通路modulus DDS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。禁用modulus DDS。0启用modulus DDS。1 / Enable the main datapath modulus DDS. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: disable modulus DDS. 1: enable modulus DDS.	0x0	R/W
0x112	DDSM_DATAPATH_	1	DDSM_SEL_	边带从调制结果中选择上边带或下边带。该控制由寄存器0x008中的MAINDAC_PAGE位分页。使用上边带。0使用下边带=频谱翻转。1 / The sideband selects the upper or lower sideband from the modulation result. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: use the upper sideband. 1: use the lower sideband = spectral inversion.	0x0	R/W
0x112	DDSM_DATAPATH_	0	EN_SYNC_ALL_CHNL_NCO_RESETS	选择用于复位和FTW更新的信号通道NCOS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。0根据通道NCO更新请求，通道NCO重置或更新其FTW。1根据主数据路径NCO更新请求，通道NCO重置或更新其FTW。 / Select the signal for the channel NCO reset and FTW update. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: per the channel NCO update request, the channel NCO resets or updates its FTW. 1: per the main datapath NCO update request, the channel NCO resets or updates its FTW.	0x1	R/W
0x113		[6:4]	DDSM_FTW_REQ_MODE	频率调谐字自动更新模式。该控制由寄存器0x008中的MAINDAC_PAGE位分页。000当写入FTW寄存器时，不会产生自动请求。001写入DDSM_FTW位[7:0]后，自动生成DDSM_FTW_LOAD_REQ。010写入DDSM_FTW位[15:8]后，自动生成DDSM_FTW_LOAD_REQ。011写入DDSM_FTW位[23:16]后自动生成DDSM_FTW_LOAD_REQ。100写入DDSM_FTW位[31:24]后，自动生成DDSM_FTW_LOAD_REQ。101写入DDSM_FTW位[39:32]后自动生成DDSM_FTW_LOAD_REQ。97110写入DDSM_FTW位[47:40]后自动生成DDSM_FTW_LOAD_REQ。 / Frequency tuning word automatic	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				update mode. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 000: when the FTW registers are written, no automatic request is generated. 001: after writing DDSM_FTW Bits[7:0],DDSM_FTW_LOAD_REQ is automatically generated. 010: after writing DDSM_FTW Bits[15:8],DDSM_FTW_LOAD_REQ is automatically generated. 011: after writing DDSM_FTW Bits[23:16],DDSM_FTW_LOAD_REQ is automatically generated. 100: after writing DDSM_FTW Bits[31:24],DDSM_FTW_LOAD_REQ is automatically generated. 101: after writing DDSM_FTW Bits[39:32],DDSM_FTW_LOAD_REQ is automatically generated. 110: after writing DDSM_FTW Bits[47:40],DDSM_FTW_LOAD_REQ is automatically generated.		
0x113		3	RESERVED	保留。 / Reserved.	0x0	R
0x113		2	DDSM_FTW_LOAD_SYSREF	利用SYSREF±的下一个上升沿触发FTW加载和复位。该位还可在检测到上升沿时加载calibration tone FTW以及主NCO FTW。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Use the next rising edge of SYSREF+/- to trigger FTW loading and reset. This bit can also load the calibration tone FTW and the main NCO FTW when a rising edge is detected. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x113		1	DDSM_FTW_LOAD_ACK	频率调谐字更新确认。如果正确加载了FTW和相位偏移字，则该位读回1。该控制由寄存器0x008中的MAINDAC_PAGE位分页。FTW未加载。0 FTW已加载。1 / Frequency tuning word update acknowledge.If the FTW and phase offset words are loaded correctly, this bit reads back 1. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: FTW not loaded. 1: FTW loaded.	0x0	R
0x113		0	DDSM_FTW_LOAD_REQ	来自SPI的频率调谐字更新请求。该位还可在检测到上升沿时加载calibration tone FTW和主NCO FTW。该控制由寄存器0x008中的	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				MAINDAC_PAGE位分页。清除DDSM_FTW_LOAD_ACK。0 0到1的转换，加载FTW。1 / Frequency tuning word update request from the SPI. This bit can also load the calibration tone FTW and the main NCO FTW when a rising edge is detected. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: clear DDSM_FTW_LOAD_ACK. 1: 0-to-1 transition, load the FTW.		
0x114	DDSM_FTW0	[7:0]	DDSM_FTW[7:0]	设置主数据路径NCO FTW。如果DDSM_MODULUS_EN为低电平，主数据路径NCO频率=fDAC×(DDSM_FTW/2^48)。如果DDSM_MODULUS_EN为高电平，主数据路径NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS.该控制由寄存器0x008中的MAINDAC_PAGE位分页。置 / Set the main datapath NCO FTW. If DDSM_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSM_FTW/2^48). If DDSM_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSM_FTW +DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x115	DDSM_FTW1	[7:0]	DDSM_FTW[15:8]	设置主数据路径NCO FTW。如果DDSM_MODULUS_EN为低电平，主数据路径NCO频率=fDAC×(DDSM_FTW /2^48。如果DDSM_MODULUS_EN为高电平，则主数据路径NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48.DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set the main datapath	0x0	R/W

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				NCO FTW. If DDSM_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSM_FTW/ 2^48 [parenthesis unclosed in source]. If DDSM_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x116	DDSM_FTW2	[7:0]	DDSM_FTW[23:16]	设置主数据路径NCO FTW。如果DDSM_MODULUS_EN为低电平，主数据路径NCO频率=fDAC×(DDSM_FTW /2^48。如果DDSM_MODULUS_EN为高电平，则主数据路径NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set the main datapath NCO FTW. If DDSM_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSM_FTW/ 2^48 [parenthesis unclosed in source]. If DDSM_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x117	DDSM_FTW3	[7:0]	DDSM_FTW[31:24]	设置主数据路径NCO FTW。如果DDSM_MODULUS_EN为低电平，主数据路径NCO频率=fDAC×(DDSM_FTW /2^48。如果DDSM_MODULUS_EN为高电平，则主数据路径NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set the main datapath	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				NCO FTW. If DDSM_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSM_FTW/ 2^48 [parenthesis unclosed in source]. If DDSM_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x118	DDSM_FTW4	[7:0]	DDSM_FTW[39:32]	设置主数据路径NCO FTW。如果DDSM_MODULUS_EN为低电平，主数据路径NCO频率=fDAC×(DDSM_FTW/2^48)。如果DDSM_MODULUS_EN为高电平，主数据路径NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS.该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set the main datapath NCO FTW. If DDSM_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSM_FTW/ 2^48). If DDSM_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x119	DDSM_FTW5	[7:0]	DDSM_FTW[47:40]	设置主数据路径NCO FTW。如果DDSM_MODULUS_EN为低电平，主数据路径NCO频率=fDAC×(DDSM_FTW/2^48)。如果DDSM_MODULUS_EN为高电平，主数据路径NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				_ACC_MODULUS.该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set the main datapath NCO FTW. If DDSM_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSM_FTW/ 2^48). If DDSM_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x11C	DDSM_PHASE_	[7:0]	DDSM_NCO_PHASE_OFFSET[7:0]	设置主数据路径NCO相位偏移。代码为16位二进制补码格式。OFFSET0度数偏移=180×（代码/215）。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set the main datapath NCO phase offset. The code is in 16-bit twos complement format.Degrees offset = 180 x (code/2^15).This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x11D	DDSM_PHASE_	[7:0]	DDSM_NCO_PHASE_OFFSET	设置主数据路径NCO相位偏移。代码为16位二进制补码OFFSET1[15:8]格式。度数偏移=180×（代码/215）。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set the main datapath NCO phase offset.The code is in 16-bit twos complement format. Degrees offset = 180 x (code/2^15). This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x124	DDSM_ACC_	[7:0]		DDSM_ACC_MODULUS[7:0]设置DDSM_ACC_MODULUS。MODULUS0如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				页。 / Set DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x125	DDSM_ACC_	[7:0]		DDSM_ACC_MODULUS[15:8]设置DDSM_ACC_MODULUS。MODULUS1如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x126	DDSM_ACC_	[7:0]		DDSM_ACC_MODULUS[23:16]设置DDSM_ACC_MODULUS。MODULUS2如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x127	DDSM_ACC_	[7:0]		DDSM_ACC_MODULUS[31:24]设置DDSM_ACC_MODULUS。MODULUS3如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x128	DDSM_ACC_	[7:0]	DDSM_ACC_MODULUS[39:32]	设置DDSM_ACC_MODULUS。MODULUS4如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x129	DDSM_ACC_	[7:0]	DDSM_ACC_MODULUS	[47:40]设置DDSM_ACC_MODULUS。MODULUS5如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_MODULUS. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x12A	DDSM_ACC_DELTA0	[7:0]	DDSM_ACC_DELTA[7:0]	设置DDSM_ACC_DELTA。如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x12B	DDSM_ACC_DELTA1	[7:0]	DDSM_ACC_DELTA[15:8]		0x0	R/W

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				设置DDSM_ACC_DELTA。如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x12C	DDSM_ACC_DELTA2	[7:0]	DDSM_ACC_DELTA[23:16]	设置DDSM_ACC_DELTA。如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x12D	DDSM_ACC_DELTA3	[7:0]	DDSM_ACC_DELTA[31:24]	设置DDSM_ACC_DELTA。如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x12E	DDSM_ACC_DELTA4	[7:0]	DDSM_ACC_DELTA[39:32]	设置DDSM_ACC_DELTA。如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/ 2^48.DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x12F	DDSM_ACC_DELTA5	[7:0]	DDSM_ACC_DELTA[47:40]	设置DDSM_ACC_DELTA。如果DDSM_MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSM_FTW+DDSM_ACC_DELTA/DDSM_ACC_MODULUS)/2^48。DDSM_ACC_DELTA必须大于0。DDSM_ACC_DELTA必须大于DDSM_ACC_MODULUS。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / Set DDSM_ACC_DELTA. If DDSM_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSM_FTW +DDSM_ACC_DELTA/ DDSM_ACC_MODULUS)/2^48.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DDSM_ACC_DELTA must be greater than 0. DDSM_ACC_DELTA must be greater than DDSM_ACC_MODULUS. This control is paged by the MAINDAC_PAGE bit in Register 0x008.		
0x130	DDSC_DATAPATH_	7	RESERVED	保留。CFG 6 DDSC_NCO_EN通道数据通路调制启用。如果选择的JESD204B模式是复数模式（通道插值>1×），则必须将使用的每个通道数据通路的该位设置为1。如果不需要调制，则将FTW设置为0。该控制由寄存器0x008中的CHANNEL_PAGE位分页。禁用通道NCO。0启用通道NCO。1 / Channel datapath modulation enable. If the selected JESD204B mode is a complex mode (channel interpolation > 1x),this bit must be set to 1 for each channel datapath used. If modulation is not required, set the FTW to 0. This control is paged by the CHANNEL_PAGE bit in Register 0x008. 0: disable the channel NCO.1: enable the channel NCO.	0x0	R
0x130	DDSC_DATAPATH_	[5:3]	RESERVED	保留。 / Reserved.	0x0	R/W
0x130	DDSC_DATAPATH_	2	DDSC_MODULUS_EN	启用通道modulus DDS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。0禁用模数DDS。1启用模数DDS。101 / Enable the channel modulus DDS. This control is paged by the CHANNEL_PAGE bit in Register 0x008. 0: disable modulus DDS. 1: enable modulus DDS.	0x0	R/W
0x130	DDSC_DATAPATH_	1	DDSC_SEL_SIDEBAND	从调制结果中选择上边带或下边带。该控制由寄存器0x008中的CHANNEL_PAGE位分页。使用上边带。0使用下边带=频谱翻转。1 /Select the upper or lower sideband from the modulation result. This control is paged by the CHANNEL_PAGE bit in Register 0x008. 0: use the upper sideband.1: use the lower sideband =spectral inversion.	0x0	R/W
0x130	DDSC_DATAPATH_	0	DDSC_EN_DC_INPUT	通过向通道DDS发送直流输入电平，启用测试tone生成。在DC_TEST_INPUT_AMPLITUDE控制器（寄存器0x148和寄存器0x149）中设置振幅。该控制由寄存器0x008中的CHANNEL_PAGE位分页。禁用测	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				试tone生成。0启用测试tone生成。1 / Enable test tone generation by sending a DC input level to the channel DDS. Set the amplitude in the DC_TEST_INPUT_AMPLITUDE control (Register 0x148 and Register 0x149). This control is paged by the CHANNEL_PAGE bit in Register 0x008. 0: disable test tone generation. 1: enable test tone generation.		
0x131	DDSC_FTW_UPDATE	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x131	DDSC_FTW_UPDATE	2	DDSC_FTW_LOAD_SYSREF	使用SYSREF±的下一个上升沿触发FTW加载和复位。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Use the next rising edge of SYSREF+/- to trigger FTW loading and reset. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x131	DDSC_FTW_UPDATE	1	DDSC_FTW_LOAD_ACK	频率调整字更新确认位。如果正确加载了FTW和相位偏移字，则该位读回1。该控制由寄存器0x008中的CHANNEL_PAGE位分页。FTW未加载。0 FTW已加载。1 / Frequency tuning word update acknowledge bit. If the FTW and phase offset words are loaded correctly, this bit reads back 1. This control is paged by the CHANNEL_PAGE bit in Register 0x008. 0: FTW not loaded.1: FTW loaded.	0x0	R
0x131	DDSC_FTW_UPDATE	0	DDSC_FTW_LOAD_REQ	来自SPI的频率调整字更新请求。该控制由寄存器0x008中的CHANNEL_PAGE位分页。FTW没有更新。0 0到1转换，加载FTW。1 /Frequency tuning word update request from the SPI. This control is paged by the CHANNEL_PAGE bit in Register 0x008. 0: FTW not updated. 1: 0-to-1 transition, load the FTW.	0x0	R/W
0x132	DDSC_FTW0	[7:0]	DDSC_FTW[7:0]	设置通道数据通路NCO FTW。如果DDSC_MODULUS_EN为低电平，主数据通路NCO频=fDAC×(DDSC_FTW/2^48)。如果DDSC_MODULUS_EN为高电平，主数据总线NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set the channel datapath NCO FTW. If DDSC_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSC_FTW +DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x133	DDSC_FTW1	[7:0]	DDSC_FTW[15:8]	设置通道数据通路NCO FTW。如果DDSC_MODULUS_EN为低电平，主数据通路NCO频=fDAC×(DDSC_FTW/2^48)。如果DDSC_MODULUS_EN为高电平，主数据总线NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set the channel datapath NCO FTW. If DDSC_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSC_FTW +DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x134	DDSC_FTW2	[7:0]	DDSC_FTW[23:16]	设置通道数据通路NCO FTW。如果DDSC_MODULUS_EN为低电平，主数据通路NCO频=fDAC×(DDSC_FTW/2^48)。如果DDSC_MODULUS_EN为高电平，主数据总线NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/	0x0	R/W

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				DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set the channel datapath NCO FTW. If DDSC_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSC_FTW +DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x135	DDSC_FTW3	[7:0]	DDSC_FTW[31:24]	设置通道数据通路NCO FTW。如果DDSC_MODULUS_EN为低电平，主数据通路NCO频=fDAC×(DDSC_FTW/2^48)。如果DDSC_MODULUS_EN为高电平，主数据总线NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set the channel datapath NCO FTW. If DDSC_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSC_FTW/2^48). If DDSC_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSC_FTW +DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x136	DDSC_FTW4	[7:0]	DDSC_FTW[39:32]	设置通道数据通路NCO FTW。如果DDSC_MODULUS_EN为低电平，主数据通路NCO频=fDAC×(DDSC_FTW/2^48)。如果DDSC_MODULUS_EN为高电平，主数据总线NCO频率	0x0	R/W

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				=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set the channel datapath NCO FTW. If DDSC_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSC_FTW/ 2^48). If DDSC_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x137	DDSC_FTW5	[7:0]	DDSC_FTW[47:40]	设置通道数据通路NCO FTW。如果DDSC_MODULUS_EN为低电平，主数据通路NCO频=fDAC×(DDSC_FTW/2^48)。如果DDSC_MODULUS_EN为高电平，主数据总线NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set the channel datapath NCO FTW. If DDSC_MODULUS_EN is low, the main datapath NCO frequency = fDAC x (DDSC_FTW/ 2^48). If DDSC_MODULUS_EN is high, the main datapath NCO frequency = fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x138	DDSC_PHASE_	[7:0]		DDSC_NCO_PHASE_OFFSET[7:0]设置通道NCO相位偏移。代码为16位二进制补码格式。OFFSET0角度偏移=180×(代码/215)。该控制由寄存器	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				0x008中的CHANNEL_PAGE位分页。 / Set the channel NCO phase offset. The code is in 16-bit twos complement format. Angle offset =180 x (code/2^15). This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x139	DDSC_PHASE_	[7:0]		DDSC_NCOOPHASE_OFFSET[15:8]设置通道NCO相位偏移。代码为16位二进制补码格式。OFFSET1角度偏移=180×(代码/215)。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set the channel NCO phase offset. The code is in 16-bit twos complement format. Angle offset =180 x (code/2^15). This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x13A	DDSC_ACC_	[7:0]		DDSC_ACC_MODULUS[7:0]设置DDSC_ACC_MODULUS。如果DDSC_ MODULUS0 MODULUS_EN为高电平，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_MODULUS.If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x13B	DDSC_ACC_	[7:0]		DDSC_ACC_MODULUS[15:8]设置DDSC_ACC_MODULUS。如果DDSC_ MODULUS1 MODULUS_EN为高电平，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_MODULUS.If DDSC_MODULUS_EN is high, the main datapath NCO frequency =	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x13C	DDSC_ACC_	[7:0]		DDSC_ACC_MODULUS[23:16]设置DDSC_ACC_MODULUS。如果DDSC_ MODULUS2 MODULUS_EN为高电平，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_MODULUS.If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x13D	DDSC_ACC_	[7:0]		DDSC_ACC_MODULUS[31:24]设置DDSC_ACC_MODULUS。如果DDSC_ MODULUS3 MODULUS_EN为高电平，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_MODULUS.If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x13E	DDSC_ACC_	[7:0]	DDSC_ACC_MODULUS[39:32]	设置DDSC_ACC_MODULUS。如果DDSC_ MODULUS4 MODULUS_EN为高电平，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_MODULUS.If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x13F	DDSC_ACC_	[7:0]	DDSC_ACC_MODULUS[47:40]	设置DDSC_ACC_MODULUS。如果DDSC_ MODULUS5 MODULUS_EN为高电平，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_MODULUS.If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x140	DDSC_ACC_DELTA0	[7:0]	DDSC_ACC_DELTA[7:0]	设置DDSC_ACC_DELTA。如果DDSC_ MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, the main datapath NCO frequency =	0x0	R/W

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				fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x141	DDSC_ACC_DELTA1	[7:0]	DDSC_ACC_DELTA[15:8]	设置DDSC_ACC_DELTA。如果DDSC_ MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x142	DDSC_ACC_DELTA2	[7:0]	DDSC_ACC_DELTA[23:16]	设置DDSC_ACC_DELTA。如果DDSC_ MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x143	DDSC_ACC_DELTA3	[7:0]	DDSC_ACC_DELTA[31:24]	设置DDSC_ACC_DELTA。如果DDSC_ MODULUS_EN为高电平时，	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x144	DDSC_ACC_DELTA4	[7:0]	DDSC_ACC_DELTA[39:32]	设置DDSC_ACC_DELTA。如果DDSC_ MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/ DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.	0x0	R/W
0x145	DDSC_ACC_DELTA5	[7:0]	DDSC_ACC_DELTA[47:40]	设置DDSC_ACC_DELTA。如果DDSC_ MODULUS_EN为高电平时，主数据通路NCO频率=fDAC×(DDSC_FTW+DDSC_ACC_DELTA/DDSC_ACC_MODULUS)/2^48。DDSC_ACC_DELTA必须大于0。DDSC_ACC_DELTA必须大于DDSC_ACC _MODULUS。该控制由寄存器0x008中的CHANNEL_PAGE位分页。 / Set DDSC_ACC_DELTA. If DDSC_MODULUS_EN is high, the main datapath NCO frequency =fDAC x (DDSC_FTW +DDSC_ACC_DELTA/	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DDSC_ACC_MODULUS)/ 2^48.DDSC_ACC_DELTA must be greater than 0. DDSC_ACC_DELTA must be greater than DDSC_ACC_MODULUS. This control is paged by the CHANNEL_PAGE bit in Register 0x008.		
0x146	CHNL_GAIN0	[7:0]	CHNL_GAIN[7:0]	设置标称通道增益值。该控制由寄存器0x008中的CHANNEL_PAGE位分页。通道增益=CHNL_GAIN/211。 /Set the nominal channel gain value. This control is paged by the CHANNEL_PAGE bit in Register 0x008. Channel gain = CHNL_GAIN/2^11.	0x0	R/W
0x147	CHNL_GAIN1	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x147	CHNL_GAIN1	[3:0]	CHNL_GAGEN[11:8]	设置标称通道增益值。该控制由寄存器0x008中的CHANNEL_PAGE位分页。通道增益=CHNL_GAIN/211。 /Set the nominal channel gain value. This control is paged by the CHANNEL_PAGE bit in Register 0x008. Channel gain = CHNL_GAIN/2^11.	0x8	R/W
0x148	DC_CAL_TONE0	[7:0]		DC_TEST_INPUT_AMPLITUDE[7:0]直流测试tone振幅。该值可独立设置I通路和Q通路振幅。将这些位设置为0x50FF，以获得满量程tone，并确保的DDSC_EN_DC_INPUT设置为1（寄存器0x130的Bit0）。该控制由寄存器0x008中的CHANNEL_PAGE控制分页。 / DC test tone amplitude.This value can independently set the I-path and Q-path amplitudes.Set these bits to 0x50FF to obtain a full-scale tone, and ensure DDSC_EN_DC_INPUT is set to 1 (Bit 0 of Register 0x130). This control is paged by the CHANNEL_PAGE control in Register 0x008.	0x0	R/W
0x149	DC_CAL_TONE1	[7:0]		DC_TEST_INPUT_AMPLITUDE[15:8]直流测试tone振幅。该值可独立设置I通路和Q通路振幅。将这些位设置为0x50FF，以获得满量程tone，并确保的DDSC_EN_DC_INPUT设置为1（寄存器0x130的Bit0）。该控制由寄存器0x008中的CHANNEL_PAGE控制分页。 / DC test tone amplitude.This value can independently set the I-path and Q-path amplitudes.Set these bits to 0x50FF to obtain a full-scale tone, and ensure	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DDSC_EN_DC_INPUT is set to 1 (Bit 0 of Register 0x130). This control is paged by the CHANNEL_PAGE control in Register 0x008.		
0x14B	PRBS	7	PRBS_GOOD_Q	DAC1良好数据指示器。1检测到正确的PRBS序列。0检测到不正确的序列。滞后；由PRBS_RESET复位为1。 / DAC1 good data indicator. 1: a correct PRBS sequence is detected.0: an incorrect sequence is detected. Latched; reset to 1 by PRBS_RESET.	0x0	R
0x14B	PRBS	6	PRBS_GOOD_I	DAC0良好数据指示器。1检测到正确的PRBS序列。0检测到不正确的序列。滞后；由PRBS_RESET复位为1。 / DAC0 good data indicator. 1: a correct PRBS sequence is detected.0: an incorrect sequence is detected. Latched; reset to 1 by PRBS_RESET.	0x0	R
0x14B	PRBS	5	RESERVED	保留。 / Reserved.	0x0	R
0x14B	PRBS	4	PRBS_INV_Q	DAC1数据反转。0预计数据正常。1预计数据反转。 / DAC1 data inversion. 0: data expected normal.1: data expected inverted.	0x1	R/W
0x14B	PRBS	3	PRBS_INV_I	DAC1数据反转。0预计数据正常。1预计数据反转。 / DAC1 data inversion. 0: data expected normal.1: data expected inverted.	0x0	R/W
0x14B	PRBS	2	PRBS_MODE	选择用于数据总线PRBS测试的PRBS多项式。7位：x7+x6+1。015位：x15+x14+1。1 / Select the PRBS polynomial used for the data bus PRBS test. 0: 7-bit: x^7 + x^6 + 1. 1:15-bit: x^15 + x^14 + 1.	0x0	R/W
0x14B	PRBS	1	PRBS_RESET	重置错误计数器。0正常运行。1重置计数器。 / Reset the error counter.0: normal operation. 1: reset the counter.	0x0	R/W
0x14B	PRBS	0	PRBS_EN	启用PRBS校验器。0禁用。1启用。 /Enable the PRBS checker. 0:disable. 1: enable.	0x0	R/W
0x14C	PRBS_ERROR_I	[7:0]	PRBS_COUNT_IDAC0PRBS	错误计数。 / Error count.	0x0	R
0x14D	PRBS_ERROR_Q	[7:0]	PRBS_COUNT_QDAC1PRBS	错误计数。 / Error count.	0x0	R
0x14E	PRBS_CHANSEL	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x14E	PRBS_CHANSEL	[2:0]	PRBS_CHANSEL	选择PRBS_GOOD_x和PRBS_COUNT_x比特字段回读对应的通道。0为PRBS_COUNT_x和PRBS_GOOD_x（通道0，DAC0）选	0x7	R/W

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				择通道0。1为PRBS_COUNT_x和PRBS_GOOD_x（通道1，DAC0）选择通道1。2为PRBS_COUNT_x和PRBS_GOOD_x（通道2，DAC0）选择通道2。3为PRBS_COUNT_x和PRBS_GOOD_x（通道0，DAC1）选择通道3。4为PRBS_COUNT_x和PRBS_GOOD_x（通道1，DAC1）选择通道4。5为PRBS_COUNT_x和PRBS_GOOD_x（通道2，DAC1）选择通道5。或PRBS_GOOD_x的所有通道，求6 PRBS_COUNT_x的所有通道之和。 / Select the channel corresponding to the PRBS_GOOD_x and PRBS_COUNT_x bit field readback.0: select Channel 0 for PRBS_COUNT_x and PRBS_GOOD_x (Channel 0, DAC0).1: select Channel 1 (Channel 1,DAC0). 2: select Channel 2 (Channel 2, DAC0). 3: select Channel 3(Channel 0, DAC1). 4: select Channel 4 (Channel 1, DAC1). 5:select Channel 5 (Channel 2, DAC1).6: OR of all channels for PRBS_GOOD_x, sum of all channels for PRBS_COUNT_x.		
0x151	DECODE_MODE	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x151	DECODE_MODE	4	MSB_SHUFFLE_ENMSB	shuffle控制。设置=1可启用MSB shuffle，设置=0则禁用MSB shuffle并使用默认（静态）温度计编码。 /Shuffle control. Setting = 1 enables MSB shuffle; setting = 0 disables MSB shuffle and uses the default(static) thermometer coding.	0x0	R/W
0x151	DECODE_MODE	[3:0]	RESERVED	保留。 / Reserved.	0x0	R
0x1DE	SPI_ENABLE	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x1DE	SPI_ENABLE	1	SPI_EN1	启用SPI控制。 / Enable SPI control.	0x1	R/W
0x1DE	SPI_ENABLE	0	SPI_EN0	启用SPI控制。 / Enable SPI control.	0x1	R/W
0x1E2	DDSM_CAL_FTW0	[7:0]	DDSM_CAL_FTW[7:0]	校准累加器的FTW。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / FTW of the calibration accumulator. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x1E3	DDSM_CAL_FTW1	[7:0]	DDSM_CAL_FTW[15:8]	校准累加器的FTW。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / FTW of the calibration accumulator. This control is paged	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				by the MAINDAC_PAGE bit in Register 0x008.		
0x1E4	DDSM_CAL_FTW2	[7:0]	DDSM_CAL_FTW[23:16]	校准累加器的FTW。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / FTW of the calibration accumulator. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x1E5	DDSM_CAL_FTW3	[7:0]	DDSM_CAL_FTW[31:24]	校准累加器的FTW。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 / FTW of the calibration accumulator. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x1E6	DDSM_CAL_MODE_DEF	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x1E6	DDSM_CAL_MODE_DEF	2	DDSM_EN_CAL_ACC	启用时钟校准累加器。必须首先将该位设置为高电平，然后将校准FTW载入寄存器0x1E2至寄存器0x1E5才能生效。该控制由寄存器0x008中的MAINDAC_PAGE位分页。禁用（不打开校准频率累加器的时钟）。0启用（打开校准频率累加器的时钟）。1 /Enable the clock calibration accumulator. This bit must first be set high, and then the calibration FTW loaded into Register 0x1E2 to Register 0x1E5, for it to take effect.This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: disable (do not turn on the calibration frequency accumulator clock). 1: enable (turn on the calibration frequency accumulator clock).	0x0	R/W
0x1E6	DDSM_CAL_MODE_DEF	1	DDSM_EN_CAL_DC_INPUT	启用校准DDS的直流输入。该控制由寄存器0x008中的MAINDAC_PAGE位分页。0数据通路信号复用到最终DDS的输入端。直流多路复用到最终DDS的输入端。1 / Enable the DC input of the calibration DDS. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: the datapath signal is multiplexed to the input of the final DDS. 1: DC is multiplexed to the input of the final DDS.	0x0	R/W
0x1E6	DDSM_CAL_MODE_DEF	0	DDSM_EN_CAL_FREQ_TUNE	仅对DAC0启用按校准频率调谐信号的功能。该控制由寄存器0x008中的MAINDAC_PAGE位分页。0禁用校准频率tuning。1启用校准频率tuning。 / Enable, for DAC0 only,the function of tuning the signal	0x0	R/W

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				per the calibration frequency. This control is paged by the MAINDAC_PAGE bit in Register 0x008. 0: disable calibration frequency tuning. 1: enable calibration frequency tuning.		
0x1E7	DATAPATH_NCO_SYNC_CFG	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x1E7	DATAPATH_NCO_SYNC_CFG	1	ALL_NCO_SYNC_ACK	确保所有激活的NCO均已加载的确认信号。该位是START_NCO_SYNC位（该寄存器的第0位）和NCORST_AFTER_ROT_EN位（寄存器0x03B，第4位）复位NCO方法的确认指示器。该控制由寄存器0x008中的MAINDAC_PAGE位分页。 /Acknowledge signal ensuring that all active NCOs have been loaded.This bit is the acknowledge indicator for the NCO reset methods of the START_NCO_SYNC bit (Bit 0 of this register) and the NCORST_AFTER_ROT_EN bit(Register 0x03B, Bit 4). This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R
0x1E7	DATAPATH_NCO_SYNC_CFG	0	START_NCO_SYNC	用于在SPI位或SYSREF±信号上升沿时启动NCO同步，取决于选择哪一个作为更新触发。接收到触发后，首先加载FTW，然后进行同步。该控制由寄存器0x008中的MAINDAC_PAGE位进行分页。 / Used to start NCO synchronization on an SPI bit or a SYSREF+/- signal rising edge,depending on which is selected as the update trigger. After the trigger is received, the FTW is loaded first,and then synchronization is performed. This control is paged by the MAINDAC_PAGE bit in Register 0x008.	0x0	R/W
0x200	MASTER_PD	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x200	MASTER_PD	0	SERDES_MASTER_PD	关闭整个JESD204B接收器（全部八个通道和偏置）。 / Shut down the entire JESD204B receiver (all eight lanes and the bias).	0x1	R/W
0x201	PHY_PD	[7:0]	PHY_PD	SPI覆盖以关闭单个PHY。第0位控制SERDIN0± PHY。第1位控制SERDIN1± PHY。第2位控制SERDIN2± PHY。第3位控制SERDIN3± PHY。第4位控制SERDIN4± PHY。第5位控制SERDIN5± PHY。第6位控制SERDIN6± PHY。第7位控制	0xEE	R/W

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				SERDIN7± PHY。 / SPI override to shut down an individual PHY. Bit 0 controls the SERDIN0+/- PHY. Bit 1 controls the SERDIN1+/- PHY. Bit 2 controls the SERDIN2+/- PHY. Bit 3 controls the SERDIN3+/- PHY. Bit 4 controls the SERDIN4+/- PHY. Bit 5 controls the SERDIN5+/- PHY. Bit 6 controls the SERDIN6+/- PHY. Bit 7 controls the SERDIN7+/- PHY.		
0x203	GENERIC_PD	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x203	GENERIC_PD	1	PD_	关闭驱动器。0启用输出引脚。1关闭输出引脚。 / Driver shutdown. 0:enable the output pin. 1: shut down the output pin.	0x0	R/W
0x203	GENERIC_PD	0	PD_	关闭驱动器。0启用输出引脚。1关闭输出引脚。 / Driver shutdown. 0:enable the output pin. 1: shut down the output pin.	0x1	R/W
0x206	CDR_RESET	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x206	CDR_RESET	0	CDR_PHY_RESETPHY	复位控制位。将该位设置为1，可在器件运行期间使PHY复位。 / Reset control bit. Setting this bit to 1 resets the PHY while the device is operating.	0x0	R/W
0x210	CBUS_ADDR	[7:0]	SERDES_CBUS_ADDRSERDES	配置控制寄存器，用于设置SERDES配置地址控制。 / Configuration control register, used to set the SERDES configuration address control.	0x0	R/W
0x212	CBUS_WRSTROBE_	[7:0]	SERDES_CBUS_WR0SERDES	配置控制寄存器，用于提交写入的PHY SERDES配置控制。 / Configuration control register, used to commit the written PHY SERDES configuration control.	0x0	R/W
0x213	CBUS_WRSTROBE_	[7:1]	RESERVED	保留。OTHER 0 SERDES_CBUS_WR1 SERDES配置控制寄存器，用于提交写入的SERDES配置控制。 /Reserved. SERDES configuration control register, used to commit the written SERDES configuration control.	0x0	R
0x216	CBUS_WDATA	[7:0]	SERDES_CBUS_DATASERDES	配置控制寄存器，用于设置SERDES配置控制数据。 / Configuration control register, used to set the SERDES configuration control data.	0x0	R/W
0x240	EQ_BOOST_PHY_	[7:6]	EQ_BOOST_PHY3	基于系统插入损耗的PHY 3均衡器设置。3_0 10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 3 equalizer setting based on the system	0x3	R/W

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				insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.		
0x240	EQ_BOOST_PHY_	[5:4]	EQ_BOOST_PHY2	基于系统插入损耗的PHY 2均衡器设置。10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 2 equalizer setting based on the system insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.	0x3	R/W
0x240	EQ_BOOST_PHY_	[3:2]	EQ_BOOST_PHY1	基于系统插入损耗的PHY 1均衡器设置。10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 1 equalizer setting based on the system insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.	0x3	R/W
0x240	EQ_BOOST_PHY_	[1:0]	EQ_BOOST_PHY0	基于系统插入损耗的PHY 0均衡器设置。10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 0 equalizer setting based on the system insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.	0x3	R/W
0x234	CDR_BITINVERSE	[7:0]	SEL_IF_PARDATAINV_DES_RC_CH	输出数据反转位控制。设置PHY x对应的位x，以反转位极性。0不反转。1反转。 / Output data inversion bit control. Set Bit x corresponding to PHY x to invert the bit polarity. 0:do not invert. 1: invert.	0x66	R/W
0x241	EQ_BOOST_PHY_	[7:6]	EQ_BOOST_PHY7	基于系统插入损耗的PHY 7均衡器设置。7_4 10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 7 equalizer setting based on the system insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.	0x3	R/W
0x241	EQ_BOOST_PHY_	[5:4]	EQ_BOOST_PHY6	基于系统插入损耗的PHY 6均衡器设置。10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 6 equalizer setting based on the system insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.	0x3	R/W
0x241	EQ_BOOST_PHY_	[3:2]	EQ_BOOST_PHY5	基于系统插入损耗的PHY 5均衡器设置。10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 5 equalizer setting based on the system insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.	0x3	R/W
0x241	EQ_BOOST_PHY_	[1:0]	EQ_BOOST_PHY4	基于系统插入损耗的PHY 4均衡器设置。10插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 4 equalizer setting based on the system insertion loss. 10: insertion loss <=11 dB. 11: insertion loss > 11 dB.	0x3	R/W

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0x242	EQ_GAIN_PHY_3_0	[7:6]	EQ_GAIN_PHY3	基于系统插入损耗的PHY 3均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 3 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x242	EQ_GAIN_PHY_3_0	[5:4]	EQ_GAIN_PHY2	基于系统插入损耗的PHY 2均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 2 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x242	EQ_GAIN_PHY_3_0	[3:2]	EQ_GAIN_PHY1	基于系统插入损耗的PHY 1均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 1 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x242	EQ_GAIN_PHY_3_0	[1:0]	EQ_GAIN_PHY0	基于系统插入损耗的PHY 0均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 0 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x243	EQ_GAIN_PHY_7_4	[7:6]	EQ_GAIN_PHY7	基于系统插入损耗的PHY 7均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 7 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x243	EQ_GAIN_PHY_7_4	[5:4]	EQ_GAIN_PHY6	基于系统插入损耗的PHY 6均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 6 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x243	EQ_GAIN_PHY_7_4	[3:2]	EQ_GAIN_PHY5	基于系统插入损耗的PHY 5均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 5 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x243	EQ_GAIN_PHY_7_4	[1:0]	EQ_GAIN_PHY4	基于系统插入损耗的PHY 4均衡器增益。01插入损耗≤ 11 dB。11插入损耗> 11 dB。 / PHY 4 equalizer gain based on the system insertion loss.01: insertion loss <= 11 dB. 11:insertion loss > 11 dB.	0x3	R/W
0x244	EQ_FB_PHY_0	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x244	EQ_FB_PHY_0	[4:0]	EQ_PHY_0PHY0		0x19	R/W

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				的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.		
0x245	EQ_FB_PHY_1	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x245	EQ_FB_PHY_1	[4:0]	EQ_PHY1PHY1	的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.	0x19	R/W
0x246	EQ_FB_PHY_2	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x246	EQ_FB_PHY_2	[4:0]	EQ_PHY2PHY2	的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.	0x19	R/W
0x247	EQ_FB_PHY_3	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x247	EQ_FB_PHY_3	[4:0]	EQ_PHY3PHY3	的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.	0x19	R/W
0x248	EQ_FB_PHY_4	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x248	EQ_FB_PHY_4	[4:0]	EQ_PHY4PHY4	的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.	0x19	R/W
0x249	EQ_FB_PHY_5	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x249	EQ_FB_PHY_5	[4:0]	EQ_PHY5PHY5	的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.	0x19	R/W
0x24A	EQ_FB_PHY_6	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x24A	EQ_FB_PHY_6	[4:0]	EQ_PHY6PHY6	的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.	0x19	R/W
0x24B	EQ_FB_PHY_7	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x24B	EQ_FB_PHY_7	[4:0]	EQ_PHY7PHY7	的SERDES均衡器设置。将此控制设置为0x1F，以获得最佳性能。 / SERDES equalizer setting. Set this control to 0x1F for best performance.	0x19	R/W

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0x250	LBT_REG_CNTRL_0	[7:0]	EN_LBT_DES_RC_CH	为每个PHY的所需物理通道启用loopback测试，位x对应PHY x。/Enable loopback test for the required physical lane of each PHY;Bit x corresponds to PHY x.	0x0	R/W
0x251	LBT_REG_CNTRL_1	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x251	LBT_REG_CNTRL_1	1	EN_LBT_HALFRATE_DES_RC	为loopback测试启用半速率模式。如果该位设置为1，则输出数据速率=输入时钟频率的2倍。如果该位设置为0，则输出数据速率=输入时钟频率。 / Enable half-rate mode for loopback test. If this bit is set to 1,the output data rate = 2x the input clock frequency. If this bit is set to 0, the output data rate = the input clock frequency.	0x1	R/W
0x251	LBT_REG_CNTRL_1	0	INIT_LBT_SYNC_DES_RC	将该位从0切换到1，然后再切换回0，启动loopback测试。 / Toggle this bit from 0 to 1 and then back to 0 to start the loopback test.	0x0	R/W
0x253		0	SEL_MODE	_该控制钮决定引脚工作的输出驱动模式。和必须设置为相同的工作模式。0设置为CMOS输出。1设置为LVDS输出。 / This control determines the output drive mode in which the pin operates. Both must be set to the same operating mode. 0: set to CMOS output. 1: set to LVDS output.	0x0	R/W
0x254		0	SEL_MODE	_该控制钮决定引脚工作的输出驱动模式。和必须设置为相同的工作模式。0设置为CMOS输出。1设置为LVDS输出。 / This control determines the output drive mode in which the pin operates. Both must be set to the same operating mode. 0: set to CMOS output. 1: set to LVDS output.	0x0	R/W
0x280	PLL_ENABLE_CTRL	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x280	PLL_ENABLE_CTRL	2	LOLSTICKYCLEAR_LCPLL_RC	清除锁定位丢失。 / Clear lock bit lost.	0x0	R/W
0x280	PLL_ENABLE_CTRL	1	LDSYNTH_LCPLL_RC	脉冲高电平启动VCO校准（无需重启调节器或重新测量温度）。 / Pulse high to start VCO calibration(without restarting the regulator or remeasuring the temperature).	0x0	R/W
0x280	PLL_ENABLE_CTRL	0	SERDES_PLL_STARTUP	将该位设置为1，SERDES电路模块断电。在SERDES配置写入结束时，将该位设置为1。将该位设置为1时，将为SERDES PLL模块上电，并启动	0x1	R/W

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				LDO和校准例程，根据设备中编程的JESD204B模式和插值选项将PLL自动锁定到适当的通道速率。SERDES_PLL_LOCK位（寄存器0x281，位0）在PLL实现锁定时读取1。 / Setting this bit to 1 powers down the SERDES circuit block. At the end of the SERDES configuration writes, set this bit to 1. When this bit is set to 1, the SERDES PLL block is powered up and the LDO and calibration routines are started, automatically locking the PLL to the appropriate lane rate according to the JESD204B mode and interpolation options programmed in the device.The SERDES_PLL_LOCK bit(Register 0x281, Bit 0) reads 1 when the PLL achieves lock.		
0x281	PLL_STATUS	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x281	PLL_STATUS	0	SERDES_PLL_LOCK	该位为高电平时，PLL锁定。 / When this bit is high, the PLL is locked.	0x0	R
0x300	GENERAL_JRX_	[7:4]	RESERVED	保留。CTRL_0 3 LINK_MODE在单链路模式下读回0，在双链路模式下读回1。 / LINK_MODE: reads back 0 in single-link mode and reads back 1 in dual-link mode.	0x0	R
0x300	GENERAL_JRX_	2	LINK_MODE	链路分页。该位选择使用哪个链路寄存器映射。该分页会影响寄存器0x400至寄存器0x4BB。0链接0的QBD0页。1链接1的QBD1页。 / Link paging. This bit selects which link register map is used. This paging affects Register 0x400 to Register 0x4BB. 0: Link 0 QBD0 page. 1: Link 1 QBD1 page.	0x0	R/W
0x300	GENERAL_JRX_	[1:0]	LINK_EN	当所有链路参数编程完毕且所有时钟准备就绪时，这些位将启动JESD204B数字接收器。位0适用于链路0，而位1适用于链路1。链路1仅在双链路模式下可用。 / When all link parameters have been programmed and all clocks are ready, these bits start the JESD204B digital receiver. Bit 0 applies to Link 0 and Bit 1 applies to Link 1. Link 1 is available only in dual-link mode.	0x0	R/W
0x302	DYN_LINK_	[7:6]	RESERVED	保留。LATENCY_0 [5:0] DYN_LINK_动态链路延迟，链路0。链路0的LMFC接收器与LATENCY_0最后到达	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				的LMFC边界之间的延迟，以PCLK周期为单位。 / Dynamic link latency,Link 0. The delay between the Link 0 LMFC receiver and the last arriving LMFC boundary, in PCLK cycles.		
0x303	DYN_LINK_	[7:6]	RESERVED	保留。LATENCY_1 [5:0] DYN_LINK_动态链路延迟，链路0。链路0的LMFC接收器与LATENCY_1最后到达的LMFC边界之间的延迟，以PCLK周期为单位。 / Dynamic link latency,Link 0. The delay between the Link 0 LMFC receiver and the last arriving LMFC boundary, in PCLK cycles.	0x0	R
0x304	LMFC_DELAY_0	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x304	LMFC_DELAY_0	[5:0]	LMFC_DELAY_0	LMFC延迟，链路0。链路0从LMFC到LMFC接收机的延迟，单位为PCLK周期。 / LMFC delay, Link 0. The delay of Link 0 from LMFC to the LMFC receiver, in PCLK cycles.	0x0	R/W
0x305	LMFC_DELAY_1	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x305	LMFC_DELAY_1	[5:0]	LMFC_DELAY_1	LMFC延迟，链路0。链路0从LMFC到LMFC接收机的延迟，单位为PCLK周期。 / LMFC delay, Link 0. The delay of Link 0 from LMFC to the LMFC receiver, in PCLK cycles.	0x0	R/W
0x306	LMFC_VAR_0	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x306	LMFC_VAR_0	[5:0]	LMFC_VAR_0	可变延迟缓冲器，链路0。这些位在从缓冲区读取数据时设置，以便在跨链路和电源周期时保持一致（以PCLK周期为单位）。最大值为0xC。 / Variable delay buffer, Link 0. These bits are set when reading data from the buffer so as to maintain consistency across links and power cycles (in PCLK cycles).The maximum value is 0xC.	0x3F	R/W
0x307	LMFC_VAR_1	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x307	LMFC_VAR_1	[5:0]	LMFC_VAR_1	可变延迟缓冲器，链路0。这些位在从缓冲区读取数据时设置，以便在跨链路和电源周期时保持一致（以PCLK周期为单位）。最大值为0xC。 / Variable delay buffer, Link 0. These bits are set when reading data from the buffer so as to maintain consistency across links and power cycles (in PCLK cycles).The maximum value is 0xC.	0x3F	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x308	XBAR_LN_0_1	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x308	XBAR_LN_0_1	[5:3]	LOGIC_LANE1_SRC	逻辑通道1源。这些位选择映射到逻辑通道1的物理通道。000数据来自SERDIN0±。001数据来自SERDIN1±。010数据来自SERDIN2±。011数据来自SERDIN3±。100数据来自SERDIN4±。101数据来自SERDIN5±。110数据来自SERDIN6±。111数据来自SERDIN7±。 / Logical Lane 1 source. These bits select the physical lane mapped to logical Lane 1. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.	0x1	R/W
0x308	XBAR_LN_0_1	[2:0]	LOGIC_LANE0_SRC	逻辑通道0源。这些位选择映射到逻辑通道0的物理通道。000数据来自SERDIN0±。001数据来自SERDIN1±。010数据来自SERDIN2±。011数据来自SERDIN3±。100数据来自SERDIN4±。101数据来自SERDIN5±。110数据来自SERDIN6±。111数据来自SERDIN7±。 / Logical Lane 0 source. These bits select the physical lane mapped to logical Lane 0. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.	0x0	R/W
0x309	XBAR_LN_2_3	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x309	XBAR_LN_2_3	[5:3]	LOGIC_LANE3_SRC	逻辑通道3源。这些位选择映射到逻辑通道3的物理通道。000数据来自SERDIN0±。001数据来自SERDIN1±。010数据来自SERDIN2±。011数据来自SERDIN3±。100数据来自SERDIN4±。101数据来自SERDIN5±。110数据来自SERDIN6±。111数据来自SERDIN7±。 / Logical Lane 3 source. These bits select the	0x3	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				physical lane mapped to logical Lane 3. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.		
0x309	XBAR_LN_2_3	[2:0]	LOGIC_LANE2_SRC	逻辑通道2源。这些位选择映射到逻辑通道2的物理通道。000数据来自SERDIN0±。001数据来自SERDIN1±。010数据来自SERDIN2±。011数据来自SERDIN3±。100数据来自SERDIN4±。101数据来自SERDIN5±。110数据来自SERDIN6±。111数据来自SERDIN7±。 / Logical Lane 2 source. These bits select the physical lane mapped to logical Lane 2. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.	0x2	R/W
0x30A	XBAR_LN_4_5	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x30A	XBAR_LN_4_5	[5:3]	LOGIC_LANE5_SRC	逻辑通道5源。这些位选择映射到逻辑通道5的物理通道。000数据来自SERDIN0±。001数据来自SERDIN1±。010数据来自SERDIN2±。011数据来自SERDIN3±。100数据来自SERDIN4±。101数据来自SERDIN5±。110数据来自SERDIN6±。111数据来自SERDIN7±。 / Logical Lane 5 source. These bits select the physical lane mapped to logical Lane 5. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.	0x5	R/W
0x30A	XBAR_LN_4_5	[2:0]	LOGIC_LANE4_SRC	逻辑通道4源。这些位选择映射到逻辑通道4的物理通道。000数据来自SERDIN0±。001数据来自	0x4	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				SERDIN1±。010数据来自 SERDIN2±。011数据来自 SERDIN3±。100数据来自 SERDIN4±。101数据来自 SERDIN5±。110数据来自 SERDIN6±。111数据来自 SERDIN7±。 / Logical Lane 4 source. These bits select the physical lane mapped to logical Lane 4. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.		
0x30B	XBAR_LN_6_7	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x30B	XBAR_LN_6_7	[5:3]	LOGIC_LANE7_SRC	逻辑通道7源。这些位选择映射到逻辑通道7的物理通道。000数据来自SERDIN0±。001数据来自 SERDIN1±。010数据来自 SERDIN2±。011数据来自 SERDIN3±。100数据来自 SERDIN4±。101数据来自 SERDIN5±。110数据来自 SERDIN6±。111数据来自 SERDIN7±。 / Logical Lane 7 source. These bits select the physical lane mapped to logical Lane 7. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.	0x7	R/W
0x30B	XBAR_LN_6_7	[2:0]	LOGIC_LANE6_SRC	逻辑通道6源。这些位选择映射到逻辑通道6的物理通道。000数据来自SERDIN0±。001数据来自 SERDIN1±。010数据来自 SERDIN2±。011数据来自 SERDIN3±。100数据来自 SERDIN4±。101数据来自 SERDIN5±。110数据来自 SERDIN6±。111数据来自 SERDIN7±。 / Logical Lane 6 source. These bits select the physical lane mapped to logical Lane 6. 000: data from SERDIN0+/-.001: data from SERDIN1+/-. 010:data from SERDIN2+/-. 011: data	0x6	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				from SERDIN3+/-. 100: data from SERDIN4+/-. 101: data from SERDIN5+/-. 110: data from SERDIN6+/-. 111: data from SERDIN7+/-.		
0x30C	FIFO_STATUS_REG_0	[7:0]	LANE_FIFO_FULL	比特x对应来自SERDINx±的数据的FIFO满标志。 / Bit x corresponds to the FIFO full flag of the data from SERDINx+/-.	0x0	R
0x30D	FIFO_STATUS_REG_1	[7:0]	LANE_FIFO_EMPTY	比特x对应来自SERDINx±的数据的FIFO空标志。 / Bit x corresponds to the FIFO empty flag of the data from SERDINx+/-.	0x0	R
0x311	SYNCOUT_GEN_0	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x311	SYNCOUT_GEN_0	3	EOMF_MASK_1	屏蔽QBD1的多帧末端(EOMF)。在多帧同步损失时发出。0多帧损失时不发出。1多帧损失时发出。 / Mask the end of multiframe (EOMF) of QBD1. Asserted on loss of multiframe synchronization. 0: not asserted on multiframe loss. 1:asserted on multiframe loss.	0x0	R/W
0x311	SYNCOUT_GEN_0	2	EOMF_MASK_0	屏蔽从来自QBD0的EOMF。在多帧同步损失时，发出。0多帧损失时不发出。1多帧损失时发出。 / Mask the EOMF from QBD0. Asserted on loss of multiframe synchronization. 0:not asserted on multiframe loss. 1:asserted on multiframe loss.	0x0	R/W
0x311	SYNCOUT_GEN_0	1	EOF_MASK_1	屏蔽来自QBD1的EOF。在帧同步损失时发出。0帧损失时不发出。1帧损失时发出。 / Mask the EOF from QBD1. Asserted on loss of frame synchronization. 0: not asserted on frame loss. 1: asserted on frame loss.	0x0	R/W
0x311	SYNCOUT_GEN_0	0	EOF_MASK_0	屏蔽来自QBD0的EOF。在帧同步损失时发出。0帧丢失时不置有效。1帧损失时置有效。 / Mask the EOF from QBD0. Asserted on loss of frame synchronization. 0: not asserted on frame loss. 1: asserted on frame loss.	0x0	R/W
0x312	SYNCOUT_GEN_1	[7:4]	SYNC_ERR_DUR	用于同步错误报告的低电平持续时间。持续时间=(0.5+代码)PCLK周期。为了最接近地匹配指定值，请将这些位尽可能设置为f/2 PCLK周期。这些位由和共享。 / Low-level duration used for synchronization error reporting. Duration = (0.5 +code) PCLK cycles. To match the	0x0	R/W

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				specified value as closely as possible, set these bits as close as possible to f/2 PCLK cycles. These bits are shared by [names blank in source text layer] and [blank].		
0x312	SYNCOUT_GEN_1	[3:0]	RESERVED	保留。 / Reserved.	0x0	R/W
0x315	PHY_PRBS_TEST_EN	[7:0]	PHY_TEST_EN	通过取消时钟控制启用PHY BER。0禁用PHY测试。1启用PHY测试。/Enable PHY BER by un-gating the clock control. 0: disable PHY test. 1:enable PHY test.	0x0	R/W
0x316	PHY_PRBS_TEST_	7	RESERVED	保留。CTRL [6:4]PHY_SRC_ERR_CNT 000报告通道0错误计数。001报告通道1错误计数。010报告通道2错误计数。011报告通道3错误计数。100报告通道4错误计数。101报告通道5错误计数。110报告通道6错误计数。111报告通道7错误计数。 / PHY_SRC_ERR_CNT:000: report Lane 0 error count. 001:report Lane 1 error count. 010:report Lane 2 error count. 011:report Lane 3 error count. 100:report Lane 4 error count. 101:report Lane 5 error count. 110:report Lane 6 error count. 111:report Lane 7 error count.	0x0	R
0x316	PHY_PRBS_TEST_	[3:2]	PHY_PRBS_PAT_SEL	为PHY BER测试选择PRBS模式。PRBS7。00 PRBS15。01 PRBS31。10未使用。11 / Select the PRBS mode for the PHY BER test. 00:PRBS7. 01: PRBS15. 10: PRBS31. 11:unused. [values re-aligned in printed order]	0x0	R/W
0x316	PHY_PRBS_TEST_	1	PHY_TEST_START	启动和停止PHY PRBS测试。0测试未启动。1测试启动。 / Start and stop the PHY PRBS test. 0: test not started. 1: test started.	0x0	R/W
0x316	PHY_PRBS_TEST_	0	PHY_TEST_RESET	重置PHY PRBS测试状态机和错误计数器。0不重置。1重置。 / Reset the PHY PRBS test state machine and error counter. 0: do not reset. 1:reset.	0x0	R/W
0x317	PHY_PRBS_TEST_THRESHOLD_LOBITS	[7:0]	PHY_PRBS_THRESHOLD_LOBITS	用于设置 PHY PRBS 测试错误标志的24 位阈值的位[7:0]。 / Bits[7:0]used to set the 24-bit threshold of the PHY PRBS test error flag.	0x0	R/W
0x318	PHY_PRBS_TEST_THRESHOLD_MIDBITS	[7:0]	PHY_PRBS_THRESHOLD_MIDBITS	用于设置 PHY PRBS 测试错误标志的24 位阈值的位[15:8]。 / Bits[15:8]used to set the 24-bit threshold of the PHY PRBS test error flag.	0x0	R/W

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0x319	PHY_PRBS_TEST_THRESHOLD_HIBITS	[7:0]	PHY_PRBS_THRESHOLD_HIBITS	用于设置 PHY PRBS 测试错误标志的24 位阈值的位[23:16]。 / Bits[23:16]used to set the 24-bit threshold of the PHY PRBS test error flag.	0x0	R/W
0x31A	PHY_PRBS_TEST_ERRCNT_LOBITS	[7:0]	PHY_PRBS_ERR_CNT_LOBITS	所选通道的报告的24位PHY BER错误计数的位[7:0]。 / Bits[7:0] of the reported 24-bit PHY BER error count of the selected lane.	0x0	R
0x31B	PHY_PRBS_TEST_ERRCNT_MIDBITS	[7:0]	PHY_PRBS_ERR_CNT_MIDBITS	所选通道的报告的24位PHY BER错误计数的位[15:8]。 / Bits[15:8] of the reported 24-bit PHY BER error count of the selected lane.	0x0	R
0x31C	PHY_PRBS_TEST_ERRCNT_HIBITS	[7:0]	PHY_PRBS_ERR_CNT_HIBITS	所选通道的报告的24位PHY BER错误计数的位[23:16]。 / Bits[23:16] of the reported 24-bit PHY BER error count of the selected lane.	0x0	R
0x31D	PHY_PRBS_TEST_STATUS	[7:0]	PHY_PRBS_PASS	报告每个通道的PHY误码率通过/未通过情况。当通道x通过时，位x为高电平。 / Report the PHY bit error rate pass/fail of each lane. When Lane x passes, Bit x is high.	0xFF	R
0x31E	PHY_DATA_SNAPSHOT_CTRL	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x31E	PHY_DATA_SNAPSHOT_CTRL	1	PHY_GRAB_MODE	该位决定是否使用触发器抓取数据。0设置PHY_GRAB_DATA时抓取数据。位1错误时抓取数据。 / This bit determines whether a trigger is used to grab data. 0: grab data when PHY_GRAB_DATA is set. 1:grab data on error.	0x0	R/W
0x31E	PHY_DATA_SNAPSHOT_CTRL	0	PHY_GRAB_DATA	将该位从0转换为1，会导致逻辑存储来自一个通道的当前接收到的数据。 / Converting this bit from 0 to 1 causes the logic to store the currently received data from one lane.	0x0	R/W
0x31F	PHY_SNAPSHOT_DATA_BYTE0	[7:0]	PHY_SNAPSHOT_D	当前接收到的数据。ATA_BYTE0代表PHY_SNAPSHOT_DATA[7:0]。 /Currently received data.Represents PHY_SNAPSHOT_DATA[7:0].	0x0	R
0x320	PHY_SNAPSHOT_DATA_BYTE1	[7:0]	PHY_SNAPSHOT_DATA_BYTE1	当前接收到的数据。代表PHY_SNAPSHOT_DATA[15:8]。 / Currently received data.Represents PHY_SNAPSHOT_DATA[15:8].	0x0	R
0x321	PHY_SNAPSHOT_DATA_BYTE2	[7:0]	PHY_SNAPSHOT_DATA_BYTE2	当前接收到的数据。代表PHY_SNAPSHOT_DATA[23:16]。/Currently received data.	0x0	R

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				Represents PHY_SNAPSHOT_DATA[23:16].		
0x322	PHY_SNAPSHOT_DATA_BYTE3	[7:0]	PHY_SNAPSHOT_DATA_BYTE3	当前接收到的数据。代表PHY_SNAPSHOT_DATA[31:24]。/Currently received data.Represents PHY_SNAPSHOT_DATA[31:24].	0x0	R
0x323	PHY_SNAPSHOT_DATA_BYTE4	[7:0]	PHY_SNAPSHOT_DATA_BYTE4	当前接收到的数据。代表PHY_SNAPSHOT_DATA[39:32]。115 / Currently received data.Represents PHY_SNAPSHOT_DATA[39:32].	0x0	R
0x32C	SHORT_TPL_TEST_0	[7:4]	SHORT_TPL_SP_SEL	短传输层样本选择。从特定DAC中选择检查哪个样本。0000样本0。0001样本1。0010样本2。0011样本3。0100样本4。0101样本5。0110样本6。0111样本7。1000样本8。1001样本9。1010样本10。1011样本11。1100样本12。1101样本13。1110样本14。1111样本15。 / Short transport layer sample selection.Select which sample from a specific DAC to check. 0000:Sample 0. 0001: Sample 1. 0010:Sample 2. 0011: Sample 3. 0100:Sample 4. 0101: Sample 5. 0110:Sample 6. 0111: Sample 7. 1000:Sample 8. 1001: Sample 9. 1010:Sample 10. 1011: Sample 11. 1100:Sample 12. 1101: Sample 13. 1110:Sample 14. 1111: Sample 15.	0x0	R/W
0x32C	SHORT_TPL_TEST_0	[3:2]	SHORT_TPL_CHAN_SEL	短传输层测试通道选择。选择要测试DACx channelizer的哪个子信道。00通道0。01通道1。10频道2. / Short transport layer test channel selection. Select which subchannel of the DACx channelizer to test. 00:Channel 0. 01: Channel 1. 10:Channel 2. [text ends here in source]	0x0	R/W
0x32C	SHORT_TPL_TEST_0	1	SHORT_TPL_TEST_RESET	重置短传输层测试。重置短传输层测试结果。不重置。0重置。1 / Reset the short transport layer test. Reset the short transport layer test results. 0: do not reset. 1: reset.	0x0	R/W
0x32C	SHORT_TPL_TEST_0	0	SHORT_TPL_TEST_EN	启用短传输层测试。0禁用。1启用。 / Enable the short transport layer test. 0: disable. 1: enable.	0x0	R/W
0x32D	SHORT_TPL_TEST_1	[7:0]	SHORT_TPL_REF_SP_LSB	短传输层参考样本，LSB。该位字段是短传输层测试期间预期DAC样本的低八位，用于与JESD204B接收机输	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				出端接收到的样本进行比较。 / Short transport layer reference sample,LSB. This bit field is the low eight bits of the expected DAC sample during the short transport layer test, used for comparison with the sample received at the JESD204B receiver output.		
0x32E	SHORT_TPL_TEST_2	[7:0]	SHORT_TPL_REF_SP_MSB	短传输层测试参考样本，MSB。该位字段是短传输层测试期间预期DAC样本的高八位，用于与JESD204B接收机输出端的接收样本进行比较。 /Short transport layer test reference sample, MSB. This bit field is the high eight bits of the expected DAC sample during the short transport layer test, used for comparison with the sample received at the JESD204B receiver output.	0x0	R/W
0x32F	SHORT_TPL_TEST_3	7	SHORT_TPL_LINK_SEL	用于在双链路JESD204B模式下运行STPL。选择STPL测试是对寻址到DAC0通道器/数据通路（链路0）的样本执行，还是对DAC1通道器/数据通路（链路1）的样本执行。测试链路0样本。0测试链路1样本。1 / Used to run STPL in dual-link JESD204B mode. Selects whether the STPL test is performed on the samples addressed to the DAC0 channelizer/datapath (Link 0) or the samples of the DAC1 channelizer/datapath (Link 1). 0:test Link 0 samples. 1: test Link 1 samples.	0x0	R/W
0x32F	SHORT_TPL_TEST_3	6	SHORT_TPL_IQ_SAMPLE_SEL	对channelizer的复数子通道（I或Q），选择进行测试的数据流（路径）。0选择数据流I测试。1选择数据流Q测试。 / For the complex subchannel (I or Q) of the channelizer, select the data stream(path) to test. 0: select data stream I for test. 1: select data stream Q for test.	0x0	R/W
0x32F	SHORT_TPL_TEST_3	[5:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x32F	SHORT_TPL_TEST_3	0	SHORT_TPL_FAIL	短传输层测试失败。该位显示所选DAC样本是否与短传输层测试的预期样本相匹配。如果匹配，则测试通过。否则，测试失败。测试通过。0测试失败。1 / Short transport layer test fail. This bit shows whether the selected DAC sample matches the expected sample of the short	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				transport layer test. If it matches,the test passes; otherwise, the test fails. 0: test passed. 1: test failed.		
0x334	JESD_BIT_INVERSE_	[7:0]	JESD_BIT_INVERSE	逻辑通道反转。该控制的每一位都会反转来自一CTRL个特定JESD204B接收机PHY的JESD204B反序列化数据。将位x设置为高电平可反转逻辑通道x上的JESD204B反序列化数据。 / Logical lane inversion. Each bit of this control inverts the JESD204B deserialized data from a specific JESD204B receiver PHY.Setting Bit x high inverts the JESD204B deserialized data on logical Lane x.	0x0	R/W
0x400	DID_REG	[7:0]	DID_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x401	BID_REG	[7:0]	BID_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x402	LID0_REG	7	RESERVED	保留。 / Reserved.	0x0	R
0x402	LID0_REG	6	ADJDIR_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x402	LID0_REG	5	PHADJ_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x402	LID0_REG	[4:0]	LL_LID0	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x403	SCR_L_REG	7	SCR_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。0加扰已禁用。1加扰已启用。 /ILAS configuration on receive Lane 0. This control is paged by the	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				LINK_PAGE control in Register 0x300. 0: scrambling disabled. 1:scrambling enabled.		
0x403	SCR_L_REG	[6:5]	RESERVED	保留。 / Reserved.	0x0	R
0x403	SCR_L_REG	[4:0]	L_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。00000每个转换装置的通道数00001每个转换设备的通道数00010每个转换设备的通道数00011每个转换设备的通道数 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x404	F_REG	[7:0]	F_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。0每帧1个八位字节。1每帧2个八位字节。10每帧3个八位字节。11每帧4个八位字节。 / ILAS configuration on receive Lane 0.This control is paged by the LINK_PAGE control in Register 0x300. 0: 1 octet per frame. 1: 2 octets per frame. 10: 3 octets per frame. 11: 4 octets per frame.	0x0	R
0x405	K_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x405	K_REG	[4:0]	K_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。00000默认值。11111每个多帧为32帧。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 00000: default value. 11111: 32 frames per multiframe.	0x0	R
0x406	M_REG	[7:0]	M_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x407	CS_N_REG	[7:6]	CS_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x407	CS_N_REG	5	RESERVED	保留。 / Reserved.	0x0	R
0x407	CS_N_REG	[4:0]	N_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.		
0x408	NP_REG	[7:5]	SUBCLASSV_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x408	NP_REG	[4:0]	NP_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x409	S_REG	[7:5]	JESDV_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。JESD204A. 000 JESD204B.001 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 000: JESD204A. 001:JESD204B.	0x0	R
0x409	S_REG	[4:0]	S_RD_1	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x40A	HD_CF_REG	7	HD_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。0低密度模式。1高密度模式。 /ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: low-density mode. 1:high-density mode.	0x0	R
0x40A	HD_CF_REG	[6:5]	RESERVED	保留。 / Reserved.	0x0	R
0x40A	HD_CF_REG	[4:0]	CF_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x40B	RES1_REG	[7:0]	RES1_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x40C	RES2_REG	[7:0]	RES2_RD	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x40D	CHECKSUM0_REG	[7:0]	LL_FCHK0	接收通道0上的ILAS配置，该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS configuration on receive Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x40E	COMPSUM0_REG	[7:0]	LL_FCMP0	计算通道0的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x412	LID1_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x412	LID1_REG	[4:0]	LL_LID1	接收通道1上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 1. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x415	CHECKSUM1_REG	[7:0]	LL_FCHK1	接收通道1上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 1. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x416	COMPSUM1_REG	[7:0]	LL_FCMP1	计算通道1的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x41A	LID2_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x41A	LID2_REG	[4:0]	LL_LID2	接收通道2上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 2. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x41D	CHECKSUM2_REG	[7:0]	LL_FCHK2	接收通道2上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 2. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x41E	COMPSUM2_REG	[7:0]	LL_FCMP2	计算通道2的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x422	LID3_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x422	LID3_REG	[4:0]	LL_LID3	接收通道3上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 3. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x425	CHECKSUM3_REG	[7:0]	LL_FCHK3	接收通道3上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 3. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x426	COMPSUM3_REG	[7:0]	LL_FCMP3	计算通道3的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x42A	LID4_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x42A	LID4_REG	[4:0]	LL_LID4	接收通道4上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 4. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x42D	CHECKSUM4_REG	[7:0]	LL_FCHK4	接收通道4上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 4. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x42E	COMPSUM4_REG	[7:0]	LL_FCMP4	计算通道4的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x432	LID5_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x432	LID5_REG	[4:0]	LL_LID5	接收通道5上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 5. This control is	0x0	R

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				paged by the LINK_PAGE control in Register 0x300.		
0x435	CHECKSUM5_REG	[7:0]	LL_FCHK5	接收通道5上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 5. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x436	COMPSUM5_REG	[7:0]	LL_FCMP5	计算通道5的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x43A	LID6_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x43A	LID6_REG	[4:0]	LL_LID6	接收通道6上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 6. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x43D	CHECKSUM6_REG	[7:0]	LL_FCHK6	接收通道6上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 6. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x43E	COMPSUM6_REG	[7:0]	LL_FCMP6	计算通道6的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x442	LID7_REG	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x442	LID7_REG	[4:0]	LL_LID7	接收通道7上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 7. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x445	CHECKSUM7_REG	[7:0]	LL_FCHK7	接收通道7上的ILAS LID配置。该控制由寄存器0x300中的LINK_PAGE控制分页。 / ILAS LID configuration on receive Lane 7. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x446	COMPSUM7_REG	[7:0]	LL_FCMP7	计算通道7的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Computed checksum of Lane 7. This control is paged by the	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				LINK_PAGE control in Register 0x300.		
0x450	ILS_DID	[7:0]	DID	器件（链路）标识号。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Device (link) identification number. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x451	ILS_BID	[7:0]	BID	Bank ID，扩展至DID。该控制由寄存器0x300中的LINK_PAGE控制分页。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Bank ID, extension of the DID. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.	0x0	R/W
0x452	ILS_LID0	7	RESERVED	保留。 / Reserved.	0x0	R
0x452	ILS_LID0	6	ADJDIR	调整DAC LMFC的方向。根据JESD204B第8.3节的规定，在链路通道0上接收链路信息。仅支持链路0。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Adjust the direction of the DAC LMFC. Per Section 8.3 of JESD204B, link information is received on link Lane 0. Link 0 only supported. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x452	ILS_LID0	5	PHADJ	向DAC发出相位调整请求。仅支持链路0。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Issue a phase adjustment request to the DAC. Link 0 only supported. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x452	ILS_LID0	[4:0]	LID0	通道标识号（链路内）。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行时不得更改。 / Lane identification number (within the link). This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475, Bit 3),	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				and must not be changed during normal operation.		
0x453	ILS_SCR_L	7	SCR	为链路启用加扰。该控制由寄存器0x300中的LINK_PAGE控制分页。0解扰已禁用。1解扰已启用。 / Enable scrambling for the link. This control is paged by the LINK_PAGE control in Register 0x300. 0:descrambling disabled. 1:descrambling enabled.	0x1	R/W
0x453	ILS_SCR_L	[6:5]	RESERVED	保留。 / Reserved.	0x0	R
0x453	ILS_SCR_L	[4:0]	L_1	每个转换器的通道数（减1）。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Number of lanes per converter (minus 1). This control is paged by the LINK_PAGE control in Register 0x300.	0x7	R/W
0x454	ILS_F	[7:0]	F_1	每通道每帧的字节数（减1）。此控制由寄存器0x300中的LINK_PAGE控制分页。 / Number of octets per lane per frame (minus 1). This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x455	ILS_K	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x455	ILS_K	[4:0]	K_1	每个多帧的帧数（减1）。该控制由寄存器0x300中的LINK_PAGE控制分页。11111每个多帧32帧。/Number of frames per multiframe(minus 1). This control is paged by the LINK_PAGE control in Register 0x300. 11111: 32 frames per multiframe.	0x1F	R/W
0x456	ILS_M	[7:0]	M_1	每个链路的子通道数（减1）。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Number of subchannels per link (minus 1). This control is paged by the LINK_PAGE control in Register 0x300.	0x1	R/W
0x457	ILS_CS_N	[7:6]	CS	每个样本的控制位数。仅支持链路0。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Number of control bits per sample. Link 0 only supported. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x457	ILS_CS_N	5	RESERVED	保留。 / Reserved.	0x0	R
0x457	ILS_CS_N	[4:0]	N_1	转换器分辨率（减1）。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Converter resolution (minus 1). This control is paged by the	0xF	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				LINK_PAGE control in Register 0x300.		
0x458	ILS_NP	[7:5]	SUBCLASSV	器件subclass版本。该控制由寄存器0x300中的LINK_PAGE控制分页。000 Subclass0。001 Subclass1。 /Device subclass version. This control is paged by the LINK_PAGE control in Register 0x300. 000:Subclass 0. 001: Subclass 1.	0x0	R/W
0x458	ILS_NP	[4:0]	NP_1	每个样本的总位数（减1）。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Total number of bits per sample (minus 1). This control is paged by the LINK_PAGE control in Register 0x300.	0xF	R/W
0x459	ILS_S	[7:5]	JESDVJESD204	版本。该控制由寄存器0x300中的LINK_PAGE控制分页。000 JESD204A. 001 JESD204B. / Version. This control is paged by the LINK_PAGE control in Register 0x300. 000: JESD204A. 001:JESD204B.	0x0	R/W
0x459	ILS_S	[4:0]	S_1	每个帧周期每个转换器的样本数（减1）。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Number of samples per converter per frame cycle (minus 1). This control is paged by the LINK_PAGE control in Register 0x300.	0x1	R/W
0x45A	ILS_HD_CF	7	HD	该控制由寄存器0x300中的LINK_PAGE控制分页。0低密度模式。1高密度模式。 / This control is paged by the LINK_PAGE control in Register 0x300. 0: low-density mode. 1: high-density mode.	0x1	R
0x45A	ILS_HD_CF	[6:5]	RESERVED	保留。 / Reserved.	0x0	R
0x45A	ILS_HD_CF	[4:0]	CF	每个样本的控制位数。仅支持链路0。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Number of control bits per sample. Link 0 only supported. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x45B	ILS_RES1	[7:0]	RES1	保留字段1。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Reserved field 1. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x45C	ILS_RES2	[7:0]	RES2	保留字段2。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Reserved	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				field 2. This control is paged by the LINK_PAGE control in Register 0x300.		
0x45D	ILS_CHECKSUM	[7:0]	FCHK0	计算的链路配置校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行期间不得更改。 /Computed link configuration checksum. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475, Bit 3),and must not be changed during normal operation.	0x0	R/W
0x46C	LANE_DESKEW	7	ILD7	通道7的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 7.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x46C	LANE_DESKEW	6	ILD6	通道6的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 6.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x46C	LANE_DESKEW	5	ILD5	通道5的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 5.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x46C	LANE_DESKEW	4	ILD4	通道4的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 4.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x46C	LANE_DESKEW	3	ILD3	通道3的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 3.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.		
0x46C	LANE_DESKEW	2	ILD2	通道2的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 2.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x46C	LANE_DESKEW	1	ILD1	通道1的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 1.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x46C	LANE_DESKEW	0	ILD0	通道0的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 0.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x46D	BAD_DISPARITY	7	BDE7	通道7的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /Disparity error status of Lane 7.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.	0x0	R
0x46D	BAD_DISPARITY	6	BDE6	通道6的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /Disparity error status of Lane 6.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.	0x0	R
0x46D	BAD_DISPARITY	5	BDE5	通道5的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				Disparity error status of Lane 5.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.		
0x46D	BAD_DISPARITY	4	BDE4	通道4的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /Disparity error status of Lane 4.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.	0x0	R
0x46D	BAD_DISPARITY	3	BDE3	通道3的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /Disparity error status of Lane 3.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.	0x0	R
0x46D	BAD_DISPARITY	2	BDE2	通道2的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /Disparity error status of Lane 2.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.	0x0	R
0x46D	BAD_DISPARITY	1	BDE1	通道1的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /Disparity error status of Lane 1.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.	0x0	R
0x46D	BAD_DISPARITY	0	BDE0	通道0的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<错误阈值(ETH)[7:0]值。1错误计数≥ETH[7:0]值。 /Disparity error status of Lane 0.This control is paged by the	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				LINK_PAGE control in Register 0x300. 0: error count < error threshold (ETH)[7:0] value. 1: error count >= ETH[7:0] value.		
0x46E	NOT_IN_TABLE	7	NIT7	通道7的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x46E	NOT_IN_TABLE	6	NIT6	通道6的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x46E	NOT_IN_TABLE	5	NIT5	通道5的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x46E	NOT_IN_TABLE	4	NIT4	通道4的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x46E	NOT_IN_TABLE	3	NIT3	通道3的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x46E	NOT_IN_TABLE	2	NIT2	通道2的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误	0x0	R

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				计数≥ETH[7:0]值。 / Not-in-table error status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.		
0x46E	NOT_IN_TABLE	1	NIT1	通道1的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x46E	NOT_IN_TABLE	0	NIT0	通道0的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x46F	UNEXPECTED_KCHAR	7	UEK7	通道7意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 7.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x46F	UNEXPECTED_KCHAR	6	UEK6	通道6意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 6.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x46F	UNEXPECTED_KCHAR	5	UEK5	通道5意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 5.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				value. 1: error count >= ETH[7:0]value.		
0x46F	UNEXPECTED_KCHAR	4	UEK4	通道4意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 4.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x46F	UNEXPECTED_KCHAR	3	UEK3	通道3意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 3.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x46F	UNEXPECTED_KCHAR	2	UEK2	通道2意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 2.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x46F	UNEXPECTED_KCHAR	1	UEK1	通道1意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 1.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x46F	UNEXPECTED_KCHAR	0	UEK0	通道0意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 0.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R

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地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x470	CODE_GRP_SYNC	7	CGS7	通道7码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x470	CODE_GRP_SYNC	6	CGS6	通道6码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x470	CODE_GRP_SYNC	5	CGS5	通道5码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x470	CODE_GRP_SYNC	4	CGS4	通道4码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x470	CODE_GRP_SYNC	3	CGS3	通道3码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x470	CODE_GRP_SYNC	2	CGS2	通道2码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x470	CODE_GRP_SYNC	1	CGS1	通道1码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.		
0x470	CODE_GRP_SYNC	0	CGS0	通道0码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x471		6	FS6	通道6帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 6.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x471		5	FS5	通道5帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 5.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x471		4	FS4	通道4帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 4.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x471		3	FS3	通道3帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 3.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x471		2	FS2	通道2帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 2.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x471		1	FS1	通道1帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 1.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x471		0	FS0	通道0帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 0.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x472	GOOD_CHECKSUM	7	CKS7	通道7的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x472	GOOD_CHECKSUM	6	CKS6	通道6的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x472	GOOD_CHECKSUM	5	CKS5	通道5的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x472	GOOD_CHECKSUM	4	CKS4	通道4的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x472	GOOD_CHECKSUM	3	CKS3	通道3的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.		
0x472	GOOD_CHECKSUM	2	CKS2	通道2的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x472	GOOD_CHECKSUM	1	CKS1	通道1的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x472	GOOD_CHECKSUM	0	CKS0	通道0的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x473	INIT_LANE_SYNC	7	ILS7	通道7初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x473	INIT_LANE_SYNC	6	ILS6	通道6初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x473	INIT_LANE_SYNC	5	ILS5	通道5初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x473	INIT_LANE_SYNC	4	ILS4	通道4初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x473	INIT_LANE_SYNC	3	ILS3	通道3初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x473	INIT_LANE_SYNC	2	ILS2	通道2初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x473	INIT_LANE_SYNC	1	ILS1	通道1初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x473	INIT_LANE_SYNC	0	ILS0	通道0初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x475	CTRLREG0	[7:4]	RESERVED	保留。 / Reserved.	0x0	R/W
0x475	CTRLREG0	3	SOFTRSTQBD	软复位。高电平有效同步复位。将所有硬件复位至开机状态。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Soft reset. Active-high synchronous reset. Resets all hardware to the power-on state.This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x475	CTRLREG0	2	FORCESYNCREQ		0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				应用程序发出的同步请求指令。高电平有效。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Synchronization request command issued by the application. Active high. This control is paged by the LINK_PAGE control in Register 0x300.		
0x475	CTRLREG0	1	RESERVED	保留。 / Reserved.	0x0	R
0x475	CTRLREG0	0	REPL_FRM_ENA	设置该电平输入后，可替换接收到的错误帧。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行时不得更改。 / After this level input is set, the received error frames can be replaced. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475, Bit 3),and must not be changed during normal operation.	0x1	R/W
0x476	CTRLREG1	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x476	CTRLREG1	4	QUAL_RDERR	同时出现不在表(NIT)和运行差异(RD)错误的报错行为。该控制由寄存器0x300中的LINK_PAGE控制分页。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。NIT对RD误差没有影响。0 NIT错误与RD错误同时出现。1 / Error reporting behavior when a not-in-table (NIT)error and a running disparity (RD)error occur simultaneously. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation. 0: NIT has no effect on the RD error. 1: NIT error and RD error occur simultaneously.	0x1	R/W
0x476	CTRLREG1	[3:1]	RESERVED	保留。 / Reserved.	0x0	R/W
0x476	CTRLREG1	0	FCHK_N	校验和计算方法。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行时不得更改。0校验和的计算方法是将JESD204B标准第8.3节表20中定义的链路配置表中的各个	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				字段相加。1校验和的计算方法是将包含打包链路配置字段的寄存器求和（寄存器0x450至寄存器0x45A之和，modulo 256）。 / Checksum calculation method. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475, Bit 3),and must not be changed during normal operation. 0: the checksum calculation method is to sum the fields in the link configuration table defined in Table 20 of Section 8.3 of the JESD204B standard. 1: the checksum calculation method is to sum the registers containing the packed link configuration fields(the sum of Register 0x450 to Register 0x45A, modulo 256).		
0x477	CTRLREG2	7	ILS_MODE	当该位设置为1时，数据链路层测试模式启用。CGS模式之后是一个永久的ILAS序列。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行期间不得更改。0正常模式。1 CGS模式之后是一个永久的ILAS序列。 / When this bit is set to 1, the data link layer test mode is enabled. The CGS mode is followed by a permanent ILAS sequence.This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475, Bit 3),and must not be changed during normal operation. 0: normal mode.1: the CGS mode is followed by a permanent ILAS sequence.	0x0	R/W
0x477	CTRLREG2	6	RESERVED	保留。 / Reserved.	0x0	R/W
0x477	CTRLREG2	5	REPDATATEST	使用JTSPAT模式启用重复数据测试。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行时不得更改。 / Enable repeated data test using JTSPAT mode. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				(Register 0x475, Bit 3), and must not be changed during normal operation.		
0x477	CTRLREG2	4	QUETESTERR	队列测试错误模式。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行时不得更改。当该位=0时，多个通道上同时出现的错误将作为0一个错误报告。当该位=1和REPDATATEST=1。所有通道检测到1的错误都会被记录在计数器中，并依次在上发出信号。 / Queue test error mode. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475, Bit 3),and must not be changed during normal operation. When this bit =0, errors occurring simultaneously on multiple lanes are reported as one error. When this bit = 1 and REPDATATEST = 1, all errors detected on all lanes are recorded in the counter and signaled sequentially.	0x0	R/W
0x477	CTRLREG2	3	AR_ECNTR	错误计数器自动复位。当AR_ECNTR=1时，导致表征的错误计数器自动复位为0。所有其他计数器不受影响。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行时不得更改。 / Error counter automatic reset. When AR_ECNTR= 1, the characterized error counter is automatically reset to 0. All other counters are unaffected. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.	0x0	R/W
0x477	CTRLREG2	[2:0]	RESERVED	保留。 / Reserved.	0x0	R
0x478	KVAL	[7:0]	KSYNC	ILAS期间的4×K多帧数。该控制由寄存器0x300中的LINK_PAGE控制分页。只有在QBD处于软复位（寄存器0x475，位3）时才能对该信号进行编程，正常运行时不得更改。 /Number of 4x K multiframes during	0x1	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				ILAS. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475, Bit 3),and must not be changed during normal operation.		
0x47C	ERRORTHRES	[7:0]	ETH	错误计数器阈值。当因BD、NIT或UEK错误而发送错误或中断时，这些位将被设置。该控制由寄存器0x300中LINK_PAGE控制分页。只有在QBD处于软复位状态时，才能对该信号进行编程。（寄存器0x475，位3），正常运行时不得更改。 / Error counter threshold. These bits are set when an error or interrupt is sent due to a BD, NIT or UEK error. This control is paged by the LINK_PAGE control in Register 0x300. This signal can be programmed only when the QBD is in soft reset (Register 0x475,Bit 3), and must not be changed during normal operation.	0xFF	R/W
0x47D	SYNC_ASSERT_MASK	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x47D	SYNC_ASSERT_MASK	[2:0]	SYNC_ASSERT_MASK	的表征能够屏蔽BD、NIT和UEK错误条件。该控制由寄存器0x300中的LINK_PAGE控制分页。高电平有效，表征能够分别屏蔽BD、NIT和UEK错误条件。当任何通道中的错误计数器达到错误阈值计数ETH[7:0]，且相应的SYNC_ASSERT_MASK位被设置时，将被表征。屏蔽位如下（与其他错误计数控制和错误计数器的位序列相反）：第2位=差分错误(BDE)。第1位=不在表错误(NIT)。第0位=意外K字符错误(UEK)。 / Characterization can mask the BD, NIT and UEK error conditions. This control is paged by the LINK_PAGE control in Register 0x300. Active high;characterization can separately mask the BD, NIT and UEK error conditions. When the error counter in any lane reaches the error threshold count ETH[7:0] and the corresponding SYNC_ASSERT_MASK bit is set, it is characterized. The mask bits are as follows (in the reverse bit order of the other error count controls and error counters): Bit 2 = disparity error (BDE). Bit 1 = not-in-table error (NIT). Bit 0 = unexpected K-	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				character error (UEK). [leading character of the description is a fragment in the source]		
0x480	ECNT_CTRL0	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x480	ECNT_CTRL0	[5:3]	ECNT_ENA0	启用链路0的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Link 0. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W
0x480	ECNT_CTRL0	[2:0]	ECNT_RST0	重置0线路的错误计数器。此控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第2位=差分错误(BDE)。第1位=不在表中错误(NIT)。第0位=意外K字符错误(UEK)。 / Reset the error counter of Link 0. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 =disparity error (BDE). Bit 1 = not-in-table error (NIT). Bit 0 =unexpected K-character error(UEK).	0x7	R/W
0x481	ECNT_CTRL1	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x481	ECNT_CTRL1	[5:3]	ECNT_ENA1	启用通道1的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W
0x481	ECNT_CTRL1	[2:0]	ECNT_RST1	重置通道1的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Reset the error counter of Lane 1. This control is paged by the	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).		
0x482	ECNT_CTRL2	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x482	ECNT_CTRL2	[5:3]	ECNT_ENA2	启用通道2的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W
0x482	ECNT_CTRL2	[2:0]	ECNT_RST2	重置通道2的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第2位=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Reset the error counter of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x7	R/W
0x483	ECNT_CTRL3	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x483	ECNT_CTRL3	[5:3]	ECNT_ENA3	启用通道3的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W
0x483	ECNT_CTRL3	[2:0]	ECNT_RST3	重置通道3的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第2位=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				(BDE)。130 / Reset the error counter of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 = unexpected K-character error (UEK). Bit 1 = not-in-table error (NIT). Bit 0 = disparity error (BDE).		
0x484	ECNT_CTRL4	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x484	ECNT_CTRL4	[5:3]	ECNT_ENA4	启用通道4的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W
0x484	ECNT_CTRL4	[2:0]	ECNT_RST4	重置通道4的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第2位=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Reset the error counter of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x7	R/W
0x485	ECNT_CTRL5	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x485	ECNT_CTRL5	[5:3]	ECNT_ENA5	启用通道5的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W
0x485	ECNT_CTRL5	[2:0]	ECNT_RST5	重置通道5的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				页。每个通道的计数器寻址如下：第2位=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Reset the error counter of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).		
0x486	ECNT_CTRL6	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x486	ECNT_CTRL6	[5:3]	ECNT_ENA6	启用通道6的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W
0x486	ECNT_CTRL6	[2:0]	ECNT_RST6	重置通道6的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第2位=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Reset the error counter of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x7	R/W
0x487	ECNT_CTRL7	[7:6]	RESERVED	保留。 / Reserved.	0x0	R
0x487	ECNT_CTRL7	[5:3]	ECNT_ENA7	启用通道7的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第5位=意外K字符错误(UEK)。第4位=不在表错误(NIT)。第3位=差异错误(BDE)。 / Enable the error counter of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 5 =unexpected K-character error(UEK). Bit 4 = not-in-table error(NIT). Bit 3 = disparity error (BDE).	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x487	ECNT_CTRL7	[2:0]	ECNT_RST7	重置通道7的错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。每个通道的计数器寻址如下：第2位=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Reset the error counter of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x7	R/W
0x488	ECNT_TCH0	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x488	ECNT_TCH0	[2:0]	ECNT_TCH0	通道0错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold enable of the Lane 0 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.	0x7	R/W
0x489	ECNT_TCH1	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x489	ECNT_TCH1	[2:0]	ECNT_TCH1	通道1错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。	0x7	R/W

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地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold enable of the Lane 1 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.		
0x48A	ECNT_TCH2	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x48A	ECNT_TCH2	[2:0]	ECNT_TCH2	通道2错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold enable of the Lane 2 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x48B	ECNT_TCH3	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x48B	ECNT_TCH3	[2:0]	ECNT_TCH3	通道3错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold enable of the Lane 3 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.	0x7	R/W
0x48C	ECNT_TCH4	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x48C	ECNT_TCH4	[2:0]	ECNT_TCH4	通道4错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold enable of the Lane 4 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.		
0x48D	ECNT_TCH5	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x48D	ECNT_TCH5	[2:0]	ECNT_TCH5	通道5错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold enable of the Lane 5 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.	0x7	R/W
0x48E	ECNT_TCH6	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x48E	ECNT_TCH6	[2:0]	ECNT_TCH6	通道6错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold	0x7	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				enable of the Lane 6 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.		
0x48F	ECNT_TCH7	[7:3]	RESERVED	保留。 / Reserved.	0x0	R
0x48F	ECNT_TCH7	[2:0]	ECNT_TCH7	通道7错误计数器的终端计数保持使能。该控制由寄存器0x300中的LINK_PAGE控制分页。设置后，指定计数器在达到0xFF时，将保持该终端计数值，直至用户重置计数器。否则，指定计数器将翻转。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。只能在QBD处于软复位（寄存器0x475，位3）时对该信号进行编程，在正常运行期间不得更改。 / Terminal count hold enable of the Lane 7 error counter.This control is paged by the LINK_PAGE control in Register 0x300. When set, the specified counter holds the terminal count value when it reaches 0xFF until the user resets the counter;otherwise, the specified counter rolls over. The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).This signal can be programmed only when the QBD is in soft reset(Register 0x475, Bit 3), and must not be changed during normal operation.	0x7	R/W
0x490	ECNT_STAT0	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x490	ECNT_STAT0	3	LANE_ENA0	该输出指示是否启用了通道0。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				whether Lane 0 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.		
0x490	ECNT_STAT0	[2:0]	ECNT_TCR0	通道0错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 0 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x0	R
0x491	ECNT_STAT1	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x491	ECNT_STAT1	3	LANE_ENA1	该输出指示是否启用了通道1。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates whether Lane 1 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x491	ECNT_STAT1	[2:0]	ECNT_TCR1	通道1错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 1 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).		
0x492	ECNT_STAT2	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x492	ECNT_STAT2	3	LANE_ENA2	该输出指示是否启用了通道2。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates whether Lane 2 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x492	ECNT_STAT2	[2:0]	ECNT_TCR2	通道2错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 2 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x0	R
0x493	ECNT_STAT3	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x493	ECNT_STAT3	3	LANE_ENA3	该输出指示是否启用了通道3。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				whether Lane 3 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.		
0x493	ECNT_STAT3	[2:0]	ECNT_TCR3	通道3错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 3 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x0	R
0x494	ECNT_STAT4	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x494	ECNT_STAT4	3	LANE_ENA4	该输出指示是否启用了通道4。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates whether Lane 4 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x494	ECNT_STAT4	[2:0]	ECNT_TCR4	通道4错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 4 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).		
0x495	ECNT_STAT5	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x495	ECNT_STAT5	3	LANE_ENA5	该输出指示是否启用了通道5。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates whether Lane 5 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x495	ECNT_STAT5	[2:0]	ECNT_TCR5	通道5错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 5 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x0	R
0x496	ECNT_STAT6	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x496	ECNT_STAT6	3	LANE_ENA6	该输出指示是否启用了通道6。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				whether Lane 6 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.		
0x496	ECNT_STAT6	[2:0]	ECNT_TCR6	通道6错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 6 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).	0x0	R
0x497	ECNT_STAT7	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x497	ECNT_STAT7	3	LANE_ENA7	该输出指示是否启用了通道7。该控制由寄存器0x300中的LINK_PAGE控制分页。 / This output indicates whether Lane 7 is enabled. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R
0x497	ECNT_STAT7	[2:0]	ECNT_TCR7	通道7错误计数器的终端计数达到指示器。该控制由寄存器0x300中的LINK_PAGE控制分页。当相应计数器的终端计数值达到0xFF时，将这些位设为1。如果设置了ECNT_TCHx，则相应计数器的终端计数值将保持不变，直到用户重置计数器；否则，计数器翻转并继续计数。每个通道的计数器寻址如下：位2=意外K字符错误(UEK)。第1位=不在表错误(NIT)。第0位=差异错误(BDE)。 / Terminal count reached indicator of the Lane 7 error counter. This control is paged by the LINK_PAGE control in Register 0x300. When the terminal	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				count value of the corresponding counter reaches 0xFF, these bits are set to 1. If ECNT_TCHx is set,the terminal count value of the corresponding counter remains unchanged until the user resets the counter; otherwise, the counter rolls over and continues counting.The counter addressing of each lane is as follows: Bit 2 =unexpected K-character error(UEK). Bit 1 = not-in-table error(NIT). Bit 0 = disparity error (BDE).		
0x4B0	LINK_STATUS0	7	BDE0	通道0的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B0	LINK_STATUS0	6	NIT0	通道0的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B0	LINK_STATUS0	5	UEK0	通道0的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 0.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x4B0	LINK_STATUS0	4	ILD0	通道0的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 0.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B0	LINK_STATUS0	3	ILS0	通道0的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				Initial lane synchronization status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.		
0x4B0	LINK_STATUS0	2	CKS0	通道0的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B0	LINK_STATUS0	1	FS0	通道0的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 0.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B0	LINK_STATUS0	0	CGS0	通道0的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 0. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B1	LINK_STATUS1	7	BDE1	通道1的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B1	LINK_STATUS1	6	NIT1	通道1的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B1	LINK_STATUS1	5	UEK1	通道1的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 1.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.		
0x4B1	LINK_STATUS1	4	ILD1	通道1的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 1.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B1	LINK_STATUS1	3	ILS1	通道1的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B1	LINK_STATUS1	2	CKS1	通道1的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B1	LINK_STATUS1	1	FS1	通道1的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 1.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B1	LINK_STATUS1	0	CGS1	通道1的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 1. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B2	LINK_STATUS2	7	BDE2	通道2的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				ETH[7:0] value. 1: error count >=ETH[7:0] value.		
0x4B2	LINK_STATUS2	6	NIT2	通道2的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B2	LINK_STATUS2	5	UEK2	通道2的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 2.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x4B2	LINK_STATUS2	4	ILD2	通道2的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 2.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B2	LINK_STATUS2	3	ILS2	通道2的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B2	LINK_STATUS2	2	CKS2	通道2的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B2	LINK_STATUS2	1	FS2	通道2的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 2.This control is paged by the LINK_PAGE control in Register	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				0x300. 0: synchronization lost. 1:synchronization achieved.		
0x4B2	LINK_STATUS2	0	CGS2	通道2的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 2. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B3	LINK_STATUS3	7	BDE3	通道3的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B3	LINK_STATUS3	6	NIT3	通道3的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B3	LINK_STATUS3	5	UEK3	通道3的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 3.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x4B3	LINK_STATUS3	4	ILD3	通道3的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 3.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B3	LINK_STATUS3	3	ILS3	通道3的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 3. This control is paged by the LINK_PAGE control in Register	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				0x300. 0: synchronization lost. 1:synchronization achieved.		
0x4B3	LINK_STATUS3	2	CKS3	通道3的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B3	LINK_STATUS3	1	FS3	通道3的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 3.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B3	LINK_STATUS3	0	CGS3	通道3的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 3. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B4	LINK_STATUS4	7	BDE4	通道4的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B4	LINK_STATUS4	6	NIT4	通道4的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B4	LINK_STATUS4	5	UEK4	通道4的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 4.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				value. 1: error count >= ETH[7:0]value.		
0x4B4	LINK_STATUS4	4	ILD4	通道4的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 4.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B4	LINK_STATUS4	3	ILS4	通道4的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B4	LINK_STATUS4	2	CKS4	通道4的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B4	LINK_STATUS4	1	FS4	通道4的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 4.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B4	LINK_STATUS4	0	CGS4	通道4的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 4. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B5	LINK_STATUS5	7	BDE5	通道5的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x4B5	LINK_STATUS5	6	NIT5	通道5的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B5	LINK_STATUS5	5	UEK5	通道5的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 5.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x4B5	LINK_STATUS5	4	ILD5	通道5的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 5.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B5	LINK_STATUS5	3	ILS5	通道5的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B5	LINK_STATUS5	2	CKS5	通道5的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B5	LINK_STATUS5	1	FS5	通道5的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 5.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x4B5	LINK_STATUS5	0	CGS5	通道5的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 5. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B6	LINK_STATUS6	7	BDE6	通道6的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B6	LINK_STATUS6	6	NIT6	通道6的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B6	LINK_STATUS6	5	UEK6	通道6的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 6.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R
0x4B6	LINK_STATUS6	4	ILD6	通道6的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 6.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B6	LINK_STATUS6	3	ILS6	通道6的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x4B6	LINK_STATUS6	2	CKS6	通道6的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B6	LINK_STATUS6	1	FS6	通道6的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 6.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B6	LINK_STATUS6	0	CGS6	通道6的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 6. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B7	LINK_STATUS7	7	BDE7	通道7的差异错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Disparity error status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B7	LINK_STATUS7	6	NIT7	通道7的不在表错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Not-in-table error status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: error count <ETH[7:0] value. 1: error count >=ETH[7:0] value.	0x0	R
0x4B7	LINK_STATUS7	5	UEK7	通道7的意外K字符错误状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0错误计数<ETH[7:0]值。1错误计数≥ETH[7:0]值。 / Unexpected K-character error status of Lane 7.This control is paged by the LINK_PAGE control in Register 0x300. 0: error count < ETH[7:0]value. 1: error count >= ETH[7:0]value.	0x0	R

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x4B7	LINK_STATUS7	4	ILD7	通道7的通道间纠偏状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0纠偏失败。1纠偏成功。 /Inter-lane deskew status of Lane 7.This control is paged by the LINK_PAGE control in Register 0x300. 0: deskew failed. 1: deskew succeeded.	0x0	R
0x4B7	LINK_STATUS7	3	ILS7	通道7的初始通道同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 /Initial lane synchronization status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B7	LINK_STATUS7	2	CKS7	通道7的计算校验和状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0校验和不正确。1校验和正确。 / Computed checksum status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: checksum incorrect. 1:checksum correct.	0x0	R
0x4B7	LINK_STATUS7	1	FS7	通道7的帧同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Frame synchronization status of Lane 7.This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B7	LINK_STATUS7	0	CGS7	通道7的码组同步状态。该控制由寄存器0x300中的LINK_PAGE控制分页。0丢失同步。1实现同步。 / Code group synchronization status of Lane 7. This control is paged by the LINK_PAGE control in Register 0x300. 0: synchronization lost. 1:synchronization achieved.	0x0	R
0x4B8	JESD_IRQ_ENABLEA	7	EN_BDE	差分错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。 /Disparity error counter. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4B8	JESD_IRQ_ENABLEA	6	EN_NIT	不在表错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。 /Not-in-table error counter. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4B8	JESD_IRQ_ENABLEA	5	EN_UEK		0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				意外K字符错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Unexpected K-character error counter. This control is paged by the LINK_PAGE control in Register 0x300.		
0x4B8	JESD_IRQ_ENABLEA	4	EN_ILD	通道间纠偏。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Inter-lane deskew. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4B8	JESD_IRQ_ENABLEA	3	EN_ILS	初始通道同步。该控制由寄存器0x300中的LINK_PAGE控制分页。 /Initial lane synchronization. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4B8	JESD_IRQ_ENABLEA	2	EN_CKS	良好校验和。该位比较两个校验和：发送端在ILAS期间通过链路发送的校验和，以及接收端根据发送端通过链路发送的ILAS数据计算的校验和。校验和IRQ只查看发送器发送的数据，而不查看编程到寄存器0x45D的校验和。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Good checksum. This bit compares two checksums: the checksum sent by the transmitter over the link during ILAS, and the checksum computed by the receiver from the ILAS data sent by the transmitter over the link. The checksum IRQ only looks at the data sent by the transmitter,and does not look at the checksum programmed into Register 0x45D.This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4B8	JESD_IRQ_ENABLEA	1	EN_FS	帧同步。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Frame synchronization. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4B8	JESD_IRQ_ENABLEA	0	EN_CGS	码组同步。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Code group synchronization. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4B9	JESD_IRQ_ENABLEB	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x4B9	JESD_IRQ_ENABLEB	0	EN_ILAS	配置不匹配（仅检查0号通道）。ILAS IRQ比较接收器获得的两组ILAS数据。第一组数据是发送器通过	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				JESD204B链路发送的ILAS数据。第二组数据是通过SPI（寄存器0x450至寄存器0x45D）编程到接收器的ILAS数据。如果有任何的数据不同，都会触发IRQ。所有ILAS数据，包括校验和，都要进行比较。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Configuration mismatch (Lane 0 checked only). The ILAS IRQ compares two sets of ILAS data obtained by the receiver. The first set is the ILAS data sent by the transmitter over the JESD204B link. The second set is the ILAS data programmed into the receiver via SPI (Register 0x450 to Register 0x45D). If any data differs, an IRQ is triggered. All ILAS data, including the checksum, is compared. This control is paged by the LINK_PAGE control in Register 0x300.		
0x4BA	JESD_IRQ_STATUSA	7	IRQ_BDE	差异错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。 /Disparity error counter. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BA	JESD_IRQ_STATUSA	6	IRQ_NIT	不在表错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。 /Not-in-table error counter. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BA	JESD_IRQ_STATUSA	5	IRQ_UEK	意外K字符错误计数器。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Unexpected K-character error counter. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BA	JESD_IRQ_STATUSA	4	IRQ_ILD	通道间纠偏。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Inter-lane deskew. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BA	JESD_IRQ_STATUSA	3	IRQ_ILS	初始车道同步。该控制由寄存器0x300中的LINK_PAGE控制分页。 /Initial lane synchronization. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BA	JESD_IRQ_STATUSA	2	IRQ_CKS	校验和正确。该控制由寄存器0x300中的LINK_PAGE控制分页。 /Checksum correct. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x4BA	JESD_IRQ_STATUSA	1	IRQ_FS	帧同步。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Frame synchronization. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BA	JESD_IRQ_STATUSA	0	IRQ_CGS	码组同步。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Code group synchronization. This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BB	JESD_IRQ_STATUSB	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x4BB	JESD_IRQ_STATUSB	0	IRQ_ILAS	配置不匹配（仅对链路0进行检查）。该控制由寄存器0x300中的LINK_PAGE控制分页。 / Configuration mismatch (checked for Link 0 only). This control is paged by the LINK_PAGE control in Register 0x300.	0x0	R/W
0x4BC	IRQ_OUTPUT_MUX_JESD	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x4BC	IRQ_OUTPUT_MUX_JESD	0	MUX_JESD_IRQ	选择哪个IRQ引脚连接到JESD204B源。将IRQ触发信号发送至引脚。0将IRQ触发信号发送至引脚。1 / Select which IRQ pin is connected to the JESD204B source. 0: send the IRQ trigger signal to the IRQ0 pin. 1:send the IRQ trigger signal to the IRQ1 pin. [pin names restored per Section 4 context; the pin glyphs are missing from the source text layer]	0x0	R/W
0x580	BE_SOFT_OFF_GAIN_CTRL	7	BE_SOFT_OFF_GAIN_EN	必须为1才能使用软关闭/打开。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Must be 1 to use soft shutdown/ startup.This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x580	BE_SOFT_OFF_GAIN_CTRL	[6:3]	RESERVED	保留。 / Reserved.	0x0	R
0x580	BE_SOFT_OFF_GAIN_CTRL	[2:0]	BE_GAIN_RAMP_RATE	设置斜率。在2(CODE+8)DAC时钟周期内，增益以32步从0升至1（或从1升至0）。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Set the ramp. Within 2^(CODE+8) DAC clock cycles, the gain ramps from 0 to 1 (or from 1 to 0) in 32 steps. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x581	BE_SOFT_OFF_ENABLE	7	ENA_SHORT_PAERR_SOFTOFF	启用短PA错误软关断。该控制由寄存器0x008中的MAINDAC_PAGE控制分	0x1	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				页。 / Enable short PA error soft shutdown. This control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x581	BE_SOFT_OFF_ENABLE	6	ENA_LONG_PAERR_SOFTOFF	启用长PA错误软关闭。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Enable long PA error soft shutdown. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x1	R/W
0x581	BE_SOFT_OFF_ENABLE	[5:4]	RESERVED	保留。 / Reserved.	0x0	R
0x581	BE_SOFT_OFF_ENABLE	3	ENA_JESD_ERR_SOFTOFF	启用JESD204B侧边错误软关闭。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Enable JESD204B side error soft shutdown. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x581	BE_SOFT_OFF_ENABLE	2	ROTATE_SOFT_OFF_EN	设置为1时，同步逻辑翻转触发DAC输出软关闭。寄存器0x03B的第0位也必须为高电平。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / When set to 1, a synchronization logic rotation triggers the DAC output soft shutdown. Bit 0 of Register 0x03B must also be high. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x1	R/W
0x581	BE_SOFT_OFF_ENABLE	1	TXEN_SOFT_OFF_EN	设置为1时，TXENx下降沿触发DAC输出软关断。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /When set to 1, a TXENx falling edge triggers the DAC output soft shutdown. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x1	R/W
0x581	BE_SOFT_OFF_ENABLE	0	SPI_SOFT_OFF_EN	当增益为1时，强制软关断。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Force soft shutdown when the gain is 1. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x582	BE_SOFT_ON_ENABLE	7	SPI_SOFT_ON_EN	当增益为0时，强制软启动。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Force soft startup when the gain is 0. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x582	BE_SOFT_ON_ENABLE	6	LONG_LEVEL_SOFTON_EN	设置为1时，该位启用长电平软开启。该控制由寄存器0x008中的	0x1	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				MAINDAC_PAGE控制分页。 / When set to 1, this bit enables long-level soft startup. This control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x582	BE_SOFT_ON_ENABLE	[5:0]	RESERVED	保留。 / Reserved.	0x0	R/W
0x583	LONG_PA_THRES_LSB	[7:0]	LONG_PA_THRESHOLD[7:0]	用于比较的长平均功率阈值。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Long average power threshold used for comparison.This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x584	LONG_PA_THRES_MSB	[7:5]	RESERVED	保留。 / Reserved.	0x0	R
0x584	LONG_PA_THRES_MSB	[4:0]	LONG_PA_THRESHOLD[12:8]	用于比较的长平均功率阈值。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Long average power threshold used for comparison.This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x585	LONG_PA_CONTROL	7	LONG_PA_ENABLE	启用长平均功率计算和错误检测。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Enable long average power calculation and error detection. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x585	LONG_PA_CONTROL	[6:4]	RESERVED	保留。 / Reserved.	0x0	R
0x585	LONG_PA_CONTROL	[3:0]	LONG_PA_AVG_TIME	设置长PA平均时间长度。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。平均时间=29+LONG_PA_AVG_TIME（PA时钟周期）。PA时钟周期的计算公式如下：如果主插值>1×，则PA时钟周期=4×主插值×DAC时钟周期。如果通道插值>1×，则PA时钟周期=8×主插值×DAC时钟周期。否则，PA时钟周期=32×DAC时钟周期。 / Set the long PA averaging time length. This control is paged by the MAINDAC_PAGE control in Register 0x008. Averaging time = 2^(9 +LONG_PA_AVG_TIME) (PA clock cycles). The PA clock cycle is calculated as follows: if the main interpolation > 1x, the PA clock cycle = 4 x main interpolation x DAC clock cycle; if the channel interpolation > 1x, the PA clock cycle = 8 x main interpolation x	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				DAC clock cycle ; otherwise, the PA clock cycle = 32 x DAC clock cycle.		
0x586	LONG_PA_POWER_LSB	[7:0]	LONG_PA_POWER[7:0]	长平均功率回读。数据总线检测到的功率=I2+Q2。数据总线计算仅使用I和Q数据总线采样的6个MSB。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Long average power readback. The power detected on the data bus = I^2 + Q^2. The data bus calculation uses only the 6 MSBs of the I and Q data bus samples. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R
0x587	LONG_PA_POWER_	[7:5]	RESERVED	保留。MSB [4:0]LONG_PA_POWER[12:8]长平均功率回读。数据总线检测到的功率=I2+Q2。数据总线计算仅使用I和Q数据总线采样的6个MSB。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Long average power readback. The power detected on the data bus = I^2 + Q^2. The data bus calculation uses only the 6 MSBs of the I and Q data bus samples. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R
0x588	SHORT_PA_THRES_	[7:0]	SHORT_PA_THRESHOLD[7:0]	用于比较的短平均功率阈值。该控制由寄存器LSB 0x008中的MAINDAC_PAGE控制分页。 / Short average power threshold used for comparison. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x589	SHORT_PA_THRES_	[7:5]	RESERVED	保留。MSB / Reserved.	0x0	R
0x589	SHORT_PA_THRES_	[4:0]	SHORT_PA_THRESHOLD[12:8]	用于比较的短平均功率阈值。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Short average power threshold used for comparison.This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x58A	SHORT_PA_CONTROL	7	SHORT_PA_ENABLE	启用短路平均功率计算和错误检测。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Enable short average power calculation and error detection [source wording]. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
0x58A	SHORT_PA_CONTROL	[6:2]	RESERVED	保留。 / Reserved.	0x0	R
0x58A	SHORT_PA_CONTROL	[1:0]	SHORT_PA_AVG_TIME	设置短PA平均长度。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。平均时间=2SHORT_PA_AVG_TIME（PA时钟周期）。PA时钟周期的计算公式如下：如果主插值>1×，则PA时钟周期=4×主插值×DAC时钟周期。如果通道插值>1×，则PA时钟周期=8×主插值×DAC时钟周期。否则，PA时钟周期=32×DAC时钟周期。 / Set the short PA averaging length. This control is paged by the MAINDAC_PAGE control in Register 0x008. Averaging time =2^SHORT_PA_AVG_TIME (PA clock cycles). The PA clock cycle is calculated as follows: if the main interpolation > 1x, the PA clock cycle = 4 x main interpolation x DAC clock cycle; if the channel interpolation > 1x, the PA clock cycle = 8 x main interpolation x DAC clock cycle ; otherwise, the PA clock cycle = 32 x DAC clock cycle.	0x0	R/W
0x58B	SHORT_PA_POWER_	[7:0]	SHORT_PA_LSBPOWER[7:0]	短平均功率回读。数据总线检测到的功率=I2+Q2。数据总线计算仅使用I和Q数据总线采样的6个MSB。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Short average power readback. The power detected on the data bus = I^2 + Q^2. The data bus calculation uses only the 6 MSBs of the I and Q data bus samples. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R
0x58C	SHORT_PA_POWER_	[7:5]	RESERVED	保留。MSB [4:0] SHORT_PA_短平均功率回读。数据总线检测到的功率POWER[12:8] =I2+Q2。数据总线计算仅使用I和Q数据总线采样的6个MSB。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Short average power readback. The power detected on the data bus =I^2 + Q^2. The data bus calculation uses only the 6 MSBs of the I and Q data bus samples. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R
0x58D	TXEN_SM_0	[7:1]	RESERVED	保留。 / Reserved.	0x1	R/W
0x58D	TXEN_SM_0	0	ENA_TXENSM		0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				启用TXEN状态机。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Enable the TXEN state machine. This control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x596	BLANKING_CTRL	[7:4]	RESERVED	保留。 / Reserved.	0x0	R
0x596	BLANKING_CTRL	3	SPI_TXEN	如果ENA_SPI_TXEN（寄存器的第2位）=1，则寄存器的值就是TXENx状态的值。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / If ENA_SPI_TXEN (Bit 2 of the register) = 1, the value of the register is the value of the TXENx state. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x596	BLANKING_CTRL	2	ENA_SPI_TXEN	通过寄存器0x008中的MAINDAC_PAGE控制来分页。 / Paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x596	BLANKING_CTRL	[1:0]	RESERVED	保留。 / Reserved.	0x0	R
0x597	JESD_PA_INT0	[7:0]	JESD_PA_INT_CNTRL[7:0]	每一位都能启用一个JESD204B PA中断。第8位=CGS。第7位=帧同步。第6位=良好校验和。第5位=初始通道同步。第4位=通道间纠偏。第3位=差分错误计数器。第2位=NIT错误计数器。第1位=UEK错误计数器。第0位=通道FIFO溢出或下溢。 / Each bit enables one JESD204B PA interrupt. Bit 8 = CGS. Bit 7 = frame synchronization. Bit 6 = good checksum. Bit 5 = initial lane synchronization. Bit 4 = inter-lane deskew. Bit 3 = disparity error counter. Bit 2 = NIT error counter.Bit 1 = UEK error counter. Bit 0 =lane FIFO overflow or underflow.	0x0	R/W
0x598	JESD_PA_INT1	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x598	JESD_PA_INT1	0	JESD_PA_INT_CNTRL[8]	每一位都能启用一个JESD204B PA中断。第8位=CGS。第7位=帧同步。第6位=良好校验和。第5位=初始通道同步。第4位=通道间纠偏。第3位=差分错误计数器。第2位=NIT错误计数器。第1位=UEK错误计数器。第0位=通道FIFO溢出或下溢。 / Each bit enables one JESD204B PA interrupt. Bit 8 = CGS. Bit 7 = frame synchronization. Bit 6 = good checksum. Bit 5 = initial lane synchronization. Bit 4 = inter-lane	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				deskew. Bit 3 = disparity error counter. Bit 2 = NIT error counter.Bit 1 = UEK error counter. Bit 0 =lane FIFO overflow or underflow.		
0x599	TXEN_FLUSH_CTRL0	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x599	TXEN_FLUSH_CTRL0	0	SPI_FLUSH_EN	启用数据通路刷新。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 / Enable datapath flush. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x1	R/W
0x705	NVM_LOADER_EN	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x705	NVM_LOADER_EN	0	NVM_BLR_EN	启用引导加载程序。启动加载程序完成或失败时，该位自清零。 / Enable the boot loader. This bit self-clears when the boot loading completes or fails.	0x0	R/W
0x790	DACPLL_PDCTRL0	7	PLL_PD5	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x790	DACPLL_PDCTRL0	[6:4]	PLL_PD4	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x790	DACPLL_PDCTRL0	3	PLL_PD3	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x790	DACPLL_PDCTRL0	2	PLL_PD2	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x790	DACPLL_PDCTRL0	1	PLL_PD1	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the	0x1	R/W

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				PLL is used, keep this value at the default (0).		
0x790	DACPLL_PDCTRL0	0	PLL_PD0	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x791	DACPLL_PDCTRL1	[7:5]	RESERVED	保留。 / Reserved.	0x0	R/W
0x791	DACPLL_PDCTRL1	4	PLL_PD10	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x791	DACPLL_PDCTRL1	3	PLL_PD9	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x791	DACPLL_PDCTRL1	2	PLL_PD8	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x791	DACPLL_PDCTRL1	1	PLL_PD7	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x791	DACPLL_PDCTRL1	0	PLL_PD6	PLL断电控制。如果旁路PLL，则将该位写入1。如果使用PLL，则将该值保持为默认值（0）。 / PLL power-down control. If the PLL is bypassed, write this bit to 1. If the PLL is used, keep this value at the default (0).	0x0	R/W
0x792	DACPLL_CTRL0	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x792	DACPLL_CTRL0	1	D_CAL_RESET	重置VCO校准。 / Reset the VCO calibration.	0x1	R/W
0x792	DACPLL_CTRL0	0		d_reset_vco_div将其设置为高电平时，VCO输出分频器处于复位状态。	0x0	R/W

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				其效果是关闭ADC时钟驱动器的输入（和输出）。 / d_reset_vco_div:when set high, the VCO output divider is in reset. Its effect is to turn off the input (and output) of the ADC clock driver.		
0x793	DACPLL_CTRL1	[7:2]	RESERVED	保留。 / Reserved.	0x0	R
0x793	DACPLL_CTRL1	[1:0]		M_DIVIDER-1 PFD的可编程预分频值（以n-1表示）。M_DIVIDER=PLL参考时钟/PFD频率。为获得最佳频谱性能，请在允许的PFD范围内选择一个高PFD频率的M分频器设置。0除以1。1除以2。10除以3。11除以4。 / Programmable prescaler value of the PFD, M_DIVIDER-1 (in n-1 notation). M_DIVIDER = PLL reference clock/PFD frequency. For best spectral performance, select an M divider setting with a high PFD frequency within the allowed PFD range. 0: divide by 1. 1: divide by 2. 10: divide by 3. 11: divide by 4.	0x0	R/W
0x794	DACPLL_CTRL2	[7:6]	RESERVED	保留。 / Reserved.	0x0	R/W
0x794	DACPLL_CTRL2	[5:0]	DACPLL_CP	电荷泵电流控制。电荷泵电流=100μA+代码×100μA。 / Charge pump current control. Charge pump current = 100 uA + code x 100 uA.	0x4	R/W
0x795	DACPLL_CTRL3	[7:4]	RESERVED	保留。 / Reserved.	0x0	R/W
0x795	DACPLL_CTRL3	[3:0]	D_CP_CALBITSDAC	PLL优化控制 / PLL optimization control.	0x8	R/W
0x796	DACPLL_CTRL4	[7:4]	PLL_CTRL0DAC	PLL优化控制 / PLL optimization control.	0xD	R/W
0x796	DACPLL_CTRL4	[3:0]	RESERVED	保留。 / Reserved.	0x2	R/W
0x797	DACPLL_CTRL5	[7:6]	RESERVED	保留。 / Reserved.	0x0	R/W
0x797	DACPLL_CTRL5	[5:0]	PLL_CTRL1DAC	PLL优化控制 / PLL optimization control.	0x20	R/W
0x798	DACPLL_CTRL6	7	RESERVED	保留。 / Reserved.	0x0	R
0x798	DACPLL_CTRL6	6	PLL_CTRL3DAC	PLL优化控制 / PLL optimization control.	0x0	R/W
0x798	DACPLL_CTRL6	[5:0]	PLL_CTRL2DAC	PLL优化控制 / PLL optimization control.	0x1C	R/W
0x799	DACPLL_CTRL7	[7:6]	ADC_CLK_DIVIDER	ADC时钟输出分频器。0除以1。1除以2。10除以3。11除以4。 / ADC clock output divider. 0: divide by 1.1: divide by 2. 10: divide by 3. 11:divide by 4.	0x0	R/W

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0x799	DACPLL_CTRL7	[5:0]	N_DIVIDER	可编程除以N值（2至50）。N_DIVIDER=（DAC频率×M_DIVIDER)/(8×基准时钟频率)。 / Programmable divide-by-N value (2 to 50). N_DIVIDER = (DAC frequency x M_DIVIDER)/(8 x reference clock frequency).	0x8	R/W
0x7A0	DACPLL_CTRL9	[7:6]	RESERVED	保留。 / Reserved.	0x2	R/W
0x7A0	DACPLL_CTRL9	5	D_EN_VAR_FINE_DAC	PLL控制PRE / PLL control PRE.	0x0	R/W
0x7A0	DACPLL_CTRL9	[4:3]	RESERVED	保留。 / Reserved.	0x2	R/W
0x7A0	DACPLL_CTRL9	2	D_EN_VAR_DAC	PLL控制COARSE_PRE / PLL control COARSE_PRE.	0x0	R/W
0x7A0	DACPLL_CTRL9	[1:0]	RESERVED	保留。 / Reserved.	0x0	R/W
0x7A2	DACPLL_CTRL10	7	RESERVED	保留。 / Reserved.	0x0	R
0x7A2	DACPLL_CTRL10	[6:5]	D_REGULATOR_DAC	PLL优化控制CAL_WAIT / PLL optimization control CAL_WAIT.	0x1	R/W
0x7A2	DACPLL_CTRL10	[4:3]	D_VCO_CAL_WAITDAC	PLL优化控制 / PLL optimization control.	0x2	R/W
0x7A2	DACPLL_CTRL10	[2:1]	D_VCO_CAL_CYCLESDAC	PLL优化控制 / PLL optimization control.	0x2	R/W
0x7A2	DACPLL_CTRL10	0	RESERVED	保留。 / Reserved.	0x1	R/W
0x7B5	PLL_STATUS	[7:1]	RESERVED	保留。 / Reserved.	0x0	R
0x7B5	PLL_STATUS	0	PLL_LOCKDAC	PLL锁定状态。 / PLL lock status.	0x0	R
0x800	DDSM_HOPF_CTRL	[7:6]	DDSM_HOPF_MODE	频率切换模式。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。0相位连续开关。改变频率调谐字，相位累加器继续累加到新的FTW。1相位不连续开关。更改频率调谐字并重置相位累加器。10相位一致开关。该模式会启动所有32个NCO相位累加器同时开始计数，并且无论选择哪个NCO输出，所有累加器都会继续计数。 / Frequency switching mode. This control is paged by the MAINDAC_PAGE control in Register 0x008. 0: phase-continuous switching. Change the frequency tuning word; the phase accumulator continues accumulating to the new FTW. 1:phase-discontinuous switching.Change the frequency tuning word and reset the phase accumulator.10: phase-coherent switching. This mode starts all 32 NCO phase accumulators counting simultaneously, and all accumulators continue counting	0x0	R/W

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				regardless of which NCO output is selected.		
0x800	DDSM_HOPF_CTRL	5	RESERVED	保留。 / Reserved.	0x0	R/W
0x800	DDSM_HOPF_CTRL	[4:0]	DDSM_HOPF_SEL	跳频选择控制。输入FTW的编号（从FTW0到FTW31），以选择该NCO的输出。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping selection control. Input the number of the FTW (from FTW0 to FTW31) to select the output of that NCO. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x806	DDSM_HOPF_FTW1_0	[7:0]	DDSM_HOPF_FTW1[7:0]	跳频FTW1。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW1. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x807	DDSM_HOPF_FTW1_1	[7:0]	DDSM_HOPF_FTW1[15:8]	跳频FTW1。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW1. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x808	DDSM_HOPF_FTW1_2	[7:0]	DDSM_HOPF_FTW1[23:16]	跳频FTW1。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW1. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x809	DDSM_HOPF_FTW1_3	[7:0]	DDSM_HOPF_FTW1[31:24]	跳频FTW1。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW1. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x80A	DDSM_HOPF_FTW2_0	[7:0]	DDSM_HOPF_FTW2[7:0]	跳频FTW2。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW2. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x80B	DDSM_HOPF_FTW2_1	[7:0]	DDSM_HOPF_FTW2[15:8]	跳频FTW2。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW2. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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0x80C	DDSM_HOPF_FTW2_2	[7:0]	DDSM_HOPF_FTW2[23:16]	跳频FTW2。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW2. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x80D	DDSM_HOPF_FTW2_3	[7:0]	DDSM_HOPF_FTW2[31:24]	跳频FTW2。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW2. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x80E	DDSM_HOPF_FTW3_0	[7:0]	DDSM_HOPF_FTW3[7:0]	跳频FTW3。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW3. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x80F	DDSM_HOPF_FTW3_1	[7:0]	DDSM_HOPF_FTW3[15:8]	跳频FTW3。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW3. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x810	DDSM_HOPF_FTW3_2	[7:0]	DDSM_HOPF_FTW3[23:16]	跳频FTW3。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW3. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x811	DDSM_HOPF_FTW3_3	[7:0]	DDSM_HOPF_FTW3[31:24]	跳频FTW3。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW3. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x812	DDSM_HOPF_FTW4_0	[7:0]	DDSM_HOPF_FTW4[7:0]	跳频FTW4。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW4. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x813	DDSM_HOPF_FTW4_1	[7:0]	DDSM_HOPF_FTW4[15:8]	跳频FTW4。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW4. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x814	DDSM_HOPF_FTW4_2	[7:0]	DDSM_HOPF_FTW4[23:16]	跳频FTW4。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW4. This	0x0	R/W

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				control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x815	DDSM_HOPF_FTW4_3	[7:0]	DDSM_HOPF_FTW4[31:24]	跳频FTW4。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW4. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x816	DDSM_HOPF_FTW5_0	[7:0]	DDSM_HOPF_FTW5[7:0]	跳频FTW5。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW5. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x817	DDSM_HOPF_FTW5_1	[7:0]	DDSM_HOPF_FTW5[15:8]	跳频FTW5。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW5. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x818	DDSM_HOPF_FTW5_2	[7:0]	DDSM_HOPF_FTW5[23:16]	跳频FTW5。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW5. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x819	DDSM_HOPF_FTW5_3	[7:0]	DDSM_HOPF_FTW5[31:24]	跳频FTW5。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW5. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x81A	DDSM_HOPF_FTW6_0	[7:0]	DDSM_HOPF_FTW6[7:0]	跳频FTW6。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW6. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x81B	DDSM_HOPF_FTW6_1	[7:0]	DDSM_HOPF_FTW6[15:8]	跳频FTW6。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW6. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x81C	DDSM_HOPF_FTW6_2	[7:0]	DDSM_HOPF_FTW6[23:16]	跳频FTW6。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW6. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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0x81D	DDSM_HOPF_FTW6_3	[7:0]	DDSM_HOPF_FTW6[31:24]	跳频FTW6。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW6. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x81E	DDSM_HOPF_FTW7_0	[7:0]	DDSM_HOPF_FTW7[7:0]	跳频FTW7。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW7. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x81F	DDSM_HOPF_FTW7_1	[7:0]	DDSM_HOPF_FTW7[15:8]	跳频FTW7。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW7. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x820	DDSM_HOPF_FTW7_2	[7:0]	DDSM_HOPF_FTW7[23:16]	跳频FTW7。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW7. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x821	DDSM_HOPF_FTW7_3	[7:0]	DDSM_HOPF_FTW7[31:24]	跳频FTW7。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW7. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x822	DDSM_HOPF_FTW8_0	[7:0]	DDSM_HOPF_FTW8[7:0]	跳频FTW8。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW8. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x823	DDSM_HOPF_FTW8_1	[7:0]	DDSM_HOPF_FTW8[15:8]	跳频FTW8。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW8. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x824	DDSM_HOPF_FTW8_2	[7:0]	DDSM_HOPF_FTW8[23:16]	跳频FTW8。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW8. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x825	DDSM_HOPF_FTW8_3	[7:0]	DDSM_HOPF_FTW8[31:24]	跳频FTW8。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW8. This	0x0	R/W

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				control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x826	DDSM_HOPF_FTW9_0	[7:0]	DDSM_HOPF_FTW9[7:0]	跳频FTW9。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW9. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x827	DDSM_HOPF_FTW9_1	[7:0]	DDSM_HOPF_FTW9[15:8]	跳频FTW9。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW9. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x828	DDSM_HOPF_FTW9_2	[7:0]	DDSM_HOPF_FTW9[23:16]	跳频FTW9。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW9. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x829	DDSM_HOPF_FTW9_3	[7:0]	DDSM_HOPF_FTW9[31:24]	跳频FTW9。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW9. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x82A	DDSM_HOPF_FTW10_0	[7:0]	DDSM_HOPF_FTW10[7:0]	跳频FTW10。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW10. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x82B	DDSM_HOPF_FTW10_1	[7:0]	DDSM_HOPF_FTW10[15:8]	跳频FTW10。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW10. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x82C	DDSM_HOPF_FTW10_2	[7:0]	DDSM_HOPF_FTW10[23:16]	跳频FTW10。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW10. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x82D	DDSM_HOPF_FTW10_3	[7:0]	DDSM_HOPF_FTW10[31:24]	跳频FTW10。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW10. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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0x82E	DDSM_HOPF_FTW11_0	[7:0]	DDSM_HOPF_FTW11[7:0]	跳频FTW11。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW11. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x82F	DDSM_HOPF_FTW11_1	[7:0]	DDSM_HOPF_FTW11[15:8]	跳频FTW11。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW11. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x830	DDSM_HOPF_FTW11_2	[7:0]	DDSM_HOPF_FTW11[23:16]	跳频FTW11。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW11. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x831	DDSM_HOPF_FTW11_3	[7:0]	DDSM_HOPF_FTW11[31:24]	跳频FTW11。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW11. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x832	DDSM_HOPF_FTW12_0	[7:0]	DDSM_HOPF_FTW12[7:0]	跳频FTW12。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW12. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x833	DDSM_HOPF_FTW12_1	[7:0]	DDSM_HOPF_FTW12[15:8]	跳频FTW12。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW12. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x834	DDSM_HOPF_FTW12_2	[7:0]	DDSM_HOPF_FTW12[23:16]	跳频FTW12。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW12. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x835	DDSM_HOPF_FTW12_3	[7:0]	DDSM_HOPF_FTW12[31:24]	跳频FTW12。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW12. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x836	DDSM_HOPF_FTW13_0	[7:0]	DDSM_HOPF_FTW13[7:0]	跳频FTW13。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW13. This	0x0	R/W

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				control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x837	DDSM_HOPF_FTW13_1	[7:0]	DDSM_HOPF_FTW13[15:8]	跳频FTW13。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW13. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x838	DDSM_HOPF_FTW13_2	[7:0]	DDSM_HOPF_FTW13[23:16]	跳频FTW13。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW13. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x839	DDSM_HOPF_FTW13_3	[7:0]	DDSM_HOPF_FTW13[31:24]	跳频FTW13。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW13. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x83A	DDSM_HOPF_FTW14_0	[7:0]	DDSM_HOPF_FTW14[7:0]	跳频FTW14。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW14. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x83B	DDSM_HOPF_FTW14_1	[7:0]	DDSM_HOPF_FTW14[15:8]	跳频FTW14。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW14. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x83C	DDSM_HOPF_FTW14_2	[7:0]	DDSM_HOPF_FTW14[23:16]	跳频FTW14。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW14. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x83D	DDSM_HOPF_FTW14_3	[7:0]	DDSM_HOPF_FTW14[31:24]	跳频FTW14。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW14. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x83E	DDSM_HOPF_FTW15_0	[7:0]	DDSM_HOPF_FTW15[7:0]	跳频FTW15。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW15. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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0x83F	DDSM_HOPF_FTW15_1	[7:0]	DDSM_HOPF_FTW15[15:8]	跳频FTW15。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW15. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x840	DDSM_HOPF_FTW15_2	[7:0]	DDSM_HOPF_FTW15[23:16]	跳频FTW15。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW15. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x841	DDSM_HOPF_FTW15_3	[7:0]	DDSM_HOPF_FTW15[31:24]	跳频FTW15。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW15. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x842	DDSM_HOPF_FTW16_0	[7:0]	DDSM_HOPF_FTW16[7:0]	跳频FTW16。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW16. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x843	DDSM_HOPF_FTW16_1	[7:0]	DDSM_HOPF_FTW16[15:8]	跳频FTW16。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW16. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x844	DDSM_HOPF_FTW16_2	[7:0]	DDSM_HOPF_FTW16[23:16]	跳频FTW16。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW16. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x845	DDSM_HOPF_FTW16_3	[7:0]	DDSM_HOPF_FTW16[31:24]	跳频FTW16。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW16. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x846	DDSM_HOPF_FTW17_0	[7:0]	DDSM_HOPF_FTW17[7:0]	跳频FTW17。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW17. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x847	DDSM_HOPF_FTW17_1	[7:0]	DDSM_HOPF_FTW17[15:8]	跳频FTW17。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW17. This	0x0	R/W

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				control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x848	DDSM_HOPF_FTW17_2	[7:0]	DDSM_HOPF_FTW17[23:16]	跳频FTW17。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW17. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x849	DDSM_HOPF_FTW17_3	[7:0]	DDSM_HOPF_FTW17[31:24]	跳频FTW17。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW17. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x84A	DDSM_HOPF_FTW18_0	[7:0]	DDSM_HOPF_FTW18[7:0]	跳频FTW18。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW18. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x84B	DDSM_HOPF_FTW18_1	[7:0]	DDSM_HOPF_FTW18[15:8]	跳频FTW18。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW18. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x84C	DDSM_HOPF_FTW18_2	[7:0]	DDSM_HOPF_FTW18[23:16]	跳频FTW18。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW18. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x84D	DDSM_HOPF_FTW18_3	[7:0]	DDSM_HOPF_FTW18[31:24]	跳频FTW18。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW18. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x84E	DDSM_HOPF_FTW19_0	[7:0]	DDSM_HOPF_FTW19[7:0]	跳频FTW19。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW19. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x84F	DDSM_HOPF_FTW19_1	[7:0]	DDSM_HOPF_FTW19[15:8]	跳频FTW19。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW19. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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0x850	DDSM_HOPF_FTW19_2	[7:0]	DDSM_HOPF_FTW19[23:16]	跳频FTW19。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW19. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x851	DDSM_HOPF_FTW19_3	[7:0]	DDSM_HOPF_FTW19[31:24]	跳频FTW19。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW19. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x852	DDSM_HOPF_FTW20_0	[7:0]	DDSM_HOPF_FTW20[7:0]	跳频FTW20。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW20. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x853	DDSM_HOPF_FTW20_1	[7:0]	DDSM_HOPF_FTW20[15:8]	跳频FTW20。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW20. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x854	DDSM_HOPF_FTW20_2	[7:0]	DDSM_HOPF_FTW20[23:16]	跳频FTW20。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW20. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x855	DDSM_HOPF_FTW20_3	[7:0]	DDSM_HOPF_FTW20[31:24]	跳频FTW20。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW20. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x856	DDSM_HOPF_FTW21_0	[7:0]	DDSM_HOPF_FTW21[7:0]	跳频FTW21。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW21. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x857	DDSM_HOPF_FTW21_1	[7:0]	DDSM_HOPF_FTW21[15:8]	跳频FTW21。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW21. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x858	DDSM_HOPF_FTW21_2	[7:0]	DDSM_HOPF_FTW21[23:16]	跳频FTW21。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW21. This	0x0	R/W

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				control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x859	DDSM_HOPF_FTW21_3	[7:0]	DDSM_HOPF_FTW21[31:24]	跳频FTW21。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW21. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x85A	DDSM_HOPF_FTW22_0	[7:0]	DDSM_HOPF_FTW22[7:0]	跳频FTW22。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW22. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x85B	DDSM_HOPF_FTW22_1	[7:0]	DDSM_HOPF_FTW22[15:8]	跳频FTW22。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW22. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x85C	DDSM_HOPF_FTW22_2	[7:0]	DDSM_HOPF_FTW22[23:16]	跳频FTW22。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW22. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x85D	DDSM_HOPF_FTW22_3	[7:0]	DDSM_HOPF_FTW22[31:24]	跳频FTW22。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW22. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x85E	DDSM_HOPF_FTW23_0	[7:0]	DDSM_HOPF_FTW23[7:0]	跳频FTW23。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW23. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x85F	DDSM_HOPF_FTW23_1	[7:0]	DDSM_HOPF_FTW23[15:8]	跳频FTW23。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW23. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x860	DDSM_HOPF_FTW23_2	[7:0]	DDSM_HOPF_FTW23[23:16]	跳频FTW23。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW23. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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0x861	DDSM_HOPF_FTW23_3	[7:0]	DDSM_HOPF_FTW23[31:24]	跳频FTW23。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW23. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x862	DDSM_HOPF_FTW24_0	[7:0]	DDSM_HOPF_FTW24[7:0]	跳频FTW24。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW24. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x863	DDSM_HOPF_FTW24_1	[7:0]	DDSM_HOPF_FTW24[15:8]	跳频FTW24。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW24. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x864	DDSM_HOPF_FTW24_2	[7:0]	DDSM_HOPF_FTW24[23:16]	跳频FTW24。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW24. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x865	DDSM_HOPF_FTW24_3	[7:0]	DDSM_HOPF_FTW24[31:24]	跳频FTW24。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW24. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x866	DDSM_HOPF_FTW25_0	[7:0]	DDSM_HOPF_FTW25[7:0]	跳频FTW25。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW25. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x867	DDSM_HOPF_FTW25_1	[7:0]	DDSM_HOPF_FTW25[15:8]	跳频FTW25。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW25. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x868	DDSM_HOPF_FTW25_2	[7:0]	DDSM_HOPF_FTW25[23:16]	跳频FTW25。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW25. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x869	DDSM_HOPF_FTW25_3	[7:0]	DDSM_HOPF_FTW25[31:24]	跳频FTW25。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW25. This	0x0	R/W

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				control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x86A	DDSM_HOPF_FTW26_0	[7:0]	DDSM_HOPF_FTW26[7:0]	跳频FTW26。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW26. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x86B	DDSM_HOPF_FTW26_1	[7:0]	DDSM_HOPF_FTW26[15:8]	跳频FTW26。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW26. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x86C	DDSM_HOPF_FTW26_2	[7:0]	DDSM_HOPF_FTW26[23:16]	跳频FTW26。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW26. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x86D	DDSM_HOPF_FTW26_3	[7:0]	DDSM_HOPF_FTW26[31:24]	跳频FTW26。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW26. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x86E	DDSM_HOPF_FTW27_0	[7:0]	DDSM_HOPF_FTW27[7:0]	跳频FTW27。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW27. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x86F	DDSM_HOPF_FTW27_1	[7:0]	DDSM_HOPF_FTW27[15:8]	跳频FTW27。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW27. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x870	DDSM_HOPF_FTW27_2	[7:0]	DDSM_HOPF_FTW27[23:16]	跳频FTW27。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW27. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x871	DDSM_HOPF_FTW27_3	[7:0]	DDSM_HOPF_FTW27[31:24]	跳频FTW27。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW27. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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0x872	DDSM_HOPF_FTW28_0	[7:0]	DDSM_HOPF_FTW28[7:0]	跳频FTW28。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW28. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x873	DDSM_HOPF_FTW28_1	[7:0]	DDSM_HOPF_FTW28[15:8]	跳频FTW28。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW28. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x874	DDSM_HOPF_FTW28_2	[7:0]	DDSM_HOPF_FTW28[23:16]	跳频FTW28。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW28. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x875	DDSM_HOPF_FTW28_3	[7:0]	DDSM_HOPF_FTW28[31:24]	跳频FTW28。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW28. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x876	DDSM_HOPF_FTW29_0	[7:0]	DDSM_HOPF_FTW29[7:0]	跳频FTW29。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW29. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x877	DDSM_HOPF_FTW29_1	[7:0]	DDSM_HOPF_FTW29[15:8]	跳频FTW29。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW29. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x878	DDSM_HOPF_FTW29_2	[7:0]	DDSM_HOPF_FTW29[23:16]	跳频FTW29。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW29. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x879	DDSM_HOPF_FTW29_3	[7:0]	DDSM_HOPF_FTW29[31:24]	跳频FTW29。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW29. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x87A	DDSM_HOPF_FTW30_0	[7:0]	DDSM_HOPF_FTW30[7:0]	跳频FTW30。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW30. This	0x0	R/W

地址 / Address	名称 / Name	位 / Bits	位名称 / Bit Name	说明 / Description	重置 / Reset	访问 / Access
				control is paged by the MAINDAC_PAGE control in Register 0x008.		
0x87B	DDSM_HOPF_FTW30_1	[7:0]	DDSM_HOPF_FTW30[15:8]	跳频FTW30。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW30. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x87C	DDSM_HOPF_FTW30_2	[7:0]	DDSM_HOPF_FTW30[23:16]	跳频FTW30。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW30. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x87D	DDSM_HOPF_FTW30_3	[7:0]	DDSM_HOPF_FTW30[31:24]	跳频FTW30。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW30. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x87E	DDSM_HOPF_FTW31_0	[7:0]	DDSM_HOPF_FTW31[7:0]	跳频FTW31。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW31. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x87F	DDSM_HOPF_FTW31_1	[7:0]	DDSM_HOPF_FTW31[15:8]	跳频FTW31。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW31. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x880	DDSM_HOPF_FTW31_2	[7:0]	DDSM_HOPF_FTW31[23:16]	跳频FTW31。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW31. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W
0x881	DDSM_HOPF_FTW31_3	[7:0]	DDSM_HOPF_FTW31[31:24]	跳频FTW31。该控制由寄存器0x008中的MAINDAC_PAGE控制分页。 /Frequency-hopping FTW31. This control is paged by the MAINDAC_PAGE control in Register 0x008.	0x0	R/W

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电源地间保护 / Power and Ground Protection

English: To improve the ESD robustness of the device, ESD protection circuits exist between the internal power pins of the device as shown in Figure 56. The forward conduction voltage drop of each ESD protection device is about 0.2 V; during power-up and normal use, these ESD protection devices must be avoided from conducting in the forward direction for extended periods.

中文： 为了提高器件的抗静电能力，器件内部的各电源引脚之间存在如下的静电保护回路，每个 ESD 保护管的正向导通压降约 0.2V，上电及正常使用中应避免这些 ESD 保护管长时间正向导通。

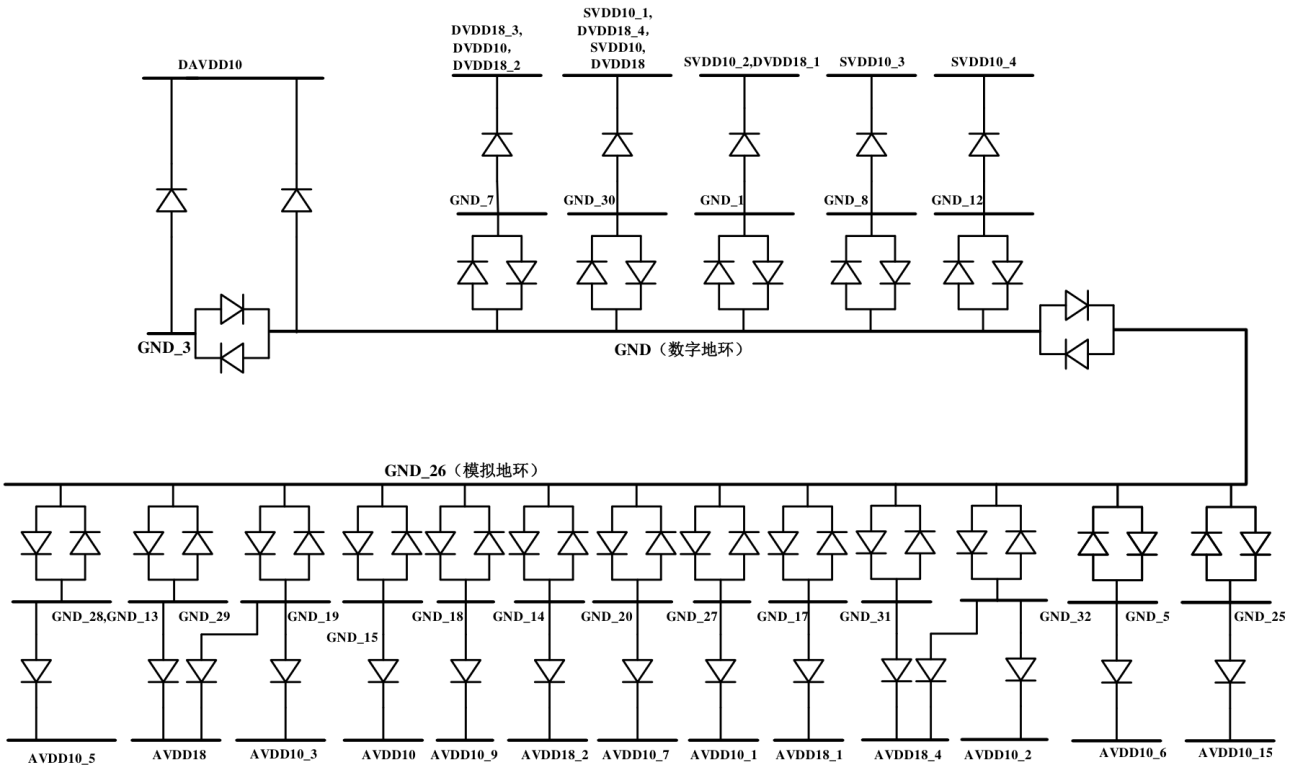


Figure 56: ESD Protection Circuit Between the Internal Power Supplies

注意事项 / Precautions

1、产品安装注意事项 / 1. Product Installation Precautions

English: 1) When soldering, pay attention to the device orientation to avoid soldering it incorrectly. 2) The instruments and meters used to debug the circuit must have good unified grounding. The PCB design must maintain good grounding and power-supply decoupling. 3) Take care not to reverse the power supply or short the input/output terminals to the power supply, which can easily cause circuit damage.

中文： 1) 焊接时请注意器件方向，以免焊错。 2) 调试电路所用的仪器、仪表一定要有良好的统一接地。PCB 板设计请务必保持接地良好、电源去耦。 3) 应注意不要将电源接反及输入输出端与电源短路，易造成电路损坏。

2、产品使用注意事项 / 2. Product Use Precautions

English: 1) It is recommended to reset the circuit first after power-up, and then use it. 2) This product has high power consumption; it is recommended to pay attention to the ambient temperature in actual use and to heat dissipation.

中文： 1) 推荐上电后首先对电路进行复位，再进行使用。 2) 本产品功耗较高，建议实际使用时关注环境温度，并注意散热。

3、产品防护注意事项 / 3. Product Protection Precautions

English: 1) All pins of this circuit are designed with ESD protection structures; however, large-energy electrical pulses can still damage the circuit, so ESD protection must be observed during testing, handling and storage. 2) Exceeding the absolute maximum ratings may cause permanent damage to the device. These are only maximum ratings and do not imply that the device can operate normally under these conditions or under any other conditions beyond those shown in this product manual. 3) Under conditions avoiding direct rain and snow, packaged products can be transported by safe means of transport, but they must not be stacked together with acidic, alkaline or other corrosive objects. The packaging should be safe, and existing means of transport can be used. 4) The storage environment of packaged products should meet the Class I warehouse conditions specified in Section 8.1 of Q/W 657A (temperature: 15 °C to 25 °C, humidity: 25% to 65%), with no acidic, alkaline or other corrosive gases around, good ventilation, and corresponding anti-static measures.

中文： 1) 该电路所有引出端均设计有静电保护结构，不过大能量电脉冲仍然可能损坏电路，因此在测试、搬运、储藏过程中，应注意静电防护。 2) 超出绝对最大额定值可能会导致器件永久性损坏。这只是额定最值，不表示在这些条件下或者在任何其它超出本产品手册中所示的条件下，器件能够正常工作。 3) 在避免雨、雪直接影响的条件下，装有产品的包装箱可以用安全的运输工具运输。但不能和带有酸性、碱性和其它腐蚀性物体堆放在一起。包装应是安全的，可以采用现有的运输工具。 4) 包装好的产品贮存环境应满足 Q/W 657A 第 8.1 规定的 I 类库房条件要求（温度：15°C~25°C，湿度：25%~65%），周围没有酸、碱或其它腐蚀性气体，通风良好，且具备相应防静电措施。

4、电装说明 / 4. Assembly Instructions

English: 1) The moisture sensitivity level of this product is MSL3. The allowable exposure time to the external environment from removal from the moisture-proof bag, dry storage or baking, to reflow soldering is: ≤30 °C/60% RH, 168 h. 2) If the device storage conditions cannot be controlled or traced, strictly perform baking at 125 °C for 8 h before assembly. 3) If the assembly environment temperature and humidity cannot be guaranteed at ≤30 °C/60% RH, complete soldering within 12 h after baking. 4) After baking, the product easily generates static electricity; ESD protection must be observed during all operations. 5) When leaded reflow soldering (Sn63Pb37) is used for board-level assembly, the recommended peak temperature range is 210 °C to 235 °C, the maximum peak temperature is not recommended to exceed 235 °C, the dwell time within ±5 °C of the peak temperature is ≤20 s, the time above the liquidus is 60 s to 90 s, the ramp-up rate is 2 °C/s to 4 °C/s, and the ramp-down rate is 2 °C/s to 6 °C/s. 6) When lead-free reflow soldering (SAC305) is used for board-level assembly, the recommended peak temperature range is 230 °C to 245 °C, the maximum peak temperature is not recommended to exceed 260 °C, the dwell time within ±5 °C of the peak temperature is ≤20 s, the time above the liquidus is 60 s to 90 s, the ramp-up rate is 2 °C/s to 4 °C/s, and the ramp-down rate is 2 °C/s to 6 °C/s. 7) If the mixed assembly process requires a temperature increase, ensure that the device body temperature does not

exceed 260 °C at the maximum (the device body temperature measurement point is on the top surface of the device during reflow soldering). 8) This product uses lead-free solder balls, with material SAC305.

中文： 1) 本产品潮湿敏感等级为 MSL3，将产品从防潮袋中取出、进行干燥储存或烘干后到回流焊前所暴露在外部环境的允许时间为：≤30°C/60RH%，168h； 2) 若器件储存条件无法控制或追溯，请在电装前严格执行 125°C，8h 烘烤； 3) 若电装环境温湿度无法保证≤30°C/60RH%，请在烘烤后 12h 内完成焊接； 4) 产品烘烤后，极易产生静电，所有操作过程需要注意 ESD 防护； 5) 板级组装采用有铅回流焊（Sn63Pb37）时，推荐峰值温度范围 210°C~235°C，最大峰值温度不建议超过 235°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C/s； 6) 板级组装采用无铅回流焊（SAC305）时，推荐峰值温度范围 230°C~245°C，最大峰值温度不建议超过 260°C，峰值温度±5°C以内停留时间≤20s，液相线以上停留时间 60~90s，升温速率 2~4°C/s，降温速率 2~6°C； 7) 若混合电装工艺需要温度升高，应保证器件本体温度最高不超过 260°C（器件本体温度测量点位于回流焊时器件上表面）； 8) 本产品采用无铅焊球，材料为 SAC305。

5、热阻 / 5. Thermal Resistance

表 51 封装热阻 / Table 51. Package Thermal Resistance

项目 / Item	实测值 / Measured Value	依据标准及方法 / Basis Standard and Method
Rthja（结到环境的热阻）/ Rthja (junction-to-ambient thermal resistance)	28.87 K/W	JESD51-2 集成电路自然对流热测试环境要求及测试方法 / JESD51-2 natural-convection thermal test environment requirements and test method for integrated circuits
Rthjt（结到器件顶面的热阻）/ Rthjt (junction-to-device-top thermal resistance)	1.314 K/W	JESD51-14 一维传热路径双界面分离法 / JESD51-14 dual-interface separation method for one-dimensional heat-transfer path
Rthj-bottom（结到器件底面的热阻）/ Rthj-bottom (junction-to-device-bottom thermal resistance)	4.125 K/W	JESD51-14 拐点理论器件内部结构分层得到 / Obtained per JESD51-14 inflection-point theory from the internal structure layering of the device
Rthj-board（结到 PCB 板背面的热阻）/ Rthj-board (junction-to-PCB-back thermal resistance)	10.18 K/W	依据 JESD51-14 双界面分离法得到 / Obtained per the JESD51-14 dual-interface separation method

常见故障及处理办法 / Common Faults and Handling Methods

English: 1. No signal output: check whether the power supply voltage, input signal and clock are correctly applied. 2. Abnormal device function: clarify the device operating mode and confirm that the configuration is correct. 3. Unstable device operation: check the power supply and ensure that the power supply voltage is stable.

中文： 1、 无信号输出：检查电源电压、输入信号、时钟是否正确加载。 2、 器件功能不正常：明确器件工作模式，确认配置是否正确。 3、 器件工作不稳定：检查电源，保证电源电压稳定。

联系方式 / Contact Information

English: For datasheets, samples and quotations, please contact: Felix Lai, Shenzhen Shenxin Technology Co., Ltd. — felix@shenxinic.com, +852 51367095, shenxinic.com.

中文： 规格书、样品与报价请联系：Felix Lai，深圳市深信科技有限公司 — felix@shenxinic.com，+852 51367095，shenxinic.com。

附加说明 / Additional Notes

English: 1. First release date of this manual: July 2026. 2. Product status of this product: ☒ In production (this part number is currently in production and formal products can be provided); ☐ Pre-release (this part number has not yet entered formal production; samples can be provided). 3. Description of the replacement of the foreign product:

中文： 1. 本说明书首次发布日期：2026 年 7 月。 2. 本产品状态：☒生产（该产品型号目前已在生产，可以提供正式产品）；☐预发布（该产品型号尚未投入正式生产，可以提供样品）。 3. 替代国外产品情况说明：

1）绝对最大额定值对比 / 1) Absolute Maximum Ratings Comparison

附表 1 绝对最大额定值对比 / Appendix Table 1. Absolute Maximum Ratings Comparison

参数 / Parameter	SXD052 规范要求 / SXD052 Specification Requirement	国外产品器件手册 / Foreign Product Datasheet	比对结果 / Comparison Result
1.8V 模拟电源（VAVDD1.8）/ 1.8 V analog supply (VAVDD1.8)	-0.3 V～+2.2 V	——	无 / None
1.0V 模拟和时钟电源（VAVDD1.0）/ 1.0 V analog and clock supply (VAVDD1.0)	-0.2 V～+1.02 V	——	无 / None
1.0V 数字电源（VDVDD1.0）/ 1.0 V digital supply (VDVDD1.0)	-0.2 V～+1.02 V	——	无 / None
1.0V 数字到模拟的电源（VDAVDD1.0）/ 1.0 V digital-to-analog supply (VDAVDD1.0)	-0.2 V～+1.02 V	——	无 / None
1.0V SERDES 电源（VSVDD1.0）/ 1.0 V SERDES supply (VSVDD1.0)	-0.2 V～+1.02 V	——	无 / None
1.8V 数字和 I/O 电源（VDVDD1.8）/ 1.8 V digital and I/O supply (VDVDD1.8)	-0.3 V～+2.2 V	——	无 / None
引出端耐焊接温度（Th）（10 s）/ Lead soldering temperature withstand (Th) (10 s)	260°C	260°C	一致 / Consistent
贮存温度（Tstg）/ Storage temperature (Tstg)	-65°C~150°C	-65°C~150°C	一致 / Consistent
结温（TJ）/ Junction temperature (TJ)	125°C	118°C	存在差异 / Different

2）推荐工作条件对比 / 2) Recommended Operating Conditions Comparison

附表 2 推荐工作条件对比 / Appendix Table 2. Recommended Operating Conditions Comparison

参数 / Parameter	SXD052 规范要求 / SXD052 Specification Requirement	国外产品器件手册 / Foreign Product Datasheet	比对结果 / Comparison Result
1.8V 模拟电源（VAVDD1.8）	1.71 V～1.89 V	1.71 V～1.89 V	一致 / Consistent

参数 / Parameter	SXD052 规范要求 / SXD052 Specification Requirement	国外产品器件手册 / Foreign Product Datasheet	比对结果 / Comparison Result
1.0V 模拟和时钟电源（VAVDD1.0）	0.95 V～1.00 V	0.95 V～1.05 V	略有差异 / Slightly different
1.0V 数字电源（VDVDD1.0）	0.95 V～1.00 V	0.95 V～1.05 V	略有差异 / Slightly different
1.0V 数字到模拟的电源（VDAVDD1.0）	0.95 V～1.00 V	0.95 V～1.05 V	略有差异 / Slightly different
1.0V SERDES 电源（VSVDD1.0）	0.95 V～1.00 V	0.95 V～1.05 V	略有差异 / Slightly different
1.8V 数字和 I/O 电源（VDVDD1.8）	1.71 V～1.89 V	1.71 V～1.89 V	一致 / Consistent
工作温度 / Operating temperature	-40°C≤TC≤85°C	-40°C≤Tj≤118°C；Tj=51°C时，TA=25°C	略有差异，SXD052 热阻（结至顶壳）（RJCT）1.314°C/W，热阻（结至环境）（RJA）28.87°C/W / Slightly different; SXD052 thermal resistance (junction-to-top-case) (RJCT) 1.314 °C/W, thermal resistance (junction-to-ambient) (RJA) 28.87 °C/W

3）性能指标对比 / 3) Performance Specification Comparison

附表 3 主要性能指标对比 / Appendix Table 3. Main Performance Specification Comparison

English: SXD052 values are measured at TC = −40 °C to 85 °C; the foreign product values are from its datasheet at TJ = −40 °C to 118 °C. Note: the typical values of both the SXD052 and the foreign product are room-temperature measured values; the SXD052 limit values are specification requirements, and the foreign product limit values are datasheet values.

中文： SXD052（实测），TC=-40°C~85°C；国外产品（数据手册），TJ=-40°C~118°C。注：SXD052、国外产品典型值均为常温实测值，SXD052 极限值为规范要求，国外产品极限值为数据手册值。

参数 / Parameter	测试条件 / Test Conditions	SXD052 最小 / Min	SXD052 典型 / Typ	SXD052 最大 / Max	国外产品 最小 / Min	国外产品 典型 / Typ	国外产品 最大 / Max	单位 / Unit	比对结果 / Result
分辨率 / Resolution	/		16			16		bits	一致 / Consistent
微分非线性误差 / DNL	/	-18	-13/6	18	—	±7	—	LSB	较国外手册进行了放宽 / Relaxed vs. the foreign datasheet
积分非线性误差 / INL	/	-30	-15/12	23	—	±7	—	LSB	较国外手册进行了放宽 / Relaxed vs. the foreign datasheet
增益误差 / Gain error	/	-20	-7.3	20	—	±15	—	%	与国外手册一致 / Consistent with the foreign datasheet
最小满量程输出电流 / Minimum full-scale output current	RSET=5kΩ	13	14.4	18	14.2	16	17.8	mA	较国外手册进行了放宽 / Relaxed
最大满量程输出电流 / Maximum full-scale output current	RSET=5kΩ	20	24.0	29	23.6	26	28.8	mA	较国外手册进行了放宽 / Relaxed
DAC 输出差分阻抗 a / DAC output differential impedance a	TC=25°C	80	106	120	—	100	—	Ω	
最小时钟输入功率 a / Minimum clock input power a	/	3	—	—	—	0	—	dBm	
最大时钟输入功率 a / Maximum clock input power a	器件上差分电阻 Rload=100Ω，TC=25°C	—	—	9	—	6	—	dBm	
时钟输入差分阻抗 a / Clock input differential impedance a	TC=25°C	80	106	120	—	100	—	Ω	国外只有典型值 / Foreign product gives typical value only
时钟输入共模电压 / Clock input common-mode voltage	交流耦合 / AC-coupled	0.4	0.477	0.6	—	0.5	—	V	
时钟输出差分阻抗 a / Clock output differential impedance a	TC=25°C	70	86	110	—	100	—	Ω	
时钟输出共模电压 / Clock output common-mode voltage	交流耦合 / AC-coupled	0.4	0.492	0.6	—	0.5	—	V	
内部基准电压 / Internal reference voltage	/	0.4	0.501	0.6	—	0.495	—	V	
AVDD1.0 电源电流 / AVDD1.0 supply current	/	—	625	1100	—	—	—	mA	与国外测试条件不一致，无国外值 / Test conditions differ from the foreign product; no foreign value

参数 / Parameter	测试条件 / Test Conditions	SXD052 最小 / Min	SXD052 典型 / Typ	SXD052 最大 / Max	国外产品 最小 / Min	国外产品 典型 / Typ	国外产品 最大 / Max	单位 / Unit	比对结果 / Result
AVDD1.8 电源电流 / AVDD1.8 supply current	/	—	78	140	—	—	—	mA	
DVDD1.0 电源电流 b / DVDD1.0 supply current b	双链路模式，模式 1（L=2，M=4，NP=16，N=16），fDAC=11000MSPS，fout=2000MHz / Dual-link mode, Mode 1, fDAC = 11000 MSPS, fout = 2000 MHz	—	952	2000	—	—	—	mA	
DVDD1.8 电源电流 / DVDD1.8 supply current	同上 / Same as above	—	36	60				mA	
SVDD1.0 电源电流 / SVDD1.0 supply current	/	—	275	600	—	—	—	mA	
总功耗 / Total power dissipation	/	—	1.95	4	—	—	—	W	
最大输出转换率 / Maximum output conversion rate	16 位分辨率，带插值，VDDXc=0.975V / 16-bit resolution, with interpolation, VDDXc = 0.975 V	11	—	—	—	—	—	GSPS	无国外值 / No foreign value
最大 SCLK 时钟速率 / Maximum SCLK clock rate	SPI 写操作 / SPI write	80	—	—	80	—	—	MHz	一致 / Consistent
SCLK 时钟高电平 / SCLK clock high level	SPI 写操作，SCLK=20MHz	5.03	—	—	5.03	—	—	ns	
SCLK 时钟低电平 / SCLK clock low level	SPI 写操作，SCLK=20MHz	1.6	—	—	1.6	—	—	ns	
SDIO 到 SCLK 建立时间 / SDIO to SCLK setup time	SPI 写操作 / SPI write	1.154	—	—	1.154	—	—	ns	
SCLK 到 SDIO 保持时间 / SCLK to SDIO hold time	SPI 写操作 / SPI write	0.577	—	—	0.577	—	—	ns	
CS 到 SCLK 建立时间 / CS to SCLK setup time	SPI 写操作 / SPI write	1.036	—	—	1.036	—	—	ns	
SCLK 到 CS 保持时间 / SCLK to CS hold time	SPI 写操作 / SPI write	-5.3	—	—	-5.3	—	—	ps	
SCLK 时钟速率 / SCLK clock rate	SPI 读操作 / SPI read	—	—	48.58	—	—	48.58	MHz	
SCLK 时钟高电平 / SCLK clock high level	SPI 读操作 / SPI read	5.03	—	—	5.03	—	—	ns	
SCLK 时钟低电平 / SCLK clock low level	SPI 读操作 / SPI read	1.6	—	—	1.6	—	—	ns	
SDIO 到 SCLK 建立时间 / SDIO to SCLK setup time	SPI 读操作 / SPI read	1.158	—	—	1.158	—	—	ns	
SCLK 到 SDIO 保持时间 / SCLK to SDIO hold time	SPI 读操作 / SPI read	0.537	—	—	0.537	—	—	ns	
CS 到 SCLK 建立时间 / CS to SCLK setup time	SPI 读操作 / SPI read	1.036	—	—	1.036	—	—	ns	
输入高电平 / Input high level	输入引脚（SDIO、SCLK、CS、RESET、TXEN0、TXEN1）/ Input pins (SDIO, SCLK, CS, RESET, TXEN0, TXEN1)	1.48	—	—	1.48	—	—	V	
输入低电平 / Input low level	同上 / Same as above	—	—	0.425	—	—	0.425	V	
输入高电平电流 / Input high-level current	同上 / Same as above	-1	0.003	1	—	—	±100	uA	较国外手册进行了放宽 / Relaxed
输入低电平电流 / Input low-level current	同上 / Same as above	-1	0.001	1	±100	—	—	uA	较国外手册进行了放宽 / Relaxed
输出高电平 / Output high level	输出引脚（SDIO，SDO），4mA 负载 / Output pins (SDIO, SDO), 4 mA load	1.52	—	—	1.52	—	—	V	一致 / Consistent
输出低电平 / Output low level	同上 / Same as above	—	—	0.175	—	—	0.175	V	
输出高电平电流 / Output high-level current	输出引脚（SDIO，SDO）/ Output pins (SDIO, SDO)	4	—	—	—	4	—	mA	国外只有典型值 / Foreign product gives typical value only
输出低电平电流 / Output low-level current	同上 / Same as above	4	—	—	—	4	—	mA	
中断输出高电平 / Interrupt output high level	中断输出引脚（IRQ0、IRQ1）/ Interrupt output pins (IRQ0, IRQ1)	1.71	—	—	1.71	—	—	V	一致 / Consistent
中断输出低电平 / Interrupt output low level	同上 / Same as above	—	—	0.075	—	—	0.075	V	
SYSREF± 输入差分阻抗 / SYSREF± input differential impedance	/	80	106	120	—	100	—	Ω	国外只有典型值 / Typical value only
SYNCOUT 输出差分电压 / SYNCOUT output differential voltage	/	320	365	460	320	390	460	mV	一致 / Consistent
SYNCOUT 输出偏移电压 / SYNCOUT output offset voltage	/	1.06	1.13	1.3	1.08	1.12	1.15	V	和国外不一样 / Different from the foreign product
SYNCOUT 输出高电平 / SYNCOUT output high level	/	1.66	1.80	—	1.69	—	—	V	
SYNCOUT 输出低电平 / SYNCOUT output low level	/	—	0.002	0.045	—	—	0.045	V	一致 / Consistent
最大通道 NCO 时钟速率 a / Maximum channel NCO clock rate a	TC=25°C	1540	—	—	—	—	1540	MHz	一致 / Consistent
最大主 NCO 时钟速率 a / Maximum main NCO clock rate a	TC=25°C	11	—	—	—	—	12	GHz	不一致 / Inconsistent
无杂散动态范围 / SFDR	-7dBFS，随机化开启，fDAC=11000MSPS，模式 1（L=2，M=4，NP=16，N=16），VDDXc=0.975V；fout=100MHz	60	72	—	—	—	—	dBc	无相同国外频点测试值 / No foreign test value at the same frequency points
无杂散动态范围 / SFDR	同上；fout=2000MHz	55	66	—	—	—	—	dBc	
无杂散动态范围 / SFDR	同上；fout=3700MHz	50	61	—	—	—	—	dBc	
非谐波无杂散动态范围 ad / Non-harmonic SFDR ad	-7dBFS，随机化开启，fDAC=11000MSPS，模式 1，VDDXc=0.975V，TC=25°C；fout=100MHz	70	82	—	—	—	—	dBc	

参数 / Parameter	测试条件 / Test Conditions	SXD052 最小 / Min	SXD052 典型 / Typ	SXD052 最大 / Max	国外产品 最小 / Min	国外产品 典型 / Typ	国外产品 最大 / Max	单位 / Unit	比对结果 / Result
非谐波无杂散动态范围 ad / Non-harmonic SFDR ad	同上；fout=2000MHz	65	77	—	—	—	—	dBc	
非谐波无杂散动态范围 ad / Non-harmonic SFDR ad	同上；fout=3700MHz	60	71	—	—	—	—	dBc	
双音互调失真 / Two-tone IMD	-7dBFS/单音，fDAC=11000MSPS，模式 1，VDDXc=0.975V；fout=2000MHz，1MHz 间距	65	78	—	—	—	—	dBc	
双音互调失真 / Two-tone IMD	同上；fout=3700MHz，1MHz 间距	60	74	—	—	—	—	dBc	
噪声频谱密度 a / NSD a	0dBFS/单音，在距离 fOUT 10% 上测量，随机化开启，fDAC=11000 MSPS，fout=2000MHz，VDDXc=0.975V，TC=25℃	140	153	—	—	—	—	dBc/Hz	
输出隔离度 ac / Output isolation ac	fDAC=11000 MSPS，fOUT=2000MHz，模式 1（L=2，M=4，NP=16，N=16），VDDXc=0.975V，TC=25℃	60	75	—	—	—	—	dB	

4）其它指标对比 / 4) Other Specification Comparison

附表 4 其它指标对比 / Appendix Table 4. Other Specification Comparison

参数 / Parameter	SXD052	国外产品 / Foreign Product	比对结果 / Comparison Result
封装形式 / Package type	BGA144	BGA144	一致 / Consistent
质量等级 / Quality grade	企标 / Enterprise standard	工业级 / Industrial grade	一致 / Consistent
尺寸 / Dimensions	10mm×10mm×1.872mm	10mm×10mm×1.56mm	长、宽与国外样品一致，增加散热盖，高度高于国外样品 / Length and width consistent with the foreign sample; a heat-dissipation lid is added, and the height is greater than the foreign sample
替代建议 / Replacement recommendation	☐直接替代 / Direct replacement；☐有效替代 / Effective replacement；☒功能替代 / Functional replacement		

English: Note: the dimensions of both the SXD052 and the foreign product are typical values.

中文： 注：SXD052、国外产品的尺寸均为典型值。