SXS046 and AD9361 Comparison Report

English translation

Full-Parameter Test Results Comparison Using a 93K Automated Test System

Contents

1. Automated test results at Tc = 25°C, −55°C and 125°C
2. TX-channel measurements using a manual test board
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Translation notes

This document translates the supplied 15-page Chinese comparison report. Numerical results, units, sample identifiers and the order of test entries are retained. Table headers referring to the domestic device and the foreign device are rendered as SXS046 and AD9361, respectively. Repeated headers and text split across source pages have been consolidated.

Blank cells and “/” are reproduced from the source and do not indicate zero. Apparent numerical or unit inconsistencies have not been corrected. Tc values identify the reported test conditions. The source does not state the frequency unit in Table 4.

The statements in Section 3 are translated from the source report. They do not constitute additional independent compatibility testing.

1. Full-Parameter Test Results Comparison

Table 1. Room-temperature measurements (Tc = 25°C)

SXS046 vs. AD9361 | 93K automated test system | Source pages 2–6

Parameter Tc = 25°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Center frequency	70		6000	70~6000	70~6000	MHz	
Minimum gain (not currently measurable; to be noted in the manual)	/	/	/	/	/	dB	
Maximum gain (relative gain)	70.592	70.999	71.649	/	71.404	dB	@800MHz
Maximum gain (relative gain)	68.932	69.942	70.419	/	68.932	dB	@2300MHz(RX1A,RX2A)
Maximum gain (relative gain)	69.217	70.125	70.427	/	69.217	dB	@2300MHz(RX1B,RX1C, RX2B,RX2C)
Maximum gain (relative gain)	60.925	61.359	61.678	/	61.148	dB	@5500MHz(RX1A,RX2A)
Gain step	0.967	0.972	0.981	/	0.978	dB	
RSSI range	93.25	94.195	96	/	96	dB	
Noise figure (NF)	1.921	2.196	2.592	/	1.925	dB	Maximum RX gain
Out-of-band input IP3 (IIP3)	-18.18	-17.711	-16.966	/	-17.22	dBm	Maximum RX gain
Out-of-band input IP2 (IIP2)	38.517	47.944	54.637	/	48.483	dBm	Maximum RX gain
DC offset	-87.956	-85.612	-83.527	/	-84.165	dBm	RX front-end input; digital-domain measurement; maximum RX gain
Quadrature gain error	0.001	0.008	0.028	/	0.012	%	Minimum RX gain
Quadrature phase error	0	0.018	0.075	/	0.006	°	Minimum RX gain
Image rejection	63.697	75.873	84.947	/	79.592	dB	Minimum RX gain
Modulation accuracy (EVM)	/	/	/	-41.536	/	dB	19.2 MHz reference clock
RX1 to RX2 isolation; RX1A to RX2A; RX1C to RX2C	84.778	86.418	87.977	/	87.977	dB	Minimum RX gain
RX1 to RX2 isolation; RX1B to RX2B	53.394	54.525	55.528	/	54.516	dB	Minimum RX gain
RX2 to RX1 isolation; RX2A to RX1A; RX2C to RX1C	74.7	75.529	79.101	/	79.101	dB	Minimum RX gain

Parameter Tc = 25°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
RX2 to RX1 isolation; RX2B to RX1B	52.649	54.485	55.569	/	52.649	dB	Minimum RX gain
Noise figure (NF)	2.845	3.230	3.821	/	3.621	dB	Maximum RX gain
Input third-order intercept point (IIP3)	-14.007	-13.003	-11.821	/	-11.821	dBm	Maximum RX gain
Input second-order intercept point (IIP2)	41.28	50.743	67.343	/	54.418	dBm	Maximum RX gain
LO leakage	-83.167	-80.842	-78.579	/	-80.143	dBm	RX front-end input
Quadrature gain error	0.001	0.005	0.021	/	0.006	%	
Quadrature phase error	0.001	0.008	0.02	/	0.005	°	
Image rejection	73.655	79.425	83.539	/	80.24	dB	
Modulation accuracy (EVM)	/	/	/	-40.11	-39.90	dB	40 MHz reference clock
RX1 to RX2 isolation; RX1A to RX2A; RX1C to RX2C	75.047	77.783	79.577	/	78.773	dB	
RX1 to RX2 isolation; RX1B to RX2B	43.006	43.938	46.667	/	46.667	dB	
RX2 to RX1 isolation; RX2A to RX1A; RX2C to RX1C	56.01	56.664	57.366	/	57.366	dB	
RX2 to RX1 isolation; RX2B to RX1B	52.226	53.549	55.576	/	54.623	dB	
Noise figure (NF)	3.611	4.078	5.376	/	3.65	dB	Maximum RX gain
Input third-order intercept point (IIP3)	-21.52	-18.467	-16.463	/	-20.554	dBm	Maximum RX gain
Input second-order intercept point (IIP2)	41.857	45.199	49.945	/	43.86	dBm	Maximum RX gain
LO leakage	-83.001	-80.583	-77.729	/	-81.197	dBm	RX front-end input
Quadrature gain error	0	0.006	0.025	/	0.004	%	
Quadrature phase error	0	0.009	0.026	/	0	°	
Image rejection	72.233	76.046	79.349	/	77.321	dB	
Modulation accuracy (EVM)	/	/	/	-36.19	/	dB	40 MHz reference clock
RX1A to RX2A isolation	56.854	60.682	62.92	/	56.854	dB	
RX2A to RX1A isolation	46.617	47.516	48.278	/	47.67	dB	
Center frequency	50	/	6000	/	50~6000	MHz	

Parameter Tc = 25°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Power control range	88.23	88.548	88.884	/	88.884	dB	
Power control accuracy	/	/	/	/	/	dB	
Output S22	/	/	/	/	/	dB	
Maximum output power	7.762	8.189	8.537	/	8.895	dBm	1 MHz single tone into 50 Ω load
Image rejection	55.708	64.017	71.519	/	67.789	dB	0 dB attenuation
Modulation accuracy (EVM)	/	/	/	-45.85	/	dB	Measured on manual test board
Output third-order intercept point (OIP3)	19.439	20.023	20.747	/	20.194	dBm	
LO leakage	-69.12	-61.216	-55.8	/	-55.8	dBc	0 dB attenuation
LO leakage	-58.821	-42.376	-35.618	/	-41.532	dBc	40 dB attenuation
Noise floor	/	/	/	-158.51	/	dBm/Hz	90 MHz offset
TX1 to TX2 isolation	76.821	77.369	78.033	/	77.655	dB	TX1 transmitting; TX2 not transmitting
TX2 to TX1 isolation	73.452	73.996	74.425	/	73.891	dB	
Maximum output power	7.26	7.717	8.158	/	8.537	dB	1 MHz single tone into 50 Ω load
Image rejection	44.499	47.993	54.235		53.806	dB	
Modulation accuracy (EVM)	/	/	/	-40.27	/	dB	
Output third-order intercept point (OIP3)	18.299	21.148	24.277	/	24.277	dBm	
Carrier leakage	-70.876	-62.738	-54.904	/	-55.3	dBc	0 dB attenuation
Carrier leakage	-57.197	-42.449	-35.037	/	-41.544	dBc	40 dB attenuation
Noise floor	/	/	/	-157.33	/	dBm/Hz	90 MHz offset
TX1 to TX2 isolation	63.789	64.019	64.227	/	63.953	dB	
TX2 to TX1 isolation	60.697	61.127	61.703	/	61.415	dB	
Output S22	/	/	/	/	/	dB	
Maximum output power	6.678	6.914	7.237	/	7.01	dBm	1 MHz single tone into 50 Ω load
Image rejection	42.842	47.241	50.922		46.193	dB	
Modulation accuracy (EVM)	/	/	/	-34.11	/	dB	

Parameter Tc = 25°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Output third-order intercept point (OIP3)	10.23	15.454	18.821	/	16.176	dBm	
Carrier leakage	-63.619	-54.237	-48.973	/	-51.83	dBc	0 dB attenuation
Carrier leakage	-60.979	-41.155	-33.946	/	-41.984	dBc	40 dB attenuation
Noise floor	/	/	/	/	/	dBm/Hz	90 MHz offset
TX1 to TX2 isolation	50.476	50.937	51.352	/	50.476	dB	
TX2 to TX1 isolation	50.2	50.397	50.646	/	50.496	dB	
Maximum input power	/	/	/	4	4	dBm	
Dynamic range	/	60	/	57	60	dB	
Accuracy	/	/	/	2	2	dB	
LO frequency step	/	/	/	4	4	Hz	
Integrated phase noise, 800MHz	/	/	/	0.074	0.078	° rms	100 Hz to 100 MHz; 30.72 MHz reference clock
Integrated phase noise, 2.4GHz	/	/	/	0.363	0.169	° rms	100 Hz to 100 MHz; 40 MHz reference clock
Integrated phase noise, 5.5GHz	/	/	/	0.596	0.499	° rms	100 Hz to 100 MHz; 40 MHz reference clock
Auxiliary ADC resolution	12	12	12	/	12	Bits	
Auxiliary ADC minimum input voltage	0	0	0	/	0	V	
Auxiliary ADC maximum input voltage	1.2695	1.273	1.2746	/	1.2695	V	
Auxiliary DAC resolution	10	10	10	/	10	Bits	
Auxiliary DAC minimum output voltage	0.397	0.408	0.418	/	0.39	V	
Auxiliary DAC maximum output voltage	3.29	3.290	3.291	/	3.291	V	
Auxiliary DAC output current	10	10	10	/	10	mA	
Logic-high input voltage (VIH)	1.44	1.44	1.44	/	1.44	V	
Logic-low input voltage (VIL)	0.36	0.36	0.36	/	0.36	V	
Logic-high input current (IIH)	0.1	0.1	0.1	/	0.1	μA	
Logic-low input current (IIL)	0.01	0.01	0.01	/	0.01	μA	
Logic-high output voltage (VOH)	1.8	1.8	1.8	/	1.8	V	

Parameter Tc = 25°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Logic-low output voltage (VOL)	0.1	0.1	0.1	/	0.1	V	
Input voltage range	875~1575	875~1575	875~1575	/	875~1575	mV	
Differential input voltage threshold	±60	±70	±80	/	±70	mV	
Differential receiver impedance	106.718	110.166	112.919	/	110.421	Ω	
Logic-high output voltage (VOH)	1344.867	1385.941	1419.922	/	1469.006	mV	
Logic-low output voltage (VOL)	1049.523	1056.647	1102.124	/	1059.053	mV	
Differential output voltage	254.528	331.835	365.283	/	414	mV	
Output offset voltage	1221.722	1239.570	1261.026	/	1288.532	mV	
Logic-high output voltage	2.8624	2.8724	2.8447	/	2.9351	V	
Logic-low output voltage	0.1584	0.159	0.1629	/	0.1375	V	
Output current	10	10	10	/	10	mA	
SPI_CLK period	20.8333	22.600	33.333	/	21.276	ns	
SPI_CLK pulse width	15	15	15	/	15	ns	
SPI_ENB setup time to first SPI_CLK rising edge	1	1	1	/	1	ns	
SPI_ENB hold time from last SPI_CLK falling edge	0	0	0	/	0	ns	
SPI_DI setup time relative to SPI_CLK (tS)	2	2	2	/	2	ns	
SPI_DI hold time relative to SPI_CLK (tH)	1	1	1	/	1	ns	
SPI_CLK rising edge to data output delay, tCO (3-wire SPI)	3.7	4.664	7.3	/	4.6	ns	
SPI_CLK rising edge to data output delay, tCO (4-wire SPI)	5.61	5.15	9.6	/	5.2	ns	
DATA_CLK period (tCP)	16.276	16.276	16.276	/	16.276	ns	61.44MHz
DATA_CLK and FB_CLK pulse width (tMP)	tCP×0.501	tCP×0.505	tCP×0.508	/	tCP×0.502	ns	61.44MHz
TX_DATA setup time relative to FB_CLK	1	1	1	/	1	ns	
TX_DATA hold time relative to FB_CLK	1	1	1	/	1	ns	
DATA_CLK to data-bus output delay	0.18	0.65	0.79	/	1.15	ns	

Parameter Tc = 25°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
DATA_CLK to RX_FRAME delay	0.87	1.124	1.31	/	1.135	ns	
DATA_CLK period (tCP)	16.276	16.276	16.276	/	16.276	ns	61.44MHz
DATA_CLK and FB_CLK pulse width (tMP)	tCP×0.527	tCP×0.531	tCP×0.534	/	tCP×0.530	ns	61.44MHz
TX_DATA setup time relative to FB_CLK	1	1	1	/	1	ns	
TX_DATA hold time relative to FB_CLK	1	1	1	/	1	ns	
DATA_CLK to data-bus output delay	0.29	/	0.73	/	1.12	ns	
DATA_CLK to RX_FRAME delay	0.79	0.93	1.05	/	0.89	ns	
DATA_CLK period (tCP)	4.069	4.069	4.069		4.069	ns	245.76MHz
DATA_CLK and FB_CLK pulse width (tMP)	tCP×0.426	tCP×0.439	tCP×0.452		tCP×0.439	ns	
TX_DATA setup time relative to FB_CLK	1	1	1		1	ns	
TX_DATA hold time relative to FB_CLK	1	1	1		1	ns	
DATA_CLK to data-bus output delay	0.2	0.35	0.5		0.59	ns	
DATA_CLK to RX_FRAME delay	0.45	0.51	0.59		0.51	ns	

1. Full-Parameter Test Results Comparison

Table 2. Low-temperature measurements (Tc = −55°C)

SXS046 vs. AD9361 | 93K automated test system | Source pages 6–10

Parameter Tc = −55°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Center frequency	70		6000		70~6000	MHz	
Minimum gain						dB	
Maximum gain	71.446	72.213	72.864		72.766	dB	@800MHz
Maximum gain	70.303	71.070	71.569		70.303	dB	@2300MHz(RX1A,RX2A)
Maximum gain	70.614	71.229	71.715		70.614	dB	@2300MHz(RX1B,RX1C, RX2B,RX2C)
Maximum gain	61.637	62.227	62.612		62.237	dB	@5500MHz(RX1A,RX2A)
Gain step	0.979	0.989	0.998		0.997	dB	
RSSI range	91	92.128	94.25		94.25	dB	
Noise figure (NF)	1.378	1.520	1.737		1.587	dB	Maximum RX gain
Input third-order intercept point (IIP3)	-19.401	-18.771	-17.961		-17.966	dBm	Maximum RX gain
Input second-order intercept point (IIP2)	37.224	46.208	54.663		46.113	dBm	Maximum RX gain
LO leakage	-89.053	-86.415	-84.059		-84.487	dBm	RX front-end input
Quadrature gain error	0	0.011	0.056		0.019	%	
Quadrature phase error	0.002	0.023	0.139		0.005	°	
Image rejection	58.208	74.165	82.466		77.586		
RX1 to RX2 isolation; RX1A to RX2A; RX1C to RX2C	85.23	86.382	87.561		87.522	dB	
RX1 to RX2 isolation; RX1B to RX2B	53.298	54.343	55.4		54.181	dB	
RX2 to RX1 isolation; RX2A to RX1A; RX2C to RX1C	73.796	75.341	79.538		79.538	dB	
RX2 to RX1 isolation; RX2B to RX1B	52.522	54.282	55.536		52.522	dB	
Noise figure (NF)	2.109	2.328	3.122		2.937	dB	Maximum RX gain

Parameter Tc = −55°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Input third-order intercept point (IIP3)	-15.855	-15.058	-13.084		-13.084	dBm	Maximum RX gain
Input second-order intercept point (IIP2)	37.017	47.439	58.567		52.282	dBm	Maximum RX gain
LO leakage	-83.591	-81.921	-79.795		-80.202	dBm	RX front-end input
Quadrature gain error	0	0.011	0.051		0.001	%	
Quadrature phase error	0	0.008	0.024		0.008	°	
Image rejection	69.846	77.902	82.409		81.043		
RX1 to RX2 isolation; RX1A to RX2A; RX1C to RX2C	73.708	78.301	80.542		79.687	dB	
RX1 to RX2 isolation; RX1B to RX2B	42.921	43.949	49.342		47.123	dB	
RX2 to RX1 isolation; RX2A to RX1A; RX2C to RX1C	55.949	56.659	57.431		57.341	dB	
RX2 to RX1 isolation; RX2B to RX1B	52.226	53.549	55.576		54.623	dB	
Noise figure (NF)	2.406	2.661	3.652		2.678	dB	Maximum RX gain
Input third-order intercept point (IIP3)	-29.468	-22.564	-18.546		-23.863	dBm	Maximum RX gain
Input second-order intercept point (IIP2)	28.046	39.960	48.646		35.864	dBm	Maximum RX gain
LO leakage	-84.594	-81.759	-79.877		-80.269	dBm	RX front-end input
Quadrature gain error	0	0.011	0.042		0	%	
Quadrature phase error	0	0.011	0.031		0.019	°	
Image rejection	70.822	75.395	79.621		72.996		
RX1A to RX2A isolation	57.425	62.819	64.587		57.425	dB	
RX2A to RX1A isolation	46.047	46.909	47.884		47.83	dB	
Center frequency	50		6000		50~6000	MHz	
Power control range	88.329	88.727	89.01		89.01	dB	
Maximum output power	8.031	8.62	8.874		9.18	dBm	1 MHz single tone into 50 Ω load
Image rejection	49.726	60.192	67.384		58.644	dB	
Output third-order intercept point (OIP3)	19.659	20.714	21.804		20.929	dBm	

Parameter Tc = −55°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Carrier leakage	-78.42	-62.008	-55.517		-55.67	dBc	0 dB attenuation
Carrier leakage	-58.742	-41.286	-33.866		-40.699	dBc	40 dB attenuation
TX1 to TX2 isolation	77.121	77.525	78.119		77.862	dB	
TX2 to TX1 isolation	73.701	74.294	74.969		73.915	dB	
Maximum output power	7.465	8.124	8.491		8.848	dB	1 MHz single tone into 50 Ω load
Image rejection	45.136	48.486	54.049		55.228	dB	
Output third-order intercept point (OIP3)	11.944	20.030	22.78		21.672	dBm	
Carrier leakage	-70.746	-61.762	-53.956		-55.817	dBc	0 dB attenuation
Carrier leakage	-56.293	-41.312	-33.845		-40.594	dBc	40 dB attenuation
TX1 to TX2 isolation	63.915	64.171	64.422		63.915	dB	
TX2 to TX1 isolation	60.688	61.125	61.563		61.438	dB	
Maximum output power	7.063	7.5856	7.886		7.659	dBm	1 MHz single tone into 50 Ω load
Output third-order intercept point (OIP3)	14.919	16.728	19.52		15.751	dBm	
Carrier leakage	-65.291	-55.830	-20.58		-51.126	dBc	0 dB attenuation
Carrier leakage	-48.588	-39.423	-17.3		-41.072	dBc	40 dB attenuation
TX1 to TX2 isolation	50.64	50.897	51.314		50.64	dB	
TX2 to TX1 isolation	50.121	50.370	50.647		50.427	dB	
Auxiliary ADC resolution	12	12	12		12	Bits	
Auxiliary ADC minimum input voltage	0	0	0		0	V	
Auxiliary ADC maximum input voltage	1.2695	1.273	1.2746		1.2695	V	
Auxiliary DAC resolution	10	10	10		10	Bits	
Auxiliary DAC minimum output voltage	0.397	0.408	0.418		0.39	V	
Auxiliary DAC maximum output voltage	3.29	3.290	3.291		3.291	V	
Auxiliary DAC output current	10	10	10		10	mA	
Logic-high input voltage (VIH)	1.44	1.44	1.44		1.44	V	

Parameter Tc = −55°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Logic-low input voltage (VIL)	0.36	0.36	0.36		0.36	V	
Logic-high input current (IIH)	0.1	0.1	0.1		0.1	μA	
Logic-low input current (IIL)	0.01	0.01	0.01		0.01	μA	
Logic-high output voltage (VOH)	1.8	1.8	1.8		1.8	V	
Logic-low output voltage (VOL)	0.1	0.1	0.1		0.1	V	
Input voltage range	875~1575	875~1575	875~1575		875~1575	mV	
Differential input voltage threshold	±60	±70	±80		±70	mV	
Differential receiver impedance	106.718	110.166	112.919		110.421	Ω	
Logic-high output voltage (VOH)	1344.867	1385.941	1419.922		1469.006	mV	
Logic-low output voltage (VOL)	1049.523	1056.647	1102.124		1059.053	mV	
Differential output voltage	254.528	331.835	365.283		414	mV	
Output offset voltage	1221.722	1239.570	1261.026		1288.532	mV	
Logic-high output voltage	2.8624	2.8724	2.8447		2.9351	V	
Logic-low output voltage	0.1584	0.159	0.1629		0.1375	V	
Output current	10	10	10		10	mA	
SPI_CLK period	20.8333	22.600	33.333		21.276	ns	
SPI_CLK pulse width	15	15	15		15	ns	
SPI_ENB setup time to first SPI_CLK rising edge	1	1	1		1	ns	
SPI_ENB hold time from last SPI_CLK falling edge	0	0	0		0	ns	
SPI_DI setup time relative to SPI_CLK (tS)	2	2	2		2	ns	
SPI_DI hold time relative to SPI_CLK (tH)	1	1	1		1	ns	
SPI_CLK rising edge to data output delay, tCO (3-wire SPI)	3.7	4.664	7.3		4.6	ns	
SPI_CLK rising edge to data output delay, tCO (4-wire SPI)	5.61	5.15	9.6		5.2	ns	
DATA_CLK period (tCP)	16.276	16.276	16.276		16.276	ns	61.44MHz

Parameter Tc = −55°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
DATA_CLK and FB_CLK pulse width (tMP)	tCP×0.50179	tCP×0.50572	tCP×0.50871		tCP×0.50242	ns	61.44MHz
TX_DATA setup time relative to FB_CLK	1	1	1		1	ns	
TX_DATA hold time relative to FB_CLK	1	1	1		1	ns	
DATA_CLK to data-bus output delay	0.18	0.65	0.79		1.15	ns	
DATA_CLK to RX_FRAME delay	0.87	1.124	1.31		1.135	ns	

1. Full-Parameter Test Results Comparison

Table 3. High-temperature measurements (Tc = 125°C)

SXS046 vs. AD9361 | 93K automated test system | Source pages 10–13

Parameter Tc = 125°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Center frequency	70		6000		70~6000	MHz	
Maximum gain	69.706	70.243	71.036		70.116	dB	@800MHz
Maximum gain	68.672	69.137	69.807		68.979	dB	@2300MHz(RX1A,RX2A)
Maximum gain	68.895	69.348	69.859		69.407	dB	@2300MHz(RX1B,RX1C, RX2B,RX2C)
Maximum gain	60.047	60.649	61.059		60.446	dB	@5500MHz(RX1A,RX2A)
Gain step	0.955	0.962	0.973		0.96	dB	
RSSI range	95	95.655	96.25		95.5	dB	
Noise figure (NF)	2.206	2.526	2.868		2.572	dB	Maximum RX gain
Input third-order intercept point (IIP3)	-17.576	-17.121	-16.478		-17.417	dBm	Maximum RX gain
Input second-order intercept point (IIP2)	39.496	49.179	56.979		42.005	dBm	Maximum RX gain
LO leakage	-86.812	-85.194	-83.089		-85.828	dBm	RX front-end input
Quadrature gain error	0.001	0.010	0.054		0.018	%	
Quadrature phase error	0.001	0.032	0.16		0.018	°	
Image rejection	56.912	72.773	85.069		74.105		
RX1 to RX2 isolation; RX1A to RX2A; RX1C to RX2C	84.741	86.353	87.94		85.931	dB	
RX1 to RX2 isolation; RX1B to RX2B	53.836	54.659	55.288		54.15	dB	
RX2 to RX1 isolation; RX2A to RX1A; RX2C to RX1C	75.137	75.620	75.94		75.436	dB	
RX2 to RX1 isolation; RX2B to RX1B	53.897	54.621	55.112		54.42	dB	
Noise figure (NF)	3.377	3.828	4.381		3.928	dB	Maximum RX gain
Input third-order intercept point (IIP3)	-13.036	-11.915	-10.916		-11.454	dBm	Maximum RX gain

Parameter Tc = 125°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Input second-order intercept point (IIP2)	42.378	52.537	60.59		42.378	dBm	Maximum RX gain
LO leakage	-82.399	-80.262	-78.569		-78.781	dBm	RX front-end input
Quadrature gain error	0	0.007	0.023		0.004	%	
Quadrature phase error	0	0.009	0.025		0.011	°	
Image rejection	73.765	78.852	83.839		76.299		
RX1 to RX2 isolation; RX1A to RX2A; RX1C to RX2C	75.511	77.709	79.114		77.352	dB	
RX1 to RX2 isolation; RX1B to RX2B	43.286	43.982	44.739		43.542	dB	
RX2 to RX1 isolation; RX2A to RX1A; RX2C to RX1C	55.897	56.666	57.153		56.862	dB	
RX2 to RX1 isolation; RX2B to RX1B	52.084	53.539	55.512		53.164	dB	
Noise figure (NF)	4.494	5.135	5.772		5.544	dB	Maximum RX gain
Input third-order intercept point (IIP3)	-20.136	-18.207	-16.788		-17.759	dBm	Maximum RX gain
Input second-order intercept point (IIP2)	40.073	46.419	53.747		43.809	dBm	Maximum RX gain
LO leakage	-81.986	-79.699	-77.581		-78.636	dBm	RX front-end input
Quadrature gain error	0	0.006	0.023		0.017	%	
Quadrature phase error	0	0.0119	0.032		0.009	°	
Image rejection	71.765	75.732	79.343		76.296		
RX1A to RX2A isolation	53.313	59.509	61.769		59.686	dB	
RX2A to RX1A isolation	46.961	47.775	48.425		47.638	dB	
Center frequency	50		6000		50~6000	MHz	
Power control range	88.142	88.473	88.768		88.383	dB	
Maximum output power	7.499	7.914	8.368		7.656	dBm	1 MHz single tone into 50 Ω load
Image rejection	50.088	63.255	76.339		61.436	dB	
Output third-order intercept point (OIP3)	19.022	19.880	21.049		19.022	dBm	
Carrier leakage	-73.411	-60.120	-54.87		-58.339	dBc	0 dB attenuation

Parameter Tc = 125°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Carrier leakage	-57.123	-43.463	-36.074		-36.074	dBc	40 dB attenuation
TX1 to TX2 isolation	76.767	77.250	77.796		77.074	dB	
TX2 to TX1 isolation	73.152	73.757	74.217		73.987	dB	
Maximum output power	6.978	7.441	7.975		7.145	dB	1 MHz single tone into 50 Ω load
Image rejection	42.502	46.933	52.378		52.967	dB	
Output third-order intercept point (OIP3)	19.375	21.150	24.447		21.935	dBm	
Carrier leakage	-72.691	-61.559	-49.759		-59.73	dBc	0 dB attenuation
Carrier leakage	-63.622	-43.759	-35.533		-36.005	dBc	40 dB attenuation
TX1 to TX2 isolation	63.758	63.961	64.177		63.814	dB	
TX2 to TX1 isolation	60.996	61.392	61.871		61.094	dB	
Maximum output power	5.886	6.299	6.802		6.03	dBm	1 MHz single tone into 50 Ω load
Image rejection	43.185	48.975	52.521		50.326	dB	
Output third-order intercept point (OIP3)	15.441	16.4724	17.623		16.778	dBm	
Carrier leakage	-65.592	-52.249	-45.756		-49.645	dBc	0 dB attenuation
Carrier leakage	-51.712	-40.926	-34.52		-37.878	dBc	40 dB attenuation
TX1 to TX2 isolation	50.913	51.052	51.444		51.444	dB	
TX2 to TX1 isolation	50.24	50.453	50.701		50.701	dB	
Auxiliary ADC resolution	12	12	12		12	Bits	
Auxiliary ADC minimum input voltage	0	0	0		0	V	
Auxiliary ADC maximum input voltage	1.2695	1.273	1.2746		1.2695	V	
Auxiliary DAC resolution	10	10	10		10	Bits	
Auxiliary DAC minimum output voltage	0.397	0.408	0.418		0.39	V	
Auxiliary DAC maximum output voltage	3.29	3.290	3.291		3.291	V	
Auxiliary DAC output current	10	10	10		10	mA	
Logic-high input voltage (VIH)	1.44	1.44	1.44		1.44	V	

Parameter Tc = 125°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
Logic-low input voltage (VIL)	0.36	0.36	0.36		0.36	V	
Logic-high input current (IIH)	0.1	0.1	0.1		0.1	μA	
Logic-low input current (IIL)	0.01	0.01	0.01		0.01	μA	
Logic-high output voltage (VOH)	1.8	1.8	1.8		1.8	V	
Logic-low output voltage (VOL)	0.1	0.1	0.1		0.1	V	
Input voltage range	875~1575	875~1575	875~1575		875~1575	mV	
Differential input voltage threshold	±60	±70	±80		±70	mV	
Differential receiver impedance	106.718	110.166	112.919		110.421	Ω	
Logic-high output voltage (VOH)	1344.867	1385.941	1419.922		1469.006	mV	
Logic-low output voltage (VOL)	1049.523	1056.647	1102.124		1059.053	mV	
Differential output voltage	254.528	331.835	365.283		414	mV	
Output offset voltage	1221.722	1239.570	1261.026		1288.532	mV	
Logic-high output voltage	2.8624	2.8724	2.8447		2.9351	V	
Logic-low output voltage	0.1584	0.159	0.1629		0.1375	V	
Output current	10	10	10		10	mA	
SPI_CLK period	20.8333	22.600	33.333		21.276	ns	
SPI_CLK pulse width	15	15	15		15	ns	
SPI_ENB setup time to first SPI_CLK rising edge	1	1	1		1	ns	
SPI_ENB hold time from last SPI_CLK falling edge	0	0	0		0	ns	
SPI_DI setup time relative to SPI_CLK (tS)	2	2	2		2	ns	
SPI_DI hold time relative to SPI_CLK (tH)	1	1	1		1	ns	
SPI_CLK rising edge to data output delay, tCO (3-wire SPI)	3.7	4.664	7.3		4.6	ns	
SPI_CLK rising edge to data output delay, tCO (4-wire SPI)	5.61	5.15	9.6		5.2	ns	
DATA_CLK period (tCP)	16.276	16.276	16.276		16.276	ns	61.44MHz

Parameter Tc = 125°C	SXS046 93K Minimum	SXS046 93K Average	SXS046 93K Maximum	SXS046 Manual board	AD9361 Measured	Unit	Test conditions
DATA_CLK and FB_CLK pulse width (tMP)	tCP×0.501	tCP×0.505	tCP×0.508		tCP×0.502	ns	61.44MHz
TX_DATA setup time relative to FB_CLK	1	1	1		1	ns	
TX_DATA hold time relative to FB_CLK	1	1	1		1	ns	
DATA_CLK to data-bus output delay	0.18	0.65	0.79		1.15	ns	
DATA_CLK to RX_FRAME delay	0.87	1.124	1.31		1.135	ns	
DATA_CLK period (tCP)	4.069	4.069	4.069		4.069	ns	245.76MHz
DATA_CLK and FB_CLK pulse width (tMP)	tCP×0.426	tCP×0.439	tCP×0.452		tCP×0.439	ns	
DATA_CLK to data-bus output delay	0.2	0.35	0.5		0.59	ns	
DATA_CLK to RX_FRAME delay	0.45	0.51	0.59		0.51	ns	
1.3 V main supply voltage	1.267~1.33	1.267~1.33	1.267~1.33			V	

2. TX-Channel Test Results Comparison

Table 4. Selected TX-channel measurements: SXS046 and AD9361

93K manual test board | Source pages 14–15. The frequency unit is not specified in the source. ADI, 85#, 90# and 105# are the original column identifiers.

Parameter	Frequency	ADI	85#	90#	105#
Output power (dBm)	450	2.73	1.85	1.88	1.9
Output power (dBm)	850	2.14	1.58	1.68	1.32
Output power (dBm)	950	1.8	1.16	1.16	0.92
Output power (dBm)	1450	-0.02	-0.65	-0.6	-0.75
Output power (dBm)	2400	-1.09	-1.71	-2.04	-2.39
Output power (dBm)	3300	-0.82	-1.59	-1.75	-2.31
Output power (dBm)	5200	-4.61	-4.88	-4.66	-5.32
Output power (dBm)	5800	-7.93	-6.86	-6.98	-7.69
LO leakage (dB)	450	58.7	53.98	58.48	58.53
LO leakage (dB)	850	59.18	58.71	59.69	59.13
LO leakage (dB)	950	67	61.17	58.07	59.82
LO leakage (dB)	1450	52.49	62.18	60.47	59.92
LO leakage (dB)	2400	52.32	51.74	52.82	53.88
LO leakage (dB)	3300	60.89	64.03	55.33	56.37
LO leakage (dB)	5200	52.56	52.84	52.43	62.19
LO leakage (dB)	5800	47.67	50.77	51.86	43.74
Image rejection (dB)	450	73.1	58.74	71.6	57.41
Image rejection (dB)	850	62.73	56.42	63.12	56.82
Image rejection (dB)	950	63.73	56.77	70.09	55.23
Image rejection (dB)	1450	66.05	58.26	63.26	62.08
Image rejection (dB)	2400	52.2	47.39	46.94	48.77
Image rejection (dB)	3300	78.12	50.75	52.59	51.92

Parameter	Frequency	ADI	85#	90#	105#
Image rejection (dB)	5200	55.55	54	49.85	50.64
Image rejection (dB)	5800	56.33	54.6	50.13	52.5
Second harmonic (dB)	450	69.57	70.75	65.7	78.15
Second harmonic (dB)	850	69.68	71.33	66.24	78.82
Second harmonic (dB)	950	69.43	70.87	65.33	81.5
Second harmonic (dB)	1450	68.35	71.88	66.39	81.24
Second harmonic (dB)	2400	62.44	62.85	64.1	74.54
Second harmonic (dB)	3300	67.73	71.84	64.27	75.55
Second harmonic (dB)	5200	61.81	56.34	59.12	56.06
Second harmonic (dB)	5800	54.65	51.04	52.82	46.16
Third harmonic (dB)	450	47.46	48.97	48.52	48.49
Third harmonic (dB)	850	45.08	46.53	46.43	46.15
Third harmonic (dB)	950	45.99	47.85	47.77	47.6
Third harmonic (dB)	1450	45.66	49.3	49.44	49.27
Third harmonic (dB)	2400	50.3	50.46	50.53	50.41
Third harmonic (dB)	3300	48.43	47.81	47.93	48.33
Third harmonic (dB)	5200	47.29	47.6	47.8	48.21
Third harmonic (dB)	5800	44.45	43.76	43.96	44.44

3. Functional Comparison: SXS046 and AD9361

The SXS046 package supports pin-to-pin replacement of the AD9361 on the existing footprint, and its functionality fully matches that of the AD9361. The configuration is identical except for one register configuration requirement, as described below.

RX and TX baseband bandwidth calibration register configuration

The clock used for baseband bandwidth calibration is derived by dividing the main clock. The RX divider is determined by Reg1F8[7:0] (BBF Tune Divide), and the TX divider by Reg0D6[7:0]. For this device, the divider must not be an odd number; that is, Reg1F8[0] and Reg0D6[0] must not be set to 1.

The divider is determined jointly by the BBPLL frequency and the baseband bandwidth, using the following formula:

BBF Tune Divide[8:0] = ceil((BBPLL Freq × ln(2)) / (BBBW × 1.4 × 2 × π))

There are two ways to avoid this issue:

1. After initialization, check the values of these two registers. If the value is 1, adjust the baseband bandwidth and reinitialize the chip. Changing the baseband bandwidth changes the division ratio, allowing an odd division ratio that would cause the issue to be changed to an even division ratio.

2. If the register values written during initialization can be modified, set Reg1F8[0] and Reg0D6[0] directly to 0, then initialize the chip. This also avoids the issue.

Translator’s note: In method 1, the source says “if the value is 1.” The preceding paragraph identifies bit 0 of each register as the relevant odd/even indicator. Register bit ranges and the formula are reproduced as written in the source.