SHENXIN TECH

SXS046

2T2R RF Transceiver SoC | 56 MHz Tunable Channel Bandwidth

2T2R 射频收发器 SoC | 56 MHz 可调谐通道带宽

Customer Edition — Bilingual / 客户版 — 双语

Derived from controlled engineering source: V1.20260807 / 源自受控工程源文件：V1.20260807

RF RANGE	CHANNEL BANDWIDTH
70 MHz to 6 GHz	<200 kHz to 56 MHz
DATA CONVERTERS	**PACKAGE**
2T2R | 12-bit DAC / ADC	CSP_BGA144 | -40°C to +85°C

DESIGN-IN POSITIONING / 设计定位

SXS046 is a Pin-to-Pin Replacement for AD9361. Existing hardware designs can reuse the PCB; register configuration adaptation is required.

SXS046 是 AD9361 的引脚对引脚（Pin-to-Pin）替代产品。现有硬件设计可复用 PCB；需要进行寄存器配置适配。

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Issued 09 October 2026 / 发布日期：2026 年 10 月 9 日

Document Control / 文档控制

Item 项目	Detail 详情
PRODUCT 产品	SXS046
ENGINEERING SOURCE VERSION 工程源文件版本	V1.20260807
CUSTOMER EDITION DATE 客户版日期	09 October 2026
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Customer-edition scope / 客户版范围

- Customer-facing edition with verified electrical specifications retained.
- 面向客户的版本，保留经核实的电气规格。
- Internal comparison notes and preliminary test-board comments have been excluded.
- 内部比较注释和初步测试板评论已排除。
- Controlled register and PCB assembly documentation is available upon request.
- 受控的寄存器和 PCB 组装文档可应请求提供。

This customer edition preserves the controlled electrical specifications and operating limits from the engineering source. Request controlled register and PCB assembly documentation before a design release.

本客户版保留了工程源文件中的受控电气规格和工作限值。在设计发布之前，请索取受控的寄存器和 PCB 组装文档。

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Customer edition excludes internal comparison notes and preliminary test-board comments. Detailed controlled engineering documentation is available from SHENXIN TECH upon request.

客户版排除了内部比较注释和初步测试板评论。详细的受控工程文档可向 SHENXIN TECH 索取。

Applications and Product Description / 应用与产品描述

Applications / 应用

- Point-to-point communication systems
- 点对点通信系统
- Microcell base stations
- 微蜂窝基站
- General-purpose radio systems
- 通用无线电系统

Features / 特性

- Supply voltages: 1.3 V / 1.8 V / 3.3 V
- 电源电压：1.3 V / 1.8 V / 3.3 V
- RF 2 × 2 transceiver integrating 12-bit DACs and ADCs
- RF 2 × 2 收发器，集成 12 位 DAC 和 ADC
- Frequency range: 70 MHz to 6.0 GHz
- 频率范围：70 MHz 至 6.0 GHz
- Supports TDD and FDD
- 支持 TDD 和 FDD
- Tunable channel bandwidth: <200 kHz to 56 MHz
- 可调谐通道带宽：<200 kHz 至 56 MHz
- TX EVM: −40 dB
- TX EVM：−40 dB
- Circuit interface: CMOS/LVDS digital interface
- 电路接口：CMOS/LVDS 数字接口
- ESD rating: Class 1B, HBM 500 V
- ESD 等级：Class 1B，HBM 500 V
- Product weight: 0.32 g ± 0.02 g
- 产品重量：0.32 g ± 0.02 g

Product Description / 产品描述

SXS046 is a high-performance, highly integrated radio-frequency (RF) fast-hopping transceiver intended for 3G and 4G base-station applications. Its programmability and wideband capability make it an ideal choice for a wide range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section, integrates frequency synthesizers, and provides a configurable digital interface to the processor, simplifying design integration. SXS046 operates from 70 MHz to 6.0 GHz, covering most licensed and unlicensed bands, and supports channel bandwidths from less than 200 kHz to 56 MHz.

SXS046 是一款高性能、高集成度的射频 (RF) 快速跳频收发器，面向 3G 和 4G 基站应用。其可编程性和宽带能力使其成为各种收发器应用的理想选择。该器件将 RF 前端与灵活的混合信号基带部分相结合，集成了频率合成器，并为处理器提供可配置的数字接口，简化了设计集成。SXS046 的工作频率范围为 70 MHz 至 6.0 GHz，覆盖大多数授权和非授权频段，支持小于 200 kHz 至 56 MHz 的通道带宽。

The two independent direct-conversion receivers provide outstanding noise figure and linearity. Each receive (RX) subsystem has independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital filtering, eliminating the need to implement these functions in the digital baseband. SXS046 also provides a flexible manual gain mode that supports external control. Each channel contains two high-

dynamic-range ADCs that first digitize the received I and Q signals and then pass them through configurable decimation filters and a 128-tap finite impulse response (FIR) filter, producing a 12-bit output at the appropriate sample rate.

两个独立的直接变频接收机提供出色的噪声系数和线性度。每个接收 (RX) 子系统具有独立的自动增益控制 (AGC)、DC 偏移校正、正交校正和数字滤波，无需在数字基带中实现这些功能。SXS046 还提供支持外部控制的灵活手动增益模式。每个通道包含两个高动态范围 ADC，先将接收到的 I 和 Q 信号数字化，然后通过可配置的抽取滤波器和 128 抽头有限冲激响应 (FIR) 滤波器，以适当的采样率产生 12 位输出。

The transmitter uses a direct-conversion architecture to achieve high modulation accuracy and extremely low noise. This transmitter design provides low TX EVM, with a value <–40 dB, leaving substantial system margin for selection of an external power amplifier. The on-chip transmit (TX) power monitors can serve as power detectors to enable highly accurate TX power measurements.

发射机采用直接变频架构，实现高调制精度和极低噪声。该发射机设计提供低 TX EVM，值 <–40 dB，为外部功率放大器的选择留有充足的系统裕量。片上发射 (TX) 功率监测器可用作功率检测器，实现高精度的 TX 功率测量。

Fully integrated phase-locked loops (PLLs) provide low-power fractional-N frequency synthesis for all receive and transmit channels. The design incorporates the channel isolation required for frequency-division duplex (FDD) systems. All VCO and loop-filter components are also integrated.

完全集成的锁相环 (PLL) 为所有接收和发射通道提供低功耗小数 N 分频频率合成。该设计集成了频分双工 (FDD) 系统所需的通道隔离。所有 VCO 和环路滤波器元件也均集成在片上。

Standard / 标准

Quality grade: Enterprise standard

质量等级：企业标准

The device uses a 10 mm × 10 mm, 144-pin chip-scale ball grid array package (CSP_BGA). The functional block diagram is shown in Figure 1.

该器件采用 10 mm × 10 mm、144 引脚芯片级球栅阵列封装 (CSP_BGA)。功能框图如图 1 所示。

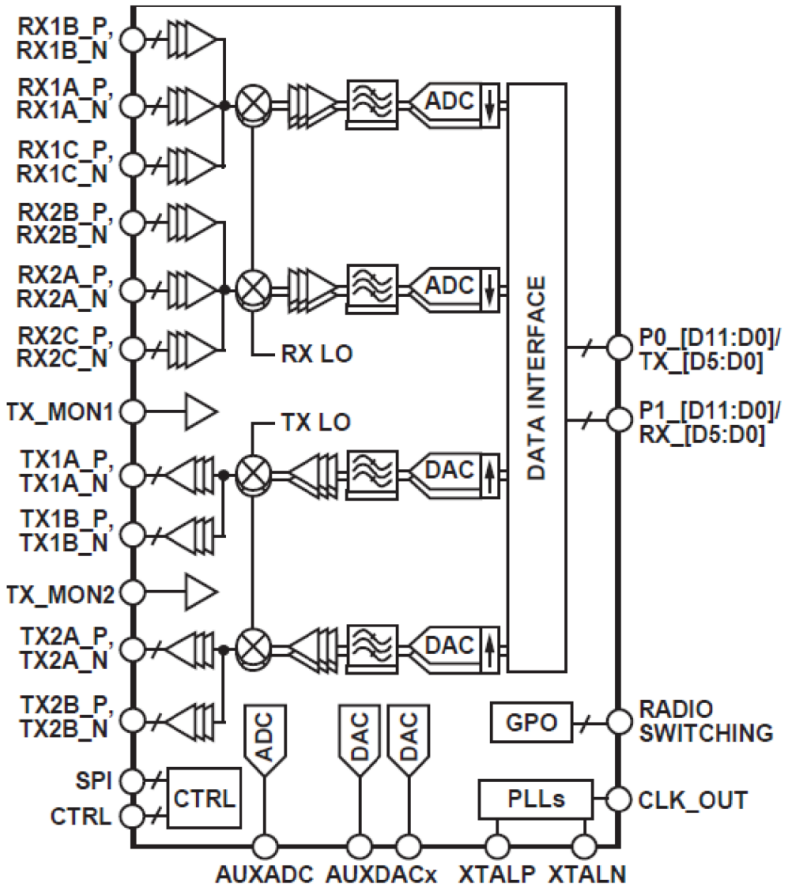


Figure 1. Functional Block Diagram / 图 1. 功能框图

Note: 1. RX and TX Baseband Bandwidth Calibration / 注：1. RX 和 TX 基带带宽校准

The clock for baseband bandwidth calibration is obtained by dividing the master clock. The RX division factor is determined by Reg1F8[7:0] (BBF Tune Divide), and the TX division factor by Reg0D6[7:0]. This division factor must not be odd; that is, Reg1F8[0] and Reg0D6[0] must not be set to 1. The division factor is jointly determined by the BBPLL frequency and the baseband bandwidth, using the following equation:

基带带宽校准时钟由主时钟分频得到。RX 分频系数由 Reg1F8[7:0]（BBF Tune Divide）决定，TX 分频系数由 Reg0D6[7:0] 决定。该分频系数不得为奇数；即 Reg1F8[0] 和 Reg0D6[0] 不得设置为 1。分频系数由 BBPLL 频率和基带带宽共同决定，公式如下：

$$\text{BBF Tune Divide}[8:0] = \text{ceil}((\text{BBPLL Freq} * \ln(2)) / (\text{BBBW} * 1.4 * 2 * \pi))$$

When initializing the chip, avoid setting the values of the two registers above to 1, and verify both register values after initialization. If a value is 1, one feasible method is to adjust the baseband bandwidth and reinitialize the chip to avoid setting either register to 1.

芯片初始化时，避免将上述两个寄存器的值设置为 1，并在初始化后核对两个寄存器的值。如果某个值为 1，一种可行的方法是调整基带带宽并重新初始化芯片，以避免任一寄存器被设置为 1。

Note: 2. RX Channel I/Q Mismatch / 注：2. RX 通道 I/Q 失配

With a 1.8G local oscillator and a high temperature of 80 °C ± 4 °C, there is a possibility of I/Q mismatch in the receive channel RX (the foreign product exhibits mismatch at −20 °C).

在本振为 1.8G、高温为 80 °C ± 4 °C 时，接收通道 RX 有可能出现 I/Q 失配（国外产品在 −20 °C 时出现失配）。

Package Outline and Product Images / 封装外形与产品图片

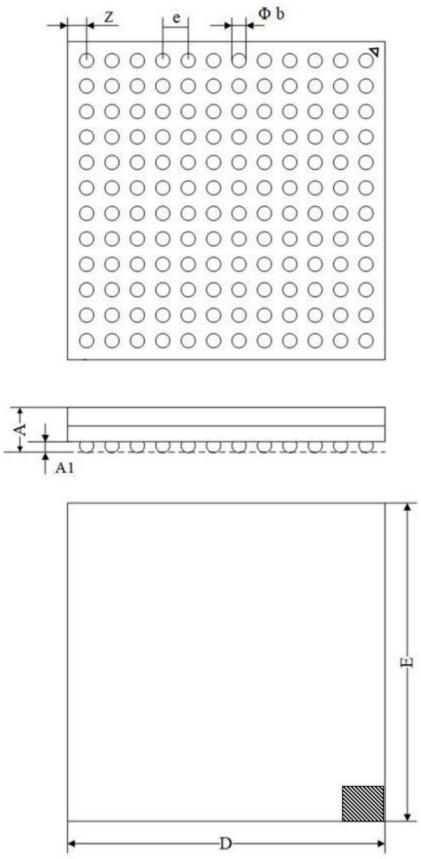


Figure 2. Package Outline Dimensions / 图 2. 封装外形尺寸

Symbol 符号	Min 最小	Nominal 标称	Max 最大	Symbol 符号	Min 最小	Nominal 标称	Max 最大
A	1.27	1.42a	1.57	e	—	0.80	—
A1	0.30	0.35a	0.40	Φb	0.40	0.45a	0.50
D	9.80	10.00a	10.20	Z	—	0.60a	0.70
E	9.80	10.00a	10.20				

Figure 3. Dimensions (Unit: mm) / 图 3. 尺寸（单位：mm）

a Actual nominal package dimension; users are advised to use this dimension as a reference when designing the application.

a 实际标称封装尺寸；建议用户在设计应用时以该尺寸为参考。

Note: For the recommended land pattern, see Assembly Instructions.

注：推荐焊盘图形见组装说明。

Pin Configuration and Pin Function Table / 引脚配置与引脚功能表

Pin Configuration (Top View) / 引脚配置（顶视图）

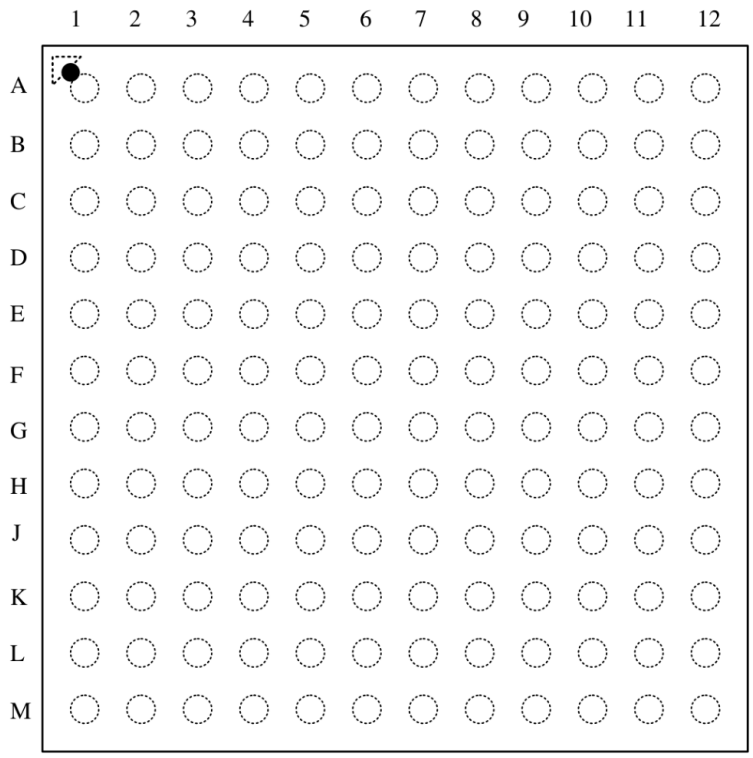


Figure 4. Pin Configuration / 图 4. 引脚配置

Pin Function Table / 引脚功能表

Pin 引脚	Symbol 符号	Function 功能	I/O I/O
A1	RX2A_N	Receive channel 2 input A, negative terminal 接收通道 2 输入 A，负端	I
A2	RX2A_P	Receive channel 2 input A, positive terminal 接收通道 2 输入 A，正端	I
A3	NC	Leave unconnected (a) 不连接 (a)	/
A4	VSSA	Analog ground 模拟地	I
A5	TX_MON2	Transmit channel 2 power-monitor input 发射通道 2 功率监测输入	I
A6	VSSA	Analog ground 模拟地	I
A7	TX2A_N	Transmit channel 2 output A, negative terminal 发射通道 2 输出 A，负端	O
A8	TX2A_P	Transmit channel 2 output A, positive terminal 发射通道 2 输出 A，正端	O
A9	TX2B_N	Transmit channel 2 output B, negative terminal 发射通道 2 输出 B，负端	O
A10	TX2B_P	Transmit channel 2 output B, positive terminal 发射通道 2 输出 B，正端	O

A11	VDDA1P1_TX_VCO	Transmit VCO supply input 发射 VCO 电源输入	I
A12	TX_EXT_LO_IN	TX external LO signal input TX 外部本振信号输入	I
B1	VSSA	Analog ground 模拟地	I
B2	VSSA	Analog ground 模拟地	I
B3	AUXDAC1	Auxiliary DAC1 output 辅助 DAC1 输出	O
B4	GPO_3	General-purpose output 3 通用输出 3	O
B5	GPO_2	General-purpose output 2 通用输出 2	O
B6	GPO_1	General-purpose output 1 通用输出 1	O
B7	GPO_0	General-purpose output 0 通用输出 0	O
B8	VDD_GPO	Auxiliary DAC and GPO supply 辅助 DAC 与 GPO 电源	I
B9	VDDA1P3_TX_LO	Transmit LO 1.3 V supply 发射本振 1.3 V 电源	I
B10	VDDA1P3_TX_VCO_LDO	Transmit VCO LDO supply input 发射 VCO LDO 电源输入	I
B11	TX_VCO_LDO_OUT	Transmit VCO LDO supply output 发射 VCO LDO 电源输出	O
B12	VSSA	Analog ground 模拟地	I
C1	RX2C_P	Receive channel 2 input C, positive terminal 接收通道 2 输入 C，正端	I
C2	VSSA	Analog ground 模拟地	I
C3	AUXDAC2	Auxiliary DAC2 output 辅助 DAC2 输出	O
C4	TEST/ENABLE	Test input 测试输入	I
C5	CTRL_IN0	Control input 0 控制输入 0	I
C6	CTRL_IN1	Control input 1 控制输入 1	I
C7	VSSA	Analog ground 模拟地	I
C8	VSSA	Analog ground 模拟地	I
C9	VSSA	Analog ground 模拟地	I
C10	VSSA	Analog ground 模拟地	I
C11	VSSA	Analog ground 模拟地	I
C12	VSSA	Analog ground 模拟地	I
D1	RX2C_N		I

		Receive channel 2 input C, negative terminal 接收通道 2 输入 C，负端	
D2	VDDA1P3_RX_RF	Receiver 1.3 V supply 接收机 1.3 V 电源	I
D3	VDDA1P3_RX_TX	1.3 V supply 1.3 V 电源	I
D4	CTRL_OUT0	Control output 0 控制输出 0	O
D5	CTRL_IN3	Control input 3 控制输入 3	I
D6	CTRL_IN2	Control input 2 控制输入 2	I
D7	P0_D9/TX_D4_P	Port P0 D9 / transmit D4, differential input, positive terminal 端口 P0 D9 / 发射 D4，差分输入，正端	I/O
D8	P0_D7/TX_D3_P	Port P0 D7 / transmit D3, differential input, positive terminal 端口 P0 D7 / 发射 D3，差分输入，正端	I/O
D9	P0_D5/TX_D2_P	Port P0 D5 / transmit D2, differential input, positive terminal 端口 P0 D5 / 发射 D2，差分输入，正端	I/O
D10	P0_D3/TX_D1_P	Port P0 D3 / transmit D1, differential input, positive terminal 端口 P0 D3 / 发射 D1，差分输入，正端	I/O
D11	P0_D1/TX_D0_P	Port P0 D1 / transmit D0, differential input, positive terminal 端口 P0 D1 / 发射 D0，差分输入，正端	I/O
D12	VSSD	Digital ground 数字地	I
E1	RX2B_P	Receive channel 2 input B, positive terminal 接收通道 2 输入 B，正端	I
E2	VDDA1P3_RX_LO	Receive LO 1.3 V supply 接收本振 1.3 V 电源	I
E3	VDDA1P3_TX_LO_BUFFER	Transmit LO 1.3 V supply 发射本振 1.3 V 电源	I
E4	CTRL_OUT1	Control output 1 控制输出 1	O
E5	CTRL_OUT2	Control output 2 控制输出 2	O
E6	CTRL_OUT3	Control output 3 控制输出 3	O
E7	P0_D11/TX_D5_P	Port P0 D11 / transmit D5, differential input, positive terminal 端口 P0 D11 / 发射 D5，差分输入，正端	I/O
E8	P0_D8/TX_D4_N	Port P0 D8 / transmit D4, differential input, negative terminal 端口 P0 D8 / 发射 D4，差分输入，负端	I/O
E9	P0_D6/TX_D3_N	Port P0 D6 / transmit D3, differential input, negative terminal 端口 P0 D6 / 发射 D3，差分输入，负端	I/O
E10	P0_D4/TX_D2_N	Port P0 D4 / transmit D2, differential input, negative terminal 端口 P0 D4 / 发射 D2，差分输入，负端	I/O
E11	P0_D2/TX_D1_N	Port P0 D2 / transmit D1, differential input, negative terminal 端口 P0 D2 / 发射 D1，差分输入，负端	I/O
E12	P0_D0/TX_D0_N	Port P0 D0 / transmit D0, differential input, negative terminal 端口 P0 D0 / 发射 D0，差分输入，负端	I/O
F1	RX2B_N	Receive channel 2 input B, negative terminal 接收通道 2 输入 B，负端	I
F2	VDDA1P3_RX_VCO_LDO	Receive VCO LDO supply input 接收 VCO LDO 电源输入	I
F3	VSSA		I

		Analog ground 模拟地	
F4	CTRL_OUT6	Control output 6 控制输出 6	O
F5	CTRL_OUT5	Control output 5 控制输出 5	O
F6	CTRL_OUT4	Control output 6 控制输出 6	O
F7	VSSD	Digital ground 数字地	I
F8	P0_D10/TX_D5_N	Port P0 D10 / transmit D5, differential input, negative terminal 端口 P0 D10 / 发射 D5，差分输入，负端	I/O
F9	VSSD	Digital ground 数字地	I
F10	FB_CLK_P	TX data clock input, positive terminal TX 数据时钟输入，正端	I
F11	VSSD	Digital ground 数字地	I
F12	VDDD1P3_DIG	1.3 V digital supply 1.3 V 数字电源	I
G1	RX_EXT_LO_IN	RX external LO signal input RX 外部本振信号输入	I
G2	RX_VCO_LDO_OUT	Receive VCO LDO output 接收 VCO LDO 输出	O
G3	VDDA1P1_RX_VCO	Receive VCO LDO input 接收 VCO LDO 输入	I
G4	CTRL_OUT7	Control output 7 控制输出 7	O
G5	EN_AGC	Manual control input for automatic gain control (AGC) 自动增益控制 (AGC) 手动控制输入	I
G6	ENABLE	Enable signal for the enable state machine 使能状态机的使能信号	I
G7	RX_FRAME_N	Receive data frame, differential output, negative terminal 接收数据帧，差分输出，负端	O
G8	RX_FRAME_P	Receive data frame, differential output, positive terminal 接收数据帧，差分输出，正端	O
G9	TX_FRAME_P	Transmit data frame, differential input, positive terminal 发射数据帧，差分输入，正端	I
G10	FB_CLK_N	Transmit data clock, differential input, negative terminal 发射数据时钟，差分输入，负端	I
G11	DATA_CLK_P	Receive data clock, differential output, positive terminal 接收数据时钟，差分输出，正端	O
G12	VSSD	Digital ground 数字地	I
H1	RX1B_P	Receive channel 1 input B, positive terminal 接收通道 1 输入 B，正端	I
H2	VSSA	Analog ground 模拟地	I
H3	VSSA	Analog ground 模拟地	I
H4	TXNRX	TX/RX state control signal for the enable state machine 使能状态机的 TX/RX 状态控制信号	I
H5	SYNC_IN		I

		Synchronization input signal 同步输入信号	
H6	VSSA	Analog ground 模拟地	I
H7	VSSD	Digital ground 数字地	I
H8	P1_D11/RX_D5_P	Port P1 D11 / receive D5, differential output, positive terminal 端口 P1 D11 / 接收 D5，差分输出，正端	I/O
H9	TX_FRAME_N	Transmit data frame, differential input, negative terminal 发射数据帧，差分输入，负端	I
H10	VSSD	Digital ground 数字地	I
H11	DATA_CLK_N	Receive data clock, differential output, negative terminal 接收数据时钟，差分输出，负端	O
H12	VDD_INTERFACE	Digital I/O supply 数字 I/O 电源	I
J1	RX1B_N	Receive channel 1 input B, negative terminal 接收通道 1 输入 B，负端	I
J2	VSSA	Analog ground 模拟地	I
J3	VDDA1P3_RX_SYNTH	1.3 V supply 1.3 V 电源	I
J4	SPI_DI	SPI serial data input SPI 串行数据输入	I
J5	SPI_CLK	SPI clock input SPI 时钟输入	I
J6	CLK_OUT|	Clock output 时钟输出	O
J7	P1_D10/RX_D5_N	Port P1 D10 / receive D5, differential output, negative terminal 端口 P1 D10 / 接收 D5，差分输出，负端	I/O
J8	P1_D9/RX_D4_P	Port P1 D9 / receive D4, differential output, positive terminal 端口 P1 D9 / 接收 D4，差分输出，正端	I/O
J9	P1_D7/RX_D3_P	Port P1 D7 / receive D3, differential output, positive terminal 端口 P1 D7 / 接收 D3，差分输出，正端	I/O
J10	P1_D5/RX_D2_P	Port P1 D5 / receive D2, differential output, positive terminal 端口 P1 D5 / 接收 D2，差分输出，正端	I/O
J11	P1_D3/RX_D1_P	Port P1 D3 / receive D1, differential output, positive terminal 端口 P1 D3 / 接收 D1，差分输出，正端	I/O
J12	P1_D1/RX_D0_P	Port P1 D1 / receive D0, differential output, positive terminal 端口 P1 D1 / 接收 D0，差分输出，正端	I/O
K1	RX1C_P	Receive channel 1 input C, positive terminal 接收通道 1 输入 C，正端	I
K2	VSSA	Analog ground 模拟地	I
K3	VDDA1P3_TX_SYNTH	1.3 V supply 1.3 V 电源	I
K4	VDDA1P3_BB	1.3 V supply 1.3 V 电源	I
K5	RESETB	Reset input 复位输入	I
K6	SPI_ENB	SPI enable input SPI 使能输入	I
K7	P1_D8/RX_D4_N		I/O

		Port P1 D8 / receive D4, differential output, negative terminal 端口 P1 D8 / 接收 D4，差分输出，负端	
K8	P1_D6/RX_D3_N	Port P1 D6 / receive D3, differential output, negative terminal 端口 P1 D6 / 接收 D3，差分输出，负端	I/O
K9	P1_D4/RX_D2_N	Port P1 D4 / receive D2, differential output, negative terminal 端口 P1 D4 / 接收 D2，差分输出，负端	I/O
K10	P1_D2/RX_D1_N	Port P1 D2 / receive D1, differential output, negative terminal 端口 P1 D2 / 接收 D1，差分输出，负端	I/O
K11	P1_D0/RX_D0_N	Port P1 D0 / receive D0, differential output, negative terminal 端口 P1 D0 / 接收 D0，差分输出，负端	I/O
K12	VSSD	Digital ground 数字地	I
L1	RX1C_N	Receive channel 1 input C, negative terminal 接收通道 1 输入 C，负端	I
L2	VSSA	Analog ground 模拟地	I
L3	VSSA	Analog ground 模拟地	I
L4	RBIAS	Bias input reference 偏置输入参考	I
L5	AUXADC	Auxiliary ADC 辅助 ADC	I
L6	SPI_DO	SPI serial output SPI 串行输出	O
L7	VSSA	Analog ground 模拟地	I
L8	VSSA	Analog ground 模拟地	I
L9	VSSA	Analog ground 模拟地	I
L10	VSSA	Analog ground 模拟地	I
L11	VSSA	Analog ground 模拟地	I
L12	VSSA	Analog ground 模拟地	I
M1	RX1A_P	Receive channel 2 input A, positive terminal 接收通道 2 输入 A，正端	I
M2	RX1A_N	Receive channel 2 input A, negative terminal 接收通道 2 输入 A，负端	I
M3	NC	Leave unconnected (a) 不连接 (a)	/
M4	VSSA	Analog ground 模拟地	I
M5	TX_MON1	Transmit channel 1 power-monitor input 发射通道 1 功率监测输入	I
M6	VSSA	Analog ground 模拟地	I
M7	TX1A_P	Transmit channel 1 output A, positive terminal 发射通道 1 输出 A，正端	O
M8	TX1A_N	Transmit channel 1 output A, negative terminal 发射通道 1 输出 A，负端	O
M9	TX1B_P		O

		Transmit channel 1 output B, positive terminal 发射通道 1 输出 B，正端	
M10	TX1B_N|	Transmit channel 1 output B, negative terminal 发射通道 1 输出 B，负端	O
M11	XTALP	Reference-frequency crystal connection / external clock input 参考频率晶体连接 / 外部时钟输入	I
M12	XTALN	Reference-frequency crystal connection 参考频率晶体连接	I

a Leave this pin floating during use. Do not connect it.

a 使用时此引脚应悬空。不要连接。

Absolute Maximum Ratings / 绝对最大额定值

Parameter 参数	Rating 额定值
Analog/digital core supply to ground (VDDx to VSSx) 模拟/数字核心电源对地 (VDDx 至 VSSx)	−0.3 V to 1.4 V
Interface supply to ground (VDD_INTERFACE to VSSx) 接口电源对地 (VDD_INTERFACE 至 VSSx)	−0.3 V to 3.0 V
GPO supply to ground (VDD_GPO to VSSx) GPO 电源对地 (VDD_GPO 至 VSSx)	−0.3 V to 3.9 V
Logic input/output to ground (VSSx) 逻辑输入/输出对地 (VSSx)	−0.3 V to VDD_INTERFACE + 0.3 V
Input current at any pin except supply pins 除电源引脚外任意引脚的输入电流	±10 mA
RF input (peak power) RF 输入（峰值功率）	2.5 dBm
TX monitor input power (peak power) TX 监测输入功率（峰值功率）	9 dBm
Package power dissipation 封装功耗	(TJMAX − TA)/θJA
Maximum junction temperature (TJMAX) 最高结温 (TJMAX)	125 °C
Storage temperature (Tstg) 存储温度 (Tstg)	−65 °C to 150 °C

Recommended Operating Conditions / 推荐工作条件

Parameter 参数	Condition 条件
Input reference clock 输入参考时钟	40 MHz
Analog/digital core supply voltage (VDDX) 模拟/数字核心电源电压 (VDDX)	1.27 V to 1.33 V
Interface voltage (VDD_INTERFACE), CMOS 接口电压 (VDD_INTERFACE)，CMOS	1.14 V to 2.625 V
Interface voltage (VDD_INTERFACE), LVDS 接口电压 (VDD_INTERFACE)，LVDS	1.71 V to 2.625 V
GPO voltage (VDD_GPO) GPO 电压 (VDD_GPO)	1.3 V to 3.3 V
Operating ambient temperature (TA) 工作环境温度 (TA)	−40 °C to 85 °C

Electrical Specifications / 电气规格

Unless otherwise specified: VDDA1P3_RX_LO = 1.3 V; VDDA1P3_TX_LO = 1.3 V; VDDA1P3_RX_RF = 1.3 V; VDDA1P3_RX_TX = 1.3 V; VDDA1P3_TX_LO_BUFFER = 1.3 V; VDDA1P3_RX_SYNTH = 1.3 V; VDDA1P3_TX_SYNTH = 1.3 V; VDDA1P3_BB = 1.3 V; VDDD1P3_DIG = 1.3 V; VDD_GPO = 3.3 V; VDD_INTERFACE = 1.8 V; VSSD = VSS = 0 V; internal LO mode; −40 °C ≤ TA ≤ 85 °C.

除非另有规定：VDDA1P3_RX_LO = 1.3 V；VDDA1P3_TX_LO = 1.3 V；VDDA1P3_RX_RF = 1.3 V；VDDA1P3_RX_TX = 1.3 V；VDDA1P3_TX_LO_BUFFER = 1.3 V；VDDA1P3_RX_SYNTH = 1.3 V；VDDA1P3_TX_SYNTH = 1.3 V；VDDA1P3_BB = 1.3 V；VDDD1P3_DIG = 1.3 V；VDD_GPO = 3.3 V；VDD_INTERFACE = 1.8 V；VSSD = VSS = 0 V；内部本振模式；−40 °C ≤ TA ≤ 85 °C。

Receiver (Frequency-Independent Parameters) / 接收机（与频率无关的参数）

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Center frequency 中心频率	F_0	RX1A/RX2A RX1A/RX2A	70	—	6000	MHz
Gain control range 增益控制范围	Gain_Range	800MHz 800MHz	—	71.5	—	dB
Gain control range 增益控制范围	Gain_Range	2300MHz(RX1A,RX2A) 2300MHz(RX1A,RX2A)	—	70	—	dB
Gain control range 增益控制范围	Gain_Range	2300MHz(RX1B,RX2B,RX1C,RX2C) 2300MHz(RX1B,RX2B,RX1C,RX2C)	—	70	—	dB
Gain control range 增益控制范围	Gain_Range	5500MHz(RX1A,RX2A) 5500MHz(RX1A,RX2A)	—	62	—	dB
Gain step 增益步进	GS	— —	—	1	—	dB
Received signal strength indicator range 接收信号强度指示范围	RSSI_Range	RX1A/RX2A RX1A/RX2A	—	95	—	dB
Received signal strength indicator accuracy 接收信号强度指示精度	—	— —	—	±2.5	—	dB

Receiver, 800 MHz / 接收机，800 MHz

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Noise figure 噪声系数	NF	Maximum RX gain 最大 RX 增益	—	2.	—	dB
Third-order input intercept point 三阶输入截点	IIP3	RX1A/RX2A, maximum RX gain RX1A/RX2A，最大 RX 增益	—	-11	—	dBm
Second-order input intercept point 二阶输入截点	IIP2	RX1A/RX2A, maximum RX gain RX1A/RX2A，最大 RX 增益	—	55	—	dBm
Digital-domain LO leakage 数字域本振泄漏	LOL	At the RX front end 在 RX 前端	—	-82	—	dBm
Quadrature gain error 正交增益误差	—	— —	—	0.2	—	%
Quadrature phase error 正交相位误差	—	— —	—	0.2	—	°
Modulation accuracy 调制精度	EVM_RX	— —	—	(Not tested)	—	—
	—		—	(Not tested)	—	—

Input S11 输入 S11		— —				
RX1A to RX2A isolation RX1A 到 RX2A 隔离度	ISO_RX	— —	—	68	—	dB
RX1C to RX2C isolation RX1C 到 RX2C 隔离度	ISO_RX	— —	—	68	—	dB
RX1B to RX2B isolation RX1B 到 RX2B 隔离度	ISO_RX	— —	—	55	—	dB
RX2A to RX1A isolation RX2A 到 RX1A 隔离度	ISO_RX	— —	—	68	—	dB
RX2C to RX1C isolation RX2C 到 RX1C 隔离度	ISO_RX	— —	—	68	—	dB
RX2B to RX1B isolation RX2B 到 RX1B 隔离度	ISO_RX	— —	—	55	—	dB

Receiver, 2.4 GHz / 接收机，2.4 GHz

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Noise figure 噪声系数	NF	Maximum RX gain 最大 RX 增益	—	3.5	—	dB
Third-order input intercept point 三阶输入截点	IIP3	RX1A/RX2A, maximum RX gain RX1A/RX2A，最大 RX 增益	—	-10	—	dBm
Second-order input intercept point 二阶输入截点	IIP2	RX1A/RX2A, maximum RX gain RX1A/RX2A，最大 RX 增益	—	48	—	dBm
Digital-domain LO leakage 数字域本振泄漏	LOL	At the RX front end 在 RX 前端	—	-82	—	dBm
Quadrature gain error 正交增益误差	—	— —	—	0.2	—	%
Quadrature phase error 正交相位误差	—	— —	—	0.2	—	°
Modulation accuracy 调制精度	EVM_RX	— —	—	(Not tested)	—	—
Input S11 输入 S11	—	— —	—	(Not tested)	—	—
RX1A to RX2A isolation RX1A 到 RX2A 隔离度	ISO_RX	— —	—	55	—	dB
RX1C to RX2C isolation RX1C 到 RX2C 隔离度	ISO_RX	— —	—	55	—	dB
RX1B to RX2B isolation RX1B 到 RX2B 隔离度	ISO_RX	— —	—	50	—	dB
RX2A to RX1A isolation RX2A 到 RX1A 隔离度	ISO_RX	— —	—	55	—	dB
RX2C to RX1C isolation RX2C 到 RX1C 隔离度	ISO_RX	— —	—	55	—	dB
RX2B to RX1B isolation RX2B 到 RX1B 隔离度	ISO_RX	— —	—	50	—	dB

Receiver, 5.5 GHz / 接收机，5.5 GHz

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Noise figure 噪声系数	NF	Maximum RX gain 最大 RX 增益	—	4	—	dB

Third-order input intercept point 三阶输入截点	IIP3	RX1A/RX2A, maximum RX gain RX1A/RX2A，最大 RX 增益	—	-4	—	dBm
Second-order input intercept point 二阶输入截点	IIP2	RX1A/RX2A, maximum RX gain RX1A/RX2A，最大 RX 增益	—	58	—	dBm
Digital-domain LO leakage 数字域本振泄漏	LOL	At the RX front end 在 RX 前端	—	-75	—	dBm
Quadrature gain error 正交增益误差	—	— —	—	0.2	—	%
Quadrature phase error 正交相位误差	—	— —	—	0.2	—	°
Modulation accuracy 调制精度	EVM_RX	— —	—	(Not tested)	—	—
Input S11 输入 S11	—	— —	—	(Not tested)	—	—
RX1A to RX2A isolation RX1A 到 RX2A 隔离度	ISO_RX	— —	—	50	—	dB
RX2A to RX1A isolation RX2A 到 RX1A 隔离度	ISO_RX	— —	—	37	—	dB

Transmitter (Frequency-Independent Parameters) / 发射机（与频率无关的参数）

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Center frequency 中心频率	F_0	TX1A/TX2A TX1A/TX2A	70	—	6000	MHz
Power control range 功率控制范围	PCR	TX1A/TX2A TX1A/TX2A	—	90	—	dB
Power control resolution 功率控制分辨率	PRes	TX1A/TX2A TX1A/TX2A	—	0.25	—	dB

Transmitter, 800 MHz / 发射机，800 MHz

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Output S22 输出 S22	—	— —	—	(Not tested)	—	—
Maximum output power 最大输出功率	PO	1 MHz single-tone signal into a 50 Ω load 1 MHz 单音信号，负载 50 Ω	—	8	—	dBm
Modulation accuracy 调制精度	EVM_TX	19.2 MHz reference clock 19.2 MHz 参考时钟	—	-45	—	dB
Third-order output intercept point 三阶输出截点	OIP3	— —	—	17	—	dBm
Carrier leakage 载波泄漏	CL	0 dB attenuation 0 dB 衰减	—	-50	—	dBc
Carrier leakage 载波泄漏	CL	40 dB attenuation 40 dB 衰减	—	-40	—	dBc
Noise floor 噪声底	NSD	TX1A/TX2A, at 90 MHz offset TX1A/TX2A，90 MHz 偏置处	—	-148	—	dBm/Hz
TX1 to TX2 isolation TX1 到 TX2 隔离度	ISO_TX	— —	—	50	—	dB
TX2 to TX1 isolation TX2 到 TX1 隔离度	ISO_TX	— —	—	50	—	dB

Transmitter, 2.4 GHz / 发射机，2.4 GHz

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Output S22 输出 S22	—	— —	—	(Not tested)	—	—
Maximum output power 最大输出功率	PO	1 MHz single-tone signal into a 50 Ω load 1 MHz 单音信号，负载 50 Ω	—	7	—	dBm
Modulation accuracy 调制精度	EVM_TX	40 MHz reference clock 40 MHz 参考时钟	—	-40	—	dB
Third-order output intercept point 三阶输出截点	OIP3	— —	—	17.5	—	dBm
Carrier leakage 载波泄漏	CL	0 dB attenuation 0 dB 衰减	—	-50	—	dBc
Carrier leakage 载波泄漏	CL	40 dB attenuation 40 dB 衰减	—	-44	—	dBc
Noise floor 噪声底	NSD	TX1A/TX2A, at 90 MHz offset TX1A/TX2A，90 MHz 偏置处	—	-138	—	dBm/Hz
TX1 to TX2 isolation TX1 到 TX2 隔离度	ISO_TX	— —	—	50	—	dB
TX2 to TX1 isolation TX2 到 TX1 隔离度	ISO_TX	— —	—	50	—	dB

Transmitter, 5.5 GHz / 发射机，5.5 GHz

Parameter 参数	Symbol 符号	Conditions 条件	Min 最小	Typ 典型	Max 最大	Unit 单位
Output S22 输出 S22	—	— —	—	(Not tested)	—	—
Maximum output power 最大输出功率	PO	7.7 MHz single-tone signal into a 50 Ω load 7.7 MHz 单音信号，负载 50 Ω	—	4.2	—	dBm
Modulation accuracy 调制精度	EVM_TX	40 MHz reference clock 40 MHz 参考时钟	—	-34.5	—	dB
Third-order output intercept point 三阶输出截点	OIP3	— —	—	13	—	dBm
Carrier leakage 载波泄漏	CL	0 dB attenuation 0 dB 衰减	—	-50	—	dBc
Carrier leakage 载波泄漏	CL	40 dB attenuation 40 dB 衰减	—	-42	—	dBc
Noise floor 噪声底	NSD	TX1A/TX2A, at 90 MHz offset TX1A/TX2A，90 MHz 偏置处	—	-137	—	dBm/Hz
TX1 to TX2 isolation TX1 到 TX2 隔离度	ISO_TX	— —	—	50	—	dB
TX2 to TX1 isolation TX2 到 TX1 隔离度	ISO_TX	— —	—	50	—	dB

Note: Typical values are test data obtained at room temperature.

注：典型值为室温下获得的测试数据。

Typical Performance Characteristics (Electrical Test Plots) / 典型性能特性（电气测试图）

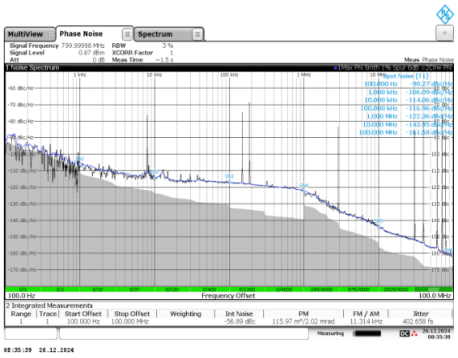


Figure 5. LO Phase Noise (800 MHz Band) / 图 5. 本振相位噪声（800 MHz 频段）

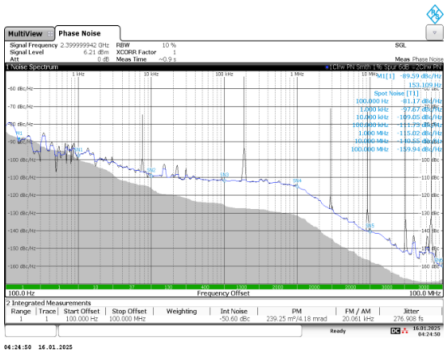


Figure 6. LO Phase Noise (2.4 GHz Band) / 图 6. 本振相位噪声（2.4 GHz 频段）

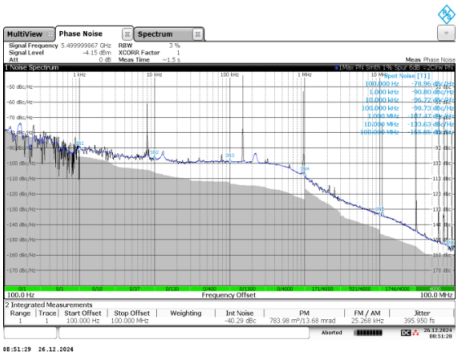


Figure 7. LO Phase Noise (5.5 GHz Band) / 图 7. 本振相位噪声（5.5 GHz 频段）

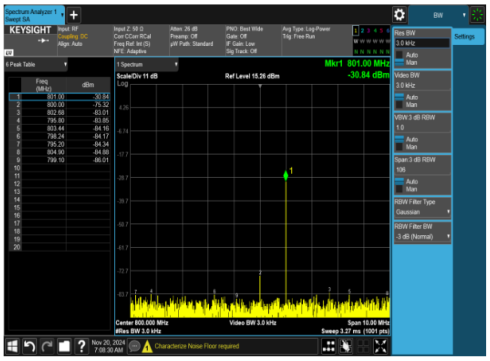


Figure 8. TX Output at 40 dB Attenuation (800 MHz Band) / 图 8. TX 输出，40 dB 衰减（800 MHz 频段）



Figure 9. TX EVM (800 MHz Band) / 图 9. TX EVM（800 MHz 频段）

Band)

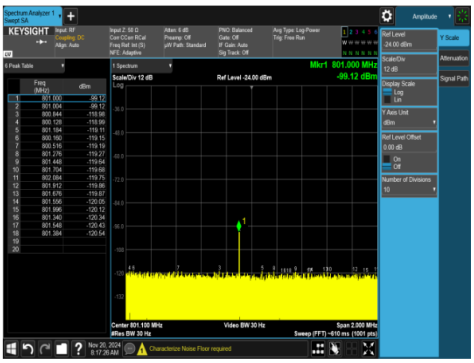


Figure 10. TX Isolation (800 MHz Band) / 图 10. TX 隔离度（800 MHz 频段）

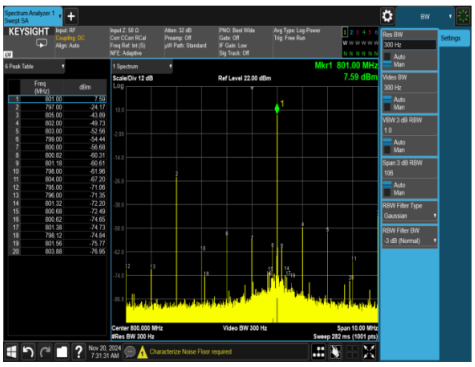


Figure 11. TX Maximum Output (800 MHz Band) / 图 11. TX 最大输出（800 MHz 频段）

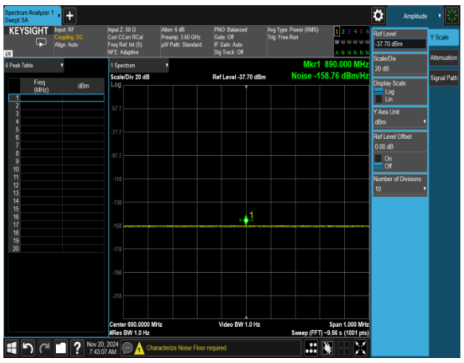


Figure 12. TX Noise Floor (800 MHz Band) / 图 12. TX 噪声底（800 MHz 频段）

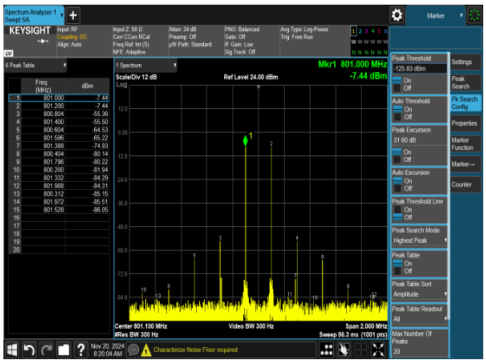


Figure 13. TX OIP3 (800 MHz Band) / 图 13. TX OIP3（800 MHz 频段）

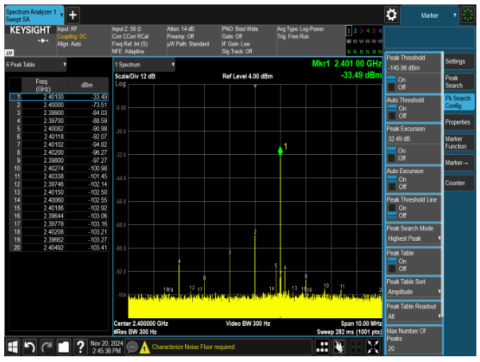


Figure 14. TX Output at 40 dB Attenuation (2.4 GHz Band) / 图 14. TX 输出，40 dB 衰减（2.4 GHz 频段）

Band)

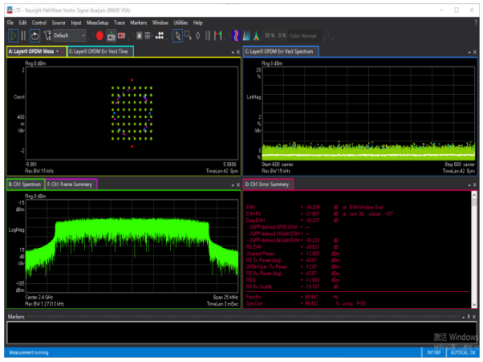


Figure 15. TX EVM (2.4 GHz Band) / 图 15. TX EVM（2.4 GHz 频段）

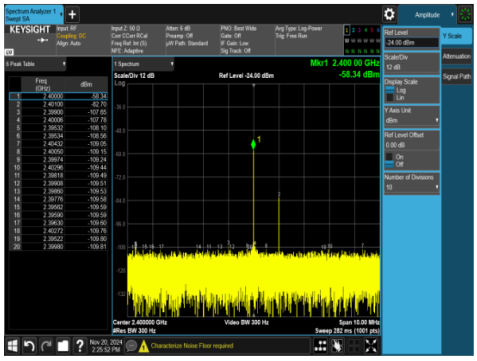


Figure 16. TX Isolation (2.4 GHz Band) / 图 16. TX 隔离度（2.4 GHz 频段）

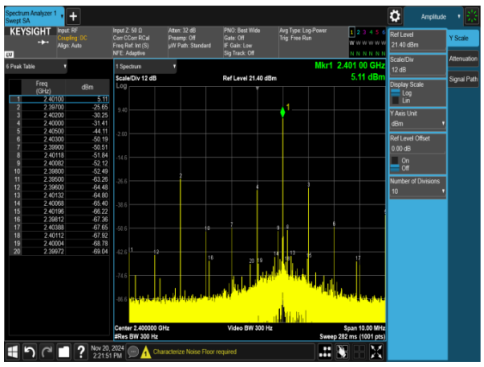


Figure 17. TX Maximum Output (2.4 GHz Band) / 图 17. TX 最大输出（2.4 GHz 频段）

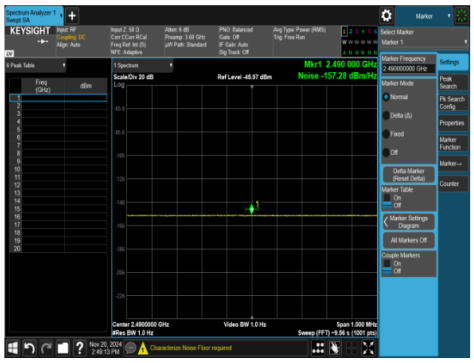


Figure 18. TX Noise Floor (2.4 GHz Band) / 图 18. TX 噪声底（2.4 GHz 频段）

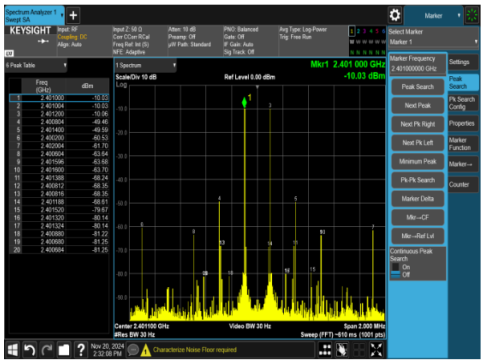


Figure 19. TX OIP3 (2.4 GHz Band) / 图 19. TX OIP3（2.4 GHz 频段）

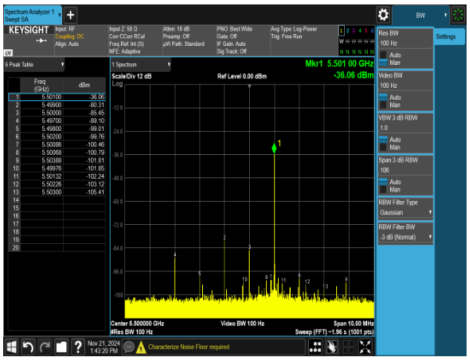


Figure 20. TX Output at 40 dB Attenuation (5.5 GHz Band) / 图 20. TX 输出，40 dB 衰减（5.5 GHz 频段）

Band)

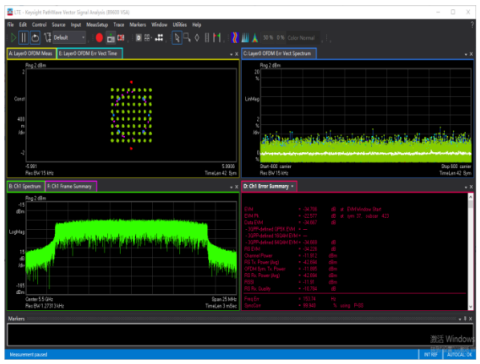


Figure 21. TX EVM (5.5 GHz Band) / 图 21. TX EVM（5.5 GHz 频段）

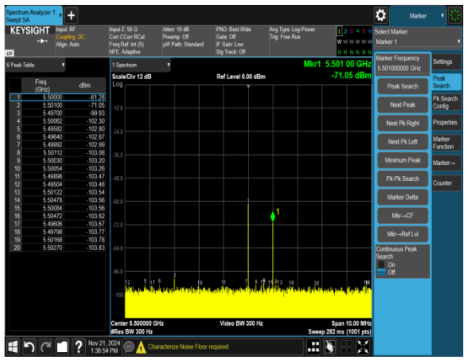


Figure 22. TX Isolation (5.5 GHz Band) / 图 22. TX 隔离度（5.5 GHz 频段）

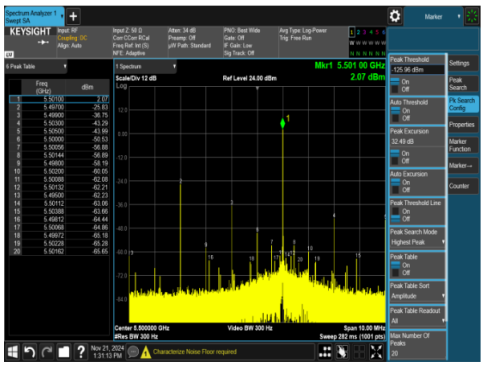


Figure 23. TX Maximum Output (5.5 GHz Band) / 图 23. TX 最大输出（5.5 GHz 频段）

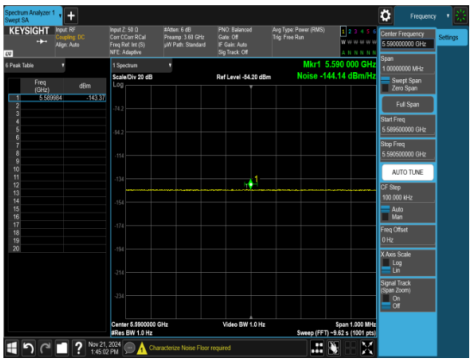


Figure 24. TX Noise Floor (5.5 GHz Band) / 图 24. TX 噪声底（5.5 GHz 频段）

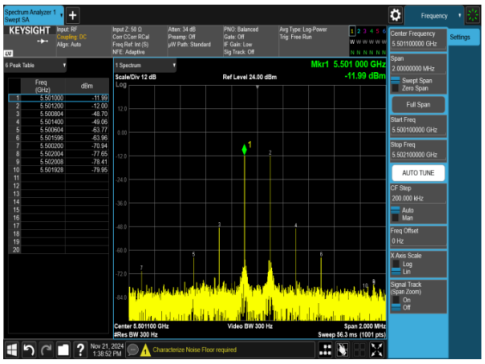


Figure 25. TX OIP3 (5.5 GHz Band) / 图 25. TX OIP3（5.5 GHz 频段）

Typical Application Circuit / 典型应用电路

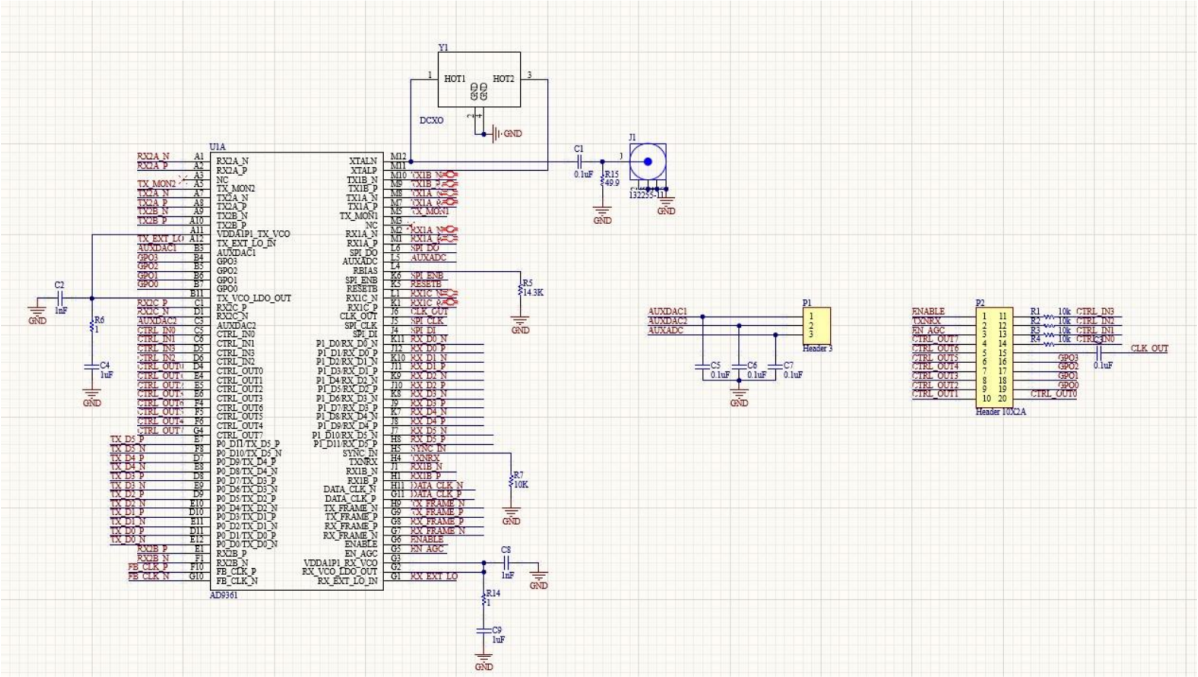


Figure 26. SXS046 Typical Application Circuit / 图 26. SXS046 典型应用电路

Functional Blocks and Operating Principles / 功能模块与工作原理

1. Overview / 1. 概述

The SXS046 dual-receiver, dual-transmitter, 56 MHz frequency-agile transceiver SoC is a semiconductor integrated circuit manufactured using a CMOS process. This highly integrated radio-frequency (RF) transceiver can be configured for a broad range of applications. A single device integrates all RF, mixed-signal, and digital blocks necessary to provide all transceiver functions. Its programmability allows this wideband transceiver to support multiple communication standards, including frequency-division duplex (FDD) and time-division duplex (TDD) systems.

SXS046 双接收、双发射、56 MHz 捷变频收发器 SoC 是一款采用 CMOS 工艺制造的半导体集成电路。这种高集成度射频 (RF) 收发器可针对广泛的应用进行配置。单个器件集成了提供全部收发功能所需的全部 RF、混合信号和数字模块。其可编程性使该宽带收发器能够支持多种通信标准，包括频分双工 (FDD) 和时分双工 (TDD) 系统。

This programmability also allows connection to a variety of baseband processors (BBPs) through a single-channel 12-bit parallel data port, a dual-channel 12-bit parallel data port, or a 12-bit low-voltage differential signaling (LVDS) interface.

这种可编程性还允许通过单通道 12 位并行数据端口、双通道 12 位并行数据端口或 12 位低压差分信号 (LVDS) 接口连接各种基带处理器 (BBP)。

The device also provides self-calibration and automatic gain control (AGC) systems to maintain high performance over a range of temperatures and input-signal conditions. In addition, several test modes allow system designers to insert test tones and create internal loopback modes to debug designs during prototyping and optimize the radio configuration for specific applications.

该器件还提供自校准和自动增益控制（AGC）系统，以在一系列温度和输入信号条件下保持高性能。此外，多种测试模式允许系统设计人员插入测试音并创建内部环回模式，以便在原型开发期间调试设计，并针对特定应用优化无线电配置。

2. Receiver / 2. 接收机

The analog input consists of a differential switched-capacitor sample-and-hold structure. The differential structure provides better AC performance at high input frequencies. The common-mode voltage of differential inputs INP and INM is 0.95 V, supplied by the on-chip VCM pin. The maximum differential input swing is 2 VPP.

模拟输入由差分开关电容采样保持结构组成。差分结构在高输入频率下提供更好的交流性能。差分输入 INP 和 INM 的共模电压为 0.95 V，由片上 VCM 引脚提供。最大差分输入摆幅为 2 VPP。

The receiver section contains all blocks required to receive RF signals and convert them into digital data for use by the BBP. Two independently controlled channels can receive signals from different sources, allowing the device to be used in multiple-input, multiple-output (MIMO) systems while sharing a common frequency synthesizer. Each channel has three inputs that can be multiplexed into the signal chain, allowing SXS046 to support diversity systems with multiple antenna inputs. The receiver is a direct-conversion system containing a low-noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band-shaping filters. These filters downconvert the received signals to baseband for digitization. An external LNA can also be connected to the device, giving designers considerable flexibility to customize the receiver front end for specific applications.

接收机部分包含接收 RF 信号并将其转换为供 BBP 使用的数字数据所需的全部模块。两个独立控制的通道可以接收来自不同来源的信号，使该器件可用于多输入多输出 (MIMO) 系统，同时共用一个频率合成器。每个通道有三个可复用至信号链的输入，使 SXS046 能够支持具有多个天线输入的分集系统。接收机是一个直接变频系统，包含低噪声放大器 (LNA)，其后是匹配的同相 (I) 和正交 (Q) 放大器、混频器和带宽整形滤波器。这些滤波器将接收信号下变频至基带以进行数字化。外部 LNA 也可以连接到该器件，为设计人员定制特定应用的接收机前端提供相当大的灵活性。

Gain control is implemented through a preprogrammed gain-index map that distributes gain among the various blocks to optimize performance at each level. This can be achieved by enabling the internal AGC in fast or slow mode, or through manual gain control, allowing the BBP to adjust gain as needed. Each channel also has independent RSSI measurement, DC-offset tracking, and all circuitry required for self-calibration. The receiver includes 12-bit sigma-delta ADCs with adjustable sampling rates to generate data streams from the received signals. The digitized signals can be further conditioned through a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sampling rate of each digital-filter block can be adjusted by changing the decimation factor to obtain the required output data rate.

增益控制通过预编程的增益索引映射实现，该映射在各个模块之间分配增益，以在每个电平下优化性能。这可以通过启用内部 AGC 的快速或慢速模式实现，或通过手动增益控制实现，允许 BBP 根据需要调整增益。每个通道还具有独立的 RSSI 测量、DC 偏移跟踪以及自校准所需的全部电路。接收机包括具有可调采样率的 12 位 sigma-delta ADC，用于从接收信号生成数据流。数字化信号可通过一系列抽取滤波器和具有附加抽取设置的完全可编程 128 抽头 FIR 滤波器进一步处理。每个数字滤波器模块的采样率可通过改变抽取因子来调整，以获得所需的输出数据率。

3. Transmitter / 3. 发射机

The transmitter section contains two identical, independently controlled channels, providing all digital-processing, mixed-signal, and RF blocks required for a direct-conversion system while sharing a common frequency synthesizer. Digital data received from the BBP passes through a fully programmable 128-tap FIR filter without an interpolation option. The FIR output is sent to a series of interpolation filters that provide additional filtering and data-rate interpolation before reaching the DACs. Each 12-bit DAC has an adjustable sampling rate. The I and Q channels are both fed to the RF block for upconversion.

发射机部分包含两个相同、独立控制的通道，在共用一个频率合成器的同时，提供直接变频系统所需的全部数字处理、混合信号和 RF 模块。来自 BBP 的数字数据通过一个无插值选项的完全可编程 128 抽头 FIR 滤波器。FIR 输出被送至一系列插值滤波器，在到达 DAC 之前提供附加滤波和数据率插值。每个 12 位 DAC 具有可调的采样率。I 和 Q 通道均被送至 RF 模块进行上变频。

When converted into analog baseband signals, the I and Q signals are filtered to remove sampling artifacts and then fed into upconversion mixers. Here, the I and Q signals are recombined and modulated at the carrier frequency for delivery to the output stage. The combined signals also pass through analog filters that provide additional band shaping before reaching the output amplifiers. Each transmit channel provides a wide range of fine attenuation adjustment to help designers optimize the signal-to-noise ratio (SNR).

当 I 和 Q 信号转换为模拟基带信号时，它们被滤波以去除采样伪影，然后送入上变频混频器。在这里，I 和 Q 信号被重新组合并在载波频率上调制，送至输出级。组合信号还通过模拟滤波器，在到达输出放大器之前提供附加的带宽整形。每个发射通道提供宽范围的精细衰减调整，帮助设计人员优化信噪比 (SNR)。

Each transmit channel includes self-calibration circuitry to support automatic real-time adjustment. The transmitter block also provides a TX monitor block for each channel. This block monitors the transmitter output and routes it back to the BBP through an unused receiver channel for signal monitoring. The TX monitor block is available only in TDD mode when the receiver is idle.

每个发射通道包括自校准电路，以支持自动实时调整。发射机模块还为每个通道提供 TX 监测模块。该模块监测发射机输出，并通过未使用的接收通道将其返回至 BBP 进行信号监测。TX 监测模块仅在接收机空闲的 TDD 模式下可用。

4. Clock Input Options / 4. 时钟输入选项

The reference clock used by SXS046 can be provided by two different sources. The first option is a dedicated crystal with a frequency between 19 MHz and 50 MHz, connected between the XTALP and XTALN pins. The second option is an external oscillator or clock-distribution device, such as AD9548, connected to XTALN with XTALP left unconnected. If an external oscillator is used, its frequency can range from 10 MHz to 80 MHz. This reference clock powers the frequency-synthesizer blocks, which generate all data clocks, sampling clocks, and local oscillators internally. Crystal-frequency errors can be removed by adjusting on-chip variable capacitance using the digitally programmable, digitally controlled crystal oscillator (DCXO) function. This capacitance can tune crystal-frequency variations in the system, producing a more accurate reference clock from which all other frequencies are generated. This function can also be used with on-chip temperature sensing to provide oscillator-frequency temperature compensation during normal operation.

SXS046 使用的参考时钟可由两种不同的来源提供。第一种选择是专用晶体，频率在 19 MHz 至 50 MHz 之间，连接在 XTALP 和 XTALN 引脚之间。第二种选择是外部振荡器或时钟分配器件，例如 AD9548，连接到 XTALN，XTALP 不连接。如果使用外部振荡器，其频率范围可为 10 MHz 至 80 MHz。该参考时钟为频率合成器模块供电，频率合成器在内部生成全部数据时钟、采样时钟和本振。晶体频率误差可通过使用数字可编程、数字控制晶体振荡器 (DCXO) 功能调整片上可变电容来消除。该电容可调节系统中的晶体频率变化，产生更准确的参考时钟，其他全部频率均由此生成。该功能还可与片上温度传感一起使用，在正常工作期间提供振荡器频率温度补偿。

5. Frequency Synthesizers / 5. 频率合成器

SXS046 contains two identical frequency synthesizers that generate the LO signals required for the RF signal paths: one for the receiver and one for the transmitter. The phase-locked loop (PLL) frequency synthesizers use a fractional-N design with fully integrated voltage-controlled oscillators (VCOs) and loop filters. In TDD operation, the synthesizers are turned on and off as required by the RX and TX frames. In FDD mode, the TX PLL and RX PLL can be active simultaneously. These PLLs require no external components.

SXS046 包含两个相同的频率合成器，生成 RF 信号路径所需的本振信号：一个用于接收机，一个用于发射机。锁相环 (PLL) 频率合成器采用小数 N 分频设计，具有完全集成的压控振荡器 (VCO) 和环路滤波器。在 TDD 工作模式下，合成器根据 RX 和 TX 帧的要求开启和关闭。在 FDD 模式下，TX PLL 和 RX PLL 可同时工作。这些 PLL 不需要外部元件。

SXS046 also contains a baseband PLL frequency synthesizer that generates all baseband-related clock signals, including the ADC and DAC sampling clocks, DATA_CLK (see “Digital Data Interface”), and all data-frame signals. This PLL has a programmable frequency range of 700 MHz to 1400 MHz, depending on the system data-rate and sampling-rate requirements.

SXS046 还包含一个基带 PLL 频率合成器，生成全部与基带相关的时钟信号，包括 ADC 和 DAC 采样时钟、DATA_CLK（见“数字数据接口”）和全部数据帧信号。该 PLL 具有 700 MHz 至 1400 MHz 的可编程频率范围，具体取决于系统数据率和采样率要求。

6. Digital Data Interface / 6. 数字数据接口

The SXS046 data interface uses parallel data ports P0 and P1 to transfer data between the device and the BBP. These ports can be configured for single-ended CMOS or differential LVDS operation. Both formats support multiple configurations to meet system requirements for data ordering and data-port connections. These include single-port and dual-port data buses, single and double data rates, and various data-ordering combinations that transfer data from different channels across the bus at the appropriate times. Bus transfers are controlled by simple hardware handshake signals. Both ports can operate in bidirectional TDD mode or full-duplex FDD mode. In FDD mode, half the bits carry transmit data and half carry receive data. The interface can also be configured to use only one data port for applications that do not require high data rates and prefer fewer interface pins.

SXS046 数据接口使用并行数据端口 P0 和 P1 在器件与 BBP 之间传输数据。这些端口可配置为单端 CMOS 或差分 LVDS 操作。两种格式都支持多种配置，以满足数据排序和数据端口连接的系统要求。这些配置包括单端口和双端口数据总线、单倍和双倍数据率，以及在适当时间跨总线传输不同通道数据的各种数据排序组合。总线传输由简单的硬件握手信号控制。两个端口都可以在双向 TDD 模式或全双工 FDD 模式下工作。在 FDD 模式下，一半位携带发射数据，另一半位携带接收数据。该接口还可配置为仅使用一个数据端口，适用于不需要高数据率且希望减少接口引脚的应用。

7. DATA_CLK Signal / 7. DATA_CLK 信号

RX data provides the DATA_CLK signal, which the BBP can use when receiving data. DATA_CLK can be set to a rate providing single-data-rate (SDR) timing, with data sampled at each rising clock edge, or double-data-rate (DDR) timing, with data captured at both rising and falling edges. This timing applies to operating modes using either one port or both ports.

RX 数据提供 DATA_CLK 信号，BBP 在接收数据时可使用该信号。DATA_CLK 可设置为提供单倍数据率 (SDR) 时序的速率，数据在每个时钟上升沿采样；或双倍数据率 (DDR) 时序，数据在上升沿和下降沿均被捕获。该时序适用于使用一个端口或两个端口的工作模式。

Registers / 寄存器

Refer to the SXS046 Register Map & Software Migration Guide. Controlled documentation is available from SHENXIN TECH upon request.

请参阅《SXS046 寄存器映射与软件迁移指南》。受控文档可向 SHENXIN TECH 索取。

ESD Protection / ESD 保护

Protection Between Power Supplies and Ground / 电源与地之间的保护

To improve the device's electrostatic-discharge immunity, the following ESD protection circuits are provided internally between the power-supply pins. Each ESD protection diode has a forward voltage drop of approximately 0.35 V. Avoid prolonged forward conduction of these protection diodes during power-up and normal operation.

为提高器件的静电放电抗扰度，电源引脚之间内部提供以下 ESD 保护电路。每个 ESD 保护二极管的正向压降约为 0.35 V。在上电和正常工作期间，避免这些保护二极管长时间正向导通。

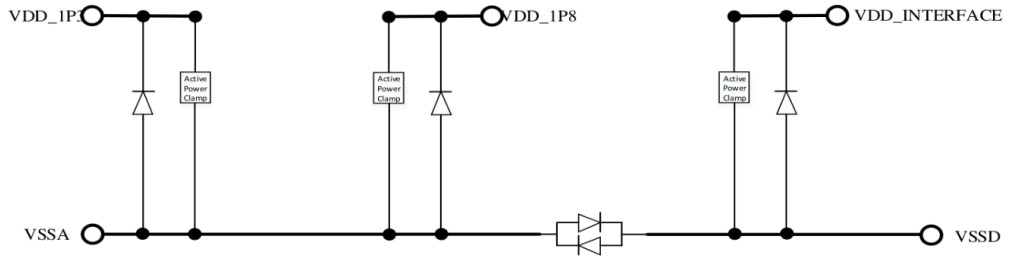


Figure 27. Internal ESD Protection Circuit Between Power Supplies / 图 27. 电源之间内部 ESD 保护电路

Precautions / 注意事项

1. Product Installation Precautions / 1. 产品安装注意事项

- Observe the device orientation during soldering to avoid incorrect installation.
- 焊接时注意器件方向，避免安装错误。
- All instruments and meters used for circuit debugging must have a sound common ground. Ensure proper grounding and power-supply decoupling in the PCB design.
- 用于电路调试的全部仪器仪表必须具有良好的公共接地。在 PCB 设计中确保正确接地和电源去耦。
- Avoid reverse power-supply connections and short circuits between the input/output terminals and the power supply, as these can damage the circuit.
- 避免电源反接和输入/输出端与电源之间短路，因为这些可能损坏电路。

2. Product Usage Precautions / 2. 产品使用注意事项

- Power-up requirements: simultaneous application of the analog and digital supplies is recommended, or apply the analog supply first.
- 上电要求：建议模拟电源和数字电源同时施加，或先施加模拟电源。
- Use low-ESR capacitors for decoupling at the LDO outputs.
- 在 LDO 输出端使用低 ESR 电容进行去耦。
- A large PCB ground area is recommended. This can eliminate potential differences caused by different grounding points and reduce the effects of board-generated capacitance on the circuit.
- 建议使用大面积的 PCB 接地。这可以消除不同接地点引起的电位差，并减少板上产生的电容对电路的影响。
- Connect one 1 µF or 0.1 µF capacitor close to each power-supply pin.
- 在每个电源引脚附近连接一个 1 µF 或 0.1 µF 电容。
- If differential analog inputs are used, the differential input traces must have equal lengths.
- 如果使用差分模拟输入，差分输入走线必须等长。
- Keep the digital and analog power supplies separate.
- 数字电源和模拟电源保持分开。

3. Product Protection Precautions / 3. 产品防护注意事项

- All device terminals incorporate ESD protection structures. However, high-energy electrical pulses may still damage the circuit. Apply ESD protection during testing, handling, and storage.
- 全部器件端子均集成 ESD 保护结构。但是，高能量电脉冲仍可能损坏电路。在测试、搬运和存储期间采取 ESD 防护。
- Exceeding the absolute maximum ratings may permanently damage the device. These are limiting ratings only and do not imply normal operation under these conditions or under any other conditions beyond those stated in this product manual.
- 超过绝对最大额定值可能对器件造成永久性损坏。这些仅为极限额定值，并不意味着在这些条件下或在本产品手册所述之外的任何其他条件下可以正常工作。
- Provided that direct exposure to rain and snow is prevented, cartons containing the product may be transported by safe means. Do not stack them with acidic, alkaline, or other corrosive materials. Packaging must be secure; existing means of transport may be used.
- 在防止雨雪直接淋袭的条件下，装有产品的纸箱可通过安全方式运输。不要与酸性、碱性或其他腐蚀性材料堆放在一起。包装必须牢固；可使用现有运输工具。
- The storage environment for packaged products must meet the Class I warehouse conditions specified in Section 8.1 of Q/W 657A: temperature 15 °C to 25 °C and humidity 25% to 65%. The environment must be

well ventilated, free of acidic, alkaline, or other corrosive gases, and equipped with appropriate ESD protection.

- 包装产品的存储环境必须满足 Q/W 657A 第 8.1 节规定的 I 类仓库条件：温度 15 °C 至 25 °C，湿度 25% 至 65%。环境必须通风良好，无酸性、碱性或其他腐蚀性气体，并配备适当的 ESD 防护。

4. Assembly Instructions and Handling Requirements (This Section Has Not Been Updated; Verification by a Specialist Is Required) / 4. 组装说明与搬运要求（本节尚未更新；需要由专业人员核实）

- This product has a moisture-sensitivity level of MSL3. The permissible exposure to ambient conditions after removal from the moisture-barrier bag, dry storage, or baking and before reflow soldering is 168 h at ≤30 °C / 60% RH.
- 本产品的湿敏等级为 MSL3。从防潮袋中取出、干燥存储或烘烤后、回流焊接之前，允许暴露于环境条件的时间为 168 h，条件为 ≤30 °C / 60% RH。
- If device storage conditions cannot be controlled or traced, strictly perform baking at 125 °C for 8 h before assembly.
- 如果器件存储条件无法控制或追溯，组装前严格按 125 °C 烘烤 8 h。
- If assembly-environment temperature and humidity cannot be maintained at ≤30 °C / 60% RH, complete soldering within 12 h after baking.
- 如果组装环境温度和湿度无法维持在 ≤30 °C / 60% RH，烘烤后在 12 h 内完成焊接。
- After baking, the product is highly susceptible to electrostatic charging. Apply ESD protection throughout all operations.
- 烘烤后，产品极易产生静电充电。在全部操作过程中采取 ESD 防护。
- For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak-temperature range is 210 °C to 235 °C. The maximum peak temperature should not exceed 235 °C. Time within ±5 °C of the peak temperature must be ≤20 s; time above liquidus must be 60 to 90 s; the heating rate must be 2 to 4 °C/s; and the cooling rate must be 2 to 6 °C/s.
- 对于使用有铅回流焊接 (Sn63Pb37) 的板级组装，推荐峰值温度范围为 210 °C 至 235 °C。最高峰值温度不应超过 235 °C。峰值温度 ±5 °C 以内的时间必须 ≤20 s；液相线以上的时间必须为 60 至 90 s；加热速率必须为 2 至 4 °C/s；冷却速率必须为 2 至 6 °C/s。
- For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak-temperature range is 230 °C to 245 °C. The maximum peak temperature should not exceed 260 °C. Time within ±5 °C of the peak temperature must be ≤20 s; time above liquidus must be 60 to 90 s; the heating rate must be 2 to 4 °C/s; and the cooling rate must be 2 to 6 °C/s.
- 对于使用无铅回流焊接 (SAC305) 的板级组装，推荐峰值温度范围为 230 °C 至 245 °C。最高峰值温度不应超过 260 °C。峰值温度 ±5 °C 以内的时间必须 ≤20 s；液相线以上的时间必须为 60 至 90 s；加热速率必须为 2 至 4 °C/s；冷却速率必须为 2 至 6 °C/s。
- 1. If a mixed assembly process requires a higher temperature, ensure that the device-body temperature does not exceed 260 °C. The device-body temperature is measured at the top surface of the device during reflow soldering.
- 1. 如果混合组装工艺需要更高的温度，确保器件本体温度不超过 260 °C。器件本体温度在回流焊接期间于器件顶面测量。
- 2. This product uses lead-free/leaded solder balls made of SAC305.
- 2. 本产品使用 SAC305 制成的无铅/有铅焊球。

Common Faults and Troubleshooting / 常见故障与处理办法

- No signal output: check whether a clock signal is present at the clock terminal, verify the power-supply and ground connections, and ensure that the input and reference voltages are correct.
- 无信号输出：检查时钟端是否有时钟信号，核对电源和接地连接，并确保输入电压和参考电压正确。
- Output data jitter: check the external circuitry and connections and ensure that the reference voltage is stable.
- 输出数据抖动：检查外部电路和连接，并确保参考电压稳定。
- Unstable device operation: check the power supply and ensure that the supply voltage is stable.
- 器件工作不稳定：检查电源，并确保电源电压稳定。

Contact Information / 联系信息

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