SHENXIN TECH

RF Agile Transceivers / High-Speed Data Converters

SXS046

2T2R RF Transceiver SoC | 56 MHz Tunable Channel Bandwidth

Customer Edition

Derived from controlled engineering source: V1.20260807

RF RANGE

70 MHz to 6 GHz

CHANNEL BANDWIDTH

<200 kHz to 56 MHz

DATA CONVERTERS

2T2R | 12-bit DAC / ADC

PACKAGE

CSP_BGA144 | -40°C to +85°C

DESIGN-IN POSITIONING

SXS046 is a Pin-to-Pin Replacement for AD9361. Existing hardware designs can reuse the PCB; register configuration adaptation is required.

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Document Control

SHENXIN TECH | Customer Edition

PRODUCT	SXS046
ENGINEERING SOURCE VERSION	V1.20260807
CUSTOMER EDITION DATE	09 October 2026
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Customer-edition scope

- Customer-facing edition with verified electrical specifications retained.
- Internal comparison notes and preliminary test-board comments have been excluded.
- Controlled register and PCB assembly documentation is available upon request.

This customer edition preserves the controlled electrical specifications and operating limits from the engineering source. Request controlled register and PCB assembly documentation before a design release.

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Customer edition excludes internal comparison notes and preliminary test-board comments. Detailed controlled engineering documentation is available from SHENXIN TECH upon request.

Applications

- Point-to-point communication systems
- Microcell base stations
- General-purpose radio systems

Features

- Supply voltages: 1.3 V / 1.8 V / 3.3 V
- RF 2 × 2 transceiver integrating 12-bit DACs and ADCs
- Frequency range: 70 MHz to 6.0 GHz
- Supports TDD and FDD
- Tunable channel bandwidth: <200 kHz to 56 MHz
- TX EVM: −40 dB
- Circuit interface: CMOS/LVDS digital interface
- ESD rating: Class 1B, HBM 500 V
- Product weight: 0.32 g ± 0.02 g

Product Description

SXS046 is a high-performance, highly integrated radio-frequency (RF) fast-hopping transceiver intended for 3G and 4G base-station applications. Its programmability and wideband capability make it an ideal choice for a wide range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section, integrates frequency synthesizers, and provides a configurable digital interface to the processor, simplifying design integration. SXS046 operates from 70 MHz to 6.0 GHz, covering most licensed and unlicensed bands, and supports channel bandwidths from less than 200 kHz to 56 MHz.

The two independent direct-conversion receivers provide outstanding noise figure and linearity. Each receive (RX) subsystem has independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital filtering, eliminating the need to implement these functions in the digital baseband. SXS046 also provides a flexible manual gain mode that supports external control. Each channel contains two high-dynamic-range ADCs that first digitize the received I and Q signals and then pass them through configurable decimation filters and a 128-tap finite impulse response (FIR) filter, producing a 12-bit output at the appropriate sample rate.

The transmitter uses a direct-conversion architecture to achieve high modulation accuracy and extremely low noise. This transmitter design provides low TX EVM, with a value <−40 dB, leaving substantial system margin for selection of an external power amplifier. The on-chip transmit (TX) power monitors can serve as power detectors to enable highly accurate TX power measurements.

Fully integrated phase-locked loops (PLLs) provide low-power fractional-N frequency synthesis for all receive and transmit channels. The design incorporates the channel isolation required for frequency-division duplex (FDD) systems. All VCO and loop-filter components are also integrated.

Standard

- Quality grade: Enterprise standard

The device uses a 10 mm × 10 mm, 144-pin chip-scale ball grid array package (CSP_BGA). The functional block diagram is shown in Figure 1.

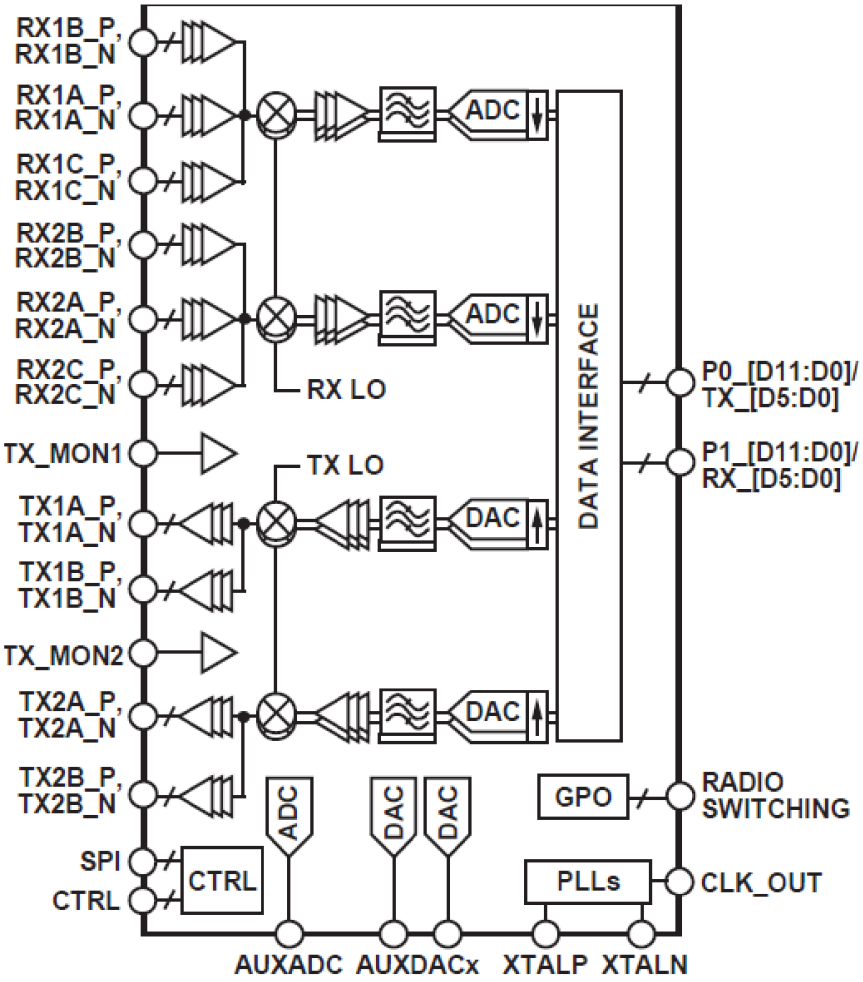


Figure 1. Functional Block Diagram

Note: 1. RX and TX Baseband Bandwidth Calibration

The clock for baseband bandwidth calibration is obtained by dividing the master clock. The RX division factor is determined by Reg1F8[7:0] (BBF Tune Divide), and the TX division factor by Reg0D6[7:0]. This division factor must not be odd; that is, Reg1F8[0] and Reg0D6[0] must not be set to 1. The division factor is jointly determined by the BBPLL frequency and the baseband bandwidth, using the following equation:

BBF Tune Divide[8:0] = ceil((BBPLL Freq * ln(2)) / (BBBW * 1.4 * 2 * π))

When initializing the chip, avoid setting the values of the two registers above to 1, and verify both register values after initialization. If a value is 1, one feasible method is to adjust the baseband bandwidth and reinitialize the chip to avoid setting either register to 1.

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Note: 2. RX Channel I/Q Mismatch

With a 1.8G local oscillator and a high temperature of 80 °C ± 4 °C, there is a possibility of I/Q mismatch in the receive channel RX (the foreign product exhibits mismatch at −20 °C).

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Package Outline and Product Images

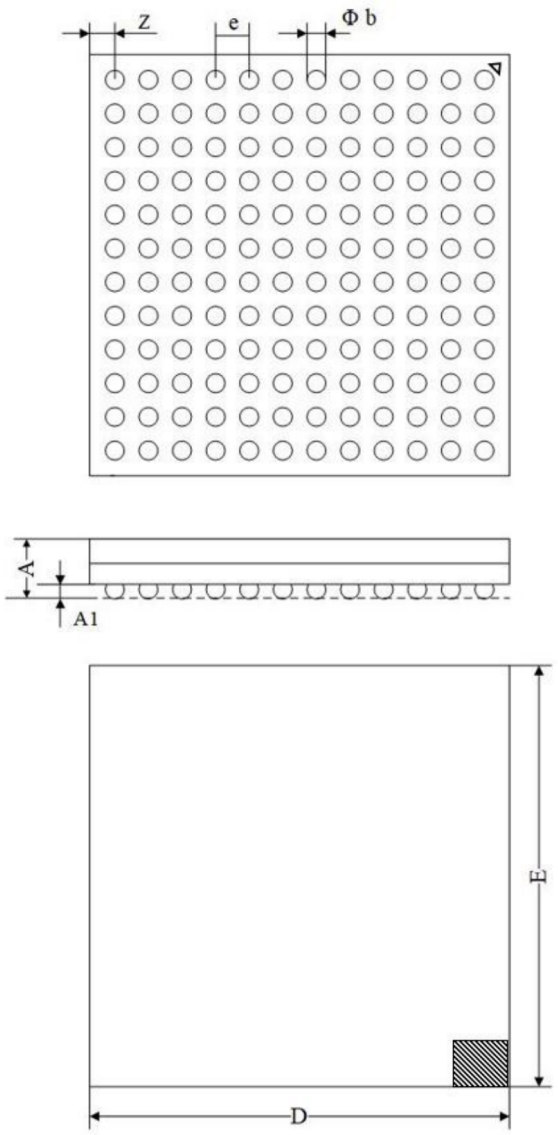


Figure 2. Package Outline Dimensions

Figure 3. Dimensions (Unit: mm)

Symbol	Min	Nominal	Max	Symbol	Min	Nominal	Max
A	1.27	1.42[a]	1.57	e	—	0.80	—
A1	0.30	0.35[a]	0.40	Φb	0.40	0.45[a]	0.50
D	9.80	10.00[a]	10.20	Z	—	0.60[a]	0.70
E	9.80	10.00[a]	10.20				

[a] Actual nominal package dimension; users are advised to use this dimension as a reference when designing the application.

Note: For the recommended land pattern, see Assembly Instructions.

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Pin Configuration (Top View)

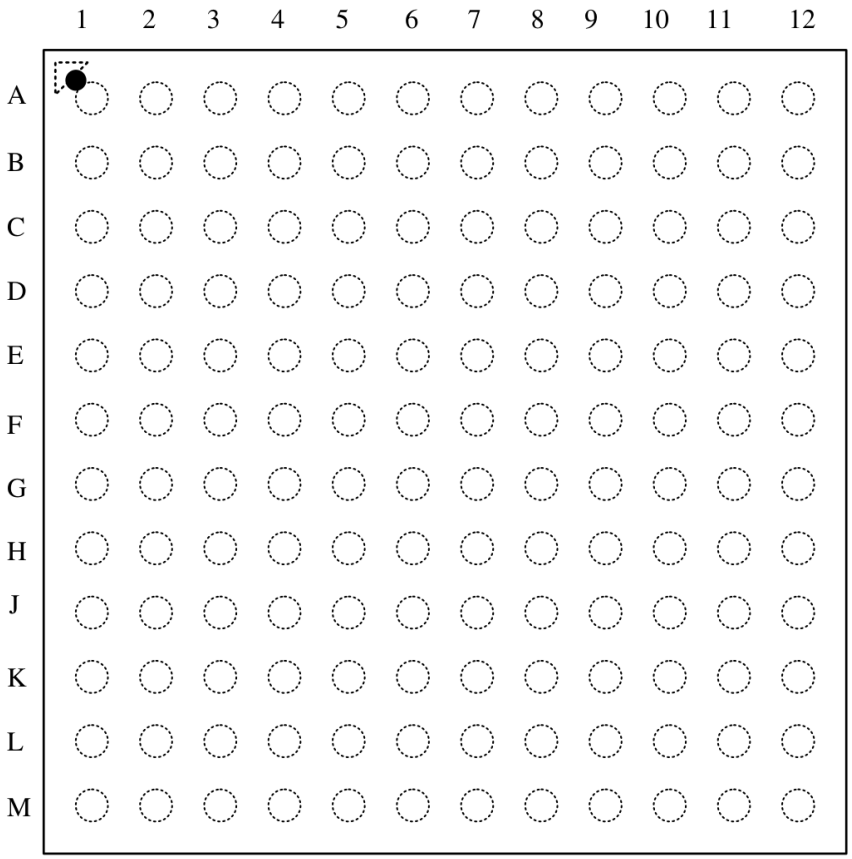


Figure 4. Pin Configuration

Pin Function Table

Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
A1	RX2A_N	Receive channel 2 input A, negative terminal	I	G1	RX_EXT_LO_IN	RX external LO signal input	I
A2	RX2A_P	Receive channel 2 input A, positive terminal	I	G2	RX_VCO_LDO_OUT	Receive VCO LDO output	O
A3	NC	Leave unconnected[a]	/	G3	VDDA1P1_RX_VCO	Receive VCO LDO input	I
A4	VSSA	Analog ground	I	G4	CTRL_OUT7	Control output 7	O
A5	TX_MON2	Transmit channel 2 power-monitor input	I	G5	EN_AGC	Manual control input for automatic gain control (AGC)	I
A6	VSSA	Analog ground	I	G6	ENABLE	Enable signal for the enable state machine	I
A7	TX2A_N	Transmit channel 2 output A, negative terminal	O	G7	RX_FRAME_N	Receive data frame, differential output, negative terminal	O
A8	TX2A_P	Transmit channel 2 output A, positive terminal	O	G8	RX_FRAME_P	Receive data frame, differential output, positive terminal	O

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Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
A9	TX2B_N	Transmit channel 2 output B, negative terminal	O	G9	TX_FRAME_P	Transmit data frame, differential input, positive terminal	I
A10	TX2B_P	Transmit channel 2 output B, positive terminal	O	G10	FB_CLK_N	Transmit data clock, differential input, negative terminal	I
A11	VDDA1P1_TX_VCO	Transmit VCO supply input	I	G11	DATA_CLK_P	Receive data clock, differential output, positive terminal	O
A12	TX_EXT_LO_IN	TX external LO signal input	I	G12	VSSD	Digital ground	I
B1	VSSA	Analog ground	I	H1	RX1B_P	Receive channel 1 input B, positive terminal	I
B2	VSSA	Analog ground	I	H2	VSSA	Analog ground	I
B3	AUXDAC1	Auxiliary DAC1 output	O	H3	VSSA	Analog ground	I

Pin Function Table (Continued)

Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
B4	GPO_3	General-purpose output 3	O	H4	TXNRX	TX/RX state control signal for the enable state machine	I
B5	GPO_2	General-purpose output 2	O	H5	SYNC_IN	Synchronization input signal	I
B6	GPO_1	General-purpose output 1	O	H6	VSSA	Analog ground	I
B7	GPO_0	General-purpose output 0	O	H7	VSSD	Digital ground	I
B8	VDD_GPO	Auxiliary DAC and GPO supply	I	H8	P1_D11/RX_D5_P	Port P1 D11 / receive D5, differential output, positive terminal	I/O
B9	VDDA1P3_TX_LO	Transmit LO 1.3 V supply	I	H9	TX_FRAME_N	Transmit data frame, differential input, negative terminal	I
B10	VDDA1P3_TX_VCO_LDO	Transmit VCO LDO supply input	I	H10	VSSD	Digital ground	I
B11	TX_VCO_LDO_OUT	Transmit VCO LDO supply output	O	H11	DATA_CLK_N	Receive data clock, differential output, negative terminal	O
B12	VSSA	Analog ground	I	H12	VDD_INTERFACE	Digital I/O supply	I
C1	RX2C_P	Receive channel 2 input C, positive terminal	I	J1	RX1B_N	Receive channel 1 input B, negative terminal	I
C2	VSSA	Analog ground	I	J2	VSSA	Analog ground	I
C3	AUXDAC2	Auxiliary DAC2 output	O	J3	VDDA1P3_RX_SYNTH	1.3 V supply	I
C4	TEST/ENABLE	Test input	I	J4	SPI_DI	SPI serial data input	I
C5	CTRL_IN0	Control input 0	I	J5	SPI_CLK	SPI clock input	I
C6	CTRL_IN1	Control input 1	I	J6	CLK_OUT	Clock output	O

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Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
C7	VSSA	Analog ground	I	J7	P1_D10/RX_D5_N	Port P1 D10 / receive D5, differential output, negative terminal	I/O
C8	VSSA	Analog ground	I	J8	P1_D9/RX_D4_P	Port P1 D9 / receive D4, differential output, positive terminal	I/O
C9	VSSA	Analog ground	I	J9	P1_D7/RX_D3_P	Port P1 D7 / receive D3, differential output, positive terminal	I/O
C10	VSSA	Analog ground	I	J10	P1_D5/RX_D2_P	Port P1 D5 / receive D2, differential output, positive terminal	I/O
C11	VSSA	Analog ground	I	J11	P1_D3/RX_D1_P	Port P1 D3 / receive D1, differential output, positive terminal	I/O
C12	VSSA	Analog ground	I	J12	P1_D1/RX_D0_P	Port P1 D1 / receive D0, differential output, positive terminal	I/O
D1	RX2C_N	Receive channel 2 input C, negative terminal	I	K1	RX1C_P	Receive channel 1 input C, positive terminal	I
D2	VDDA1P3_RX_RF	Receiver 1.3 V supply	I	K2	VSSA	Analog ground	I
D3	VDDA1P3_RX_TX	1.3 V supply	I	K3	VDDA1P3_TX_SYNTH	1.3 V supply	I
D4	CTRL_OUT0	Control output 0	O	K4	VDDA1P3_BB	1.3 V supply	I
D5	CTRL_IN3	Control input 3	I	K5	RESETB	Reset input	I

Pin Function Table (Continued)

Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
D6	CTRL_IN2	Control input 2	I	K6	SPI_ENB	SPI enable input	I
D7	P0_D9/TX_D4_P	Port P0 D9 / transmit D4, differential input, positive terminal	I/O	K7	P1_D8/RX_D4_N	Port P1 D8 / receive D4, differential output, negative terminal	I/O
D8	P0_D7/TX_D3_P	Port P0 D7 / transmit D3, differential input, positive terminal	I/O	K8	P1_D6/RX_D3_N	Port P1 D6 / receive D3, differential output, negative terminal	I/O
D9	P0_D5/TX_D2_P	Port P0 D5 / transmit D2, differential input, positive terminal	I/O	K9	P1_D4/RX_D2_N	Port P1 D4 / receive D2, differential output, negative terminal	I/O
D10	P0_D3/TX_D1_P	Port P0 D3 / transmit D1, differential input, positive terminal	I/O	K10	P1_D2/RX_D1_N	Port P1 D2 / receive D1, differential output, negative terminal	I/O
D11	P0_D1/TX_D0_P	Port P0 D1 / transmit D0, differential input, positive terminal	I/O	K11	P1_D0/RX_D0_N	Port P1 D0 / receive D0, differential output, negative terminal	I/O
D12	VSSD	Digital ground	I	K12	VSSD	Digital ground	I
E1	RX2B_P	Receive channel 2 input B, positive terminal	I	L1	RX1C_N	Receive channel 1 input C, negative terminal	I
E2	VDDA1P3_RX_LO	Receive LO 1.3 V supply	I	L2	VSSA	Analog ground	I

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Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
E3	VDDA1P3_TX_LO_BUFFER	Transmit LO 1.3 V supply	I	L3	VSSA	Analog ground	I
E4	CTRL_OUT1	Control output 1	O	L4	RBIAS	Bias input reference	I
E5	CTRL_OUT2	Control output 2	O	L5	AUXADC	Auxiliary ADC	I
E6	CTRL_OUT3	Control output 3	O	L6	SPI_DO	SPI serial output	O
E7	P0_D11/TX_D5_P	Port P0 D11 / transmit D5, differential input, positive terminal	I/O	L7	VSSA	Analog ground	I
E8	P0_D8/TX_D4_N	Port P0 D8 / transmit D4, differential input, negative terminal	I/O	L8	VSSA	Analog ground	I
E9	P0_D6/TX_D3_N	Port P0 D6 / transmit D3, differential input, negative terminal	I/O	L9	VSSA	Analog ground	I
E10	P0_D4/TX_D2_N	Port P0 D4 / transmit D2, differential input, negative terminal	I/O	L10	VSSA	Analog ground	I
E11	P0_D2/TX_D1_N	Port P0 D2 / transmit D1, differential input, negative terminal	I/O	L11	VSSA	Analog ground	I
E12	P0_D0/TX_D0_N	Port P0 D0 / transmit D0, differential input, negative terminal	I/O	L12	VSSA	Analog ground	I
F1	RX2B_N	Receive channel 2 input B, negative terminal	I	M1	RX1A_P	Receive channel 2 input A, positive terminal	I
F2	VDDA1P3_RX_VCO_LDO	Receive VCO LDO supply input	I	M2	RX1A_N	Receive channel 2 input A, negative terminal	I
F3	VSSA	Analog ground	I	M3	NC	Leave unconnected[a]	/
F4	CTRL_OUT6	Control output 6	O	M4	VSSA	Analog ground	I
F5	CTRL_OUT5	Control output 5	O	M5	TX_MON1	Transmit channel 1 power-monitor input	I
F6	CTRL_OUT4	Control output 6	O	M6	VSSA	Analog ground	I

Pin Function Table (Continued)

Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
F7	VSSD	Digital ground	I	M7	TX1A_P	Transmit channel 1 output A, positive terminal	O
F8	P0_D10/TX_D5_N	Port P0 D10 / transmit D5, differential input, negative terminal	I/O	M8	TX1A_N	Transmit channel 1 output A, negative terminal	O
F9	VSSD	Digital ground	I	M9	TX1B_P	Transmit channel 1 output B, positive terminal	O
F10	FB_CLK_P	TX data clock input, positive terminal	I	M10	TX1B_N	Transmit channel 1 output B, negative terminal	O

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Pin	Symbol	Function	I/O	Pin	Symbol	Function	I/O
F11	VSSD	Digital ground	I	M11	XTALP	Reference-frequency crystal connection / external clock input	I
F12	VDDD1P3_DIG	1.3 V digital supply	I	M12	XTALN	Reference-frequency crystal connection	I

[a] Leave this pin floating during use. Do not connect it.

Absolute Maximum Ratings

Parameter	Rating
Analog/digital core supply to ground (VDDx to VSSx)	−0.3 V to 1.4 V
Interface supply to ground (VDD_INTERFACE to VSSx)	−0.3 V to 3.0 V
GPO supply to ground (VDD_GPO to VSSx)	−0.3 V to 3.9 V
Logic input/output to ground (VSSx)	−0.3 V to VDD_INTERFACE + 0.3 V
Input current at any pin except supply pins	±10 mA
RF input (peak power)	2.5 dBm
TX monitor input power (peak power)	9 dBm
Package power dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum junction temperature (T_{JMAX})	125 °C
Storage temperature (T_{stg})	−65 °C to 150 °C

Recommended Operating Conditions

Parameter	Condition
Input reference clock	40 MHz
Analog/digital core supply voltage (VDDX)	1.27 V to 1.33 V
Interface voltage (VDD_INTERFACE), CMOS	1.14 V to 2.625 V
Interface voltage (VDD_INTERFACE), LVDS	1.71 V to 2.625 V
GPO voltage (VDD_GPO)	1.3 V to 3.3 V
Operating ambient temperature (T_A)	−40 °C to 85 °C

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Electrical Specifications

Unless otherwise specified: VDDA1P3_RX_LO = 1.3 V; VDDA1P3_TX_LO = 1.3 V; VDDA1P3_RX_RF = 1.3 V; VDDA1P3_RX_TX = 1.3 V; VDDA1P3_TX_LO_BUFFER = 1.3 V; VDDA1P3_RX_SYNTH = 1.3 V; VDDA1P3_TX_SYNTH = 1.3 V; VDDA1P3_BB = 1.3 V; VDDD1P3_DIG = 1.3 V; VDD_GPO = 3.3 V; VDD_INTERFACE = 1.8 V; VSSD = VSS = 0 V; internal LO mode; −40 °C ≤ T_A ≤ 85 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Receiver (Frequency-Independent Parameters)						
Center frequency	F_0	RX1A/RX2A	70	—	6000	MHz
Gain control range	Gain_Range	800MHz	—	71.5	—	dB
Gain control range	Gain_Range	2300MHz(RX1A,RX2A)	—	70	—	dB
Gain control range	Gain_Range	2300MHz(RX1B,RX2B,RX1C, RX2C)	—	70	—	dB
Gain control range	Gain_Range	5500MHz(RX1A,RX2A)	—	62	—	dB
Gain step	GS	—	—	1	—	dB
Received signal strength indicator range	RSSI_Range	RX1A/RX2A	—	95	—	dB
Received signal strength indicator accuracy	—	—	—	±2.5	—	dB
Receiver, 800 MHz						
Noise figure	NF	Maximum RX gain	—	2.	—	dB
Third-order input intercept point	IIP3	RX1A/RX2A, maximum RX gain	—	-11	—	dBm
Second-order input intercept point	IIP2	RX1A/RX2A, maximum RX gain	—	55	—	dBm
Digital-domain LO leakage	LOL	At the RX front end	—	-82	—	dBm
Quadrature gain error	—	—	—	0.2	—	%
Quadrature phase error	—	—	—	0.2	—	°
Modulation accuracy	EVM_RX	—	—	(Not tested)	—	—
Input S11	—	—	—	(Not tested)	—	—

Electrical Specifications (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RX1A to RX2A isolation	ISO_RX	—	—	68	—	dB
RX1C to RX2C isolation	ISO_RX	—	—	68	—	dB
RX1B to RX2B isolation	ISO_RX	—	—	55	—	dB
RX2A to RX1A isolation	ISO_RX	—	—	68	—	dB
RX2C to RX1C isolation	ISO_RX	—	—	68	—	dB
RX2B to RX1B isolation	ISO_RX	—	—	55	—	dB

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Receiver, 2.4 GHz						
Noise figure	NF	Maximum RX gain	—	3.5	—	dB
Third-order input intercept point	IIP3	RX1A/RX2A, maximum RX gain	—	-10	—	dBm
Second-order input intercept point	IIP2	RX1A/RX2A, maximum RX gain	—	48	—	dBm
Digital-domain LO leakage	LOL	At the RX front end	—	-82	—	dBm
Quadrature gain error	—	—	—	0.2	—	%
Quadrature phase error	—	—	—	0.2	—	°
Modulation accuracy	EVM_RX	—	—	(Not tested)	—	—
Input S11	—	—	—	(Not tested)	—	—
RX1A to RX2A isolation	ISO_RX	—	—	55	—	dB
RX1C to RX2C isolation	ISO_RX	—	—	55	—	dB
RX1B to RX2B isolation	ISO_RX	—	—	50	—	dB
RX2A to RX1A isolation	ISO_RX	—	—	55	—	dB
RX2C to RX1C isolation	ISO_RX	—	—	55	—	dB
RX2B to RX1B isolation	ISO_RX	—	—	50	—	dB
Receiver, 5.5 GHz						
Noise figure	NF	Maximum RX gain	—	4	—	dB
Third-order input intercept point	IIP3	RX1A/RX2A, maximum RX gain	—	-4	—	dBm
Second-order input intercept point	IIP2	RX1A/RX2A, maximum RX gain	—	58	—	dBm
Digital-domain LO leakage	LOL	At the RX front end	—	-75	—	dBm
Quadrature gain error	—	—	—	0.2	—	%
Quadrature phase error	—	—	—	0.2	—	°
Modulation accuracy	EVM_RX	—	—	(Not tested)	—	—
Input S11	—	—	—	(Not tested)	—	—
RX1A to RX2A isolation	ISO_RX	—	—	50	—	dB
RX2A to RX1A isolation	ISO_RX	—	—	37	—	dB
Transmitter (Frequency-Independent Parameters)						
Center frequency	F_0	TX1A/TX2A	70	—	6000	MHz
Power control range	PCR	TX1A/TX2A	—	90	—	dB
Power control resolution	PRes	TX1A/TX2A	—	0.25	—	dB
Transmitter, 800 MHz						
Output S22	—	—	—	(Not tested)	—	—

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum output power	PO	1 MHz single-tone signal into a 50 Ω load	—	8	—	dBm
Modulation accuracy	EVM_TX	19.2 MHz reference clock	—	-45	—	dB

Electrical Specifications (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Third-order output intercept point	OIP3	—	—	17	—	dBm
Carrier leakage	CL	0 dB attenuation	—	-50	—	dBc
Carrier leakage	CL	40 dB attenuation	—	-40	—	dBc
Noise floor	NSD	TX1A/TX2A, at 90 MHz offset	—	-148	—	dBm/Hz
TX1 to TX2 isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 isolation	ISO_TX	—	—	50	—	dB
Transmitter, 2.4 GHz						
Output S22	—	—	—	(Not tested)	—	—
Maximum output power	PO	1 MHz single-tone signal into a 50 Ω load	—	7	—	dBm
Modulation accuracy	EVM_TX	40 MHz reference clock	—	-40	—	dB
Third-order output intercept point	OIP3	—	—	17.5	—	dBm
Carrier leakage	CL	0 dB attenuation	—	-50	—	dBc
Carrier leakage	CL	40 dB attenuation	—	-44	—	dBc
Noise floor	NSD	TX1A/TX2A, at 90 MHz offset	—	-138	—	dBm/Hz
TX1 to TX2 isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 isolation	ISO_TX	—	—	50	—	dB
Transmitter, 5.5 GHz						
Output S22	—	—	—	(Not tested)	—	—
Maximum output power	PO	7.7 MHz single-tone signal into a 50 Ω load	—	4.2	—	dBm
Modulation accuracy	EVM_TX	40 MHz reference clock	—	-34.5	—	dB
Third-order output intercept point	OIP3	—	—	13	—	dBm
Carrier leakage	CL	0 dB attenuation	—	-50	—	dBc
Carrier leakage	CL	40 dB attenuation	—	-42	—	dBc
Noise floor	NSD	TX1A/TX2A, at 90 MHz offset	—	-137	—	dBm/Hz
TX1 to TX2 isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 isolation	ISO_TX	—	—	50	—	dB

Note: Typical values are test data obtained at room temperature.

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Typical Performance Characteristics (Electrical Test Plots)

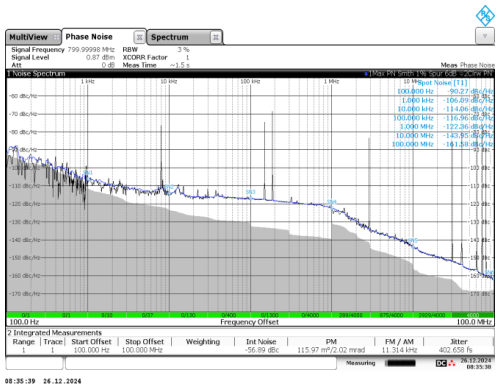


Figure 5. LO Phase Noise (800 MHz Band)

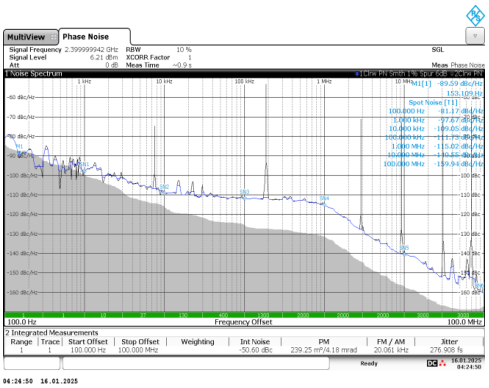


Figure 6. LO Phase Noise (2.4 GHz Band)

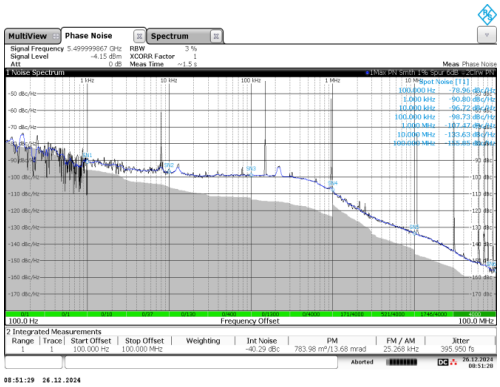


Figure 7. LO Phase Noise (5.5 GHz Band)

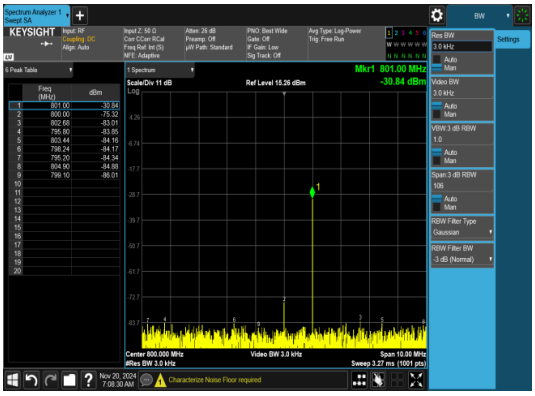


Figure 8. TX Output at 40 dB Attenuation (800 MHz Band)

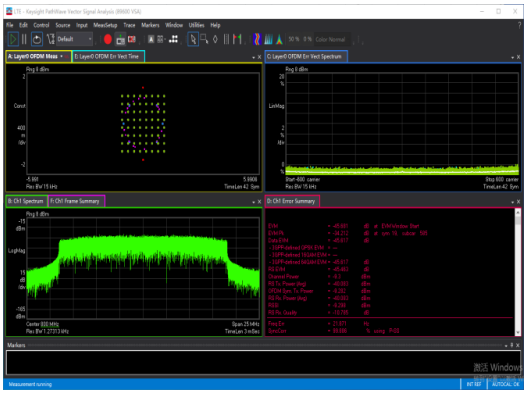


Figure 9. TX EVM (800 MHz Band)

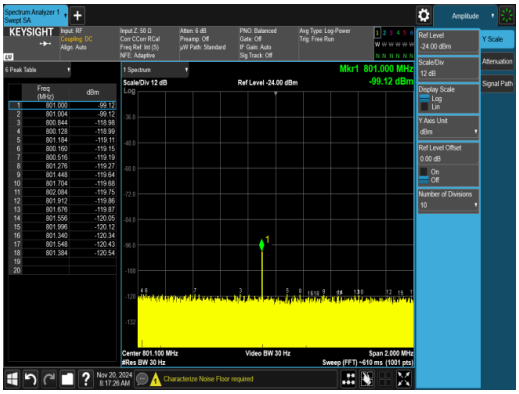


Figure 10. TX Isolation (800 MHz Band)

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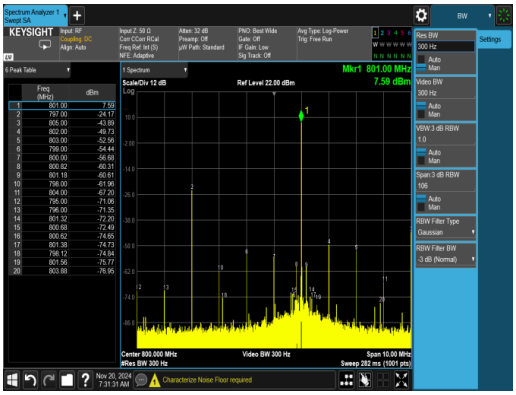


Figure 11. TX Maximum Output (800 MHz Band)

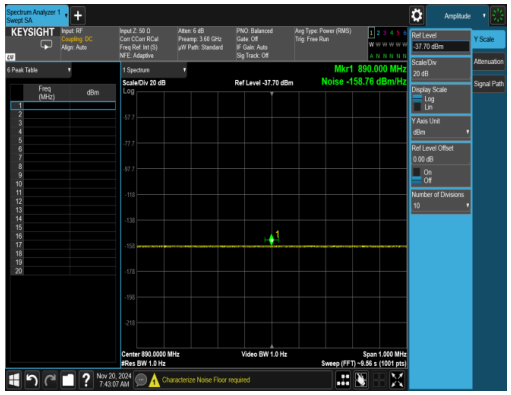


Figure 12. TX Noise Floor (800 MHz Band)

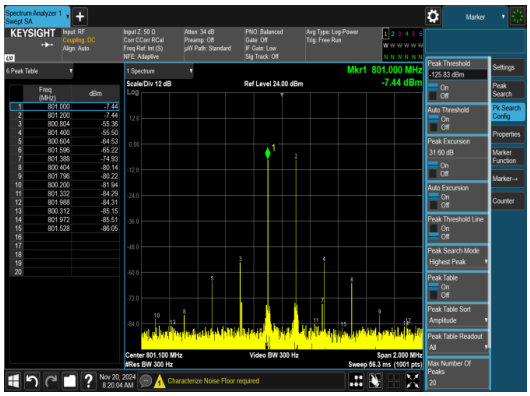


Figure 13. TX OIP3 (800 MHz Band)

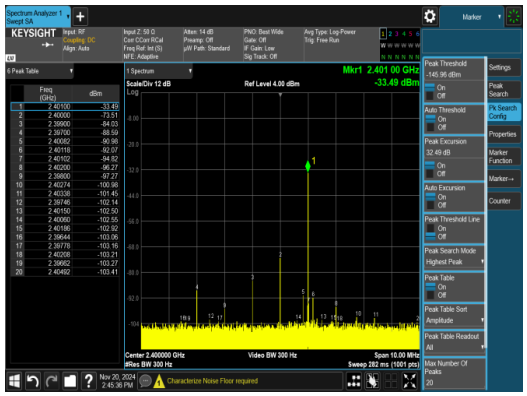


Figure 14. TX Output at 40 dB Attenuation (2.4 GHz Band)



Figure 15. TX EVM (2.4 GHz Band)

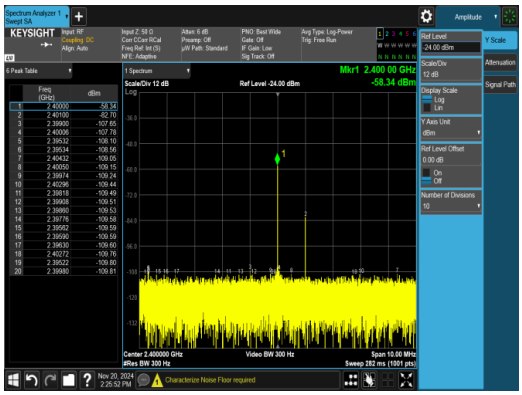


Figure 16. TX Isolation (2.4 GHz Band)

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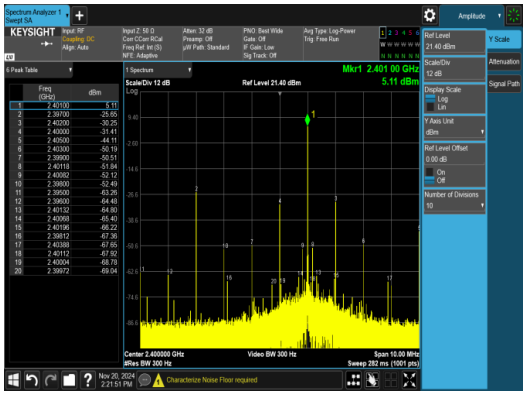


Figure 17. TX Maximum Output (2.4 GHz Band)

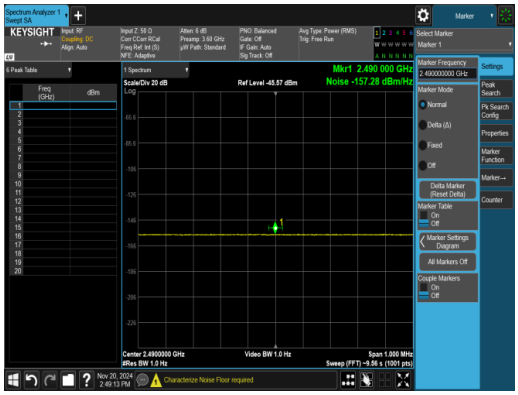


Figure 18. TX Noise Floor (2.4 GHz Band)

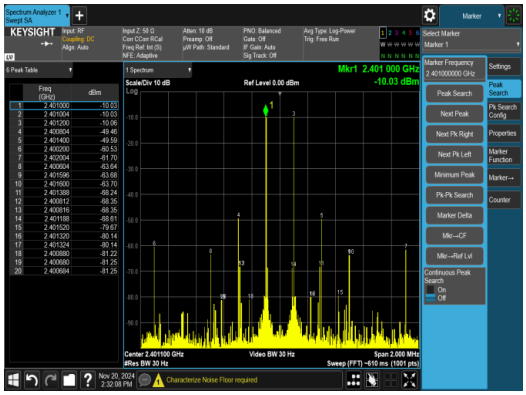


Figure 19. TX OIP3 (2.4 GHz Band)

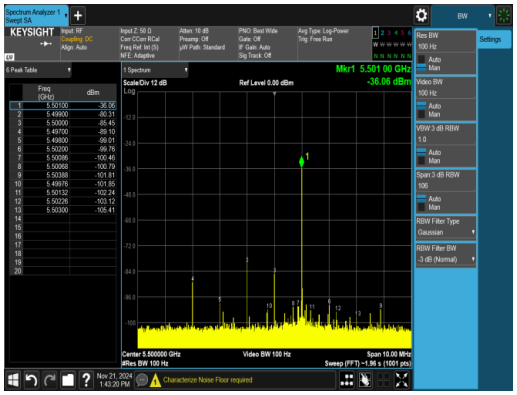


Figure 20. TX Output at 40 dB Attenuation (5.5 GHz Band)

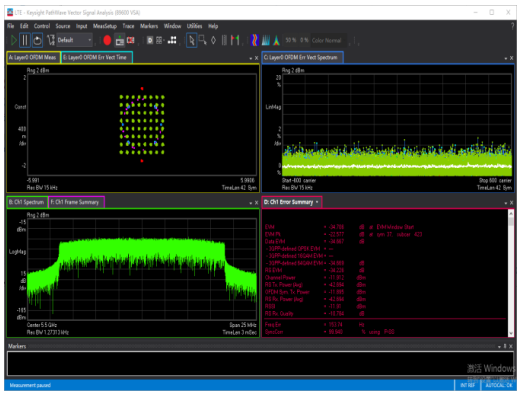


Figure 21. TX EVM (5.5 GHz Band)

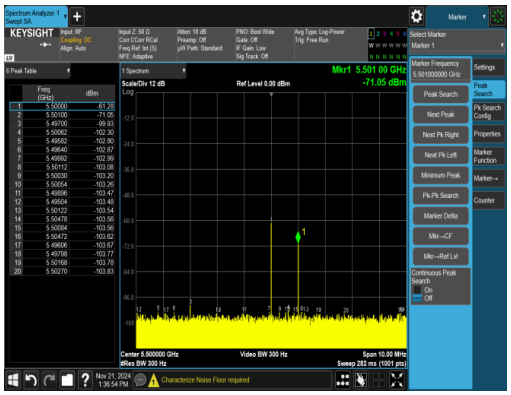


Figure 22. TX Isolation (5.5 GHz Band)

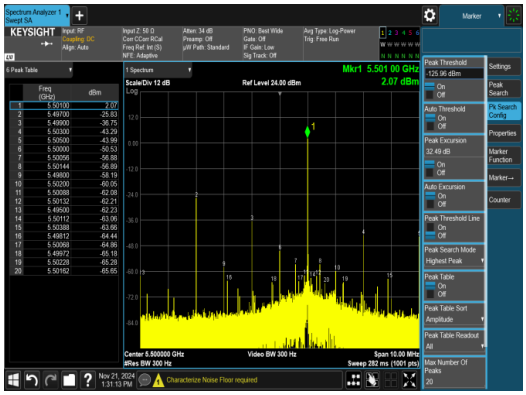


Figure 23. TX Maximum Output (5.5 GHz Band)



Figure 24. TX Noise Floor (5.5 GHz Band)

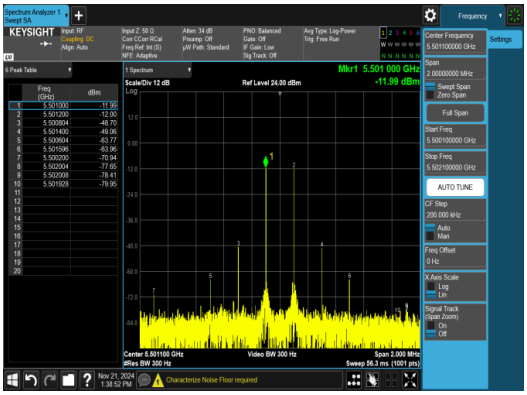


Figure 25. TX OIP3 (5.5 GHz Band)

Typical Application Circuit

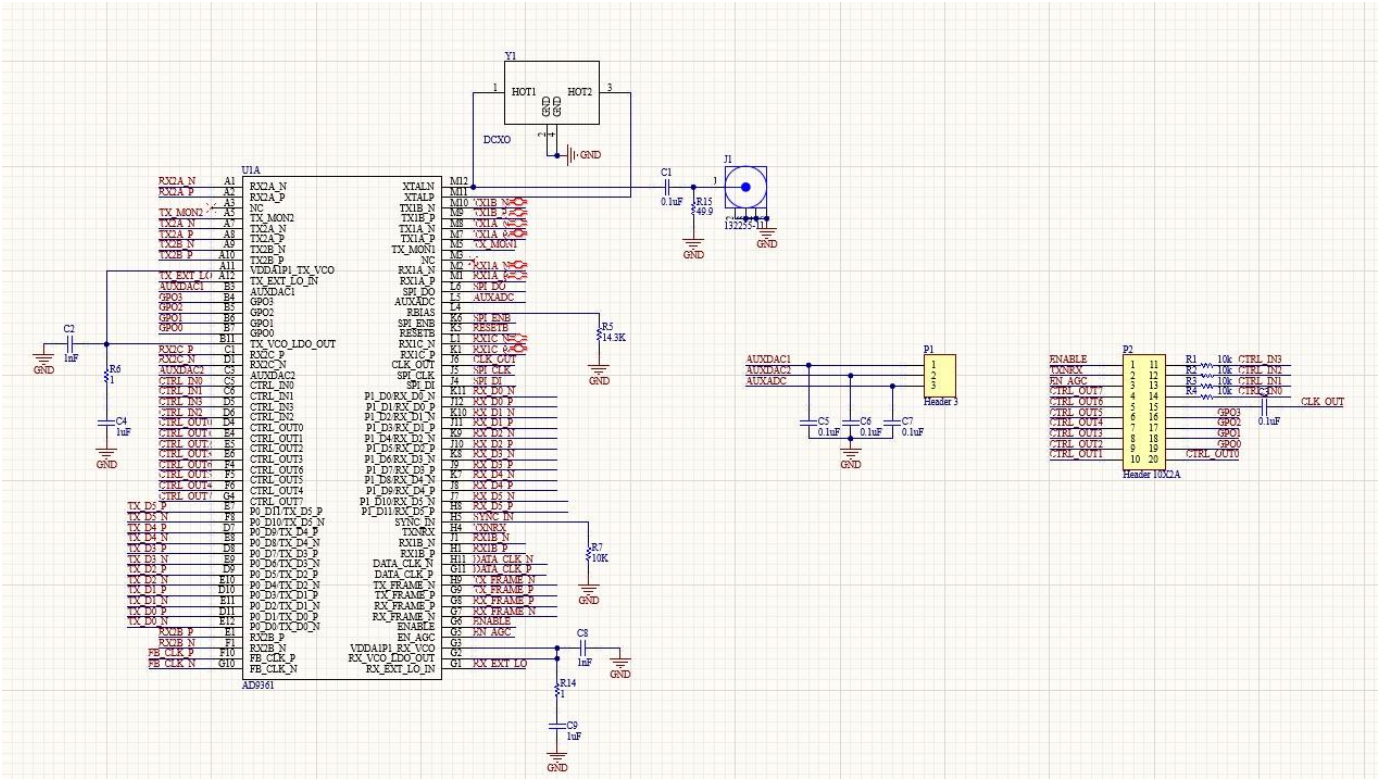


Figure 26. SXS046 Typical Application Circuit

Functional Blocks and Operating Principles

1. Overview

The SXS046 dual-receiver, dual-transmitter, 56 MHz frequency-agile transceiver SoC is a semiconductor integrated circuit manufactured using a CMOS process. This highly integrated radio-frequency (RF) transceiver can be configured for a broad range of applications. A single device integrates all RF, mixed-signal, and digital blocks necessary to provide all transceiver functions. Its programmability allows this wideband transceiver to support multiple communication standards, including frequency-division duplex (FDD) and time-division duplex (TDD) systems.

This programmability also allows connection to a variety of baseband processors (BBPs) through a single-channel 12-bit parallel data port, a dual-channel 12-bit parallel data port, or a 12-bit low-voltage differential signaling (LVDS) interface.

The device also provides self-calibration and automatic gain control (AGC) systems to maintain high performance over a range of temperatures and input-signal conditions. In addition, several test modes allow system designers to insert test tones and create internal loopback modes to debug designs during prototyping and optimize the radio configuration for specific applications.

2. Receiver

The analog input consists of a differential switched-capacitor sample-and-hold structure, as shown in Figure 13. The differential structure provides better AC performance at high input

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frequencies. The common-mode voltage of differential inputs INP and INM is 0.95 V, supplied by the on-chip VCM pin. The maximum differential input swing is 2 VPP.

The receiver section contains all blocks required to receive RF signals and convert them into digital data for use by the BBP. Two independently controlled channels can receive signals from different sources, allowing the device to be used in multiple-input, multiple-output (MIMO) systems while sharing a common frequency synthesizer. Each channel has three inputs that can be multiplexed into the signal chain, allowing SXS046 to support diversity systems with multiple antenna inputs. The receiver is a direct-conversion system containing a low-noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band-shaping filters. These filters downconvert the received signals to baseband for digitization. An external LNA can also be connected to the device, giving designers considerable flexibility to customize the receiver front end for specific applications.

Gain control is implemented through a preprogrammed gain-index map that distributes gain among the various blocks to optimize performance at each level. This can be achieved by enabling the internal AGC in fast or slow mode, or through manual gain control, allowing the BBP to adjust gain as needed. Each channel also has independent RSSI measurement, DC-offset tracking, and all circuitry required for self-calibration. The receiver includes 12-bit sigma-delta ADCs with adjustable sampling rates to generate data streams from the received signals. The digitized signals can be further conditioned through a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sampling rate of each digital-filter block can be adjusted by changing the decimation factor to obtain the required output data rate.

3. Transmitter

The transmitter section contains two identical, independently controlled channels, providing all digital-processing, mixed-signal, and RF blocks required for a direct-conversion system while sharing a common frequency synthesizer. Digital data received from the BBP passes through a fully programmable 128-tap FIR filter without an interpolation option. The FIR output is sent to a series of interpolation filters that provide additional filtering and data-rate interpolation before reaching the DACs. Each 12-bit DAC has an adjustable sampling rate. The I and Q channels are both fed to the RF block for upconversion.

When converted into analog baseband signals, the I and Q signals are filtered to remove sampling artifacts and then fed into upconversion mixers. Here, the I and Q signals are recombined and modulated at the carrier frequency for delivery to the output stage. The combined signals also pass through analog filters that provide additional band shaping before reaching the output amplifiers. Each transmit channel provides a wide range of fine attenuation adjustment to help designers optimize the signal-to-noise ratio (SNR).

Each transmit channel includes self-calibration circuitry to support automatic real-time adjustment. The transmitter block also provides a TX monitor block for each channel. This block monitors the transmitter output and routes it back to the BBP through an unused receiver channel for signal monitoring. The TX monitor block is available only in TDD mode when the receiver is idle.

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4. Clock Input Options

The reference clock used by SXS046 can be provided by two different sources. The first option is a dedicated crystal with a frequency between 19 MHz and 50 MHz, connected between the XTALP and XTALN pins. The second option is an external oscillator or clock-distribution device, such as AD9548, connected to XTALN with XTALP left unconnected. If an external oscillator is used, its frequency can range from 10 MHz to 80 MHz. This reference clock powers the frequency-synthesizer blocks, which generate all data clocks, sampling clocks, and local oscillators internally. Crystal-frequency errors can be removed by adjusting on-chip variable capacitance using the digitally programmable, digitally controlled crystal oscillator (DCXO) function. This capacitance can tune crystal-frequency variations in the system, producing a more accurate reference clock from which all other frequencies are generated. This function can also be used with on-chip temperature sensing to provide oscillator-frequency temperature compensation during normal operation.

5. Frequency Synthesizers

SXS046 contains two identical frequency synthesizers that generate the LO signals required for the RF signal paths: one for the receiver and one for the transmitter. The phase-locked loop (PLL) frequency synthesizers use a fractional-N design with fully integrated voltage-controlled oscillators (VCOs) and loop filters. In TDD operation, the synthesizers are turned on and off as required by the RX and TX frames. In FDD mode, the TX PLL and RX PLL can be active simultaneously. These PLLs require no external components.

SXS046 also contains a baseband PLL frequency synthesizer that generates all baseband-related clock signals, including the ADC and DAC sampling clocks, DATA_CLK (see “Digital Data Interface”), and all data-frame signals. This PLL has a programmable frequency range of 700 MHz to 1400 MHz, depending on the system data-rate and sampling-rate requirements.

6. Digital Data Interface

The SXS046 data interface uses parallel data ports P0 and P1 to transfer data between the device and the BBP. These ports can be configured for single-ended CMOS or differential LVDS operation. Both formats support multiple configurations to meet system requirements for data ordering and data-port connections. These include single-port and dual-port data buses, single and double data rates, and various data-ordering combinations that transfer data from different channels across the bus at the appropriate times. Bus transfers are controlled by simple hardware handshake signals. Both ports can operate in bidirectional TDD mode or full-duplex FDD mode. In FDD mode, half the bits carry transmit data and half carry receive data. The interface can also be configured to use only one data port for applications that do not require high data rates and prefer fewer interface pins.

7. DATA_CLK Signal

RX data provides the DATA_CLK signal, which the BBP can use when receiving data. DATA_CLK can be set to a rate providing single-data-rate (SDR) timing, with data sampled at each rising clock edge, or double-data-rate (DDR) timing, with data captured at both rising and falling edges. This timing applies to operating modes using either one port or both ports.

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Registers

Refer to the SXS046 Register Map & Software Migration Guide.

Controlled documentation is available from SHENXIN TECH upon request.

Protection Between Power Supplies and Ground

To improve the device’s electrostatic-discharge immunity, the following ESD protection circuits are provided internally between the power-supply pins. Each ESD protection diode has a forward voltage drop of approximately 0.35 V. Avoid prolonged forward conduction of these protection diodes during power-up and normal operation.

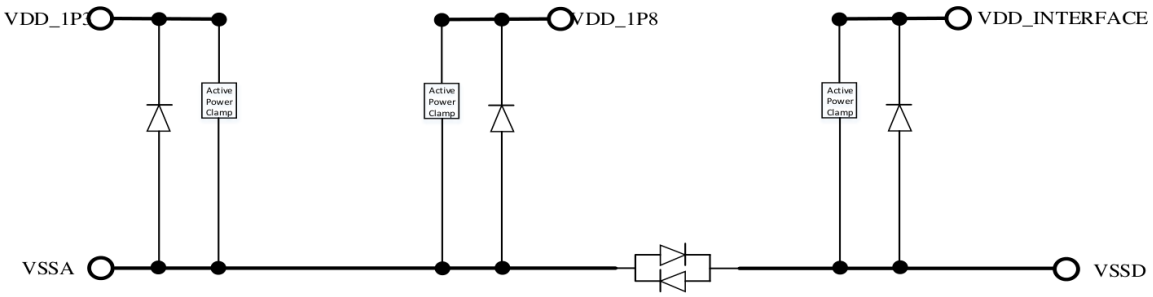


Figure 27. Internal ESD Protection Circuit Between Power Supplies

Precautions

1. Product Installation Precautions

1. Observe the device orientation during soldering to avoid incorrect installation.
2. All instruments and meters used for circuit debugging must have a sound common ground. Ensure proper grounding and power-supply decoupling in the PCB design.
3. Avoid reverse power-supply connections and short circuits between the input/output terminals and the power supply, as these can damage the circuit.

2. Product Usage Precautions

1. Power-up requirements: simultaneous application of the analog and digital supplies is recommended, or apply the analog supply first.
2. Use low-ESR capacitors for decoupling at the LDO outputs.
3. A large PCB ground area is recommended. This can eliminate potential differences caused by different grounding points and reduce the effects of board-generated capacitance on the circuit.
4. Connect one 1 µF or 0.1 µF capacitor close to each power-supply pin.
5. If differential analog inputs are used, the differential input traces must have equal lengths.
6. Keep the digital and analog power supplies separate.

3. Product Protection Precautions

1. All device terminals incorporate ESD protection structures. However, high-energy electrical pulses may still damage the circuit. Apply ESD protection during testing, handling, and storage.
2. Exceeding the absolute maximum ratings may permanently damage the device. These are limiting ratings only and do not imply normal operation under these conditions or under any other conditions beyond those stated in this product manual.
3. Provided that direct exposure to rain and snow is prevented, cartons containing the product may be transported by safe means. Do not stack them with acidic, alkaline, or other corrosive materials. Packaging must be secure; existing means of transport may be used.
4. The storage environment for packaged products must meet the Class I warehouse conditions specified in Section 8.1 of Q/W 657A: temperature 15 °C to 25 °C and humidity 25% to 65%. The environment must be well ventilated, free of acidic, alkaline, or other corrosive gases, and equipped with appropriate ESD protection.

4. Assembly and Handling Requirements

1. This product has a moisture-sensitivity level of MSL3. The permissible exposure to ambient conditions after removal from the moisture-barrier bag, dry storage, or baking and before reflow soldering is 168 h at ≤30 °C / 60% RH.
2. If device storage conditions cannot be controlled or traced, strictly perform baking at 125 °C for 8 h before assembly.

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3. If assembly-environment temperature and humidity cannot be maintained at ≤30 °C / 60% RH, complete soldering within 12 h after baking.
4. After baking, the product is highly susceptible to electrostatic charging. Apply ESD protection throughout all operations.
5. For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak-temperature range is 210 °C to 235 °C. The maximum peak temperature should not exceed 235 °C. Time within ±5 °C of the peak temperature must be ≤20 s; time above liquidus must be 60 to 90 s; the heating rate must be 2 to 4 °C/s; and the cooling rate must be 2 to 6 °C/s.
6. For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak-temperature range is 230 °C to 245 °C. The maximum peak temperature should not exceed 260 °C. Time within ±5 °C of the peak temperature must be ≤20 s; time above liquidus must be 60 to 90 s; the heating rate must be 2 to 4 °C/s; and the cooling rate must be 2 to 6 °C.

1. If a mixed assembly process requires a higher temperature, ensure that the device-body temperature does not exceed 260 °C. The device-body temperature is measured at the top surface of the device during reflow soldering.
2. This product uses lead-free/leaded solder balls made of SAC305.

Common Faults and Troubleshooting

1. No signal output: check whether a clock signal is present at the clock terminal, verify the power-supply and ground connections, and ensure that the input and reference voltages are correct.
2. Output data jitter: check the external circuitry and connections and ensure that the reference voltage is stable.
3. Unstable device operation: check the power supply and ensure that the supply voltage is stable.

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