SHENXIN TECH

SXS055

2T2R RF Transceiver SoC | 20 MHz Tunable Channel Bandwidth

2T2R 射频收发器 SoC | 20 MHz 可调谐通道带宽

Customer Edition — Bilingual / 客户版 — 双语

Derived from controlled engineering source: V1.20260728 / 源自受控工程源文件：V1.20260728

RF RANGE	CHANNEL BANDWIDTH
325 MHz to 3.8 GHz	Up to 20 MHz
DATA CONVERTERS	**PACKAGE**
2T2R | 12-bit DAC / ADC	CSP_BGA144 | -40°C to +85°C

DESIGN-IN POSITIONING / 设计定位

SXS055 is a Pin-to-Pin Replacement for AD9363. Existing hardware designs can reuse the PCB; register configuration adaptation is required.

SXS055 是 AD9363 的引脚对引脚（Pin-to-Pin）替代产品。现有硬件设计可复用 PCB；需要进行寄存器配置适配。

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Issued 09 October 2026 / 发布日期：2026 年 10 月 9 日

Document Control / 文档控制

SHENXIN TECH | Customer Edition / 客户版

PRODUCT / 产品	SXS055
ENGINEERING SOURCE VERSION / 工程源文件版本	V1.20260728
CUSTOMER EDITION DATE / 客户版日期	09 October 2026
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Customer-edition scope / 客户版范围

- Customer-facing edition with verified electrical specifications retained.
- 面向客户的版本，保留经核实的电气规格。
- Internal comparison notes and preliminary test-board comments have been excluded.
- 内部对比注释和初步测试板评论已排除。
- Controlled register and PCB assembly documentation is available upon request.
- 受控的寄存器和 PCB 组装文档可根据要求提供。

This customer edition preserves the controlled electrical specifications and operating limits from the engineering source. Request controlled register and PCB assembly documentation before a design release.

本客户版保留了工程源文件中受控的电气规格和工作限值。在设计发布之前，请索取受控的寄存器和 PCB 组装文档。

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Customer edition excludes internal comparison notes and preliminary test-board comments. Detailed controlled engineering documentation is available from SHENXIN TECH upon request.
客户版不包含内部对比注释和初步测试板评论。详细的受控工程文档可根据要求从 SHENXIN TECH 获取。

1. Applications and Scope / 应用和范围

- Point-to-point communication systems
- 点对点通信系统
- Pico/femtocell base stations
- 微微/毫微微蜂窝基站
- General-purpose radio systems
- 通用无线电系统

2. Standards / 标准

Detailed specification and confirmation number: SXS055 RF Agile Transceiver Detailed Specification
详细规格和确认编号：SXS055 射频捷变收发器详细规范

Quality grade: Industrial grade
质量等级：工业级

3. Product Features / 产品特性

- Supply voltages: 1.3V / 1.8V / 3.3V
- 供电电压：1.3V / 1.8V / 3.3V
- Integrated RF 2×2 transceiver with 12-bit DACs and ADCs
- 集成 RF 2×2 收发器，带 12 位 DAC 和 ADC
- Frequency range: 325 MHz to 3.8 GHz
- 频率范围：325 MHz 至 3.8 GHz
- Supports TDD and FDD
- 支持 TDD 和 FDD
- Tunable channel bandwidth: up to 20 MHz
- 可调谐通道带宽：最高 20 MHz
- TX EVM: −34 dB
- TX EVM：−34 dB
- Digital interface: CMOS / LVDS
- 数字接口：CMOS / LVDS
- ESD rating: Class 1B, HBM 500V
- ESD 等级：Class 1B，HBM 500V
- Product weight: 0.32 g ± 0.02 g
- 产品重量：0.32 g ± 0.02 g

4. Product Description / 产品描述

The SXS055 is a high-performance, highly integrated RF agile transceiver designed for 3G and 4G pico/femtocell base station applications. Its programmability and wideband capability make it suitable for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and an integrated frequency synthesizer, simplifying the design process by providing a configurable digital interface to connect with a processor. The SXS055 operates over a frequency range of 325 MHz to 3.8 GHz, covering most licensed and unlicensed bands. It supports channel bandwidths up to 20 MHz.

SXS055 是一款高性能、高集成度的射频捷变收发器，为 3G 和 4G
微微/毫微微蜂窝基站应用而设计。其可编程性和宽带能力使其适用于广泛的收发器应用。该器件将 RF 前端与灵活的混

合信号基带部分和集成频率合成器相结合，通过提供可配置的数字接口与处理器连接，简化了设计过程。SXS055 的工作频率范围为 325 MHz 至 3.8 GHz，覆盖大多数许可和非许可频段。它支持最高 20 MHz 的通道带宽。

The two independent direct conversion receivers of the SXS055 deliver industry-leading noise figure and linearity. Each receive subsystem includes independent Automatic Gain Control (AGC), DC offset correction, quadrature correction, and digital filtering, eliminating the need to implement these functions in the digital baseband. The SXS055 also offers a flexible manual gain mode that can be controlled externally. Two high-dynamic-range ADCs per channel digitize the received I and Q signals, which are then processed by configurable decimation filters and a 128-tap Finite Impulse Response (FIR) filter, ultimately outputting 12-bit signals at the appropriate sample rate.

SXS055 的两个独立的直接变频接收器提供业界领先的噪声系数和线性度。每个接收子系统包括独立的自动增益控制（AGC）、DC 偏移校正、正交校正和数字滤波，无需在数字基带中实现这些功能。SXS055 还提供可外部控制的灵活手动增益模式。每通道的两个高动态范围 ADC 将接收的 I 和 Q 信号数字化，然后由可配置的抽取滤波器和 128 抽头有限冲激响应（FIR）滤波器处理，最终以适当的采样率输出 12 位信号。

The transmitter of the SXS055 uses a direct conversion architecture that achieves high modulation accuracy with ultra-low noise. This transmitter design produces an industry-leading transmit EVM (Error Vector Magnitude) of −34 dB, providing sufficient system margin for the selection of an external Power Amplifier (PA). An on-board transmit power monitor can be used as a power detector, enabling high-accuracy transmit power measurement.

SXS055 的发射器采用直接变频架构，实现高调制精度和超低噪声。这种发射器设计产生业界领先的 −34 dB 发射 EVM（误差矢量幅度），为外部功率放大器（PA）的选择提供充足的系统裕量。片上发射功率监测器可用作功率检测器，实现高精度的发射功率测量。

The fully integrated Phase-Locked Loop (PLL) of the SXS055 provides low-power fractional-N frequency synthesis for all receive and transmit channels. The channel isolation required for FDD systems is integrated into the design. All Voltage-Controlled Oscillator (VCO) and loop filter components are integrated.

SXS055 的全集成锁相环（PLL）为所有接收和发射通道提供低功耗分数 N 分频频率合成。FDD 系统所需的通道隔离已集成到设计中。所有压控振荡器（VCO）和环路滤波器组件都已集成。

The device is packaged in a 10 mm × 10 mm, 144-pin Chip-Scale Ball Grid Array package (CSP_BGA). The functional block diagram of the product is shown in Figure 1.

该器件采用 10 mm × 10 mm、144 引脚芯片级球栅阵列封装（CSP_BGA）。产品的功能框图如图 1 所示。

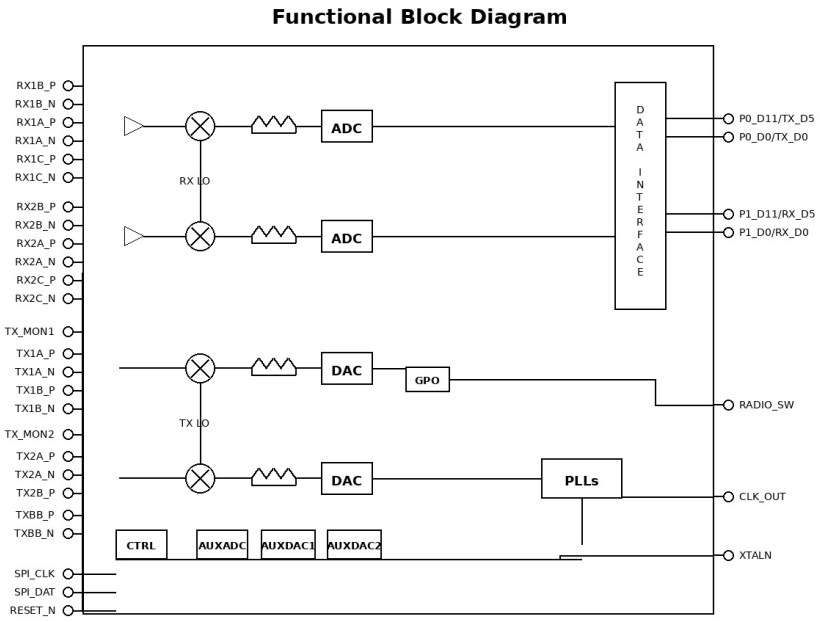


Figure 1. Functional Block Diagram

Figure 1. Functional Block Diagram / 图 1. 功能框图

Notes: / 注：

1. RX and TX Baseband Bandwidth Calibration. The clock for baseband bandwidth calibration is derived from the main clock divider. The RX divide ratio is determined by Reg1F8[7:0] (BBF Tune Divide), and the TX divide ratio is determined by Reg0D6[7:0]. This divide ratio must not be odd; i.e., Reg1F8[0] and Reg0D6[0] must not be set to 1. The divide ratio is jointly determined by the BBPLL frequency and the baseband bandwidth, according to the following formula: BBF Tune Divide[8:0] = ceil((BBPLL Freq × ln(2)) / (BBBW × 1.4 × 2π)). During chip initialization, avoid setting the values of the two registers listed above to 1. After initialization, verify the values of these two registers. If the value is 1, a feasible approach is to adjust the baseband bandwidth and re-initialize the chip to avoid setting these two register values to 1.

1. RX 和 TX 基带带宽校准。基带带宽校准的时钟源自主时钟分频器。RX 分频比由 Reg1F8[7:0]（BBF Tune Divide）决定，TX 分频比由 Reg0D6[7:0] 决定。该分频比不得为奇数；即 Reg1F8[0] 和 Reg0D6[0] 不得设置为 1。分频比由 BBPLL 频率和基带带宽共同决定，公式如下：BBF Tune Divide[8:0] = ceil((BBPLL Freq × ln(2)) / (BBBW × 1.4 × 2π))。在芯片初始化期间，避免将上述两个寄存器的值设置为 1。初始化后，验证这两个寄存器的值。如果值为 1，可行的方法是调整基带带宽并重新初始化芯片，以避免将这两个寄存器值设置为 1。

2. RX I/Q Mismatch. At the 1.8 GHz local oscillator, the RX channel may exhibit I/Q mismatch at a high temperature of 80°C ± 4°C. (Comparable off-the-shelf products exhibit mismatch at −20°C.)

2. RX I/Q 失配。在 1.8 GHz 本振下，RX 通道在 80°C ± 4°C 高温时可能出现 I/Q 失配。（同类市售产品在 −20°C 时出现失配。）

5. Product Outline and Physical Pictures / 产品外形和实物图片

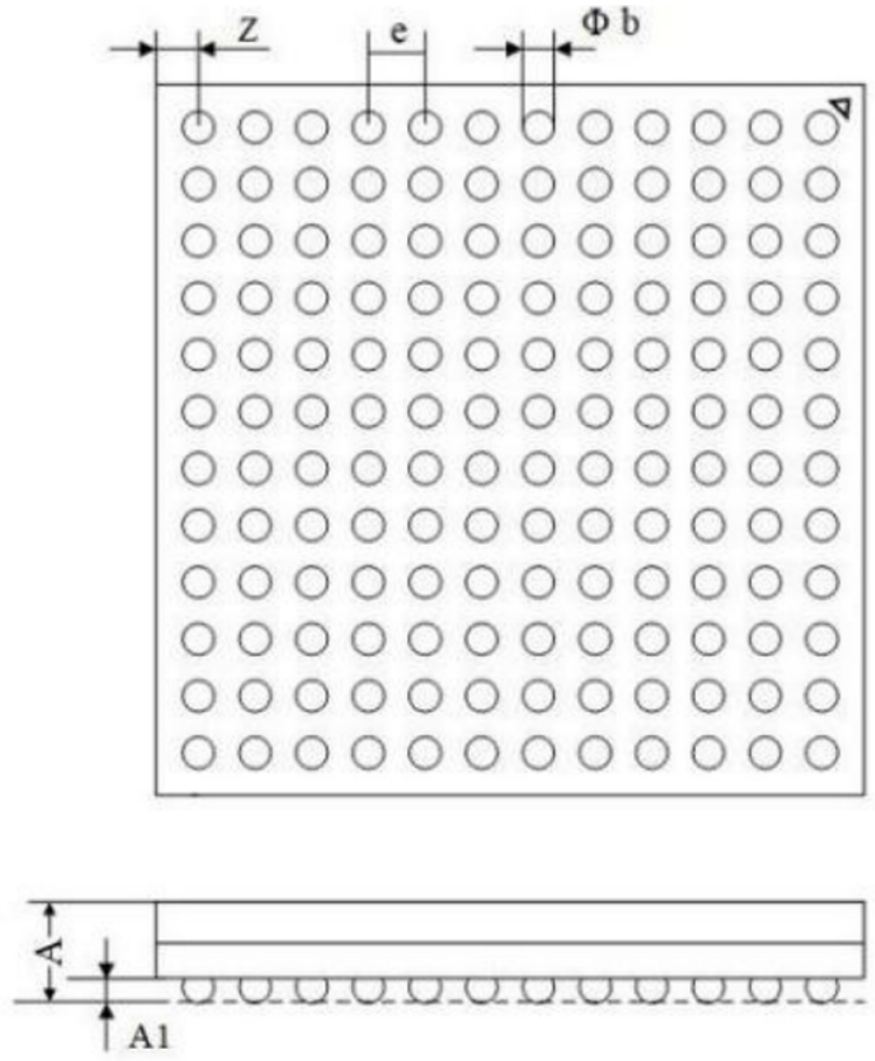


Figure 2. Package Outline Dimensions

Figure 2. Package Outline Dimensions • Figure 3. Unit: mm / 图 2. 封装外形尺寸 • 图 3. 单位：mm

Dimension Symbol / 尺寸符号	Min. / 最小	Nom. / 标称	Max. / 最大	Dimension Symbol / 尺寸符号	Min. / 最小	Nom. / 标称	Max. / 最大
A	1.27	1.42a	1.57	e	—	0.80	—
A1	0.30	0.35a	0.40	Φb	0.40	0.45a	0.50
D	9.80	10.00a	10.20	Z	—	0.60a	0.70
E	9.80	10.00a	10.20				

a Actual nominal package value; recommended for users' reference when designing pad dimensions.
a 实际标称封装值；建议用户在设计焊盘尺寸时参考。

Note: For recommended pad design, refer to the electrical mounting instructions.
注：推荐的焊盘设计请参考电气安装说明。

6. Pin Configuration (Top View) / 引脚配置（顶视图）

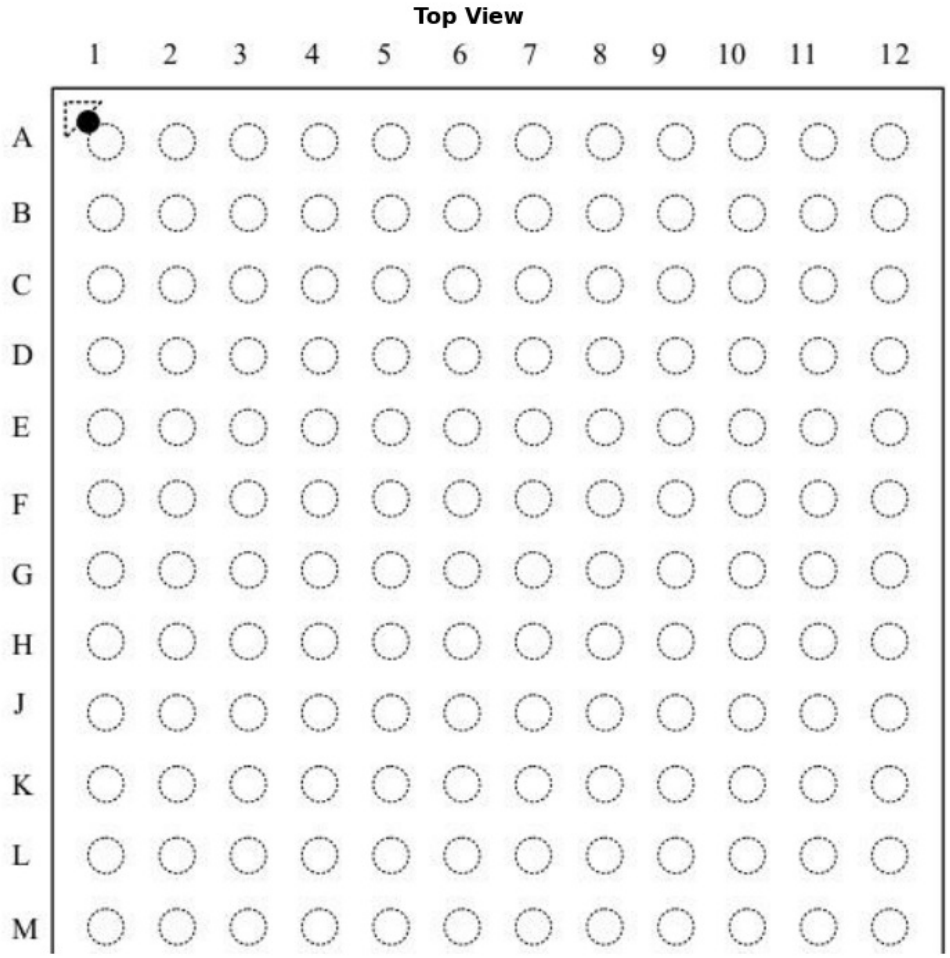


Figure 4. Pin Configuration (Top View)

Figure 4. Pin Configuration (Top View) / 图 4. 引脚配置（顶视图）

7. Pin Function Description Table / 引脚功能描述表

Pin No. / 引脚号	Symbol / 符号	Name / Description / 名称 / 说明	I/O
A1	RX2A_N	RX Channel 2 Input A Negative RX 通道 2 输入 A 负端	I

Pin No. / 引脚号	Symbol / 符号	Name / Description / 名称 / 说明	I/O
A2	RX2A_P	RX Channel 2 Input A Positive RX 通道 2 输入 A 正端	I
A3	NC	No Connect [a] 不连接 [a]	/
A4	VSSA	Analog Ground 模拟地	I
A5	TX_MON2	TX Channel 2 Power Monitor Input TX 通道 2 功率监测输入	I
A6	VSSA	Analog Ground 模拟地	I
A7	TX2A_N	TX Channel 2 Output A Negative TX 通道 2 输出 A 负端	O
A8	TX2A_P	TX Channel 2 Output A Positive TX 通道 2 输出 A 正端	O
A9	TX2B_N	TX Channel 2 Output B Negative TX 通道 2 输出 B 负端	O
A10	TX2B_P	TX Channel 2 Output B Positive TX 通道 2 输出 B 正端	O
A11	VDDA1P1_TX_VCO	TX VCO Power Input TX VCO 电源输入	I
A12	VSSA	Analog Ground 模拟地	I
B1	VSSA	Analog Ground 模拟地	I
B2	VSSA	Analog Ground 模拟地	I
B3	AUXDAC1	Auxiliary DAC 1 Output 辅助 DAC 1 输出	O
B4	GPO_3	General Purpose Output 3 通用输出 3	O
B5	GPO_2	General Purpose Output 2 通用输出 2	O
B6	GPO_1	General Purpose Output 1 通用输出 1	O
B7	GPO_0	General Purpose Output 0 通用输出 0	O
B8	VDD_GPO	Auxiliary DAC and GPO Power 辅助 DAC 和 GPO 电源	I
B9	VDDA1P3_TX_LO	TX LO 1.3V Power TX LO 1.3V 电源	I
B10	VDDA1P3_TX_VCO_LDO	TX VCO LDO Power Input TX VCO LDO 电源输入	I
B11	TX_VCO_LDO_OUT	TX VCO LDO Power Output TX VCO LDO 电源输出	O
B12	VSSA	Analog Ground 模拟地	I
C1	RX2C_P	RX Channel 2 Input C Positive RX 通道 2 输入 C 正端	I
C2	VSSA	Analog Ground 模拟地	I
C3	AUXDAC2	Auxiliary DAC 2 Output 辅助 DAC 2 输出	O

Pin No. / 引脚号	Symbol / 符号	Name / Description / 名称 / 说明	I/O
C4	TEST/ENABLE	Test Input 测试输入	I
C5	CTRL_IN0	Control Input 0 控制输入 0	I
C6	CTRL_IN1	Control Input 1 控制输入 1	I
C7	VSSA	Analog Ground 模拟地	I
C8	VSSA	Analog Ground 模拟地	I
C9	VSSA	Analog Ground 模拟地	I
C10	VSSA	Analog Ground 模拟地	I
C11	VSSA	Analog Ground 模拟地	I
C12	VSSA	Analog Ground 模拟地	I
D1	RX2C_N	RX Channel 2 Input C Negative RX 通道 2 输入 C 负端	I
D2	VDDA1P3_RX_RF	Receiver 1.3V Power 接收器 1.3V 电源	I
D3	VDDA1P3_RX_TX	1.3V Power 1.3V 电源	I
D4	CTRL_OUT0	Control Output 0 控制输出 0	O
D5	CTRL_IN3	Control Input 3 控制输入 3	I
D6	CTRL_IN2	Control Input 2 控制输入 2	I
D7	P0_D9/TX_D4_P	P0 Port D9 / TX D4 Differential Input Positive P0 端口 D9 / TX D4 差分输入正端	I/O
D8	P0_D7/TX_D3_P	P0 Port D7 / TX D3 Differential Input Positive P0 端口 D7 / TX D3 差分输入正端	I/O
D9	P0_D5/TX_D2_P	P0 Port D5 / TX D2 Differential Input Positive P0 端口 D5 / TX D2 差分输入正端	I/O
D10	P0_D3/TX_D1_P	P0 Port D3 / TX D1 Differential Input Positive P0 端口 D3 / TX D1 差分输入正端	I/O
D11	P0_D1/TX_D0_P	P0 Port D1 / TX D0 Differential Input Positive P0 端口 D1 / TX D0 差分输入正端	I/O
D12	VSSD	Digital Ground 数字地	I
E1	RX2B_P	RX Channel 2 Input B Positive RX 通道 2 输入 B 正端	I
E2	VDDA1P3_RX_LO	RX LO 1.3V Power RX LO 1.3V 电源	I
E3	VDDA1P3_TX_LO_BUFFER	TX LO Buffer 1.3V Power TX LO 缓冲器 1.3V 电源	I
E4	CTRL_OUT1	Control Output 1 控制输出 1	O
E5	CTRL_OUT2	Control Output 2 控制输出 2	O

Pin No. / 引脚号	Symbol / 符号	Name / Description / 名称 / 说明	I/O
E6	CTRL_OUT3	Control Output 3 控制输出 3	O
E7	P0_D11/TX_D5_P	P0 Port D11 / TX D5 Differential Input Positive P0 端口 D11 / TX D5 差分输入正端	I/O
E8	P0_D8/TX_D4_N	P0 Port D8 / TX D4 Differential Input Negative P0 端口 D8 / TX D4 差分输入负端	I/O
E9	P0_D6/TX_D3_N	P0 Port D6 / TX D3 Differential Input Negative P0 端口 D6 / TX D3 差分输入负端	I/O
E10	P0_D4/TX_D2_N	P0 Port D4 / TX D2 Differential Input Negative P0 端口 D4 / TX D2 差分输入负端	I/O
E11	P0_D2/TX_D1_N	P0 Port D2 / TX D1 Differential Input Negative P0 端口 D2 / TX D1 差分输入负端	I/O
E12	P0_D0/TX_D0_N	P0 Port D0 / TX D0 Differential Input Negative P0 端口 D0 / TX D0 差分输入负端	I/O
F1	RX2B_N	RX Channel 2 Input B Negative RX 通道 2 输入 B 负端	I
F2	VDDA1P3_RX_VCO_LDO	RX VCO LDO Power Input RX VCO LDO 电源输入	I
F3	VSSA	Analog Ground 模拟地	I
F4	CTRL_OUT6	Control Output 6 控制输出 6	O
F5	CTRL_OUT5	Control Output 5 控制输出 5	O
F6	CTRL_OUT4	Control Output 6 控制输出 6	O
F7	VSSD	Digital Ground 数字地	I
F8	P0_D10/TX_D5_N	P0 Port D10 / TX D5 Differential Input Negative P0 端口 D10 / TX D5 差分输入负端	I/O
F9	VSSD	Digital Ground 数字地	I
F10	FB_CLK_P	TX Data Clock Input Positive TX 数据时钟输入正端	I
F11	VSSD	Digital Ground 数字地	I
F12	VDDD1P3_DIG	1.3V Digital Power 1.3V 数字电源	I
G1	VSSA	Analog Ground 模拟地	I
G2	RX_VCO_LDO_OUT	RX VCO LDO Output RX VCO LDO 输出	O
G3	VDDA1P1_RX_VCO	RX VCO LDO Input RX VCO LDO 输入	I
G4	CTRL_OUT7	Control Output 7 控制输出 7	O
G5	EN_AGC	Manual Control Input for AGC AGC 手动控制输入	I
G6	ENABLE	State Machine Enable Signal 状态机使能信号	I
G7	RX_FRAME_N	RX Data Frame Differential Output Negative RX 数据帧差分输出负端	O

Pin No. / 引脚号	Symbol / 符号	Name / Description / 名称 / 说明	I/O
G8	RX_FRAME_P	RX Data Frame Differential Output Positive RX 数据帧差分输出正端	O
G9	TX_FRAME_P	TX Data Frame Differential Input Positive TX 数据帧差分输入正端	I
G10	FB_CLK_N	TX Data Clock Differential Input Negative TX 数据时钟差分输入负端	I
G11	DATA_CLK_P	RX Data Clock Differential Output Positive RX 数据时钟差分输出正端	O
G12	VSSD	Digital Ground 数字地	I
H1	RX1B_P	RX Channel 1 Input B Positive RX 通道 1 输入 B 正端	I
H2	VSSA	Analog Ground 模拟地	I
H3	VSSA	Analog Ground 模拟地	I
H4	TXNRX	Enable State Machine TX/RX State Control Signal 使能状态机 TX/RX 状态控制信号	I
H5	VSSA	Analog Ground 模拟地	I
H6	VSSA	Analog Ground 模拟地	I
H7	VSSD	Digital Ground 数字地	I
H8	P1_D11/RX_D5_P	P1 Port D11 / RX D5 Differential Output Positive P1 端口 D11 / RX D5 差分输出正端	I/O
H9	TX_FRAME_N	TX Data Frame Differential Input Negative TX 数据帧差分输入负端	I
H10	VSSD	Digital Ground 数字地	I
H11	DATA_CLK_N	RX Data Clock Differential Output Negative RX 数据时钟差分输出负端	O
H12	VDD_INTERFACE	Digital I/O Power 数字 I/O 电源	I
J1	RX1B_N	RX Channel 1 Input B Negative RX 通道 1 输入 B 负端	I
J2	VSSA	Analog Ground 模拟地	I
J3	VDDA1P3_RX_SYNTH	1.3V Power 1.3V 电源	I
J4	SPI_DI	SPI Serial Data Input SPI 串行数据输入	I
J5	SPI_CLK	SPI Clock Input SPI 时钟输入	I
J6	CLK_OUT	Clock Output 时钟输出	O
J7	P1_D10/RX_D5_N	P1 Port D10 / RX D5 Differential Output Negative P1 端口 D10 / RX D5 差分输出负端	I/O
J8	P1_D9/RX_D4_P	P1 Port D9 / RX D4 Differential Output Positive P1 端口 D9 / RX D4 差分输出正端	I/O
J9	P1_D7/RX_D3_P	P1 Port D7 / RX D3 Differential Output Positive P1 端口 D7 / RX D3 差分输出正端	I/O

Pin No. / 引脚号	Symbol / 符号	Name / Description / 名称 / 说明	I/O
J10	P1_D5/RX_D2_P	P1 Port D5 / RX D2 Differential Output Positive P1 端口 D5 / RX D2 差分输出正端	I/O
J11	P1_D3/RX_D1_P	P1 Port D3 / RX D1 Differential Output Positive P1 端口 D3 / RX D1 差分输出正端	I/O
J12	P1_D1/RX_D0_P	P1 Port D1 / RX D0 Differential Output Positive P1 端口 D1 / RX D0 差分输出正端	I/O
K1	RX1C_P	RX Channel 1 Input C Positive RX 通道 1 输入 C 正端	I
K2	VSSA	Analog Ground 模拟地	I
K3	VDDA1P3_TX_SYNTH	1.3V Power 1.3V 电源	I
K4	VDDA1P3_BB	1.3V Power 1.3V 电源	I
K5	RESET	Asynchronous Reset Input 异步复位输入	I
K6	SPI_EN	SPI Enable Input SPI 使能输入	I
K7	P1_D8/RX_D4_N	P1 Port D8 / RX D4 Differential Output Negative P1 端口 D8 / RX D4 差分输出负端	I/O
K8	P1_D6/RX_D3_N	P1 Port D6 / RX D3 Differential Output Negative P1 端口 D6 / RX D3 差分输出负端	I/O
K9	P1_D4/RX_D2_N	P1 Port D4 / RX D2 Differential Output Negative P1 端口 D4 / RX D2 差分输出负端	I/O
K10	P1_D2/RX_D1_N	P1 Port D2 / RX D1 Differential Output Negative P1 端口 D2 / RX D1 差分输出负端	I/O
K11	P1_D0/RX_D0_N	P1 Port D0 / RX D0 Differential Output Negative P1 端口 D0 / RX D0 差分输出负端	I/O
K12	VSSD	Digital Ground 数字地	I
L1	RX1C_N	RX Channel 1 Input C Negative RX 通道 1 输入 C 负端	I
L2	VSSA	Analog Ground 模拟地	I
L3	VSSA	Analog Ground 模拟地	I
L4	RBIAS	Bias Input Reference 偏置输入参考	I
L5	AUXADC	Auxiliary ADC 辅助 ADC	I
L6	SPI_DO	SPI Serial Output SPI 串行输出	O
L7	VSSA	Analog Ground 模拟地	I
L8	VSSA	Analog Ground 模拟地	I
L9	VSSA	Analog Ground 模拟地	I
L10	VSSA	Analog Ground 模拟地	I
L11	VSSA	Analog Ground 模拟地	I

Pin No. / 引脚号	Symbol / 符号	Name / Description / 名称 / 说明	I/O
L12	VSSA	Analog Ground 模拟地	I
M1	RX1A_P	RX Channel 1 Input A Positive RX 通道 1 输入 A 正端	I
M2	RX1A_N	RX Channel 1 Input A Negative RX 通道 1 输入 A 负端	I
M3	NC	No Connect [a] 不连接 [a]	/
M4	VSSA	Analog Ground 模拟地	I
M5	TX_MON1	TX Channel 1 Power Monitor Input TX 通道 1 功率监测输入	I
M6	VSSA	Analog Ground 模拟地	I
M7	TX1A_P	TX Channel 1 Output A Positive TX 通道 1 输出 A 正端	O
M8	TX1A_N	TX Channel 1 Output A Negative TX 通道 1 输出 A 负端	O
M9	TX1B_P	TX Channel 1 Output B Positive TX 通道 1 输出 B 正端	O
M10	TX1B_N	TX Channel 1 Output B Negative TX 通道 1 输出 B 负端	O
M11	NC	No Connect [a] 不连接 [a]	I
M12	XTALN	Reference Frequency Crystal Connection 参考频率晶体连接	I

a Leave this pin unconnected during use; do not connect to this pin.

a 使用期间请勿连接此引脚；不要连接到此引脚。

8. Absolute Maximum Ratings / 绝对最大额定值

Analog/digital core supply voltage to ground (VDDx to VSSx) 模拟/数字核心电源对地电压（VDDx 至 VSSx）	−0.3 V to 1.4 V
Interface voltage to ground (VDD_INTERFACE to VSSx) 接口对地电压（VDD_INTERFACE 至 VSSx）	−0.3 V to 3.0 V
GPO voltage to ground (VDD_GPO to VSSx) GPO 对地电压（VDD_GPO 至 VSSx）	−0.3 V to 3.9 V
Logic input/output to ground (VSSx) 逻辑输入/输出对地（VSSx）	−0.3 V to VDD_INTERFACE + 0.3 V
Input current on any pin except power pins 除电源引脚外任何引脚的输入电流	±10 mA
RF input (peak power) RF 输入（峰值功率）	2.5 dBm
TX monitor input power (peak power) TX 监测输入功率（峰值功率）	9 dBm
Package power dissipation 封装功耗	(TJMAX − TA) / θJA
Maximum junction temperature (TJMAX) 最高结温（TJMAX）	110°C
Operating temperature range (TA) 工作温度范围（TA）	−40°C to 85°C

Storage temperature (Tstg) 存储温度（Tstg）	−65°C to 150°C

9. Recommended Operating Conditions / 推荐工作条件

Input reference clock 输入参考时钟	40 MHz
Analog/digital core supply voltage (VDDx) 模拟/数字核心电源电压（VDDx）	1.3 V
Interface voltage (VDD_INTERFACE) 接口电压（VDD_INTERFACE）	1.8 V / 2.5 V
GPO voltage (VDD_GPO) GPO 电压（VDD_GPO）	3.3 V
Operating ambient temperature (TA) 工作环境温度（TA）	−40°C to 85°C

10. Electrical Specifications / 电气规格

Unless otherwise noted: VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, all other VDDx pins = 1.3 V, TA = 25°C.

除非另有说明：VDD_GPO = 3.3 V，VDD_INTERFACE = 1.8 V，所有其他 VDDx 引脚 = 1.3 V，TA = 25°C。

Parameter / 参数	Symbol / 符号	Conditions / 条件	Min. / 最小	Typ. / 典型	Max. / 最大	Unit / 单位
Receiver (Frequency-Independent Parameters) / 接收器（与频率无关的参数）						
Center Frequency 中心频率	F_0	RX1A / RX2A	325	—	3800	MHz
Gain Control Range 增益控制范围	Gain_Range	800 MHz	—	71.5	—	dB
Gain Control Range 增益控制范围	Gain_Range	2300 MHz (RX1A, RX2A) 2300 MHz（RX1A、RX2A）	—	70	—	dB
Gain Control Range 增益控制范围	Gain_Range	2300 MHz (RX1B, RX2B, RX1C, RX2C) 2300 MHz（RX1B、RX2B、RX1C、RX2C）	—	70	—	dB
Gain Step 增益步进	GS	—	—	1	—	dB
RSSI Range RSSI 范围	RSSI_Range	RX1A / RX2A	—	95	—	dB
RSSI Accuracy RSSI 精度	—	—	—	±2.5	—	dB
Receiver, 800 MHz / 接收器，800 MHz						
Noise Figure 噪声系数	NF	Maximum RX gain RX 最大增益	—	2.5	—	dB
Third-Order Input Intercept Point 三阶输入截断点	IIP3	RX1A/RX2A, maximum RX gain RX1A/RX2A，RX 最大增益	—	−11	—	dBm
Second-Order Input Intercept Point 二阶输入截断点	IIP2	RX1A/RX2A, maximum RX gain RX1A/RX2A，RX 最大增益	—	55	—	dBm
Digital LO Leakage 数字本振泄漏	LOL	At RX front end RX 前端处	—	−82	—	dBm
Quadrature Gain Error 正交增益误差	—	—	—	0.2	—	%

Parameter / 参数	Symbol / 符号	Conditions / 条件	Min. / 最小	Typ. / 典型	Max. / 最大	Unit / 单位
Quadrature Phase Error 正交相位误差	—	—	—	0.2	—	deg
Modulation Accuracy 调制精度	EVM_RX	—	—	(Not tested)	—	—
Input S11 输入 S11	—	—	—	(Not tested)	—	—
RX1A to RX2A Isolation RX1A 到 RX2A 隔离度	ISO_RX	—	—	68	—	dB
RX1C to RX2C Isolation RX1C 到 RX2C 隔离度	ISO_RX	—	—	68	—	dB
RX1B to RX2B Isolation RX1B 到 RX2B 隔离度	ISO_RX	—	—	55	—	dB
RX2A to RX1A Isolation RX2A 到 RX1A 隔离度	ISO_RX	—	—	68	—	dB
RX2C to RX1C Isolation RX2C 到 RX1C 隔离度	ISO_RX	—	—	68	—	dB
RX2B to RX1B Isolation RX2B 到 RX1B 隔离度	ISO_RX	—	—	55	—	dB
Receiver, 2.4 GHz / 接收器，2.4 GHz						
Noise Figure 噪声系数	NF	Maximum RX gain RX 最大增益	—	3.5	—	dB
Third-Order Input Intercept Point 三阶输入截断点	IIP3	RX1A/RX2A, maximum RX gain RX1A/RX2A，RX 最大增益	—	−10	—	dBm
Second-Order Input Intercept Point 二阶输入截断点	IIP2	RX1A/RX2A, maximum RX gain RX1A/RX2A，RX 最大增益	—	48	—	dBm
Digital LO Leakage 数字本振泄漏	LOL	At RX front end RX 前端处	—	−82	—	dBm
Quadrature Gain Error 正交增益误差	—	—	—	0.2	—	%
Quadrature Phase Error 正交相位误差	—	—	—	0.2	—	deg
Modulation Accuracy 调制精度	EVM_RX	—	—	(Not tested)	—	—
Input S11 输入 S11	—	—	—	(Not tested)	—	—
RX1A to RX2A Isolation RX1A 到 RX2A 隔离度	ISO_RX	—	—	55	—	dB
RX1C to RX2C Isolation RX1C 到 RX2C 隔离度	ISO_RX	—	—	55	—	dB
RX1B to RX2B Isolation RX1B 到 RX2B 隔离度	ISO_RX	—	—	50	—	dB
RX2A to RX1A Isolation RX2A 到 RX1A 隔离度	ISO_RX	—	—	55	—	dB
RX2C to RX1C Isolation RX2C 到 RX1C 隔离度	ISO_RX	—	—	55	—	dB
RX2B to RX1B Isolation RX2B 到 RX1B 隔离度	ISO_RX	—	—	50	—	dB
Transmitter (Frequency-Independent Parameters) / 发射器（与频率无关的参数）						

Parameter / 参数	Symbol / 符号	Conditions / 条件	Min. / 最小	Typ. / 典型	Max. / 最大	Unit / 单位
Center Frequency 中心频率	F_0	TX1A / TX2A	325	—	3800	MHz
Power Control Range 功率控制范围	PCR	TX1A / TX2A	—	90	—	dB
Power Control Resolution 功率控制分辨率	PRes	TX1A / TX2A	—	0.25	—	dB
Transmitter, 800 MHz / 发射器，800 MHz						
Output S22 输出 S22	—	—	—	(Not tested)	—	—
Maximum Output Power 最大输出功率	PO	1 MHz single-tone into 50 Ω load 1 MHz 单音输入 50 Ω 负载	—	8	—	dBm
Modulation Accuracy 调制精度	EVM_TX	19.2 MHz reference clock 19.2 MHz 参考时钟	—	−45	—	dB
Third-Order Output Intercept Point 三阶输出截断点	OIP3	—	—	17	—	dBm
Carrier Leakage 载波泄漏	CL	0 dB attenuation 0 dB 衰减	—	−50	—	dBc
Carrier Leakage 载波泄漏	CL	40 dB attenuation 40 dB 衰减	—	−40	—	dBc
Noise Spectral Density 噪声频谱密度	NSD	TX1A/TX2A, at 90 MHz offset TX1A/TX2A，90 MHz 偏移处	—	−148	—	dBm/Hz
TX1 to TX2 Isolation TX1 到 TX2 隔离度	ISO_TX	—	—	50	—	dB
TX2 to TX1 Isolation TX2 到 TX1 隔离度	ISO_TX	—	—	50	—	dB
Transmitter, 2.4 GHz / 发射器，2.4 GHz						
Output S22 输出 S22	—	—	—	(Not tested)	—	—
Maximum Output Power 最大输出功率	PO	1 MHz single-tone into 50 Ω load 1 MHz 单音输入 50 Ω 负载	—	7	—	dBm
Modulation Accuracy 调制精度	EVM_TX	40 MHz reference clock 40 MHz 参考时钟	—	−40	—	dB
Third-Order Output Intercept Point 三阶输出截断点	OIP3	—	—	17.5	—	dBm
Carrier Leakage 载波泄漏	CL	0 dB attenuation 0 dB 衰减	—	−50	—	dBc
Carrier Leakage 载波泄漏	CL	40 dB attenuation 40 dB 衰减	—	−44	—	dBc
Noise Spectral Density 噪声频谱密度	NSD	TX1A/TX2A, at 90 MHz offset TX1A/TX2A，90 MHz 偏移处	—	−138	—	dBm/Hz
TX1 to TX2 Isolation TX1 到 TX2 隔离度	ISO_TX	—	—	50	—	dB
TX2 to TX1 Isolation TX2 到 TX1 隔离度	ISO_TX	—	—	50	—	dB

Note: Typical values are measured at room temperature.

注：典型值在室温下测得。

11. Typical Characteristic Curves / 典型特性曲线

Note: All test curves are measured under typical conditions unless otherwise noted.

注：除非另有说明，所有测试曲线均在典型条件下测得。

11.1 LO Phase Noise / 本振相位噪声

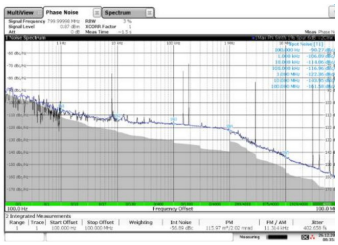


Figure 5. LO Phase Noise (800 MHz Band)

Figure 5. LO Phase Noise (800 MHz Band) / 图 5. 本振相位噪声（800 MHz 频段）

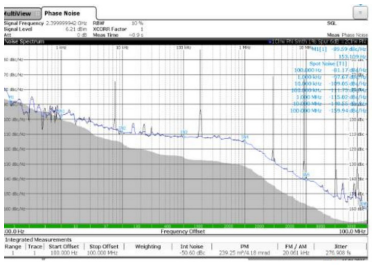


Figure 6. LO Phase Noise (2.4 GHz Band)

Figure 6. LO Phase Noise (2.4 GHz Band) / 图 6. 本振相位噪声（2.4 GHz 频段）

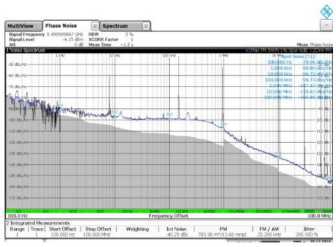


Figure 7. LO Phase Noise (5.5 GHz Band)

Figure 7. LO Phase Noise (5.5 GHz Band) / 图 7. 本振相位噪声（5.5 GHz 频段）

11.2 TX Performance – 800 MHz Band / TX 性能 – 800 MHz 频段

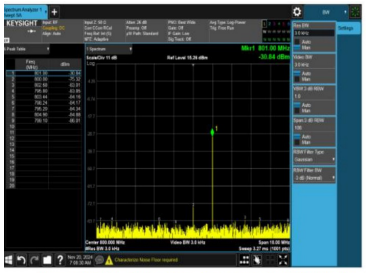


Figure 8. TX 40dB Attenuated Output (800 MHz Band)

Figure 8. TX 40 dB Atten. Output (800 MHz) / 图 8. TX 40 dB 衰减输出（800 MHz）



Figure 9. TX EVM (800 MHz Band)

Figure 9. TX EVM (800 MHz) / 图 9. TX EVM（800 MHz）

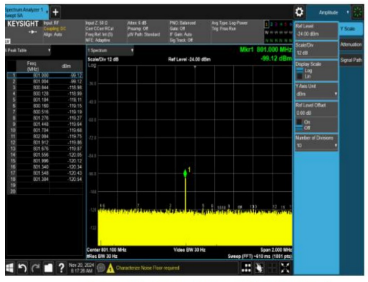


Figure 10. TX Isolation (800 MHz Band)

Figure 10. TX Isolation (800 MHz) / 图 10. TX 隔离度（800 MHz）

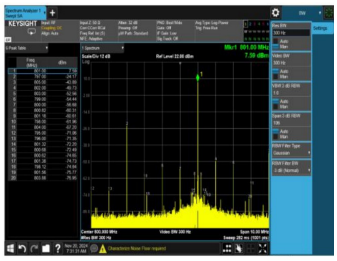


Figure 11. TX Max Output Power (800 MHz Band)

Figure 11. TX Max Output (800 MHz) / 图 11. TX 最大输出（800 MHz）

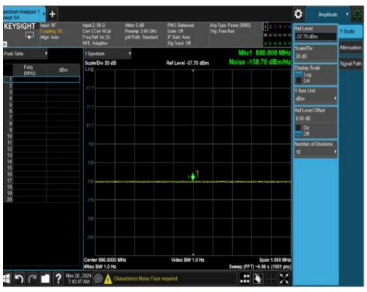


Figure 12. TX Noise Floor (800 MHz Band)

Figure 12. TX Noise Floor (800 MHz) / 图 12. TX 噪声底（800 MHz）



Figure 13. TX OIP3 (800 MHz Band)

Figure 13. TX OIP3 (800 MHz) / 图 13. TX OIP3（800 MHz）

11.3 TX Performance – 2.4 GHz Band / TX 性能 – 2.4 GHz 频段



Figure 14. TX 40dB Attenuated Output (2.4 GHz Band)

Figure 14. TX 40 dB Atten. Output (2.4 GHz) / 图 14. TX 40 dB 衰减输出（2.4 GHz）



Figure 15. TX EVM (2.4 GHz Band)

Figure 15. TX EVM (2.4 GHz) / 图 15. TX EVM（2.4 GHz）



Figure 16. TX Isolation (2.4 GHz Band)

Figure 16. TX Isolation (2.4 GHz) / 图 16. TX 隔离度（2.4 GHz）

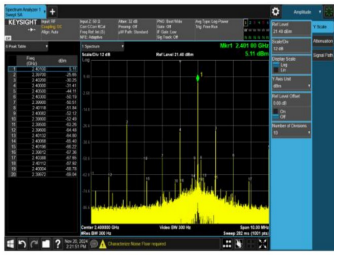


Figure 17. TX Max Output Power (2.4 GHz Band)

Figure 17. TX Max Output (2.4 GHz) / 图 17. TX 最大输出（2.4 GHz）

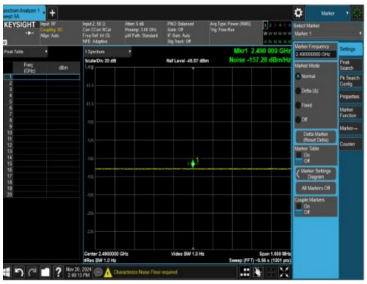


Figure 18. TX Noise Floor (2.4 GHz Band)

Figure 18. TX Noise Floor (2.4 GHz) / 图 18. TX 噪声底（2.4 GHz）



Figure 19. TX OIP3 (2.4 GHz Band)

Figure 19. TX OIP3 (2.4 GHz) / 图 19. TX OIP3（2.4 GHz）

11.4 TX Performance – 5.5 GHz Band / TX 性能 – 5.5 GHz 频段



Figure 20. TX 40dB Attenuated Output (5.5 GHz Band)

Figure 20. TX 40 dB Atten. Output (5.5 GHz) / 图 20. TX 40 dB 衰减输出（5.5 GHz）



Figure 21. TX EVM (5.5 GHz) / 图 21. TX EVM（5.5 GHz）



Figure 22. TX Isolation (5.5 GHz Band)

Figure 22. TX Isolation (5.5 GHz) / 图 22. TX 隔离度（5.5 GHz）

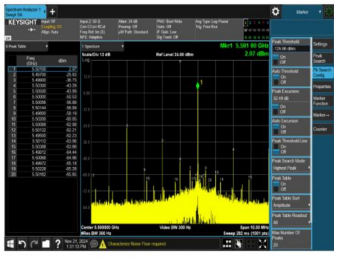


Figure 23. TX Max Output Power (5.5 GHz Band)

Figure 23. TX Max Output (5.5 GHz) / 图 23. TX 最大输出（5.5 GHz）



Figure 24. TX Noise Floor (5.5 GHz Band)

Figure 24. TX Noise Floor (5.5 GHz) / 图 24. TX 噪声底（5.5 GHz）

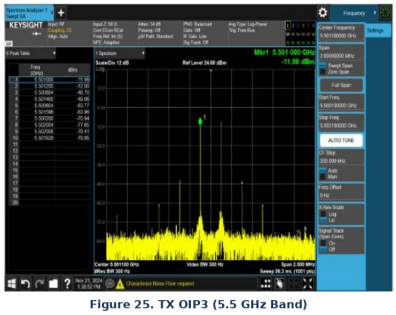


Figure 25. TX OIP3 (5.5 GHz Band)

Figure 25. TX OIP3 (5.5 GHz) / 图 25. TX OIP3（5.5 GHz）

12. Typical Application Circuit / 典型应用电路

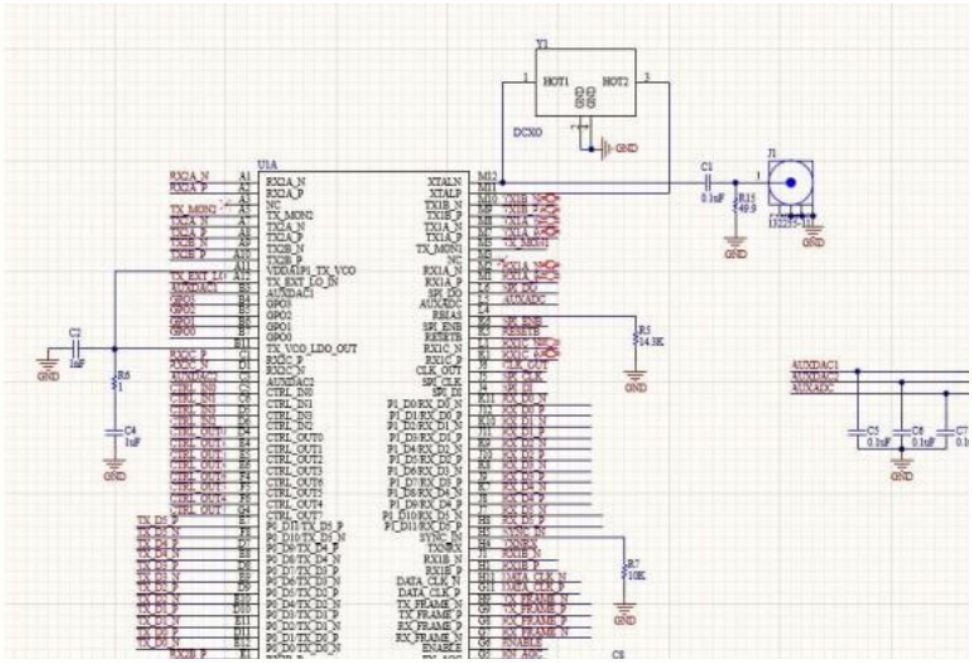


Figure 26. SXS055 Typical Application Circuit Diagram

Figure 26. Typical Application Circuit / 图 26. 典型应用电路

13. Functional Blocks and Operating Principle / 功能模块和工作原理

13.1 General Description / 概述

The SXS055 is a highly integrated radio frequency (RF) transceiver configurable for a wide range of applications. The device integrates all necessary RF, mixed-signal, and digital modules to provide complete transceiver functionality in a single device. Its programmability enables this wideband transceiver to adapt to multiple communication standards, including both FDD and TDD systems. This programmability also allows the device to interface with various baseband processors (BBPs) via a single 12-bit parallel data port, dual 12-bit parallel data ports, or a 12-bit low-voltage differential signaling (LVDS) interface.

SXS055 是一款高集成度的射频（RF）收发器，可配置用于广泛的应用。该器件集成了所有必要的 RF、混合信号和数字模块，在单个器件中提供完整的收发器功能。其可编程性使这款宽带收发器能够适应多种通信标准，包括 FDD 和 TDD 系统。这种可编程性还允许该器件通过单个 12 位并行数据端口、双 12 位并行数据端口或 12 位低压差分信号（LVDS）接口与各种基带处理器（BBP）连接。

The SXS055 also provides self-calibration and AGC systems to maintain high performance levels across varying temperature and input signal conditions. In addition, the device includes multiple test modes that allow system designers to insert test tones and build internal loopback modes during the prototype design phase, enabling design debugging and optimization of radio configurations for specific applications.

SXS055 还提供自校准和 AGC 系统，以在不同的温度和输入信号条件下保持高性能水平。此外，该器件包括多种测试模式，允许系统设计师在原型设计阶段插入测试音调和构建内部环回模式，从而实现设计调试和针对特定应用的无线电配置优化。

13.2 Receiver / 接收器

The analog input incorporates a differential switched-capacitor sample-and-hold structure. The differential structure provides superior AC characteristics at high-frequency inputs. The common-mode voltage of the differential inputs INP and INM is 0.95 V, supplied by the on-chip VCM pin. The maximum differential input amplitude is 2 VPP.

模拟输入采用差分开关电容采样保持结构。差分结构在高频输入时提供卓越的 AC 特性。差分输入 INP 和 INM 的共模电压为 0.95 V，由片上 VCM 引脚提供。最大差分输入幅度为 2 VPP。

The receiver section contains all necessary modules for receiving RF signals and converting them into digital data usable by the BBP. There are two independently controlled channels that can receive signals from different sources, enabling the device to be used in multiple-input multiple-output (MIMO) systems while sharing a common frequency synthesizer. Each channel has three inputs that can be multiplexed to the signal chain, allowing the SXS055 to be used in diversity systems with multiple antenna inputs.

接收器部分包含接收 RF 信号并将其转换为 BBP 可用数字数据所需的所有模块。有两个独立控制的通道可以接收来自不同源的信号，使该器件能够在共享一个共同频率合成器的同时用于多输入多输出（MIMO）系统。每个通道有三个输入，可以多路复用到信号链，允许 SXS055 用于具有多个天线输入的分集系统。

The receiver is a direct-conversion system comprising a low-noise amplifier (LNA), followed by in-phase (I) and quadrature (Q) amplifiers, a mixer, and channel-shaping filters that down-convert the received signal to baseband for digitization. An external LNA can also be connected to the device, providing designers with maximum flexibility to customize the receiver front-end for specific applications.

接收器是一个直接变频系统，包括一个低噪声放大器（LNA），其后是同相（I）和正交（Q）放大器、混频器和通道整形滤波器，将接收信号下变频到基带进行数字化。外部 LNA
也可以连接到该器件，为设计师提供最大的灵活性来为特定应用定制接收器前端。

Gain control is achieved through a pre-programmed gain index table that distributes gain among modules to optimize performance at each level. This can be implemented by enabling internal AGC in either fast or slow mode, or through manual gain control, allowing the BBP to adjust gain as needed. In addition, each channel features independent RSSI measurement, DC offset tracking, and all necessary circuitry for self-calibration.

增益控制通过预编程的增益索引表实现，该表在各模块之间分配增益，以优化每个级别的性能。这可以通过在快速或慢速模式下启用内部 AGC 来实现，或通过手动增益控制，允许 BBP 根据需要调整增益。此外，每个通道具有独立的 RSSI 测量、DC 偏移跟踪和自校准所需的所有电路。

The receiver includes a 12-bit sigma-delta ADC with adjustable sampling rate that generates a data stream from the received signal. The digitized signal can be further conditioned through a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sampling rate of each digital filter module can be adjusted by modifying the decimation factor to produce the required output data rate.

接收器包括一个采样率可调的 12 位 sigma-delta
ADC，从接收信号生成数据流。数字化信号可以通过一系列抽取滤波器和一个具有额外抽取设置的完全可编程的 128 抽头 FIR 滤波器进一步调理。每个数字滤波器模块的采样率可以通过修改抽取因子来调整，以产生所需的输出数据率。

13.3 Transmitter / 发射器

The transmitter section contains two identical, independently controlled channels that provide all necessary digital processing, mixed-signal, and RF modules to implement a direct-conversion system while sharing a general-purpose frequency synthesizer. Digital data received from the BBP passes through a fully programmable 128-tap FIR filter without interpolation options. The FIR output is fed to a series of interpolation filters that provide additional filtering and data rate interpolation before reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both I and Q channels feed into the RF module for up-conversion.

发射器部分包含两个相同、独立控制的通道，提供实现直接变频系统所需的所有数字处理、混合信号和 RF 模块，同时共享一个通用频率合成器。从 BBP 接收的数字数据通过一个没有插值选项的完全可编程的 128 抽头 FIR 滤波器。FIR 输出被送入一系列插值滤波器，在到达 DAC 之前提供额外的滤波和数据率插值。每个 12 位 DAC 具有可调的采样率。I 和 Q 通道都进入 RF 模块进行上变频。

When converted to baseband analog signals, the I and Q signals are filtered to remove sampling images and then fed into the up-conversion mixer. Here, the I and Q signals are recombined and modulated at the carrier frequency for transmission to the output stage. The combined signal also passes through analog filters that provide additional channel shaping before being transmitted to the output amplifier. Each transmit channel provides a wide, fine-gain attenuation adjustment range to help designers optimize the signal-to-noise ratio (SNR).

当转换为基带模拟信号时，I 和 Q 信号被滤波以去除采样镜像，然后送入上变频混频器。在这里，I 和 Q 信号被重新组合并在载波频率上调制，以传输到输出级。组合信号还通过模拟滤波器，在传输到输出放大器之前提供额外的通道整形。

每个发射通道提供宽的、精细增益的衰减调整范围，以帮助设计师优化信噪比（SNR）。

Each transmit channel includes built-in self-calibration circuitry to support automatic real-time adjustment. The transmitter module also provides a TX monitor module for each channel. This module monitors the transmitter output and routes it back to the BBP through an unused receiver channel for signal monitoring. The TX monitor module is only available in TDD mode when the receiver is idle.

每个发射通道包括内置的自校准电路，以支持自动实时调整。发射器模块还为每个通道提供 TX 监测模块。该模块监测发射器输出，并通过未使用的接收器通道将其路由回 BBP 进行信号监测。TX 监测模块仅在接收器空闲的 TDD 模式下可用。

13.4 Clock Input Options / 时钟输入选项

The reference clock used for SXS055 operation can be provided by two different clock sources. The first option is to use a dedicated crystal oscillator with a frequency between 19 MHz and 50 MHz, connected between the XTALP and XTALN pins. The second option is to connect an external oscillator or clock distribution device (such as the AD9548) to the XTALN pin (with the XTALP pin left open). If an external oscillator is used, the frequency can range from 10 MHz to 80 MHz.

用于 SXS055 操作的参考时钟可以由两种不同的时钟源提供。第一个选项是使用频率在 19 MHz 和 50 MHz 之间的专用晶体振荡器，连接在 XTALP 和 XTALN 引脚之间。第二个选项是将外部振荡器或时钟分配器件（例如 AD9548）连接到 XTALN 引脚（XTALP 引脚保持开路）。如果使用外部振荡器，频率范围可以从 10 MHz 到 80 MHz。

This reference clock is used to clock the frequency synthesizer modules, which internally generate all data clocks, sampling clocks, and local oscillators. Crystal frequency error can be eliminated by using digitally programmable, digitally controlled crystal oscillator (DCXO) functionality to adjust on-chip variable capacitors. These capacitors can trim the crystal frequency variation in the system, resulting in a more accurate reference clock from which all other frequencies are derived. This feature can also be used in conjunction with the on-chip temperature detection function to provide oscillator frequency temperature compensation during normal operation.

该参考时钟用于为频率合成器模块提供时钟，这些模块在内部生成所有数据时钟、采样时钟和本振。晶体频率误差可以通过使用数字可编程、数字控制晶体振荡器（DCXO）功能来调整片上可变电容来消除。这些电容可以微调系统中的晶体频率变化，从而产生更准确的参考时钟，所有其他频率都源自该时钟。此功能还可以与片上温度检测功能结合使用，在正常操作期间提供振荡器频率温度补偿。

13.5 Frequency Synthesizer / 频率合成器

The SXS055 contains two identical frequency synthesizers for generating the required LO signals for the RF signal paths: one for the receiver and one for the transmitter. The phase-locked loop (PLL) frequency synthesizer employs a fractional-N design incorporating fully integrated voltage-controlled oscillators (VCOs) and loop filters. In TDD operation mode, the frequency synthesizer is enabled and disabled according to the requirements of RX and TX frames. In FDD mode, the TX PLL and RX PLL can be active simultaneously. These PLLs require no external components.

SXS055 包含两个相同的频率合成器，用于为 RF 信号路径生成所需的 LO 信号：一个用于接收器，一个用于发射器。锁相环（PLL）频率合成器采用分数 N 分频设计，包含完全集成的压控振荡器（VCO）和环路滤波器。在 TDD 操作模式下，频率合成器根据 RX 和 TX 帧的要求启用和禁用。在 FDD 模式下，TX PLL 和 RX PLL 可以同时活动。这些 PLL 不需要外部组件。

The SXS055 also includes a baseband PLL frequency synthesizer for generating all baseband-related clock signals. These include ADC and DAC sampling clocks, the DATA_CLK signal (see the “Digital Data Interface” section), and all data framing signals. The PLL programming frequency range is 700 MHz to 1400 MHz, depending on the system data rate and sampling rate requirements.

SXS055 还包括一个基带 PLL 频率合成器，用于生成所有与基带相关的时钟信号。这些包括 ADC 和 DAC 采样时钟、DATA_CLK 信号（见“数字数据接口”部分）和所有数据帧信号。PLL 编程频率范围为 700 MHz 至 1400 MHz，取决于系统数据率和采样率要求。

13.6 Digital Data Interface / 数字数据接口

The SXS055 data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP. The data ports can be configured as single-ended CMOS or differential LVDS formats. Both formats can be configured in multiple ways to meet system requirements for data ordering and data port connections. These include single-port data bus, dual-port data bus, single data rate, dual data rate, and various data ordering combinations to transfer data from different channels across the bus at the appropriate time. Bus transmission is controlled through simple hardware handshaking signals. The two ports can operate in bidirectional (TDD) mode or full-duplex (FDD) mode, where in the latter mode half of the bits are used for transmit data and half for receive data. The interface can also be configured to use only one data port for applications that do not require high data rates and prefer to use fewer interface pins.

SXS055 数据接口使用并行数据端口（P0 和 P1）在器件和 BBP 之间传输数据。数据端口可配置为单端 CMOS 或差分 LVDS 格式。两种格式都可以多种方式配置，以满足系统对数据顺序和数据端口连接的要求。这些包括单端口数据总线、双端口数据总线、单数据率、双数据率，以及各种数据顺序组合，以便在适当的时间通过总线传输来自不同通道的数据。总线传输通过简单的硬件握手信号控制。两个端口可以在双向（TDD）模式或全双工（FDD）模式下操作，在后一种模式下，一半位用于发射数据，一半用于接收数据。该接口还可以配置为仅使用一个数据端口，用于不需要高数据率并倾向于使用更少接口引脚的应用。

13.7 DATA_CLK Signal / DATA_CLK 信号

A DATA_CLK signal is provided with the RX data, which the BBP can use when receiving data. DATA_CLK can be set to provide single data rate (SDR) timing (where data is sampled on each rising clock edge) or dual data rate (DDR) timing (where data is captured on both rising and falling edges simultaneously). This timing applies to operation modes using either a single port or two ports.

DATA_CLK 信号与 RX 数据一起提供，BBP 在接收数据时可以使用。DATA_CLK 可设置为提供单数据率（SDR）时序（数据在每个时钟上升沿采样）或双数据率（DDR）时序（数据在上升沿和下降沿同时捕获）。此时序适用于使用单个端口或两个端口的操作模式。

14. Registers / 寄存器

Refer to the SXS055 Register Map Manual (register-compatible with the foreign reference device).

请参考 SXS055 寄存器映射手册（与国外参考器件寄存器兼容）。

Refer to the SXS055 Register Map & Software Migration Guide. Controlled documentation is available upon request.

请参考 SXS055 寄存器映射和软件迁移指南。受控文档可根据要求提供。

15. Power Supply – Ground Protection (ESD) / 电源 – 接地保护（ESD）

To improve the electrostatic discharge (ESD) immunity of the device, ESD protection circuits exist between various power supply pins inside the device. Each ESD protection diode has a forward conduction voltage drop of approximately 0.35 V. During power-up and normal operation, prolonged forward conduction of these ESD protection diodes should be avoided.

为了提高器件的静电放电（ESD）抗扰度，器件内部各电源引脚之间存在 ESD 保护电路。每个 ESD 保护二极管的正向导通压降约为 0.35 V。在上电和正常操作期间，应避免这些 ESD 保护二极管长时间正向导通。

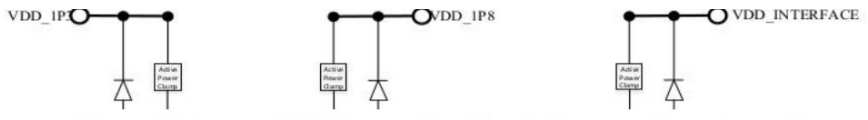


Figure 27. Internal ESD Protection Circuit Between Power Supplies

Figure 27. Internal ESD Protection Circuit / 图 27. 内部 ESD 保护电路

16. Precautions / 注意事项

16.1 Installation Notes / 安装注意事项

1. Pay attention to device orientation during soldering to avoid mis-soldering.

1. 焊接时注意器件方向，避免焊接错误。

2. Instruments and meters used for circuit debugging must have good unified grounding. PCB design must ensure good grounding and power supply decoupling.
2. 用于电路调试的仪器仪表必须具有良好的统一接地。PCB 设计必须确保良好的接地和电源去耦。

3. Ensure that power supply polarity is not reversed and that input/output terminals are not short-circuited to the power supply, as this may cause circuit damage.
3. 确保电源极性不反接，输入/输出端子不与电源短路，因为这可能导致电路损坏。

16.2 Operation Notes / 操作注意事项

1. Power-up requirements: It is recommended that the analog power supply and digital power supply be powered up simultaneously, or that the analog power supply is powered up first.
1. 上电要求：建议模拟电源和数字电源同时上电，或先给模拟电源上电。

2. Use capacitors with low ESR for decoupling at the LDO output.
2. 在 LDO 输出端使用低 ESR 电容进行去耦。

3. In applications, large-area PCB grounding is recommended. This eliminates potential differences that may exist due to different ground points and reduces the effect of capacitance generated by the circuit board on the circuit.
3. 在应用中，建议大面积 PCB 接地。这消除了由于不同接地点可能存在的电位差，并减少了电路板产生的电容对电路的影响。

4. Each power supply pin requires a nearby 1 µF or 0.1 µF capacitor.
4. 每个电源引脚附近需要一个 1 µF 或 0.1 µF 电容。

5. For the analog input section, if differential input is used, the differential input traces must be of equal length.
5. 对于模拟输入部分，如果使用差分输入，差分输入走线必须等长。

6. Digital and analog power supplies must be separated.
6. 数字和模拟电源必须分开。

16.3 Protection Notes / 防护注意事项

1. All output pins of this circuit are designed with electrostatic protection structures; however, high-energy electrical pulses may still damage the circuit. Therefore, electrostatic protection should be observed during testing, handling, and storage.
1. 该电路的所有输出引脚都设计有静电保护结构；然而，高能量电脉冲仍可能损坏电路。因此，在测试、处理和存储期间应遵守静电保护。

1. All device terminals incorporate ESD-protection structures; however, high-energy electrical pulses may still damage the device. Apply ESD protection during testing, handling, and storage.
1. 所有器件端子都包含 ESD 保护结构；然而，高能量电脉冲仍可能损坏器件。在测试、处理和存储期间应用 ESD 保护。

2. Exceeding absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.
2. 超过绝对最大额定值可能对器件造成永久性损坏。这些只是应力额定值；并不意味着器件在这些或任何其他超出本规范操作部分所示条件的条件下能正常工作。

3. When protected from direct exposure to rain and snow, product packaging can be transported using safe transportation tools. However, products must not be stored together with acidic, alkaline, or other corrosive substances. Packaging should be safe; existing transportation tools may be used.
3. 在防止直接暴露于雨雪的情况下，产品包装可以使用安全的运输工具运输。然而，产品不得与酸性、碱性或其他腐蚀性物质一起存储。包装应安全；可以使用现有的运输工具。

4. The storage environment for packaged products must meet Class I warehouse requirements as specified in Section 8.1 of Q/W 657A (temperature: 15°C to 25°C, humidity: 25% to 65%). The area must be free of acidic, alkaline, or other corrosive gases, well-ventilated, and equipped with appropriate anti-static measures.
4. 包装产品的存储环境必须满足 Q/W 657A 第 8.1 节规定的 I 类仓库要求（温度：15°C 至 25°C，湿度：25% 至 65%）。该区域必须无酸性、碱性或其他腐蚀性气体，通风良好，并配备适当的防静电措施。

16.4 Assembly Notes / 组装注意事项

1. This product has a moisture sensitivity level of MSL3. After removal from the moisture-proof bag, the maximum allowable exposure time to the ambient environment before dry storage or baking and reflow is: ≤30°C/60%RH, 168h.

1. 本产品湿度敏感等级为
MSL3。从防潮袋中取出后，在干燥存储或烘烤和回流焊之前，允许暴露于环境的最大时间为：≤30°C/60%RH，168h。

2. If device storage conditions cannot be controlled or traced, strictly perform baking at 125°C for 8 hours before assembly.
2. 如果器件存储条件无法控制或追溯，在组装前严格执行 125°C 烘烤 8 小时。

3. If the assembly environment temperature and humidity cannot be guaranteed at ≤30°C/60%RH, complete soldering within 12 hours after baking.
3. 如果组装环境的温度和湿度无法保证在 ≤30°C/60%RH，在烘烤后 12 小时内完成焊接。

4. After baking, the product is highly prone to static electricity generation; ESD protection must be observed during all handling procedures.
4. 烘烤后，产品极易产生静电；在所有处理程序中必须遵守 ESD 保护。

5. For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C to 235°C. The maximum peak temperature is not recommended to exceed 235°C. Time within ±5°C of peak temperature ≤20s, time above liquidus 60 to 90s, ramp-up rate 2 to 4°C/s, ramp-down rate 2 to 6°C/s.
5. 对于使用有铅回流焊（Sn63Pb37）的板级组装，推荐的峰值温度范围为 210°C 至 235°C。最大峰值温度不建议超过 235°C。在峰值温度 ±5°C 内的时间 ≤20s，液相线以上时间 60 至 90s，升温速率 2 至 4°C/s，降温速率 2 至 6°C/s。

6. For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C to 245°C. The maximum peak temperature is not recommended to exceed 260°C. Time within ±5°C of peak temperature ≤20s, time above liquidus 60 to 90s, ramp-up rate 2 to 4°C/s, ramp-down rate 2 to 6°C/s.
6. 对于使用无铅回流焊（SAC305）的板级组装，推荐的峰值温度范围为 230°C 至 245°C。最大峰值温度不建议超过 260°C。在峰值温度 ±5°C 内的时间 ≤20s，液相线以上时间 60 至 90s，升温速率 2 至 4°C/s，降温速率 2 至 6°C/s。

7. If the mixed assembly process requires elevated temperature, ensure that the maximum body temperature of the device does not exceed 260°C (device body temperature is measured at the top surface of the device during reflow soldering).
7. 如果混合组装工艺需要升高的温度，确保器件的最大本体温度不超过
260°C（器件本体温度在回流焊期间在器件顶表面测得）。

8. This product uses lead-free/leaded solder balls with SAC305 material.
8. 本产品使用 SAC305 材料的无铅/有铅焊球。

17. Common Faults and Remedies / 常见故障和解决方法

1. No signal output: Check whether there is a clock input at the clock output pin, verify that power and ground signal connections are normal, and ensure that input voltage and reference voltage are accurate.
1. 无信号输出：检查时钟输出引脚是否有时钟输入，验证电源和地信号连接是否正常，并确保输入电压和参考电压准确。

1. No signal output: Verify that a valid clock is present at the clock input pin, verify that power and ground connections are normal, and ensure that input and reference voltages are within specification.
1. 无信号输出：验证时钟输入引脚是否有有效时钟，验证电源和地连接是否正常，并确保输入和参考电压在规范范围内。

2. Output data jitter: Check external circuits and connections, and ensure the reference voltage is stable.
2. 输出数据抖动：检查外部电路和连接，并确保参考电压稳定。

3. Unstable device operation: Check the power supply and ensure the power supply voltage is stable.
3. 器件操作不稳定：检查电源并确保电源电压稳定。

Note: For technical support, please contact SHENXIN TECH at felix@shenxinic.com or +852 51367095.
注：技术支持请联系 SHENXIN TECH：felix@shenxinic.com 或 +852 51367095。

18. Contact Information / 联系信息

For technical support, ordering information, or any other inquiries, please contact SHENXIN TECH:
如需技术支持、订购信息或任何其他咨询，请联系 SHENXIN TECH：

Item / 项目	Details / 详情
Company / 公司	Shenzhen Shenxin Technology Co., Ltd. / 深圳市深信科技有限公司

Brand / 品牌	SHENXIN TECH
Email / 电子邮件	felix@shenxinic.com
Phone / 电话	+852 51367095
Website / 网站	www.shenxinic.com

19. Additional Information (Appendix) / 附加信息（附录）

1. Initial release date of this datasheet: July 2026.

1. 本数据手册的首次发布日期：2026 年 7 月。

2. Product status: ☒ In production (this product model is currently in production and formal products can be provided) ☒ Pre-release (this product model has not yet entered formal production; samples can be provided)

2. 产品状态：☒ 量产中（该产品型号目前正在量产，可提供正式产品）☒ 预发布（该产品型号尚未进入正式量产；可提供样品）

3. Notes on replacement of imported devices:

3. 进口器件替代说明：

Appendix Table 1. Absolute Maximum Rating Comparison / 附表 1. 绝对最大额定值对比

Parameter / 参数	SXS055 Specification / SXS055 规格	Foreign Reference Device / 国外参考器件	Comparison Result / 对比结果
Analog and digital core supply voltage to ground (VDDx to VSSx) 模拟和数字核心电源对地电压（VDDx 至 VSSx）	−0.3 V to 1.4 V	−0.3 V to 1.4 V	Identical / 相同
Interface voltage to ground (VDD_INTERFACE to VSSx) 接口对地电压（VDD_INTERFACE 至 VSSx）	−0.3 V to 3.0 V	−0.3 V to 3.0 V	Identical / 相同
GPO voltage to ground (VDD_GPO to VSSx) GPO 对地电压（VDD_GPO 至 VSSx）	−0.3 V to 3.9 V	−0.3 V to 3.9 V	Identical / 相同
Logic input/output to ground (VSSx) 逻辑输入/输出对地（VSSx）	−0.3 V to VDD_INTERFACE + 0.3 V	−0.3 V to VDD_INTERFACE + 0.3 V	Identical / 相同
Input current on any pin except power supply pins 除电源引脚外任何引脚的输入电流	±10 mA	±10 mA	Identical / 相同
RF input (peak power) RF 输入（峰值功率）	2.5 dBm	2.5 dBm	Identical / 相同
TX monitor input power (peak power) TX 监测输入功率（峰值功率）	9 dBm	9 dBm	Identical / 相同
Package power dissipation 封装功耗	(TJMAX − TA)/θJA	(TJMAX − TA)/θJA	Identical / 相同
Maximum junction temperature (TJMAX) 最高结温（TJMAX）	110°C	110°C	Identical / 相同
Operating temperature range (TA) 工作温度范围（TA）	−40°C to 85°C	−40°C to 85°C	Identical / 相同
Storage temperature range (Tstg) 存储温度范围（Tstg）	−65°C to 150°C	−65°C to 150°C	Identical / 相同

Appendix Table 2. Recommended Operating Conditions Comparison / 附表 2. 推荐工作条件对比

Parameter / 参数	SXS055 Specification / SXS055 规格	Foreign Reference Device / 国外参考器件	Comparison Result / 对比结果
Input reference clock 输入参考时钟	40 MHz	40 MHz	Identical / 相同
Analog and digital core supply voltage (VDDx) 模拟/数字核心电源电压（VDDx）	1.3 V	1.3 V	Identical / 相同
Interface voltage (VDD_INTERFACE) 接口电压（VDD_INTERFACE）	1.8 V / 2.5 V	1.8 V / 2.5 V	Identical / 相同
GPO voltage (VDD_GPO) GPO 电压（VDD_GPO）	3.3 V	3.3 V	Identical / 相同
Operating ambient temperature (TA) 工作环境温度（TA）	−40°C to 85°C	−40°C to 85°C	Identical / 相同