SHENXIN TECH

RF Agile Transceivers / High-Speed Data Converters

SXS055

2T2R RF Agile Transceiver SoC | 20 MHz Tunable Channel Bandwidth

Customer Edition

Derived from controlled engineering source: V1.20260728

RF RANGE

325 MHz to 3.8 GHz

CHANNEL BANDWIDTH

Up to 20 MHz

DATA CONVERTERS

2T2R | 12-bit DAC / ADC

PACKAGE

CSP_BGA144 | -40°C to +85°C

DESIGN-IN POSITIONING

A highly integrated RF agile transceiver for point-to-point communication, pico/femtocell base stations, and general-purpose radio systems.

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Document Control

SHENXIN TECH | Customer Edition

PRODUCT	SXS055
ENGINEERING SOURCE VERSION	V1.20260728
CUSTOMER EDITION DATE	09 October 2026
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Customer-edition scope

- Customer-facing edition with verified electrical specifications retained.
- Internal comparison notes and preliminary test-board comments have been excluded.
- Controlled register and PCB assembly documentation is available upon request.

This customer edition preserves the controlled electrical specifications and operating limits from the engineering source. Request controlled register and PCB assembly documentation before a design release.

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Customer edition excludes internal comparison notes and preliminary test-board comments. Detailed controlled engineering documentation is available from SHENXIN TECH upon request.

1. Applications and Scope

- Point-to-point communication systems
- Pico/femtocell base stations
- General-purpose radio systems

2. Standards

- Detailed specification and confirmation number: *SXS055 RF Agile Transceiver Detailed Specification*
- Quality grade: Industrial grade

3. Product Features

- Supply voltages: 1.3V / 1.8V / 3.3V
- Integrated RF 2×2 transceiver with 12-bit DACs and ADCs
- Frequency range: 325 MHz to 3.8 GHz
- Supports TDD and FDD
- Tunable channel bandwidth: up to 20 MHz
- TX EVM: −34 dB
- Digital interface: CMOS / LVDS
- ESD rating: Class 1B, HBM 500V
- Product weight: 0.32 g ± 0.02 g

4. Product Description

The SXS055 is a high-performance, highly integrated RF agile transceiver designed for 3G and 4G pico/femtocell base station applications. Its programmability and wideband capability make it suitable for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and an integrated frequency synthesizer, simplifying the design process by providing a configurable digital interface to connect with a processor. The SXS055 operates over a frequency range of 325 MHz to 3.8 GHz, covering most licensed and unlicensed bands. It supports channel bandwidths up to 20 MHz.

The two independent direct conversion receivers of the SXS055 deliver industry-leading noise figure and linearity. Each receive subsystem includes independent Automatic Gain Control (AGC), DC offset correction, quadrature correction, and digital filtering, eliminating the need to implement these functions in the digital baseband. The SXS055 also offers a flexible manual gain mode that can be controlled externally. Two high-dynamic-range ADCs per channel digitize the received I and Q signals, which are then processed by configurable decimation filters and a 128-tap Finite Impulse Response (FIR) filter, ultimately outputting 12-bit signals at the appropriate sample rate.

The transmitter of the SXS055 uses a direct conversion architecture that achieves high modulation accuracy with ultra-low noise. This transmitter design produces an industry-leading transmit EVM (Error Vector Magnitude) of −34 dB, providing sufficient system margin for the selection of an external Power Amplifier (PA). An on-board transmit power monitor can be used as a power detector, enabling high-accuracy transmit power measurement.

The fully integrated Phase-Locked Loop (PLL) of the SXS055 provides low-power fractional-N frequency synthesis for all receive and transmit channels. The channel isolation required for FDD systems is integrated into the design. All Voltage-Controlled Oscillator (VCO) and loop filter components are integrated.

The device is packaged in a 10 mm × 10 mm, 144-pin Chip-Scale Ball Grid Array package (CSP_BGA).

The functional block diagram of the product is shown in Figure 1.

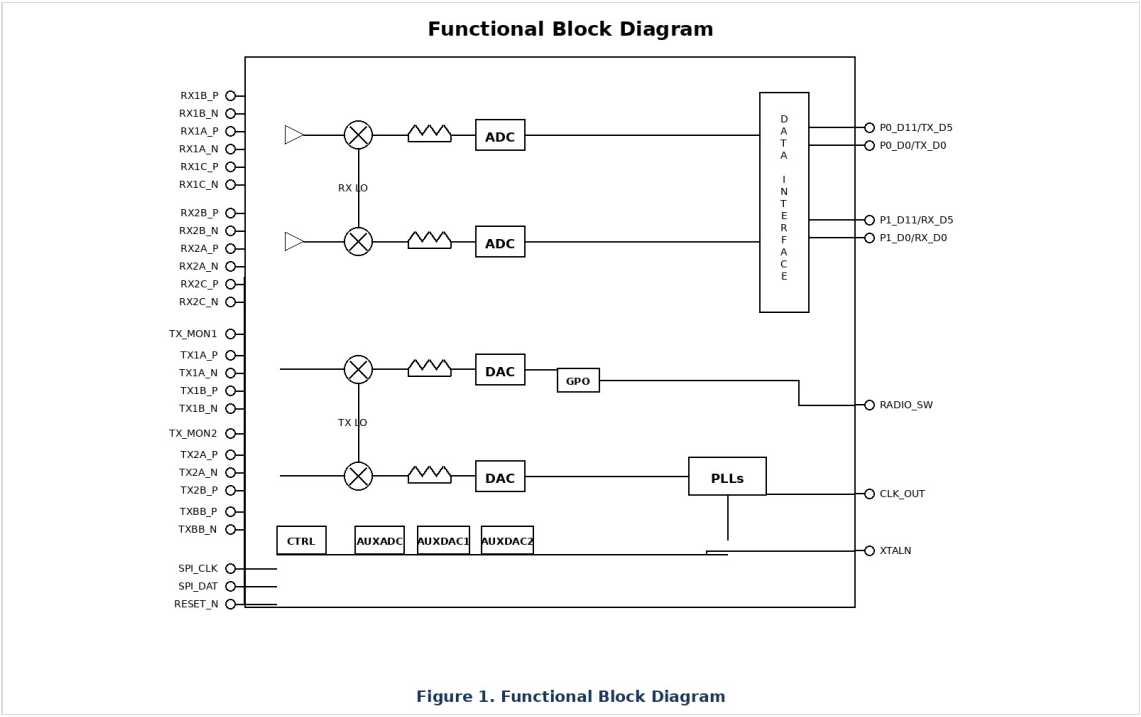


Figure 1. Functional Block Diagram

Figure 1. Functional Block Diagram

Notes:

1. **RX and TX Baseband Bandwidth Calibration**
   The clock for baseband bandwidth calibration is derived from the main clock divider. The RX divide ratio is determined by Reg1F8[7:0] (BBF Tune Divide), and the TX divide ratio is determined by Reg0D6[7:0]. This divide ratio must not be odd; i.e., Reg1F8[0] and Reg0D6[0] must not be set to 1. The divide ratio is jointly determined by the BBPLL frequency and the baseband bandwidth, according to the following formula:
   `BBF Tune Divide[8:0] = ceil((BBPLL Freq × ln(2)) / (BBBW × 1.4 × 2π))`
   During chip initialization, avoid setting the values of the two registers listed above to 1. After initialization, verify the values of these two registers. If the value is 1, a feasible approach is to adjust the baseband bandwidth and re-initialize the chip to avoid setting these two register values to 1.
2. **RX I/Q Mismatch**
   At the 1.8 GHz local oscillator, the RX channel may exhibit I/Q mismatch at a high temperature of 80°C ± 4°C. (Comparable off-the-shelf products exhibit mismatch at −20°C.)

5. Product Outline and Physical Pictures

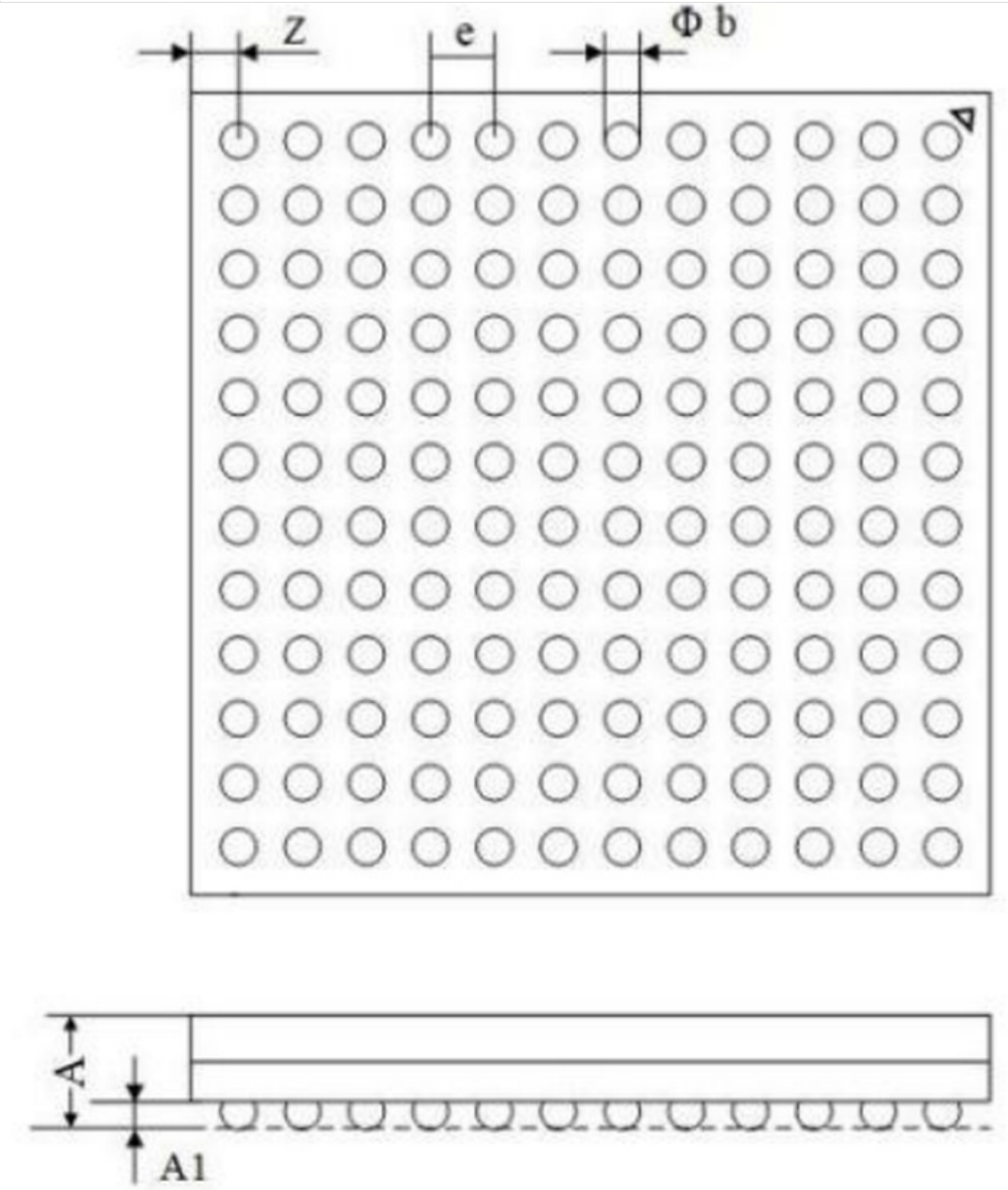


Figure 2. Package Outline Dimensions

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Figure 3. Unit: mm

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	1.27	1.42[a]	1.57	e	—	0.80	—
A_1	0.30	0.35[a]	0.40	Φb	0.40	0.45[a]	0.50
D	9.80	10.00[a]	10.20	Z	—	0.60[a]	0.70
E	9.80	10.00[a]	10.20				

[a] Actual nominal package value; recommended for users' reference when designing pad dimensions.
Note: For recommended pad design, refer to the electrical mounting instructions.

6. Pin Configuration (Top View)

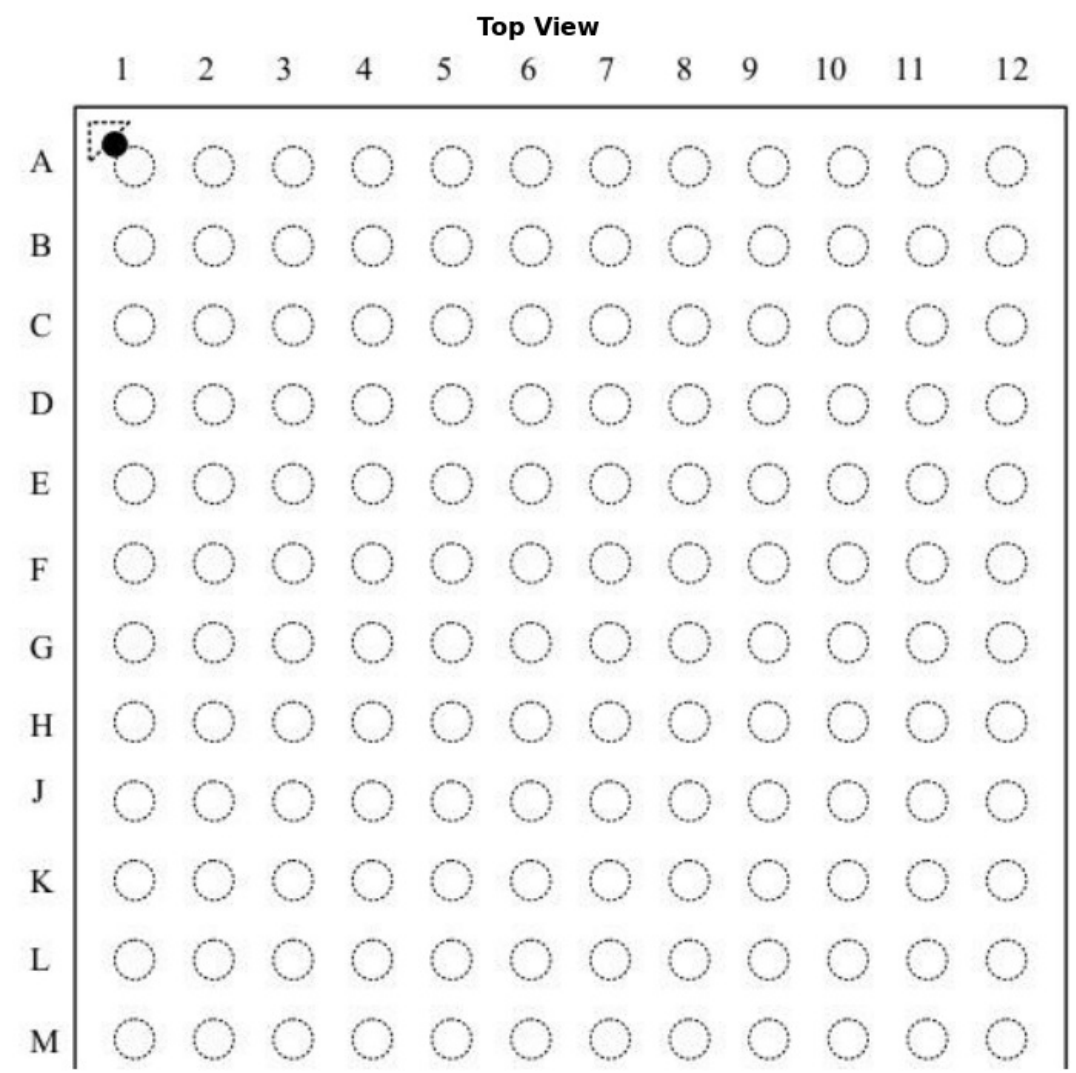


Figure 4. Pin Configuration (Top View)

Figure 4. Pin Configuration (Top View)

7. Pin Function Description Table

Pin No.	Symbol	Name / Description	I/O	Pin No.	Symbol	Name / Description	I/O
A1	RX2A_N	RX Channel 2 Input A Negative	I	**G1**	VSSA	Analog Ground	I
A2	RX2A_P	RX Channel 2 Input A Positive	I	**G2**	RX_VCO_LDO_OUT	RX VCO LDO Output	O
A3	NC	No Connect[a]	/	**G3**	VDDA1P1_RX_VCO	RX VCO LDO Input	I
A4	VSSA	Analog Ground	I	**G4**	CTRL_OUT7	Control Output 7	O
A5	TX_MON2	TX Channel 2 Power Monitor Input	I	**G5**	EN_AGC	Manual Control Input for AGC	I
A6	VSSA	Analog Ground	I	**G6**	ENABLE	State Machine Enable Signal	I
A7	TX2A_N	TX Channel 2 Output A Negative	O	**G7**	RX_FRAME_N	RX Data Frame Differential Output Negative	O
A8	TX2A_P	TX Channel 2 Output A Positive	O	**G8**	RX_FRAME_P	RX Data Frame Differential Output Positive	O
A9	TX2B_N	TX Channel 2 Output B Negative	O	**G9**	TX_FRAME_P	TX Data Frame Differential	I

						Input Positive	
A10	TX2B_P	TX Channel 2 Output B Positive	O	**G10**	FB_CLK_N	TX Data Clock Differential Input Negative	I
A11	VDDA1P1_TX_VCO	TX VCO Power Input	I	**G11**	DATA_CLK_P	RX Data Clock Differential Output Positive	O
A12	VSSA	Analog Ground	I	**G12**	VSSD	Digital Ground	I
B1	VSSA	Analog Ground	I	**H1**	RX1B_P	RX Channel 1 Input B Positive	I
B2	VSSA	Analog Ground	I	**H2**	VSSA	Analog Ground	I
B3	AUXDAC1	Auxiliary DAC 1 Output	O	**H3**	VSSA	Analog Ground	I
B4	GPO_3	General Purpose Output 3	O	**H4**	TXNRX	Enable State Machine TX/RX State Control Signal	I
B5	GPO_2	General Purpose Output 2	O	**H5**	VSSA	Analog Ground	I
B6	GPO_1	General Purpose Output 1	O	**H6**	VSSA	Analog Ground	I
B7	GPO_0	General Purpose Output 0	O	**H7**	VSSD	Digital Ground	I
B8	VDD_GPO	Auxiliary DAC and GPO Power	I	**H8**	P1_D11/RX_D5_P	P1 Port D11 / RX D5 Differential Output Positive	I/O
B9	VDDA1P3_TX_LO	TX LO 1.3V Power	I	**H9**	TX_FRAME_N	TX Data Frame Differential Input Negative	I
B10	VDDA1P3_TX_VCO_LDO	TX VCO LDO Power Input	I	**H10**	VSSD	Digital Ground	I
B11	TX_VCO_LDO_OUT	TX VCO LDO Power Output	O	**H11**	DATA_CLK_N	RX Data Clock Differential Output Negative	O
B12	VSSA	Analog Ground	I	**H12**	VDD_INTERFACE	Digital I/O Power	I
C1	RX2C_P	RX Channel 2 Input C Positive	I	**J1**	RX1B_N	RX Channel 1 Input B Negative	I
C2	VSSA	Analog Ground	I	**J2**	VSSA	Analog Ground	I
C3	AUXDAC2	Auxiliary DAC 2 Output	O	**J3**	VDDA1P3_RX_SYNTH	1.3V Power	I
C4	TEST/ENABLE	Test Input	I	**J4**	SPI_DI	SPI Serial Data Input	I
C5	CTRL_IN0	Control Input 0	I	**J5**	SPI_CLK	SPI Clock Input	I
C6	CTRL_IN1	Control Input 1	I	**J6**	CLK_OUT	Clock Output	O
C7	VSSA	Analog Ground	I	**J7**	P1_D10/RX_D5_N	P1 Port D10 / RX D5 Differential Output Negative	I/O
C8	VSSA	Analog Ground	I	**J8**	P1_D9/RX_D4_P	P1 Port D9 / RX D4 Differential Output Positive	I/O
C9	VSSA	Analog Ground	I	**J9**	P1_D7/RX_D3_P	P1 Port D7 / RX D3 Differential Output Positive	I/O
C10	VSSA	Analog Ground	I	**J10**	P1_D5/RX_D2_P	P1 Port D5 / RX D2 Differential Output Positive	I/O
C11	VSSA	Analog Ground	I	**J11**	P1_D3/RX_D1_P	P1 Port D3 / RX D1 Differential Output Positive	I/O
C12	VSSA	Analog Ground	I	**J12**	P1_D1/RX_D0_P	P1 Port D1 / RX D0 Differential Output Positive	I/O
D1	RX2C_N	RX Channel 2 Input C Negative	I	**K1**	RX1C_P	RX Channel 1 Input C Positive	I
D2	VDDA1P3_RX_RF	Receiver 1.3V Power	I	**K2**	VSSA	Analog Ground	I
D3	VDDA1P3_RX_TX	1.3V Power	I	**K3**	VDDA1P3_TX_SYNTH	1.3V Power	I
D4	CTRL_OUT0	Control Output 0	O	**K4**	VDDA1P3_BB	1.3V Power	I
D5	CTRL_IN3	Control Input 3	I	**K5**	RESET	Asynchronous Reset Input	I
D6	CTRL_IN2	Control Input 2	I	**K6**	SPI_EN	SPI Enable Input	I
D7	P0_D9/TX_D4_P	P0 Port D9 / TX D4 Differential Input Positive	I/O	**K7**	P1_D8/RX_D4_N	P1 Port D8 / RX D4 Differential Output Negative	I/O
D8	P0_D7/TX_D3_P	P0 Port D7 / TX D3 Differential Input Positive	I/O	**K8**	P1_D6/RX_D3_N	P1 Port D6 / RX D3 Differential Output Negative	I/O
D9	P0_D5/TX_D2_P	P0 Port D5 / TX D2 Differential Input Positive	I/O	**K9**	P1_D4/RX_D2_N	P1 Port D4 / RX D2 Differential Output Negative	I/O
D10	P0_D3/TX_D1_P	P0 Port D3 / TX D1 Differential Input Positive	I/O	**K10**	P1_D2/RX_D1_N	P1 Port D2 / RX D1 Differential Output Negative	I/O
D11	P0_D1/TX_D0_P	P0 Port D1 / TX D0 Differential	I/O	**K11**	P1_D0/RX_D0_N	P1 Port D0 / RX D0 Differential	I/O

		Input Positive				Output Negative	
D12	VSSD	Digital Ground	I	**K12**	VSSD	Digital Ground	I
E1	RX2B_P	RX Channel 2 Input B Positive	I	**L1**	RX1C_N	RX Channel 1 Input C Negative	I
E2	VDDA1P3_RX_LO	RX LO 1.3V Power	I	**L2**	VSSA	Analog Ground	I
E3	VDDA1P3_TX_LO_BUFFER	TX LO Buffer 1.3V Power	I	**L3**	VSSA	Analog Ground	I
E4	CTRL_OUT1	Control Output 1	O	**L4**	RBIAS	Bias Input Reference	I
E5	CTRL_OUT2	Control Output 2	O	**L5**	AUXADC	Auxiliary ADC	I
E6	CTRL_OUT3	Control Output 3	O	**L6**	SPI_DO	SPI Serial Output	O
E7	P0_D11/TX_D5_P	P0 Port D11 / TX D5 Differential Input Positive	I/O	**L7**	VSSA	Analog Ground	I
E8	P0_D8/TX_D4_N	P0 Port D8 / TX D4 Differential Input Negative	I/O	**L8**	VSSA	Analog Ground	I
E9	P0_D6/TX_D3_N	P0 Port D6 / TX D3 Differential Input Negative	I/O	**L9**	VSSA	Analog Ground	I
E10	P0_D4/TX_D2_N	P0 Port D4 / TX D2 Differential Input Negative	I/O	**L10**	VSSA	Analog Ground	I
E11	P0_D2/TX_D1_N	P0 Port D2 / TX D1 Differential Input Negative	I/O	**L11**	VSSA	Analog Ground	I
E12	P0_D0/TX_D0_N	P0 Port D0 / TX D0 Differential Input Negative	I/O	**L12**	VSSA	Analog Ground	I
F1	RX2B_N	RX Channel 2 Input B Negative	I	**M1**	RX1A_P	RX Channel 1 Input A Positive	I
F2	VDDA1P3_RX_VCO_LDO	RX VCO LDO Power Input	I	**M2**	RX1A_N	RX Channel 1 Input A Negative	I
F3	VSSA	Analog Ground	I	**M3**	NC	No Connect[a]	/
F4	CTRL_OUT6	Control Output 6	O	**M4**	VSSA	Analog Ground	I
F5	CTRL_OUT5	Control Output 5	O	**M5**	TX_MON1	TX Channel 1 Power Monitor Input	I
F6	CTRL_OUT4	Control Output 6	O	**M6**	VSSA	Analog Ground	I
F7	VSSD	Digital Ground	I	**M7**	TX1A_P	TX Channel 1 Output A Positive	O
F8	P0_D10/TX_D5_N	P0 Port D10 / TX D5 Differential Input Negative	I/O	**M8**	TX1A_N	TX Channel 1 Output A Negative	O
F9	VSSD	Digital Ground	I	**M9**	TX1B_P	TX Channel 1 Output B Positive	O
F10	FB_CLK_P	TX Data Clock Input Positive	I	**M10**	TX1B_N	TX Channel 1 Output B Negative	O
F11	VSSD	Digital Ground	I	**M11**	NC	No Connect[a]	I
F12	VDDD1P3_DIG	1.3V Digital Power	I	**M12**	XTALN	Reference Frequency Crystal Connection	I

[a] Leave this pin unconnected during use; do not connect to this pin.

8. Absolute Maximum Ratings

- Analog/digital core supply voltage to ground (V_{DDx} to V_{SSx}): −0.3 V to 1.4 V
- Interface voltage to ground ($V_{DD_INTERFACE}$ to V_{SSx}): −0.3 V to 3.0 V
- GPO voltage to ground (V_{DD_GPO} to V_{SSx}): −0.3 V to 3.9 V
- Logic input/output to ground (V_{SSx}): −0.3 V to $V_{DD_INTERFACE}$ + 0.3 V
- Input current on any pin except power pins: ±10 mA
- RF input (peak power): 2.5 dBm
- TX monitor input power (peak power): 9 dBm
- Package power dissipation: ($T_{JMAX} - T_A$) / θ_{JA}
- Maximum junction temperature (T_{JMAX}): 110°C
- Operating temperature range (T_A): −40°C to 85°C
- Storage temperature (T_{stg}): −65°C to 150°C

9. Recommended Operating Conditions

- Input reference clock: 40 MHz
- Analog/digital core supply voltage (V_{DDx}): 1.3 V
- Interface voltage ($V_{DD_INTERFACE}$): 1.8 V / 2.5 V
- GPO voltage (V_{DD_GPO}): 3.3 V
- Operating ambient temperature (T_A): −40°C to 85°C

10. Electrical Specifications

Unless otherwise noted: VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, all other VDDx pins = 1.3 V, T_A = 25°C.

Parameter	Symbol	Conditions	Reference Value			Unit
			Min.	Typ.	Max.	
Receiver (Frequency-Independent Parameters)						
Center Frequency	F_0	RX1A / RX2A	325	—	3800	MHz
Gain Control Range	Gain_Range	800 MHz	—	71.5	—	dB
		2300 MHz (RX1A, RX2A)	—	70	—	dB
		2300 MHz (RX1B, RX2B, RX1C, RX2C)	—	70	—	dB
Gain Step	GS	—	—	1	—	dB
RSSI Range	RSSI_Range	RX1A / RX2A	—	95	—	dB
RSSI Accuracy	—	—	—	±2.5	—	dB
Receiver, 800 MHz						
Noise Figure	NF	Maximum RX gain	—	2.5	—	dB
Third-Order Input Intercept Point	IIP3	RX1A/RX2A, maximum RX gain	—	−11	—	dBm
Second-Order Input Intercept Point	IIP2	RX1A/RX2A, maximum RX gain	—	55	—	dBm
Digital LO Leakage	LOL	At RX front end	—	−82	—	dBm
Quadrature Gain Error	—	—	—	0.2	—	%
Quadrature Phase Error	—	—	—	0.2	—	deg
Modulation Accuracy	EVM_RX	—	—	(Not tested)	—	—
Input S_{11}	—	—	—	(Not tested)	—	—
RX1A to RX2A Isolation	ISO_RX	—	—	68	—	dB

RX1C to RX2C Isolation	ISO_RX	—	—	68	—	dB
RX1B to RX2B Isolation	ISO_RX	—	—	55	—	dB
RX2A to RX1A Isolation	ISO_RX	—	—	68	—	dB
RX2C to RX1C Isolation	ISO_RX	—	—	68	—	dB
RX2B to RX1B Isolation	ISO_RX	—	—	55	—	dB
Receiver, 2.4 GHz						
Noise Figure	NF	Maximum RX gain	—	3.5	—	dB
Third-Order Input Intercept Point	IIP3	RX1A/RX2A, maximum RX gain	—	−10	—	dBm
Second-Order Input Intercept Point	IIP2	RX1A/RX2A, maximum RX gain	—	48	—	dBm
Digital LO Leakage	LOL	At RX front end	—	−82	—	dBm
Quadrature Gain Error	—	—	—	0.2	—	%
Quadrature Phase Error	—	—	—	0.2	—	deg
Modulation Accuracy	EVM_RX	—	—	(Not tested)	—	—
Input S_{11}	—	—	—	(Not tested)	—	—
RX1A to RX2A Isolation	ISO_RX	—	—	55	—	dB
RX1C to RX2C Isolation	ISO_RX	—	—	55	—	dB
RX1B to RX2B Isolation	ISO_RX	—	—	50	—	dB
RX2A to RX1A Isolation	ISO_RX	—	—	55	—	dB
RX2C to RX1C Isolation	ISO_RX	—	—	55	—	dB
RX2B to RX1B Isolation	ISO_RX	—	—	50	—	dB
Transmitter (Frequency-Independent Parameters)						
Center Frequency	F_0	TX1A / TX2A	325	—	3800	MHz
Power Control Range	PCR	TX1A / TX2A	—	90	—	dB
Power Control Resolution	PRes	TX1A / TX2A	—	0.25	—	dB
Transmitter, 800 MHz						
Output S_{22}	—	—	—	(Not tested)	—	—
Maximum Output Power	P_O	1 MHz single-tone into 50 Ω load	—	8	—	dBm
Modulation Accuracy	EVM_TX	19.2 MHz reference clock	—	−45	—	dB
Third-Order Output Intercept Point	OIP3	—	—	17	—	dBm
Carrier Leakage	CL	0 dB attenuation	—	−50	—	dBc
		40 dB attenuation	—	−40	—	dBc
Noise Spectral Density	NSD	TX1A/TX2A, at 90 MHz offset	—	−148	—	dBm/Hz
TX1 to TX2 Isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 Isolation	ISO_TX	—	—	50	—	dB
Transmitter, 2.4 GHz						
Output S_{22}	—	—	—	(Not tested)	—	—
Maximum Output Power	P_O	1 MHz single-tone into 50 Ω load	—	7	—	dBm
Modulation Accuracy	EVM_TX	40 MHz reference clock	—	−40	—	dB
Third-Order Output Intercept Point	OIP3	—	—	17.5	—	dBm
Carrier Leakage	CL	0 dB attenuation	—	−50	—	dBc
		40 dB attenuation	—	−44	—	dBc
Noise Spectral Density	NSD	TX1A/TX2A, at 90 MHz offset	—	−138	—	dBm/Hz
TX1 to TX2 Isolation	ISO_TX	—	—	50	—	dB
TX2 to TX1 Isolation	ISO_TX	—	—	50	—	dB

Note: Typical values are measured at room temperature.

11. Typical Characteristic Curves

Note: All test curves are measured under typical conditions unless otherwise noted.

11.1 LO Phase Noise

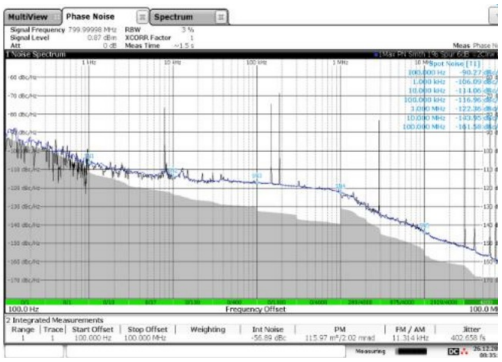


Figure 5. LO Phase Noise (800 MHz Band)

Figure 5. LO Phase Noise (800 MHz Band)

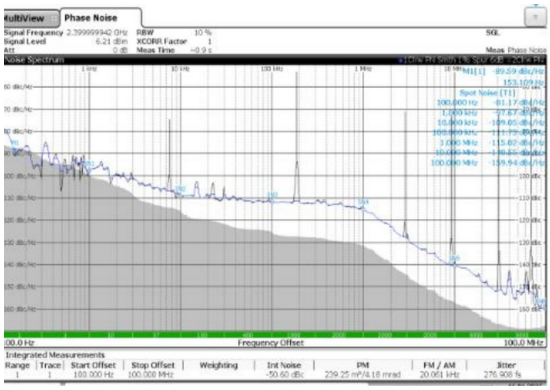


Figure 6. LO Phase Noise (2.4 GHz Band)

Figure 6. LO Phase Noise (2.4 GHz Band)

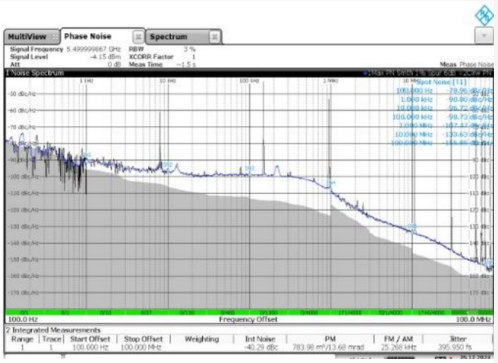


Figure 7. LO Phase Noise (5.5 GHz Band)

Figure 7. LO Phase Noise (5.5 GHz Band)

11.2 TX Performance – 800 MHz Band

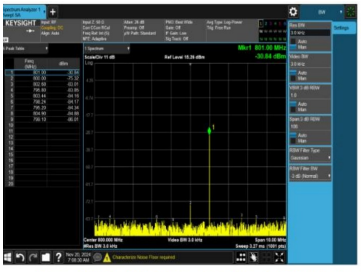


Figure 8. TX 40dB Attenuated Output (800 MHz Band)

Figure 8. TX 40 dB Atten. Output (800 MHz)

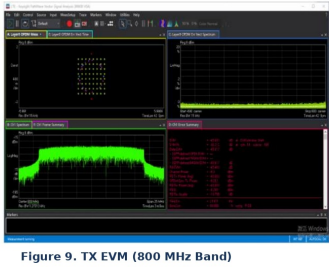


Figure 9. TX EVM (800 MHz Band)

Figure 9. TX EVM (800 MHz)

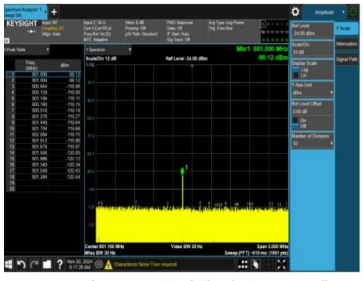


Figure 10. TX Isolation (800 MHz Band)

Figure 10. TX Isolation (800 MHz)

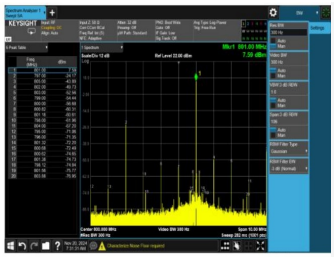

Figure 11. TX Max Output Power (800 MHz Band)

Figure 11. TX Max Output (800 MHz)


Figure 12. TX Noise Floor (800 MHz Band)

Figure 12. TX Noise Floor (800 MHz)


Figure 13. TX OIP3 (800 MHz Band)

Figure 13. TX OIP3 (800 MHz)

11.3 TX Performance – 2.4 GHz Band


Figure 14. TX 40dB Attenuated Output (2.4 GHz Band)

Figure 14. TX 40 dB Atten. Output (2.4 GHz)


Figure 15. TX EVM (2.4 GHz Band)

Figure 15. TX EVM (2.4 GHz)


Figure 16. TX Isolation (2.4 GHz Band)

Figure 16. TX Isolation (2.4 GHz)

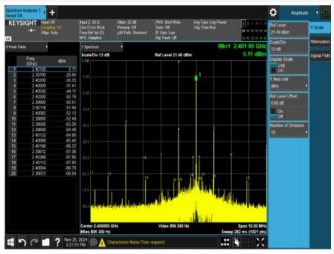

Figure 17. TX Max Output Power (2.4 GHz Band)

Figure 17. TX Max Output (2.4 GHz)

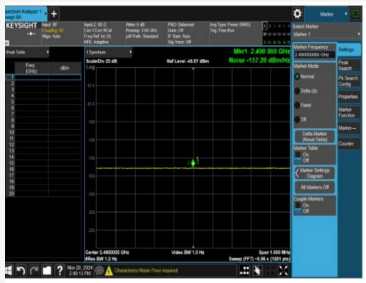

Figure 18. TX Noise Floor (2.4 GHz Band)

Figure 18. TX Noise Floor (2.4 GHz)


Figure 19. TX OIP3 (2.4 GHz Band)

Figure 19. TX OIP3 (2.4 GHz)

11.4 TX Performance – 5.5 GHz Band


Figure 20. TX 40dB Attenuated Output (5.5 GHz Band)

Figure 20. TX 40 dB Atten. Output (5.5 GHz)


Figure 21. TX EVM (5.5 GHz Band)

Figure 21. TX EVM (5.5 GHz)


Figure 22. TX Isolation (5.5 GHz Band)

Figure 22. TX Isolation (5.5 GHz)

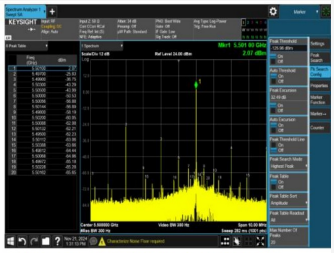


Figure 23. TX Max Output Power (5.5 GHz Band)

Figure 23. TX Max Output (5.5 GHz)



Figure 24. TX Noise Floor (5.5 GHz Band)

Figure 24. TX Noise Floor (5.5 GHz)

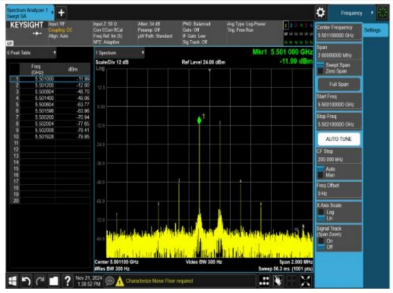


Figure 25. TX OIP3 (5.5 GHz Band)

Figure 25. TX OIP3 (5.5 GHz)

12. Typical Application Circuit

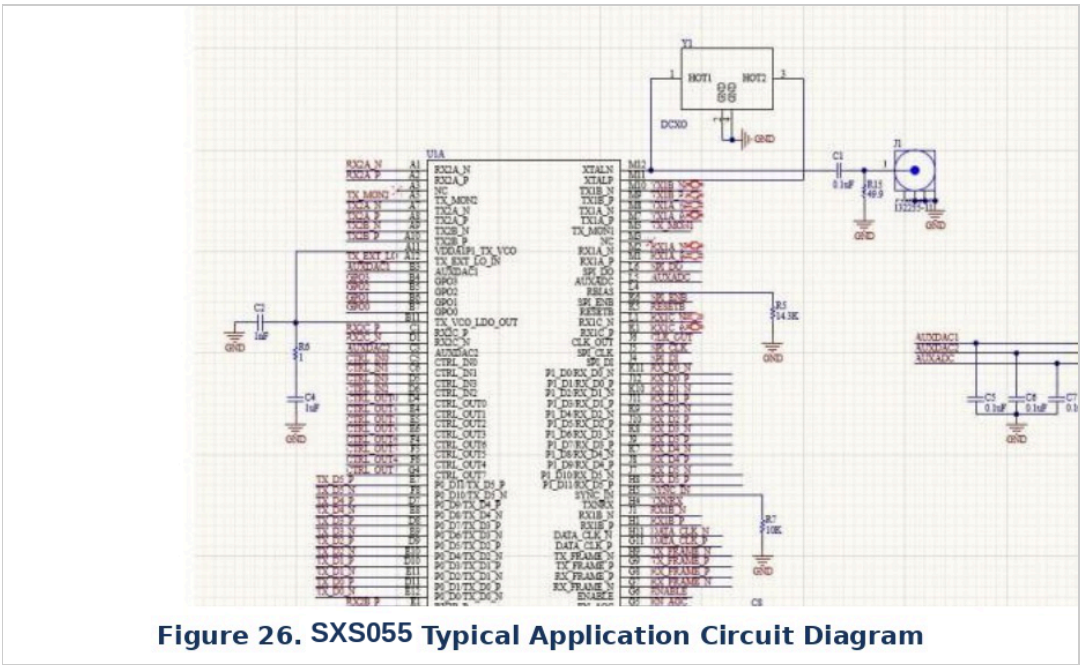


Figure 26. Typical Application Circuit

13. Functional Blocks and Operating Principle

13.1 General Description

The SXS055 is a highly integrated radio frequency (RF) transceiver configurable for a wide range of applications. The device integrates all necessary RF, mixed-signal, and digital modules to provide complete transceiver functionality in a single device. Its programmability enables this wideband transceiver to adapt to multiple communication standards, including both FDD and TDD systems. This programmability also allows the device to interface with various baseband processors (BBPs) via a single 12-bit parallel data port, dual 12-bit parallel data ports, or a 12-bit low-voltage differential signaling (LVDS) interface.

The SXS055 also provides self-calibration and AGC systems to maintain high performance levels across varying temperature and input signal conditions. In addition, the device includes multiple test modes that allow system designers to insert test tones and build internal loopback modes during the prototype design phase, enabling design debugging and optimization of radio configurations for specific applications.

13.2 Receiver

The analog input incorporates a differential switched-capacitor sample-and-hold structure . The differential structure provides superior AC characteristics at high-frequency inputs. The common-mode voltage of the differential inputs INP and INM is 0.95 V, supplied by the on-chip VCM pin. The maximum differential input amplitude is 2 V_{PP}.

The receiver section contains all necessary modules for receiving RF signals and converting them into digital data usable by the BBP. There are two independently controlled channels that can receive signals from different sources, enabling the device to be used in multiple-input multiple-output (MIMO) systems while sharing a common frequency synthesizer. Each channel has three inputs that can be multiplexed to the signal chain, allowing the SXS055 to be used in diversity systems with multiple antenna inputs.

The receiver is a direct-conversion system comprising a low-noise amplifier (LNA), followed by in-phase (I) and quadrature (Q) amplifiers, a mixer, and channel-shaping filters that down-convert the received signal to baseband for digitization. An external LNA can also be connected to the device, providing designers with maximum flexibility to customize the receiver front-end for specific applications.

Gain control is achieved through a pre-programmed gain index table that distributes gain among modules to optimize performance at each level. This can be implemented by enabling internal AGC in either fast or slow mode, or through manual gain control, allowing the BBP to adjust gain as needed. In addition, each channel features independent RSSI measurement, DC offset tracking, and all necessary circuitry for self-calibration.

The receiver includes a 12-bit sigma-delta ADC with adjustable sampling rate that generates a data stream from the received signal. The digitized signal can be further conditioned through a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sampling rate of each digital filter module can be adjusted by modifying the decimation factor to produce the required output data rate.

13.3 Transmitter

The transmitter section contains two identical, independently controlled channels that provide all necessary digital processing, mixed-signal, and RF modules to implement a direct-conversion system while sharing a general-purpose frequency synthesizer. Digital data received from the BBP passes through a fully programmable 128-tap FIR filter without interpolation options. The FIR output is fed to a series of interpolation filters that provide additional filtering and data rate interpolation before reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both I and Q channels feed into the RF module for up-conversion.

When converted to baseband analog signals, the I and Q signals are filtered to remove sampling images and then fed into the up-conversion mixer. Here, the I and Q signals are recombined and modulated at the carrier frequency for transmission to the output stage. The combined signal also passes through analog filters that provide additional channel shaping before being transmitted to the output amplifier. Each transmit channel provides a wide, fine-gain attenuation adjustment range to help designers optimize the signal-to-noise ratio (SNR).

Each transmit channel includes built-in self-calibration circuitry to support automatic real-time adjustment. The transmitter module also provides a TX monitor module for each channel. This module monitors the transmitter output and routes it back to the BBP through an unused receiver channel for signal monitoring. The TX monitor module is only available in TDD mode when the receiver is idle.

13.4 Clock Input Options

The reference clock used for SXS055 operation can be provided by two different clock sources. The first option is to use a dedicated crystal oscillator with a frequency between 19 MHz and 50 MHz, connected between the XTALP and XTALN pins. The second option is to connect an external oscillator or clock distribution device (such as the AD9548) to the XTALN pin (with the XTALP pin left open). If an external oscillator is used, the frequency can range from 10 MHz to 80 MHz.

This reference clock is used to clock the frequency synthesizer modules, which internally generate all data clocks, sampling clocks, and local oscillators. Crystal frequency error can be eliminated by using digitally programmable, digitally controlled crystal oscillator (DCXO) functionality to adjust on-chip variable capacitors. These capacitors can trim the crystal frequency variation in the system, resulting in a more accurate reference clock from which all other frequencies are derived. This feature can also be used in conjunction with the on-chip temperature detection function to provide oscillator frequency temperature compensation during normal operation.

13.5 Frequency Synthesizer

The SXS055 contains two identical frequency synthesizers for generating the required LO signals for the RF signal paths: one for the receiver and one for the transmitter. The phase-locked loop (PLL) frequency synthesizer employs a fractional-N design incorporating fully integrated voltage-controlled oscillators (VCOs) and loop filters. In TDD operation mode, the frequency synthesizer is enabled and disabled according to the requirements of RX and TX frames. In FDD mode, the TX PLL and RX PLL can be active simultaneously. These PLLs require no external components.

The SXS055 also includes a baseband PLL frequency synthesizer for generating all baseband-related clock signals. These include ADC and DAC sampling clocks, the DATA_CLK signal (see the "Digital Data Interface" section), and all data framing signals. The PLL programming frequency range is 700 MHz to 1400 MHz, depending on the system data rate and sampling rate requirements.

13.6 Digital Data Interface

The SXS055 data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP. The data ports can be configured as single-ended CMOS or differential LVDS formats. Both formats can be configured in multiple ways to meet system requirements for data ordering and data port connections. These include single-port data bus, dual-port data bus, single data rate, dual data rate, and various data ordering combinations to transfer data from different channels across the bus at the appropriate time. Bus transmission is controlled through simple hardware handshaking signals. The two ports can operate in bidirectional (TDD) mode or full-duplex (FDD) mode, where in the latter mode half of the bits are used for transmit data and half for receive data. The interface can also be configured to use only one data port for applications that do not require high data rates and prefer to use fewer interface pins.

13.7 DATA_CLK Signal

A DATA_CLK signal is provided with the RX data, which the BBP can use when receiving data. DATA_CLK can be set to provide single data rate (SDR) timing (where data is sampled on each rising clock edge) or dual data rate (DDR) timing (where data is captured on both rising and falling edges simultaneously). This timing applies to operation modes using either a single port or two ports.

14. Registers

Refer to the SXS055 Register Map & Software Migration Guide. Controlled documentation is available upon request.

15. Power Supply – Ground Protection (ESD)

To improve the electrostatic discharge (ESD) immunity of the device, ESD protection circuits exist between various power supply pins inside the device. Each ESD protection diode has a forward conduction voltage drop of approximately 0.35 V. During power-up and normal operation, prolonged forward conduction of these ESD protection diodes should be avoided.

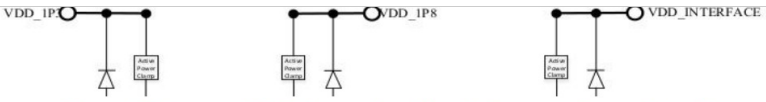


Figure 27. Internal ESD Protection Circuit Between Power Supplies

Figure 27. Internal ESD Protection Circuit

16. Precautions

16.1 Installation Notes

1. Pay attention to device orientation during soldering to avoid mis-soldering.
2. Instruments and meters used for circuit debugging must have good unified grounding. PCB design must ensure good grounding and power supply decoupling.
3. Ensure that power supply polarity is not reversed and that input/output terminals are not short-circuited to the power supply, as this may cause circuit damage.

16.2 Operation Notes

1. Power-up requirements: It is recommended that the analog power supply and digital power supply be powered up simultaneously, or that the analog power supply is powered up first.
2. Use capacitors with low ESR for decoupling at the LDO output.
3. In applications, large-area PCB grounding is recommended. This eliminates potential differences that may exist due to different ground points and reduces the effect of capacitance generated by the circuit board on the circuit.
4. Each power supply pin requires a nearby 1 µF or 0.1 µF capacitor.
5. For the analog input section, if differential input is used, the differential input traces must be of equal length.
6. Digital and analog power supplies must be separated.

1. All device terminals incorporate ESD-protection structures; however, high-energy electrical pulses may still damage the device. Apply ESD protection during testing, handling, and storage.

2. Exceeding absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.
3. When protected from direct exposure to rain and snow, product packaging can be transported using safe transportation tools. However, products must not be stored together with acidic, alkaline, or other corrosive substances. Packaging should be safe; existing transportation tools may be used.
4. The storage environment for packaged products must meet Class I warehouse requirements as specified in Section 8.1 of Q/W 657A (temperature: 15°C to 25°C, humidity: 25% to 65%). The area must be free of acidic, alkaline, or other corrosive gases, well-ventilated, and equipped with appropriate anti-static measures.

16.4 Assembly Notes

1. This product has a moisture sensitivity level of MSL3. After removal from the moisture-proof bag, the maximum allowable exposure time to the ambient environment before dry storage or baking and reflow

is: ≤30°C/60%RH, 168h.

2. If device storage conditions cannot be controlled or traced, strictly perform baking at 125°C for 8 hours before assembly.
3. If the assembly environment temperature and humidity cannot be guaranteed at ≤30°C/60%RH, complete soldering within 12 hours after baking.
4. After baking, the product is highly prone to static electricity generation; ESD protection must be observed during all handling procedures.
5. For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210°C to 235°C. The maximum peak temperature is not recommended to exceed 235°C. Time within ±5°C of peak temperature ≤20s, time above liquidus 60 to 90s, ramp-up rate 2 to 4°C/s, ramp-down rate 2 to 6°C/s.
6. For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230°C to 245°C. The maximum peak temperature is not recommended to exceed 260°C. Time within ±5°C of peak temperature ≤20s, time above liquidus 60 to 90s, ramp-up rate 2 to 4°C/s, ramp-down rate 2 to 6°C.
7. If the mixed assembly process requires elevated temperature, ensure that the maximum body temperature of the device does not exceed 260°C (device body temperature is measured at the top surface of the device during reflow soldering).
8. This product uses lead-free/leaded solder balls with SAC305 material.

17. Common Faults and Remedies

1. No signal output: Verify that a valid clock is present at the clock input pin, verify that power and ground connections are normal, and ensure that input and reference voltages are within specification.

2. **Output data jitter:** Check external circuits and connections, and ensure the reference voltage is stable.
3. **Unstable device operation:** Check the power supply and ensure the power supply voltage is stable.

> **Note:** For technical support, please contact SHENXIN TECH at felix@shenxinic.com or +852 51367095.

18. Contact Information

For technical support, ordering information, or any other inquiries, please contact SHENXIN TECH:

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